

DMA for UCAS

0.1.0

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Chapter 1

Hierarchical Index

1.1 Class Hierarchy

This inheritance list is sorted roughly, but not completely, alphabetically:

fifo	10
dma	7

Chapter 2

Class Index

2.1 Class List

Here are the classes, structs, unions and interfaces with brief descriptions:

dma	7
fifo	10

Chapter 3

File Index

3.1 File List

Here is a list of all files with brief descriptions:

FinalElec.srcs/sources_1/new/ dma.v	15
FinalElec.srcs/sources_1/new/ fifo.v	
First in first out memory module	15

Chapter 4

Class Documentation

4.1 dma Module Reference

Inheritance diagram for dma:



- [clk](#)
- [rst](#)
- [dir](#)
- [float_direction](#)
- [mem_to_dma_valid](#)
- [mem_to_dma_enable](#)
- [cpu_to_dma_valid](#)
- [cpu_to_dma_enable](#)
- [dma_to_mem_valid](#)
- [dma_to_mem_enable](#)
- [dma_to_cpu_valid](#)
- [dma_to_cpu_enable](#)
- [\[3:0\] mem_data_out](#)
- [\[7:0\] cpu_data_out](#)
- [reg \[3:0\] mem_data_in](#)
- [reg \[7:0\] cpu_data_in](#)
- [buffer_cpu_to_mem](#) [fifo](#)
- [buffer_valid_cpu_to_mem](#) [reg\[2:0\]](#)
- [buffer_valid_mem_to_cpu](#) [reg\[2:0\]](#)
- [buffer_empty_cpu_to_mem](#) [reg](#)
- [buffer_empty_mem_to_cpu](#) [reg](#)

4.1.1 Member Data Documentation

4.1.1.1 clk

`clk` [Input]

4.1.1.2 dma_to_cpu_valid

`dma_to_cpu_valid` [Output]

4.1.1.3 dma_to_cpu_enable

`dma_to_cpu_enable` [Output]

4.1.1.4 mem_data_out

`mem_data_out` [Input]

4.1.1.5 cpu_data_out

`cpu_data_out` [Input]

4.1.1.6 mem_data_in

`mem_data_in` [Output]

4.1.1.7 cpu_data_in

`cpu_data_in` [Output]

4.1.1.8 buffer_valid_cpu_to_mem

`buffer_valid_cpu_to_mem` [Signal]

4.1.1.9 buffer_valid_mem_to_cpu

`buffer_valid_mem_to_cpu` [Signal]

4.1.1.10 buffer_empty_cpu_to_mem

`buffer_empty_cpu_to_mem` [Signal]

4.1.1.11 buffer_empty_mem_to_cpu

`buffer_empty_mem_to_cpu` [Signal]

4.1.1.12 rst

`rst` [Input]

4.1.1.13 dir

`dir` [Input]

4.1.1.14 float_direction

`float_direction` [Input]

4.1.1.15 mem_to_dma_valid

`mem_to_dma_valid` [Input]

4.1.1.16 mem_to_dma_enable

`mem_to_dma_enable` [Input]

4.1.1.17 `cpu_to_dma_valid`

`cpu_to_dma_valid` [Input]

4.1.1.18 `cpu_to_dma_enable`

`cpu_to_dma_enable` [Input]

4.1.1.19 `dma_to_mem_valid`

`dma_to_mem_valid` [Output]

4.1.1.20 `dma_to_mem_enable`

`dma_to_mem_enable` [Output]

4.1.1.21 `fifo`

`fifo` [Module Instance]

The documentation for this module was generated from the following file:

- `FinalElec.srscs/sources_1/new/dma.v`

4.2 `fifo` Module Reference

Inheritance diagram for `fifo`:



- `ALWAYS_0` rst
Reset part.
- `ALWAYS_1` clk

Clock part.

- `clk`
clock input.
- `rst`
reset signal. The buffer will be set to 0 if reset.
- `dir`
- `[3:0] narrow_port_in`
- `[7:0] wide_port_in`
- `reg [3:0] narrow_port_out`
- `reg [7:0] wide_port_out`
- `input_valid`
- `_enable`
- `reg input_enable`
- `_valid`
- `buffer reg[63:0]`
- `width reg[56:0]`
- `narrow_buffer reg[7:0]`
- `narrow_width reg[8:0]`
- `direction reg`

4.2.1 Detailed Description

FIFO chip of different data width with two directions. The direction will be determined when `rst` is set to 1. if `direction` is 0, data will be sent from `narrow_port` to `wide_port`, if `direction` is 1, the behavior is different.

4.2.2 Member Function Documentation

4.2.2.1 ALWAYS_0()

```
ALWAYS_0 (
    rst ) [Always Construct]
```

Reset part.

the `reg direction` will be set to the input `dir`.

4.2.2.2 ALWAYS_1()

```
ALWAYS_1 (
    clk ) [Always Construct]
```

Clock part.

if `direction` equals 1, `narrow` is input.

if `direction` equals 0, `wide` is input.

4.2.3 Member Data Documentation

4.2.3.1 clk

`clk` [Input]

clock input.

4.2.3.2 rst

`rst` [Input]

reset signal. The buffer will be set to 0 if reset.

4.2.3.3 dir

`dir` [Input]

4.2.3.4 narrow_port_in

`narrow_port_in` [Input]

4.2.3.5 wide_port_in

`wide_port_in` [Input]

4.2.3.6 narrow_port_out

`narrow_port_out` [Output]

4.2.3.7 wide_port_out

`wide_port_out` [Output]

4.2.3.8 input_valid

`input_valid` [Input]

4.2.3.9 _enable

`_enable` [Input]

4.2.3.10 input_enable

`input_enable` [Output]

4.2.3.11 _valid

`_valid` [Output]

4.2.3.12 buffer

`buffer` [Signal]

4.2.3.13 width

`width` [Signal]

4.2.3.14 narrow_buffer

`narrow_buffer` [Signal]

4.2.3.15 narrow_width

`narrow_width` [Signal]

4.2.3.16 direction

`direction` [Signal]

The documentation for this module was generated from the following file:

- FinalElec.srcs/sources_1/new/[fifo.v](#)

Chapter 5

File Documentation

5.1 FinalElec.srcs/sources_1/new/dma.v File Reference

Classes

- Module [dma](#)
- include [fifo.v](#)

5.1.1 Variable Documentation

5.1.1.1 fifo.v

[fifo.v](#) [Include]

5.2 FinalElec.srcs/sources_1/new/fifo.v File Reference

First in first out memory module.

Classes

- Module [fifo](#)

5.2.1 Detailed Description

First in first out memory module.

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- ALWAYS_1
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