**Hardware Design and Lab: Lab4**

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**Catalog**

**1. Advanced Question:**

**First-In First Out (FIFO) Queue……………………………P3**

**2. Advanced Question:**

**Round-Robin FIFO Arbiter…...…………………………….P8**

**3. Advanced Question:**

**4-bit Ping-Pong Counter…….……………………………...P12**

**4. Advanced Question:**

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1. **Basic Question**
2. **Many-to-one LFSR**
3. **State Transition Diagram**

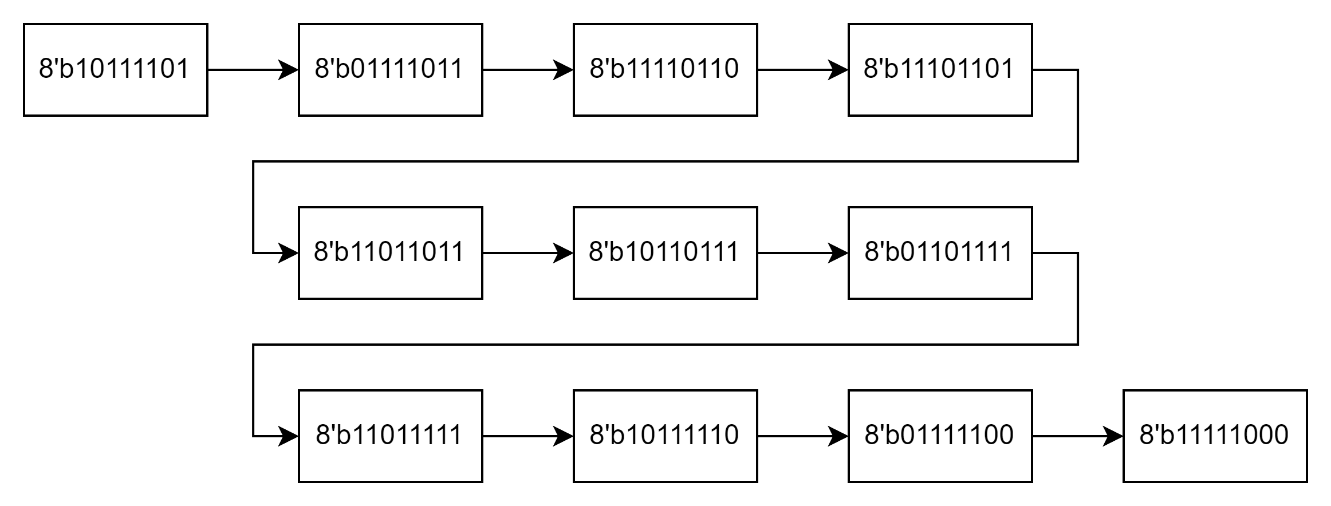
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Figure 1.1

1. **Basic Question**

If we reset the DFFs to 8'd0, then DFFs will remain 8'd0 because (DFF[1] ^ DFF[2]) ^ (DFF[3] ^ DFF[7]) is 0. Therefore, out will be a constant 1'b0.

1. **One-to-many LFSR**
2. **State Transition Diagram**

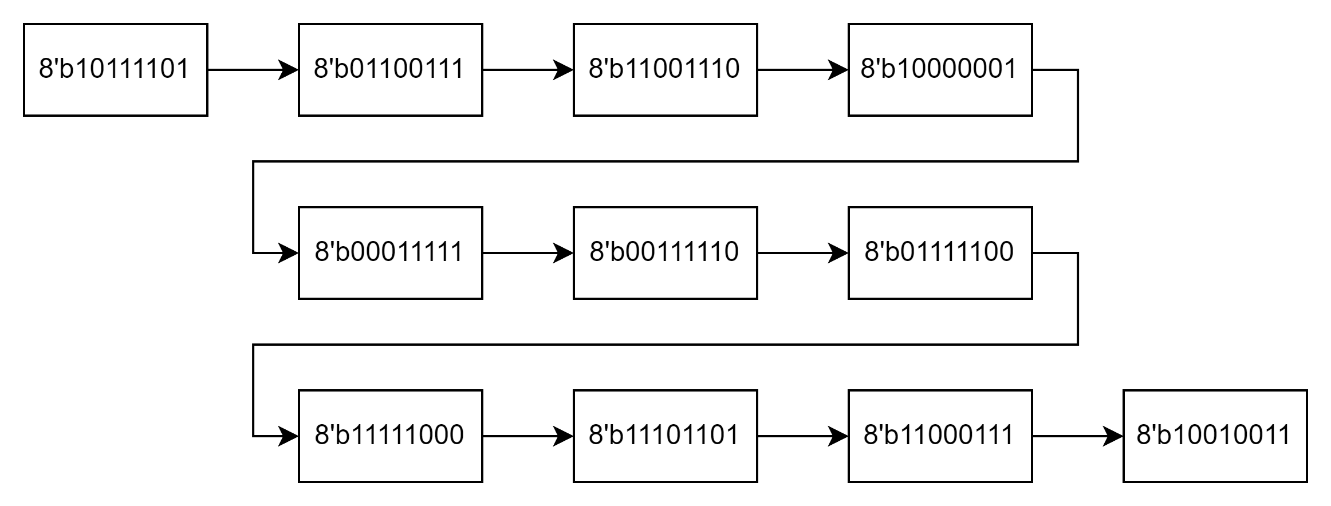
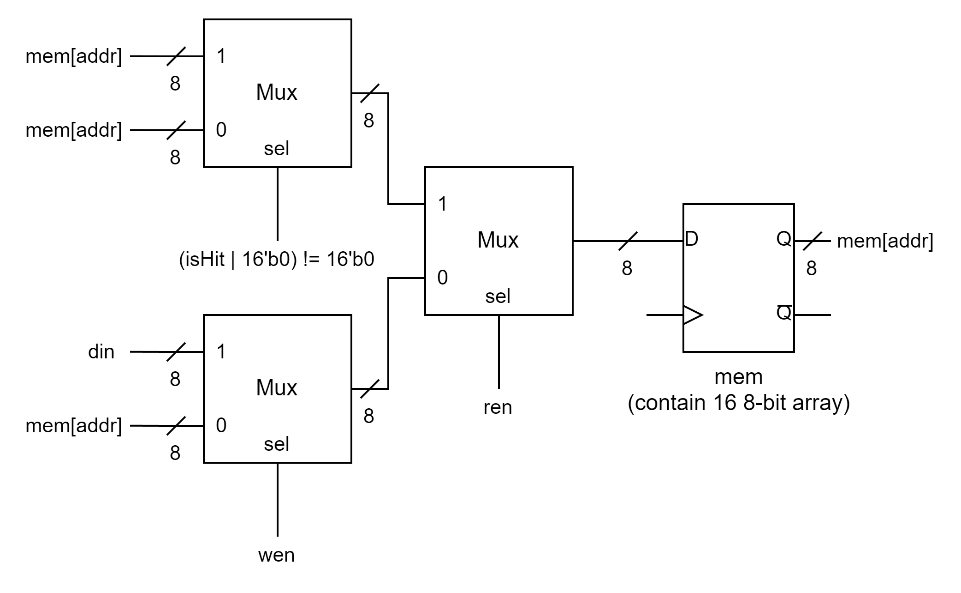


Figure 1.2

1. **Basic Question**

If we reset the DFFs to 8'd0, then DFFs will remain 8'd0 because DFF[7] XOR any other bit is 0. Therefore, out will be a constant 1'b0.

1. **Advanced Question: Content-addressable memory (CAM) design**
2. **Block Diagram**

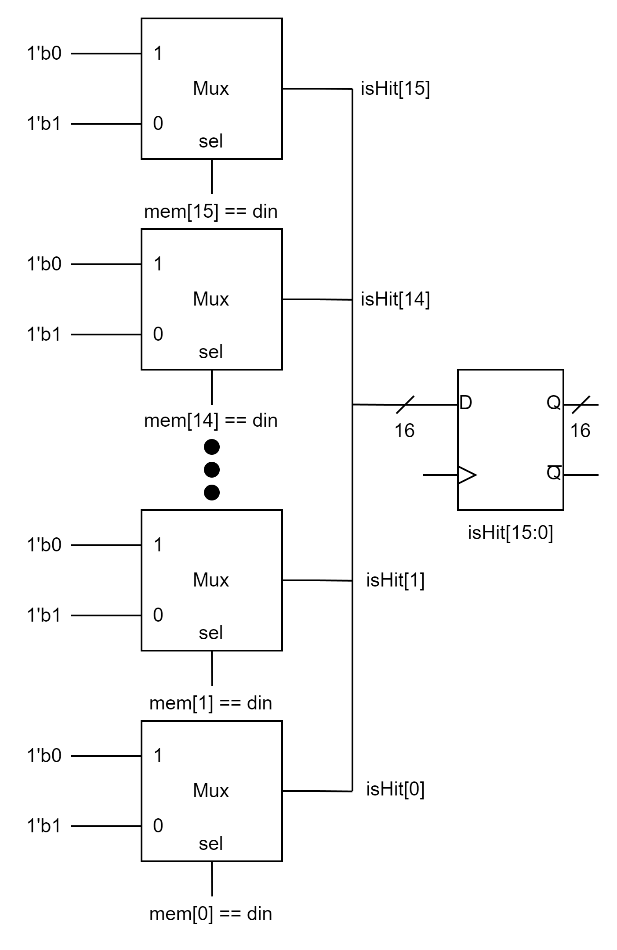
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Figure 2.2

mem

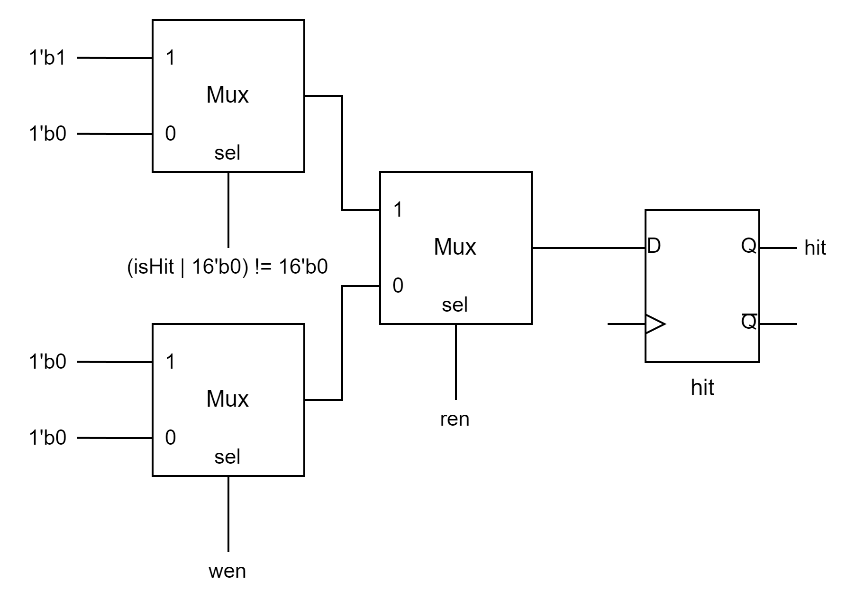
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Figure 2.1

isHit[15:0]

Figure 2.3

hit

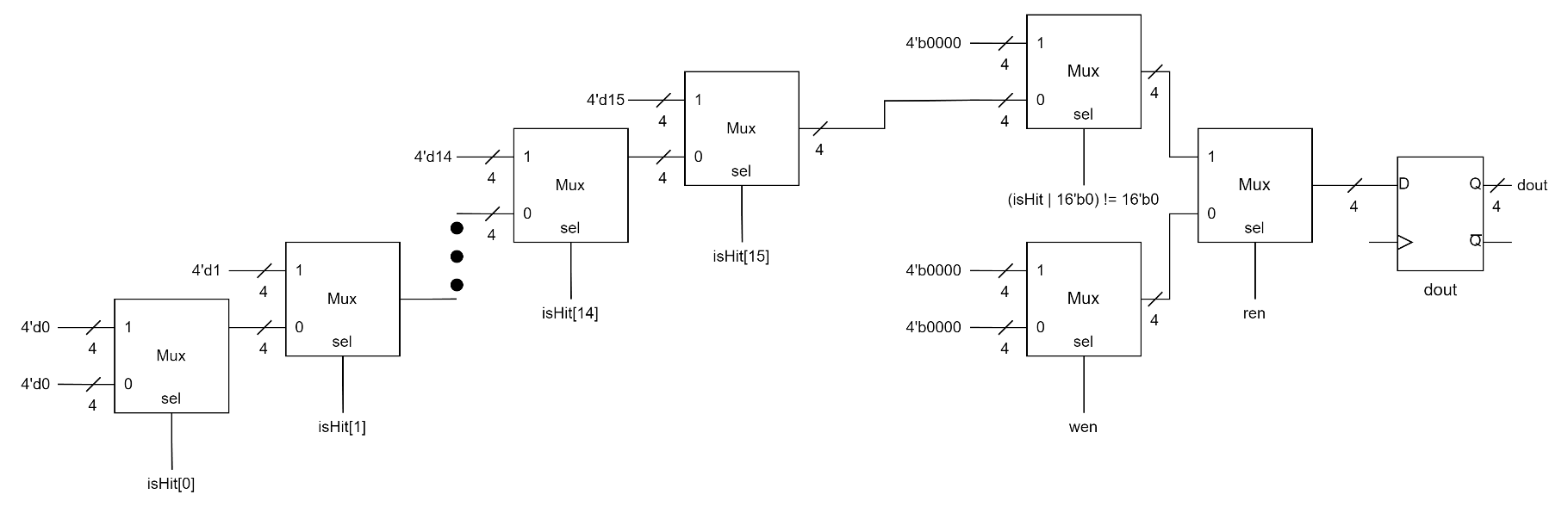
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Figure 2.4

dout

1. **Explanation**

In this problem, I defined a reg called **isHit[15:0]** as **Figure 2.1** to save the hit status. If the i-th bit in **isHit** equal to **din**, then **isHit[i]** will be set to 1'b1. Otherwise it will be set to 1'b0. **Figure 2.2** shows how I design the memory. If **ren** is 1'b0 and **wen** is 1'b1, then **din** will be written into **mem[addr]**. Otherwise, **mem[addr]** will not change. As mention above, **isHit** == **16'b0** means that there is no hit condition happened. Therefore, I designed **hit** as it shows in **Figure 2.3**. According to the specification, if **hit** == **1'b1**, we should output the largest address of the bits that is hit. So I designed the circuit as it shows in **Figure 2.4** to realize this function.

1. **Testbench**

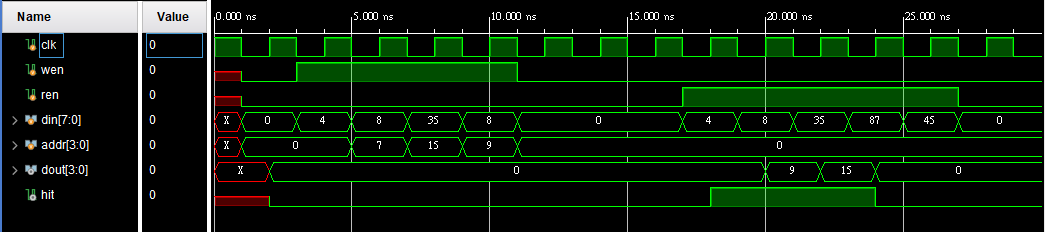
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Figure 2.5 wave form 1

First, I use the input data from lecture slide to test if there is something wrong or not. As the result showed in **Figure 2.5**, we can see that everything works correctly. And then I also add some extra testcases to check if the design work correctly. As **Figure 2.6** shows, it seems that it works correctly.

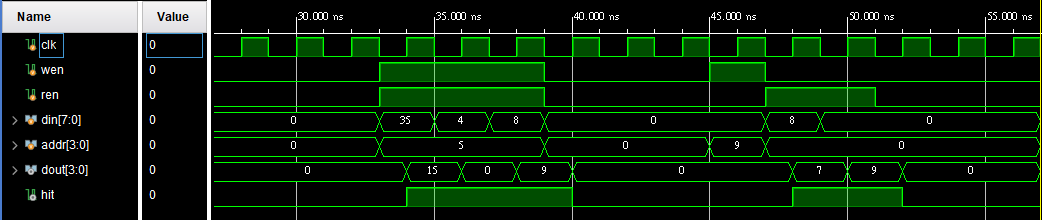


Figure 2.6 wave form 2

1. **Advanced Question: Scan Chain Design**
2. **Block Diagram**

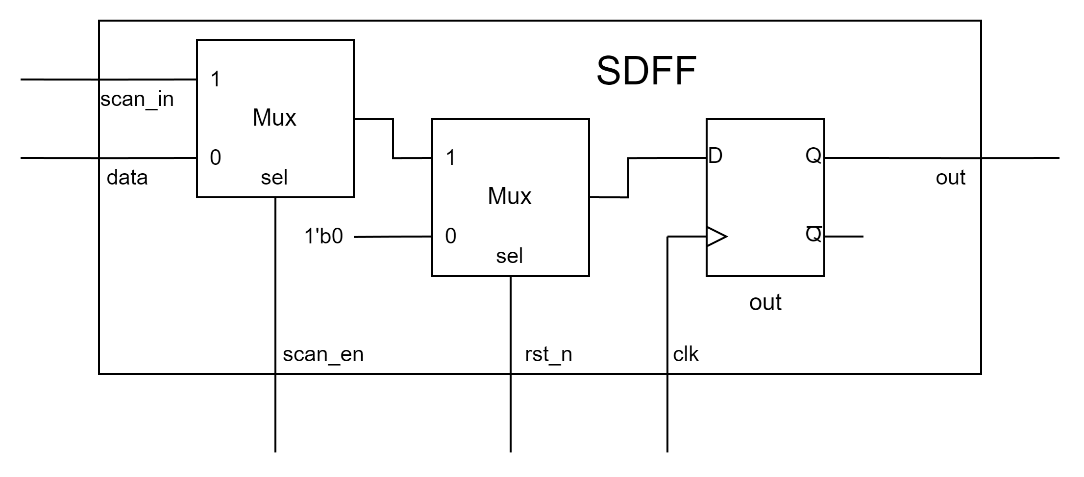
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Figure 3.1

SDFF

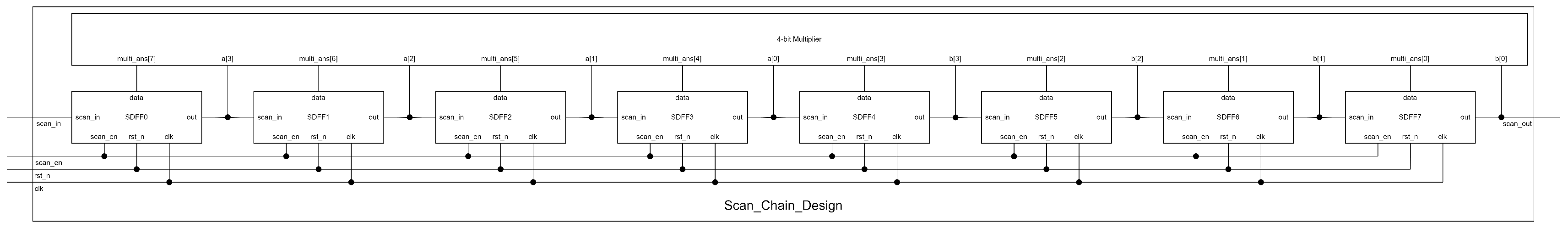
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Figure 3.2

Scan\_Chain\_Design (Left Part)

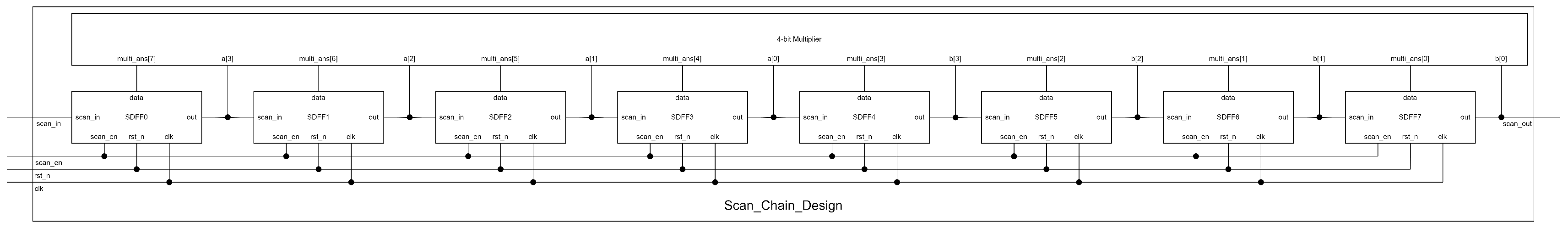
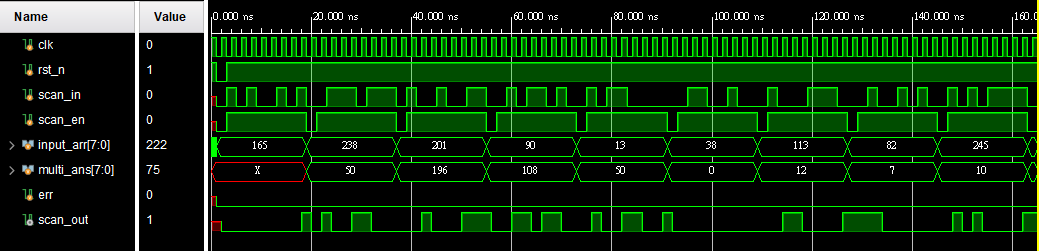
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Figure 3.3

Scan\_Chain\_Design (Right Part)

1. **Explanation**

In this problem, the lecture slides provide a complete design. Thus I realize the circuit by Verilog according to the **Figure 3.1**, **Figure 3.2**, and **Figure 3.3**. Note that **4-bit Multiplier** is designed by behavioral-level code.

1. **Testbench**

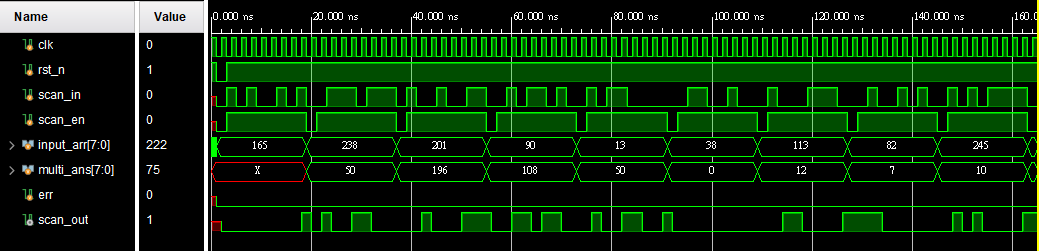


Figure 3.4

Wave form

In this problem, I found that it is difficult to judge the results with the naked eyes. Therefore, as I've learned form Lab2, I defined a signal called **err** to help me check the result. In testbench, the input sequence will be stored in **input\_arr[7:0]** first. And then it will be scan bit by bit into the DFFs. After input 8 bits of data, it will count **multi\_ans[7:0]** as **input\_arr[7:4]** \* **input\_arr[3:0]** and then **input\_ans** will be set to the next testcase. After **scan\_en** pulled up again, the testbench will check the output bit by bit compare to **multi\_ans**. If detecting any errors, **err** will be pulled up. Note that **err** will be reset to 1'b0 while **scan\_en** is **1'b0**. In this way, I can check the output more efficiently and precisely.

1. **Advanced Question: Built-in Self Test**
2. **Block Diagram**

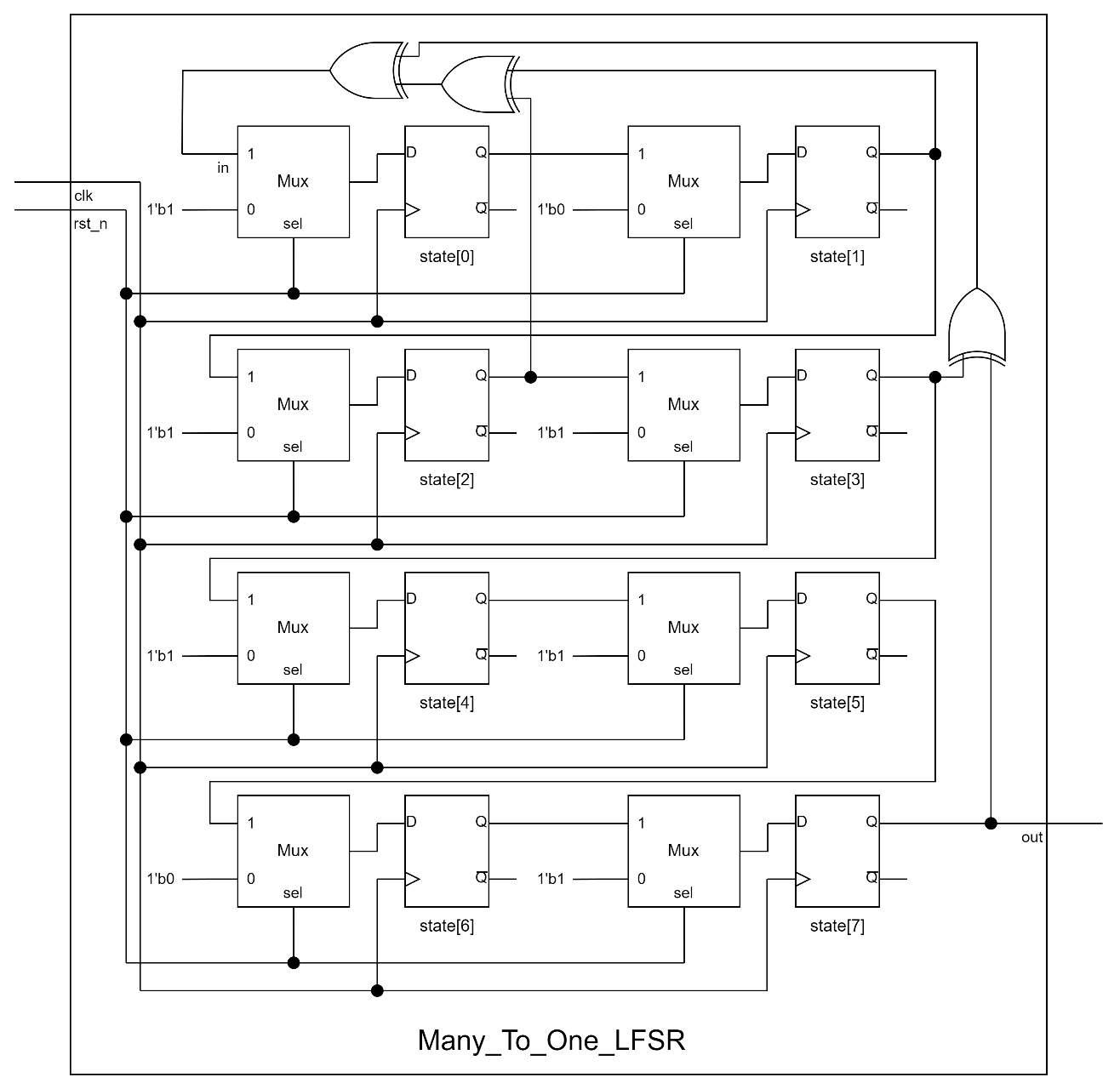
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Figure 4.1 Many\_To\_One\_LFSR

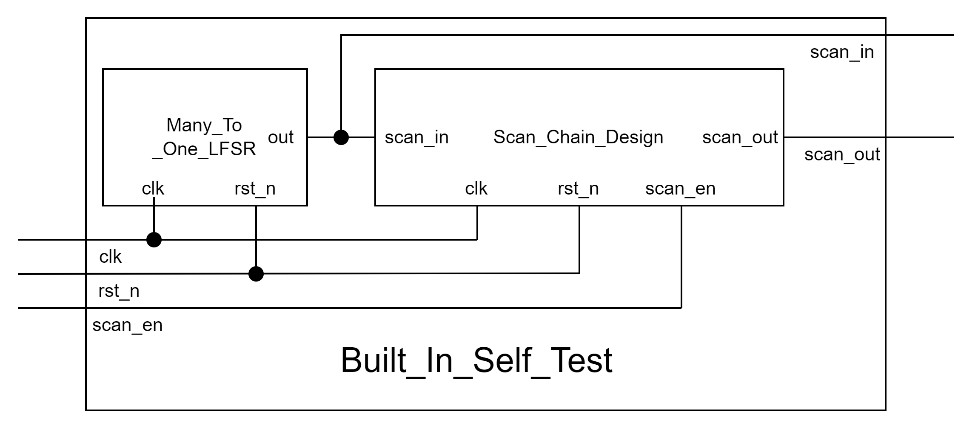
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Figure 4.2 Built\_In\_Self\_Test

1. **Explanation**

In this problem, I only have to combine to modules I 've designed in the previous problems. **Figure 4.1** shows how I designed **Many\_To\_One\_LFSR**. **Figure 4.2** shows how I connect these two modules together.

1. **Testbench**

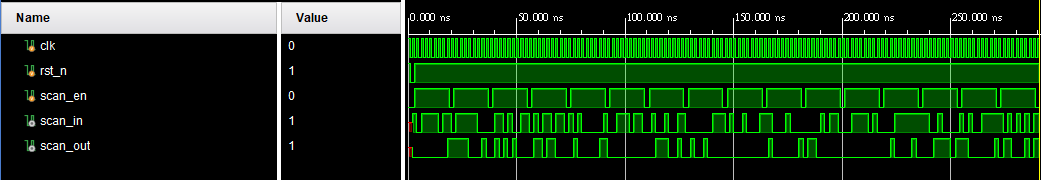


Figure 4.3 wave form

In this design, testcases are generated by **Many\_To\_One\_LFSR**. It seems that the method of how I designed in the testbench of **Scan\_Chain\_Design** is risky because there are some chances that I have some wrong cases in my testbench. Therefore, I write a code in C++ to simulate the testcases and check the results one by one. And every result seems right.

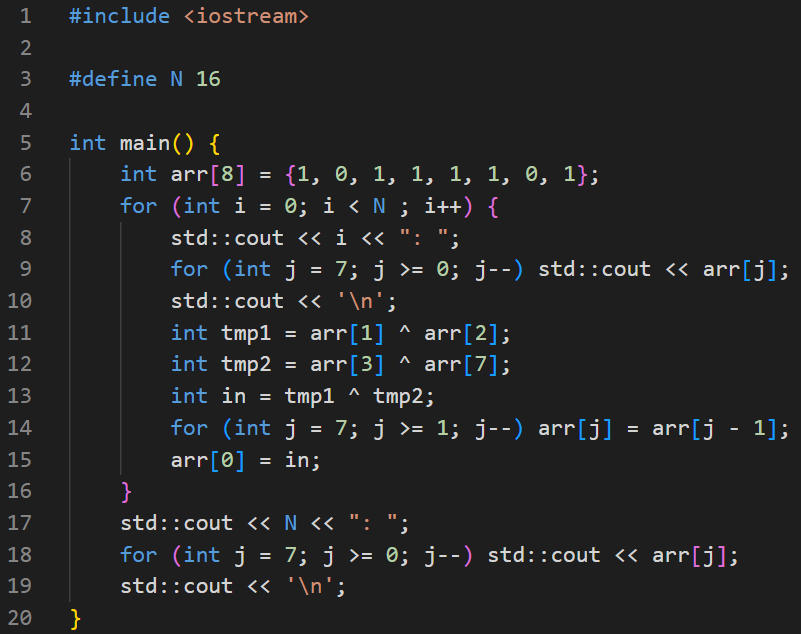


Figure 4.4

C++ code for simulating the testcases

1. **Advanced Question: Built-in Self Test FPGA**
2. **Block Diagram**

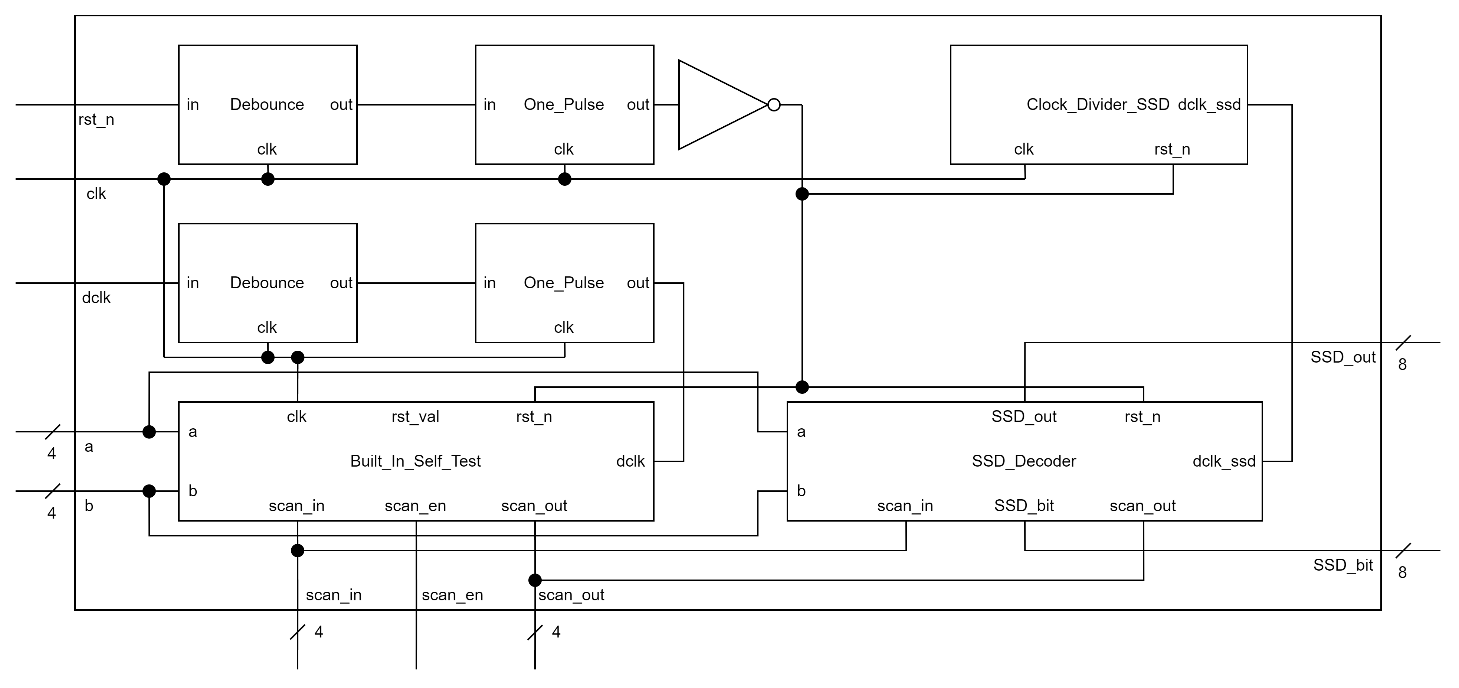
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Figure 5.1

The whole design of this problem

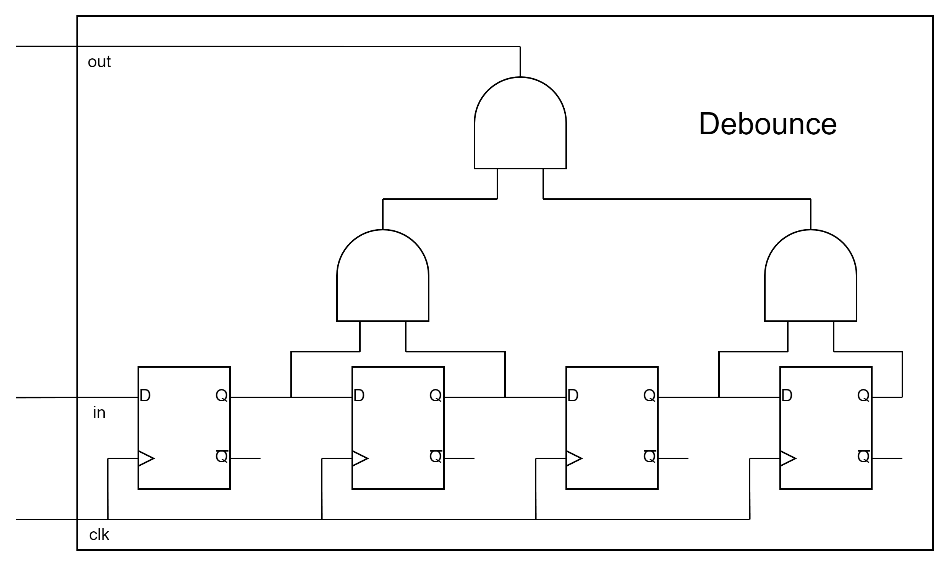
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Figure 5.2

Debounce

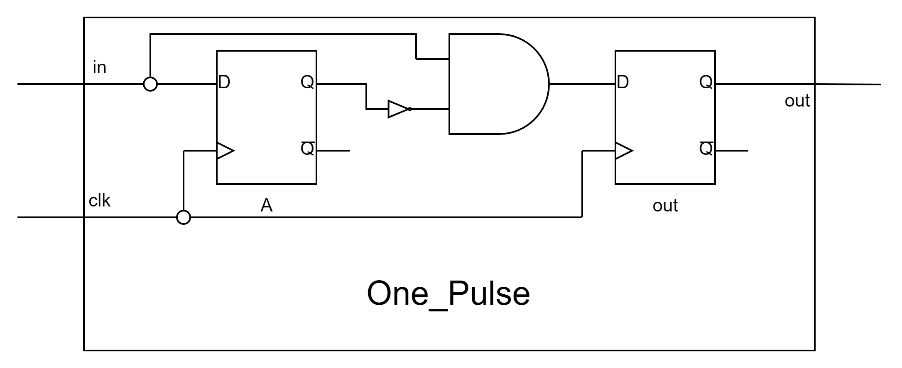
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Figure 5.3

One\_Pulse

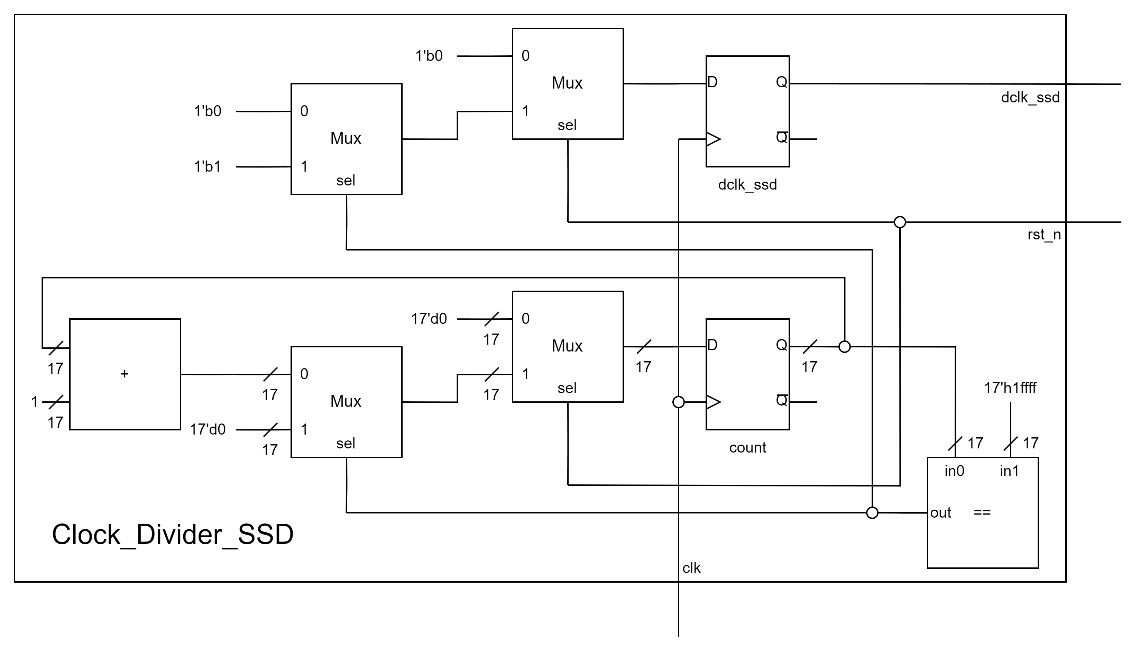
****

Figure 5.4

Clock\_Devider\_SSD

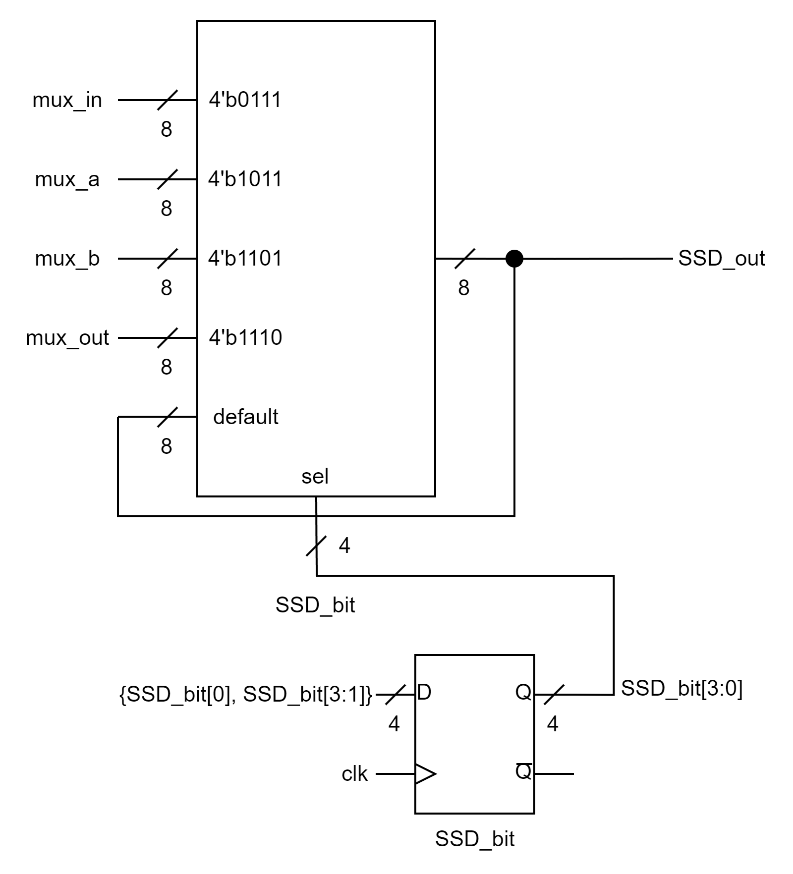
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Figure 5.5

SSD\_Decoder

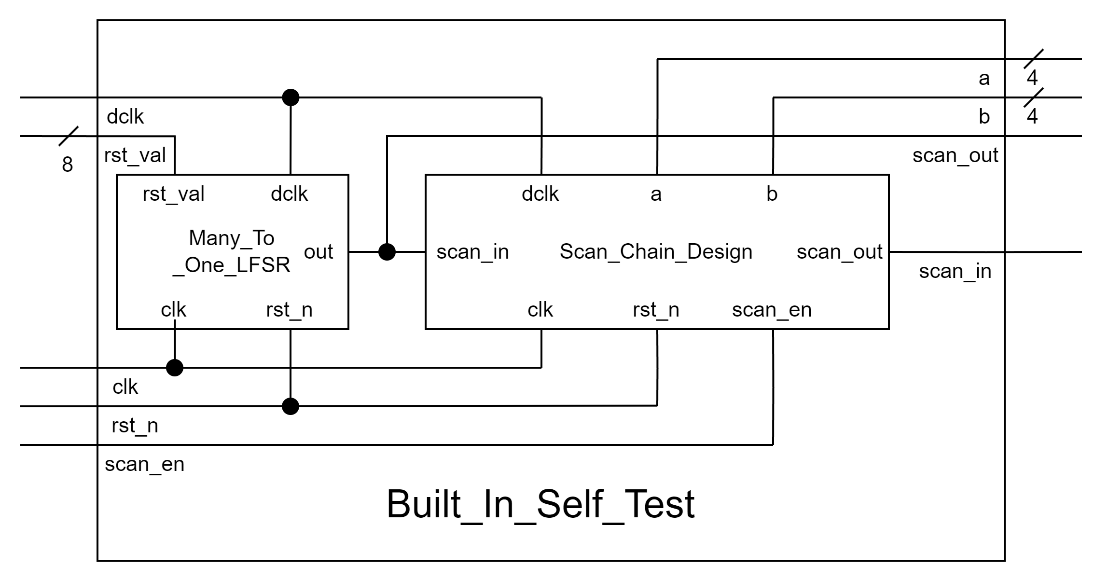
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Figure 5.6

Built\_In\_Self\_Test

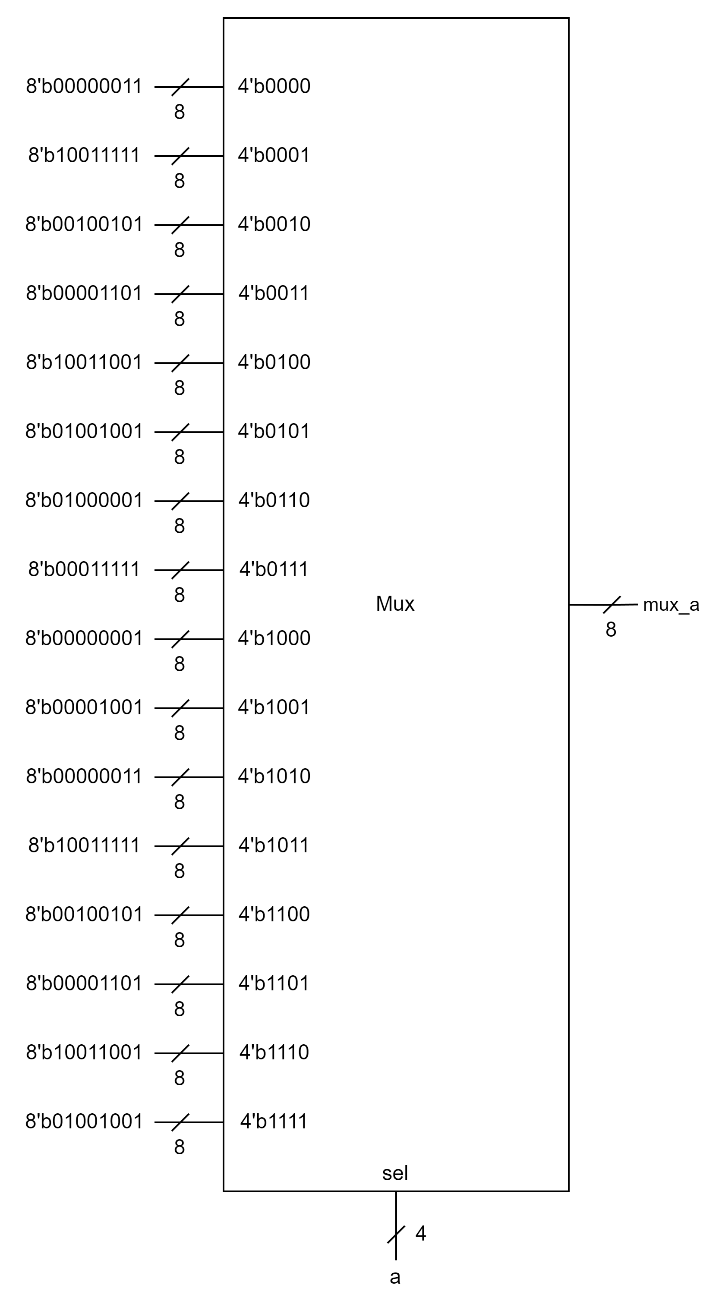
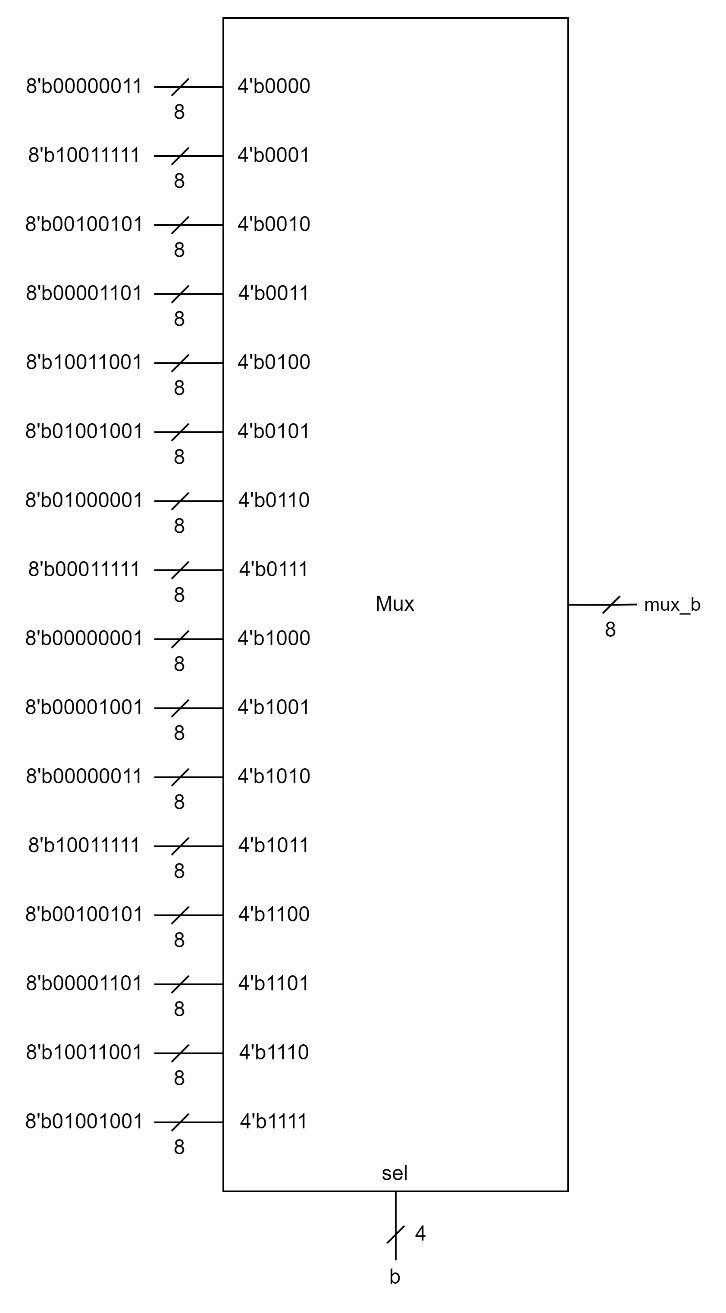
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Figure 5.8

mux\_b

Figure 5.7

mux\_a

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Figure 5.10

mux\_out

Figure 5.9

mux\_in

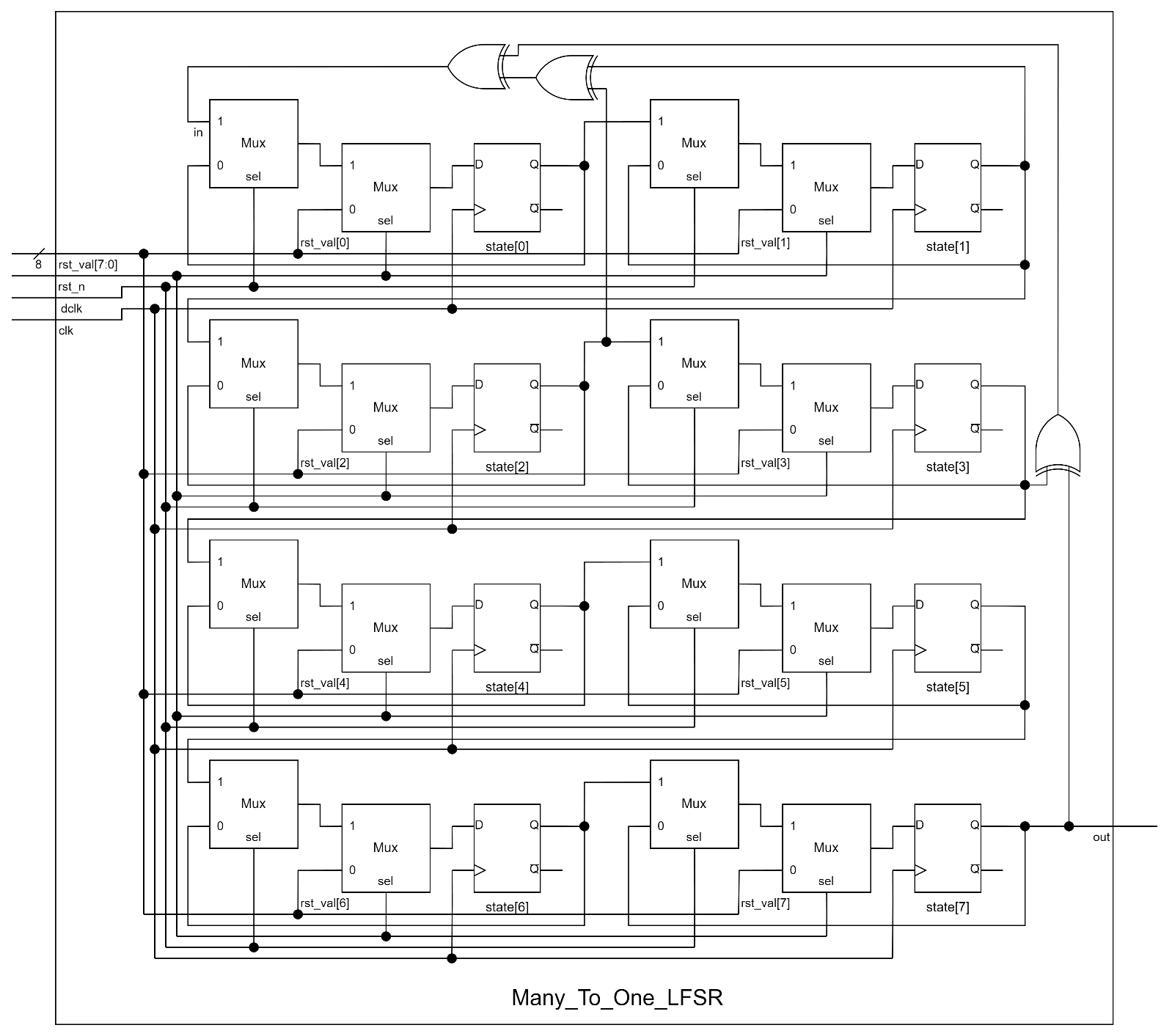
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Figure 5.11

Many\_To\_One\_LFSR

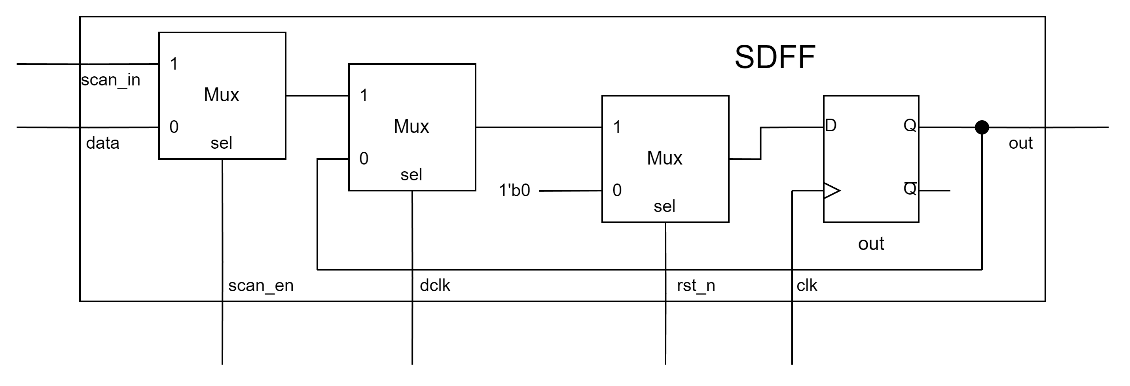
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Figure 5.12

SDFF

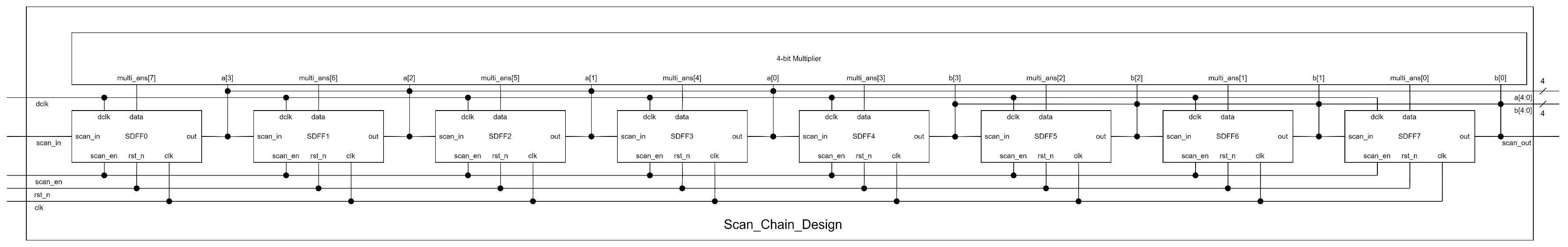
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Figure 5.13

Scan\_Chain\_Design (Left Part)

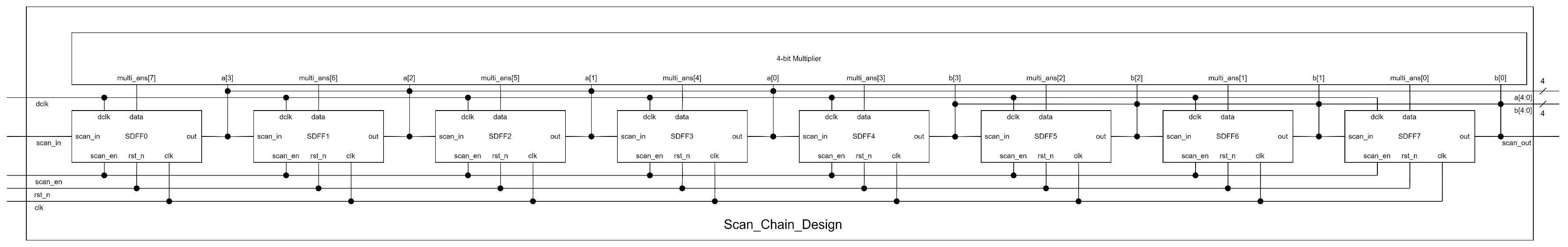
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Figure 5.14

Scan\_Chain\_Design (Left Part)

1. **Explanation**

According to the specification, I divided the circuit into different modules as **Figure 5.1** shows.

1. **What I Have Learned**

In this lab, I learned how to write my code in a good code style, separating combinational circuit and sequential circuit. In **Round-Robin FIFO Arbiter**, I had a big obstacle about how to let **valid** work properly. Therefore, I drew out wave form and analyzed it to help me solve this problem. In FPGA question, I had some strange results while I was debugging. The result seemed not related to my code. Instead, it turned out unexpected. I spent two whole days to think which part went wrong. Finally, I found that according to my original code, if **rst\_n** was pulled down, **dclk** would be reset and the **tmp\_rst\_n** would be set at the same time, which was ambiguous to Verilog. (Originally, I designed **tmp\_rst\_n** as **tmp\_flip** as mentioned above) From this event, I will be more careful about this problem and try not make this error again.