**Hardware Design and Lab: Lab5**

**Team 28**

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**Catalog**

**1. FPGA Question:**

**Sliding Window Sequence Detector……………...………………P3**

**2. FPGA Question:**

**Vending Machine…………………………………..…...………….P5**

**5. What I Have Learned…...................................................P14**

1. **Advanced Question: Sliding Window Sequence Detector**
2. **Finite State Diagram**

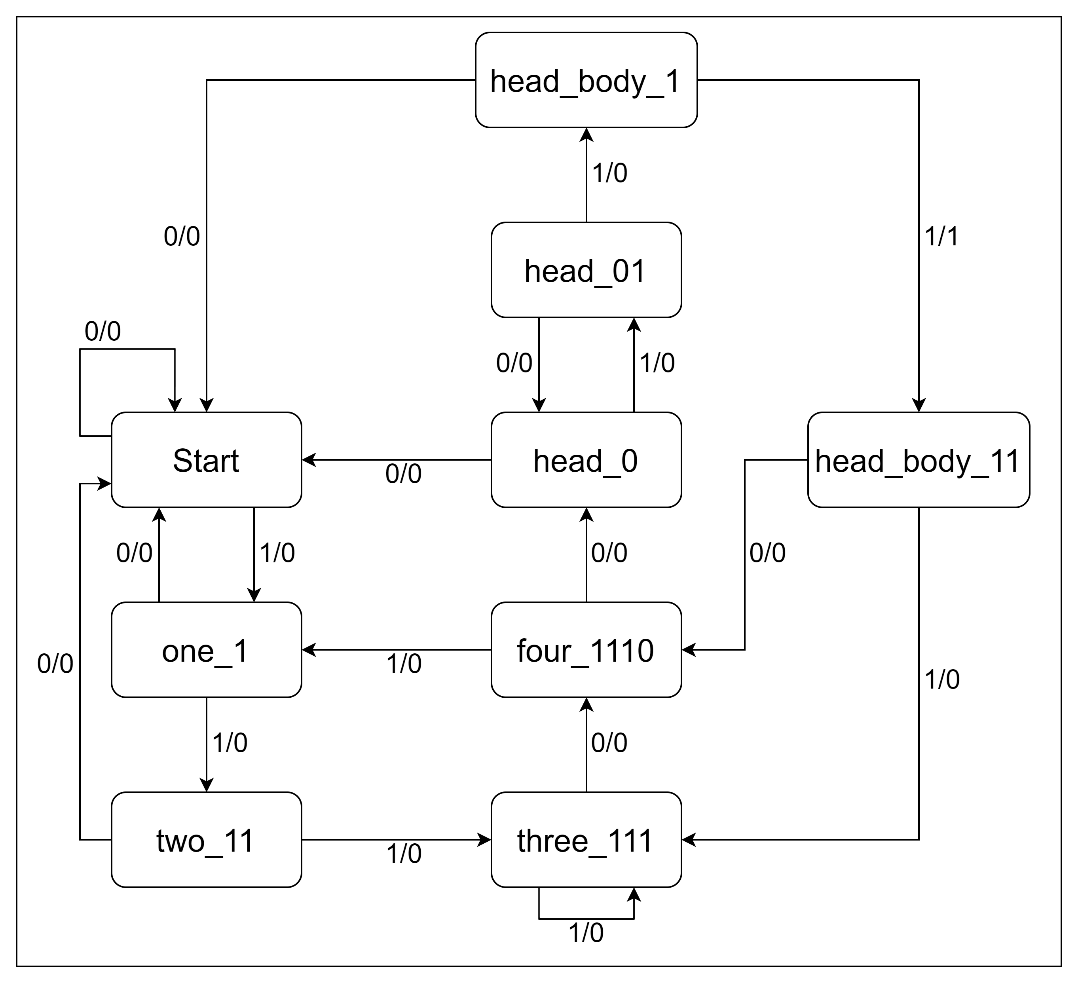
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Figure 1.1

1. **Explanation**

**Start:** Detect 0 bit that match the pattern.

**one\_1:** Detect the first bit **1** of the pattern.

**two\_11:** Detect the second bit **1** of the pattern.

**three\_111:** Detect the third bit **1** of the pattern.

**four\_1110:** Detect the fourth bit **0** of the pattern.

**head:** It means 1110.

**head\_0:** Detect **0** of the "several **01**".

**head\_01:** Detect **1** of the "several **01**".

**body:** It means "several **01**".

**head\_body\_1:** Detect the second-to-last bit **1** of the pattern.

**head\_body\_11:** Detect the last bit **1** of the pattern

1. **Testbench**

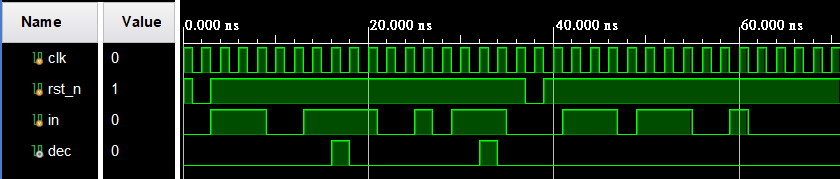


Figure 1.2

I use the testcase of the lab slide to check if there is something wrong and it seems that the design works properly.

1. **Vending Machine**
2. **Finite State Diagram**

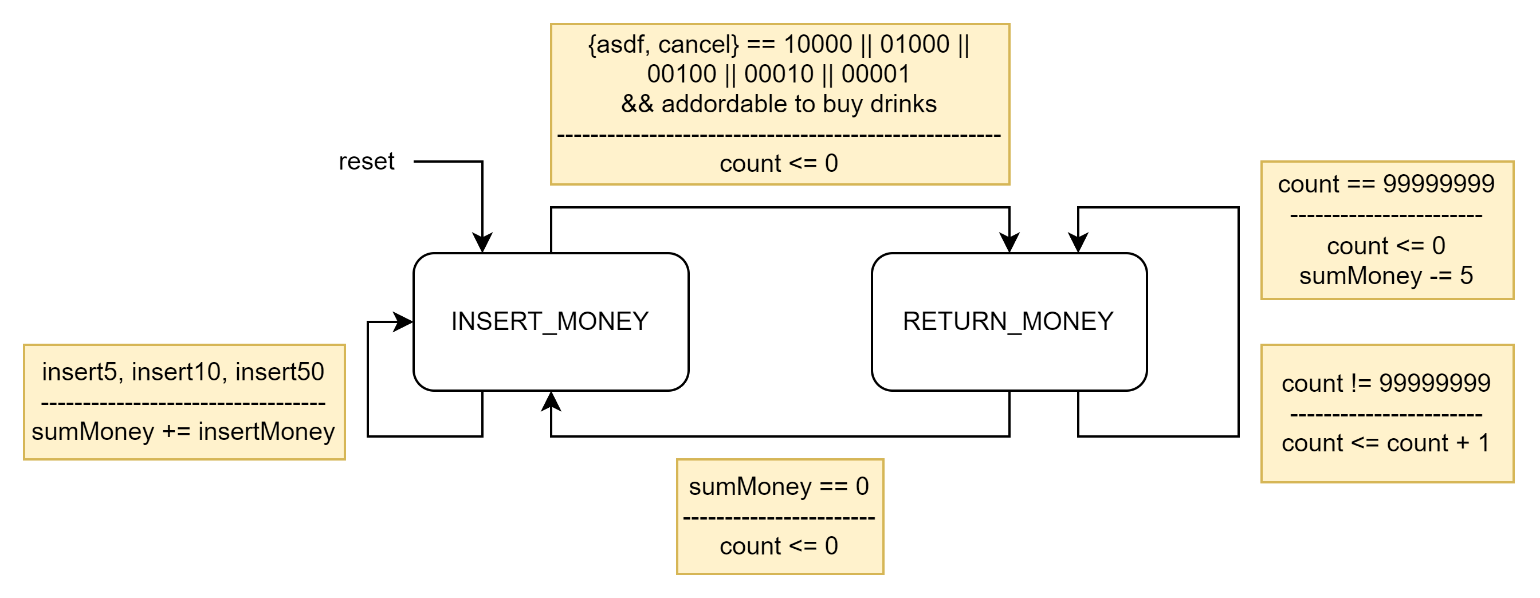
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Figure 2.1

1. **Block Diagram**

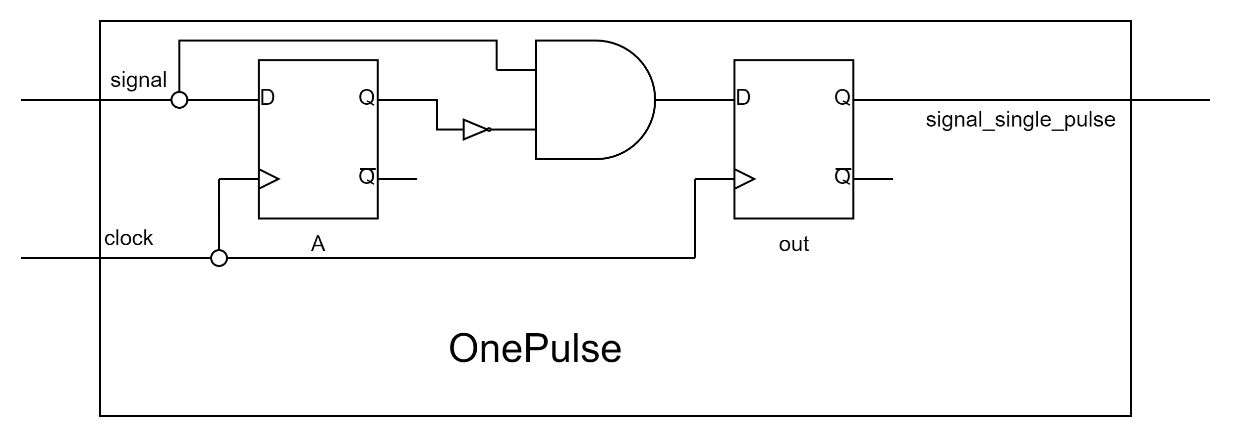


Figure 2.2

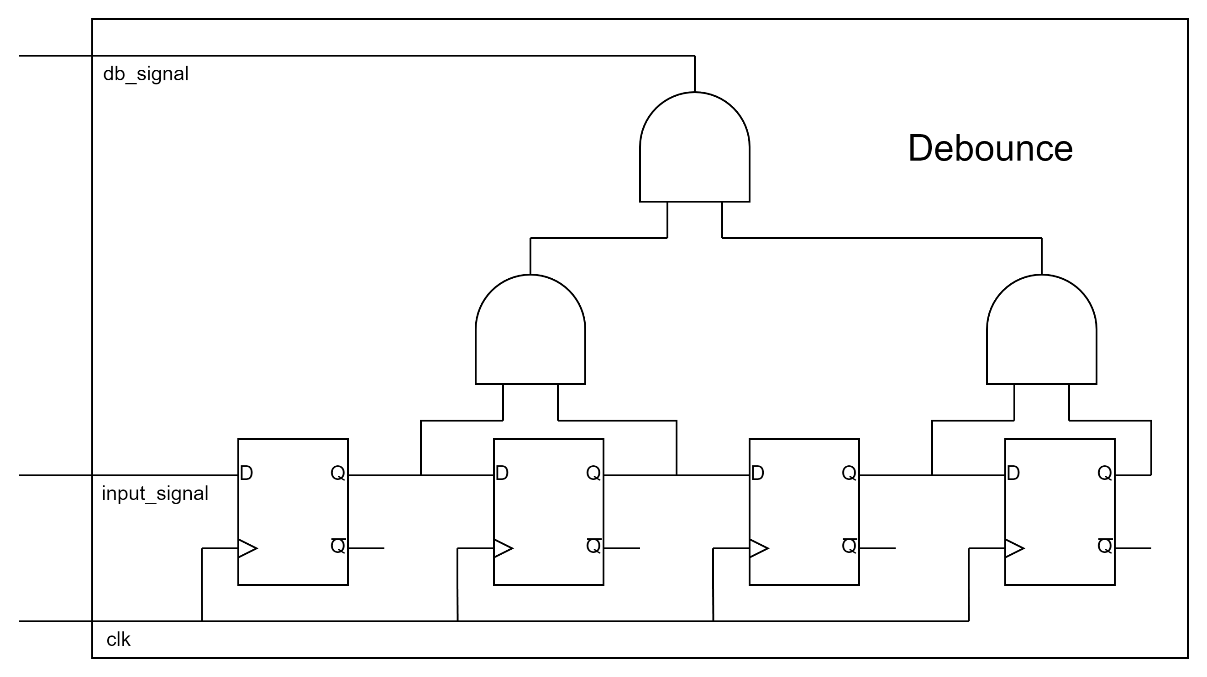


Figure 2.3

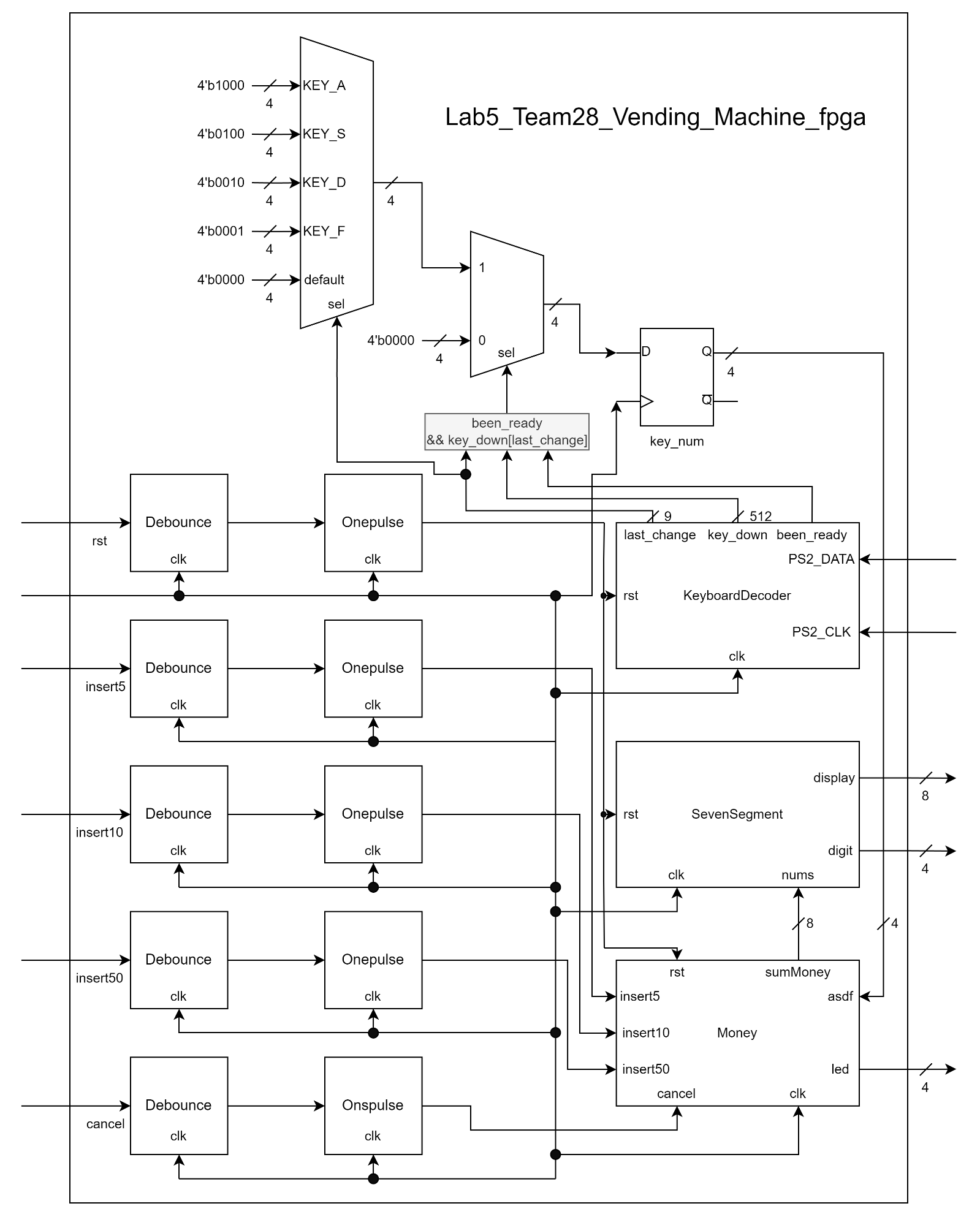


Figure 2.4

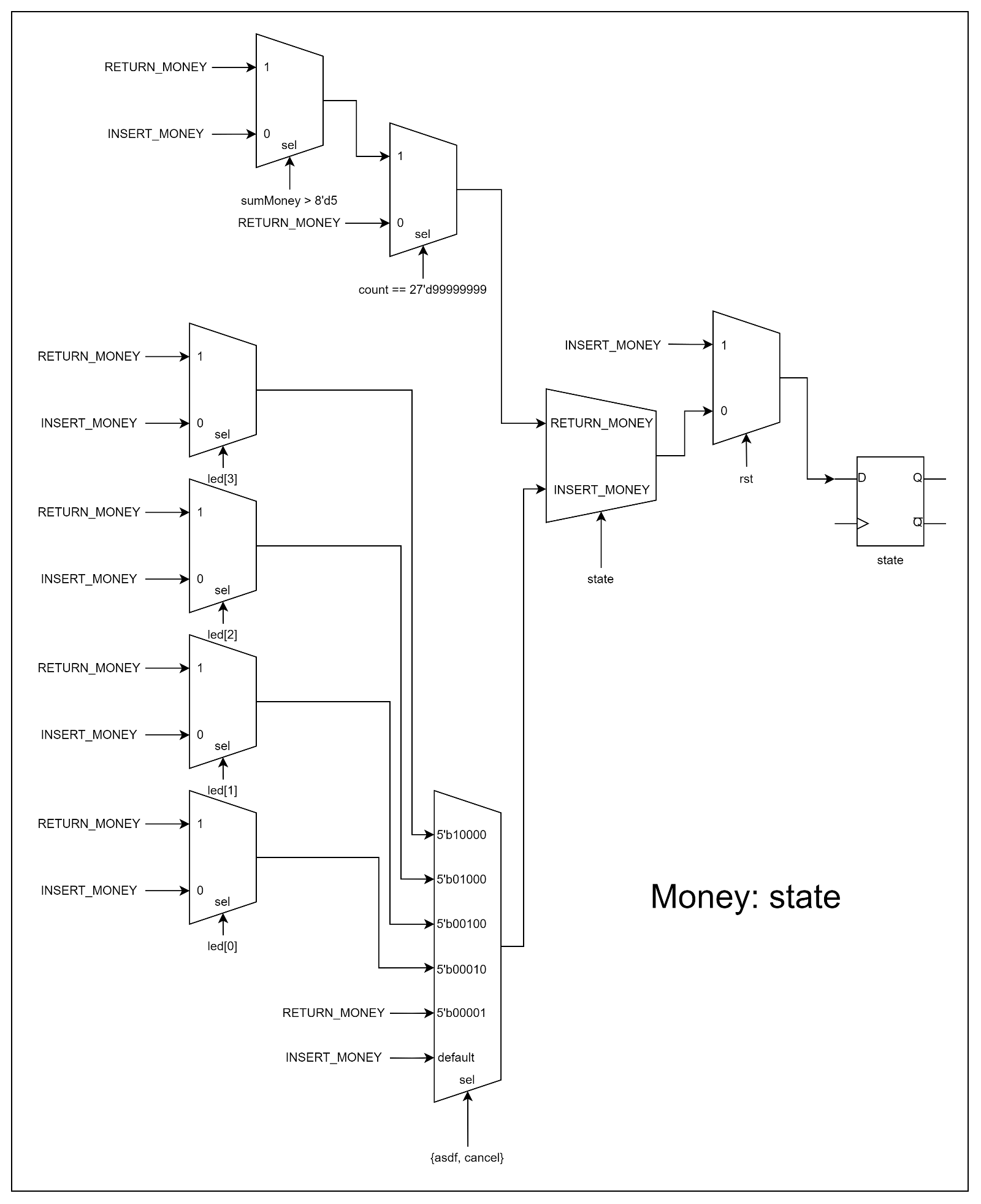


Figure 2.5

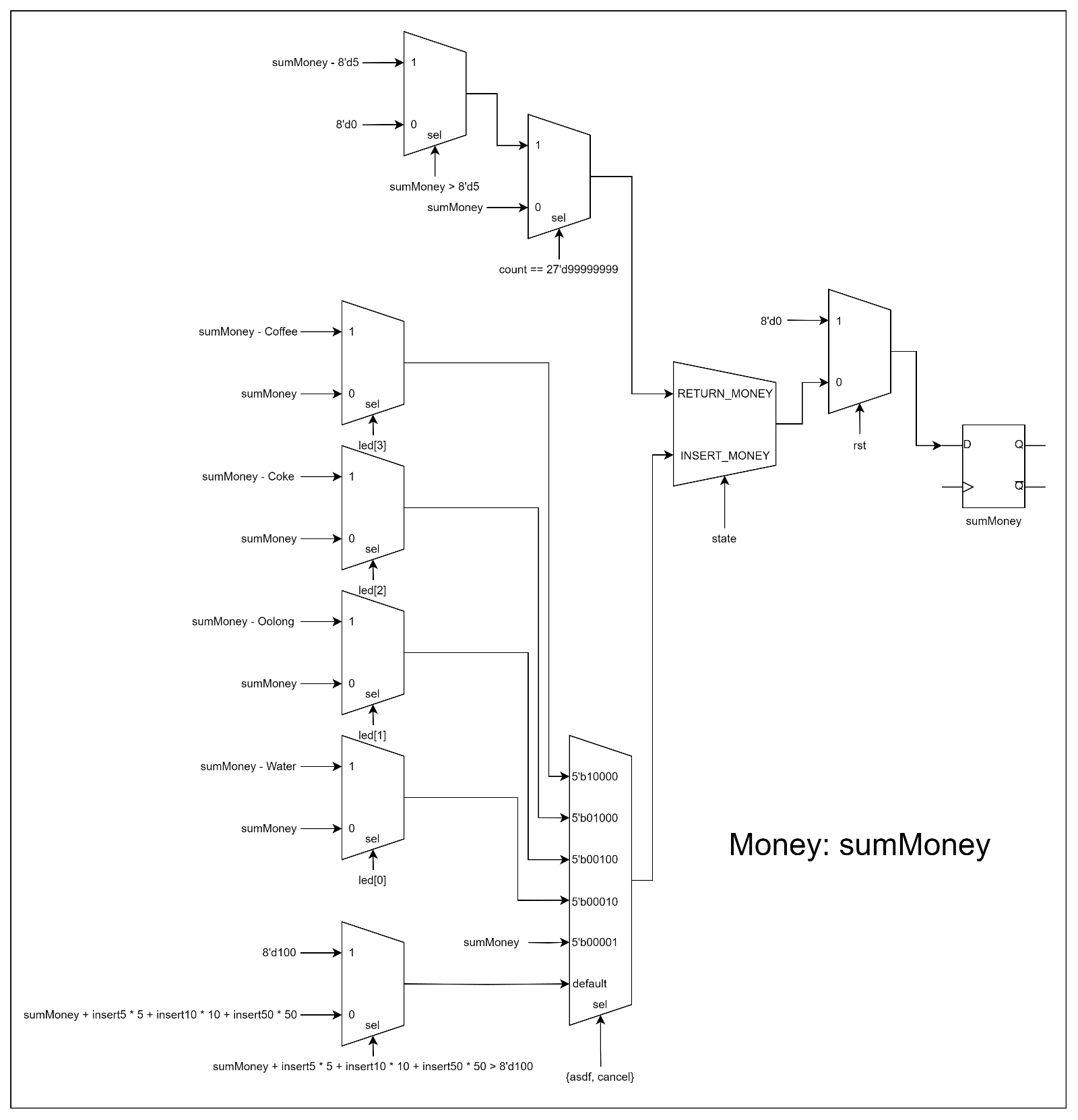


Figure 2.6

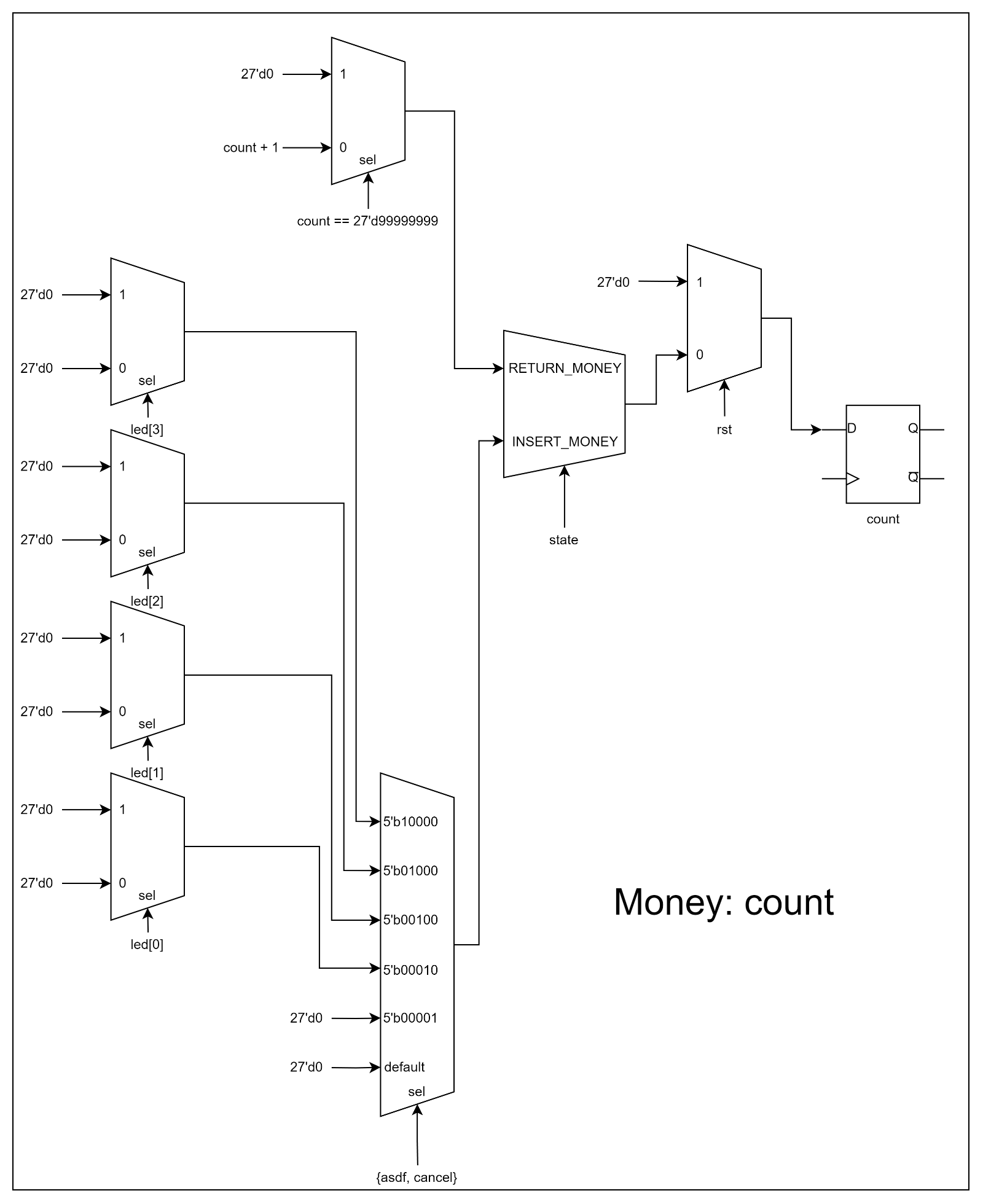


Figure 2.7

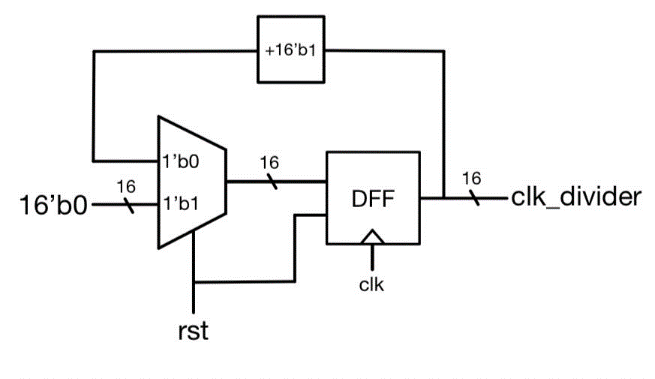
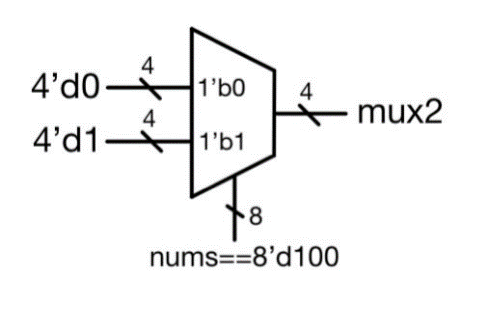


Figure 2.9

Figure 2.8

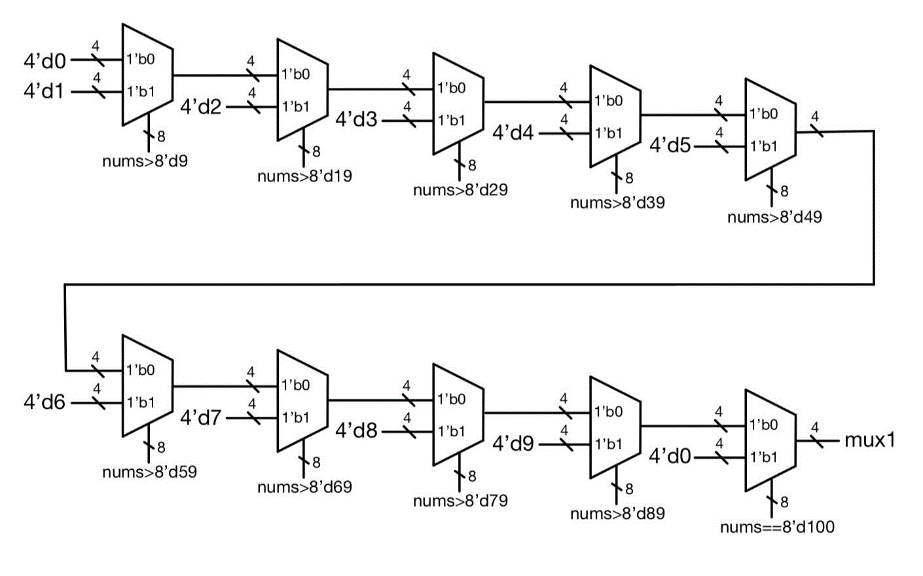
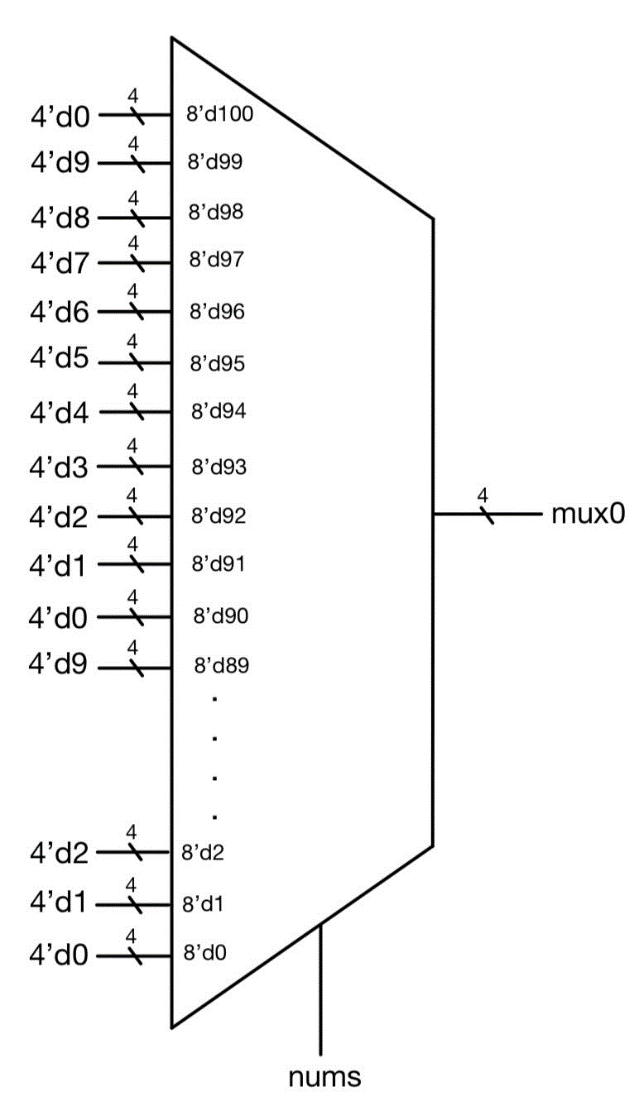


Figure 2.10

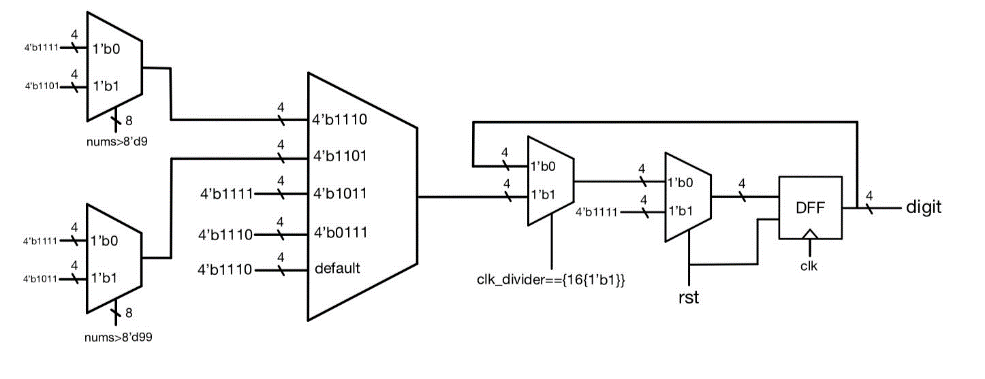
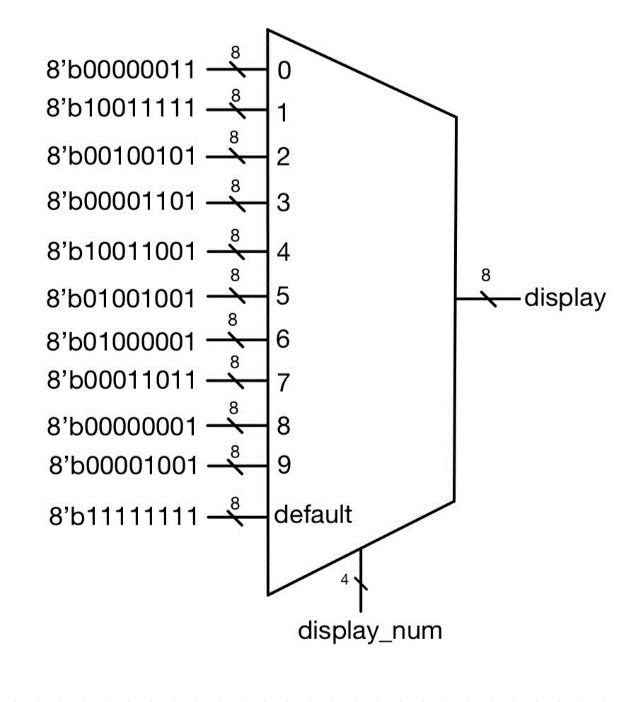


Figure 2.11

Figure 2.12



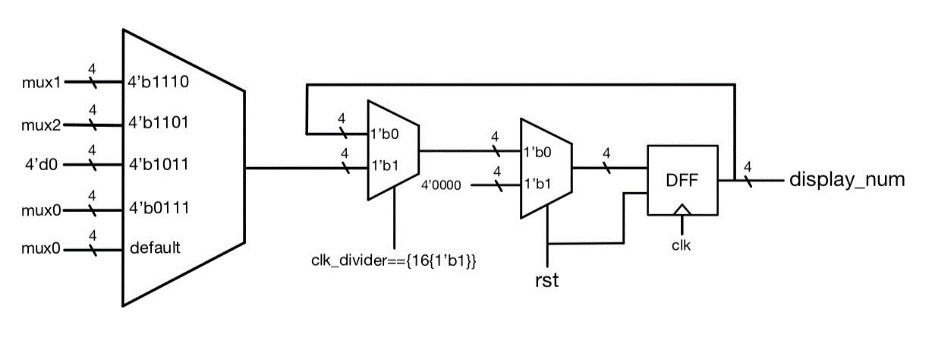


Figure 2.13

Figure 2.14

1. **Explanation**

如**Figure 2.1**所示我將使用狀態分成兩種，第一種是**INSERT\_MONEY**，一開始reset會進到這個狀態，等待使用者投錢，並用七段顯示器顯示使用者投入了多少錢，一旦使用者選擇了飲料而且投進去的錢足夠多，或是使用者按了**cancel**按鈕，則會進入第二種狀態**RETURN\_MONEY**，在這個狀態之下，販賣機對於投錢、選擇飲料和**cancel**按鈕不會做出反應，七段顯示器會以每秒減少5元的速度改變數值，直到**sumMoney**變為0，接者會回到**INSERT\_MONEY**等待後續的操作。整體的電路圖如**Figure 2.4**所示，其中**OnePulse**與**Debounce**是沿用上一個Lab使用的module (**Figure 2.2, Figure 2.3**)。Money這個module的電路圖為**Figure 2.5 ~ Figure 2.7**，大致分為三塊電路：**state, sumMoney, count**。其中**state**用來記錄狀態變化，**sumMoney**用來記錄販賣機內有多少錢，**count**則是計數器，用來devide clock。**SevenSegment**這個module的電路圖為**Figure 2.8 ~ Figure 2.14**，**mux2, mux1, mux0**分別代表百位數、十位數與個位數。