Department of Computer Science
National Tsing Hua University
CS4100 Computer Architecture
Spring, 2024, Homework 5
Due date: 5/26/2024 23:59

1. Assembly Coding

a. Test Result

Testcase 1

Source code — Input type: Assembly

```
# Reference: https://www.geeksforgeeks.org/longest-common
.data
.align 4

# ========testcase1==========
A: .word 1, 2, 3, 2, 1
i: .word 5
B: .word 8, 7, 6, 4
j: .word 4
strOutput: .string "Max length of common subarray: "
# output: Max length of common subarray: 0
# ============================

# ========testcase2==========
# A: .word 1, 2, 8, 2, 1
# i: .word 5
```

Console

```
Max length of common subarray: 0
```

Testcase 2

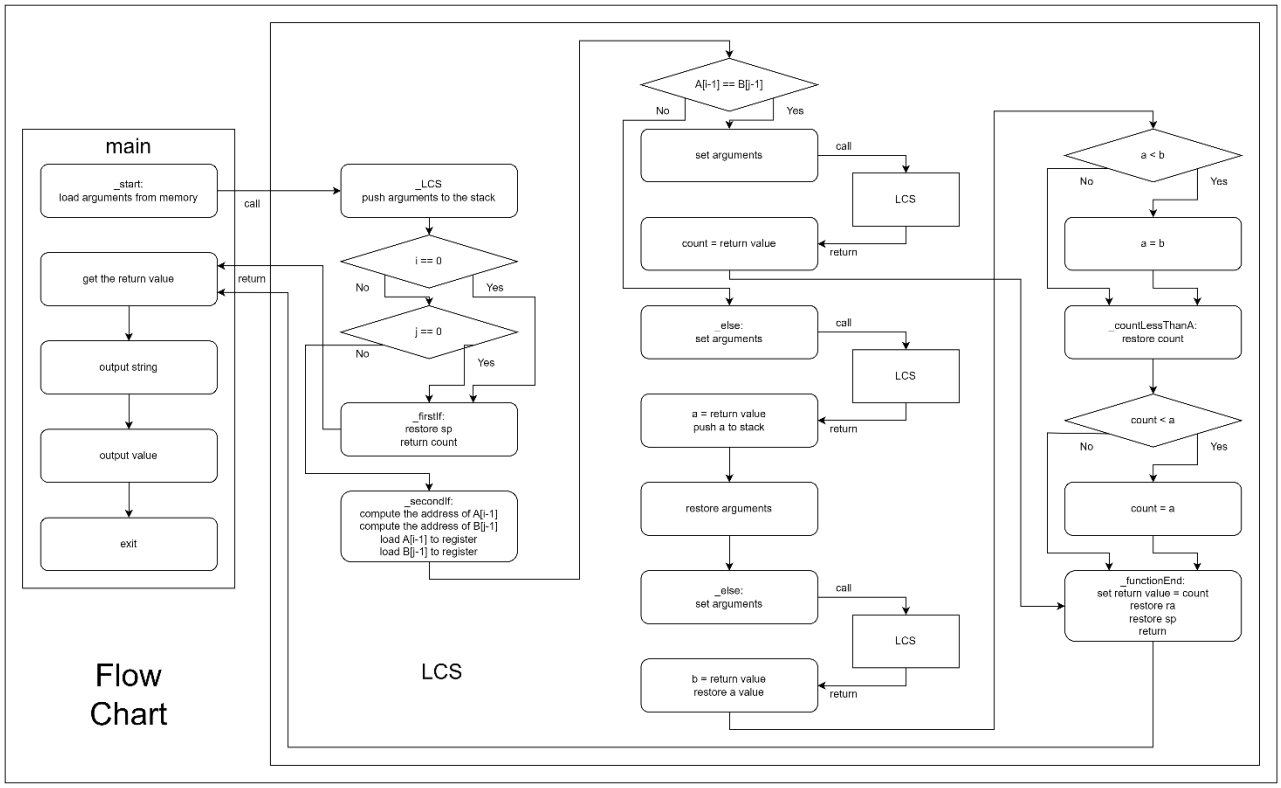
Source code — Input type: Assembly

```
# strOutput: .string "Max length of common subarray: "
# output: Max length of common subarray: 0
# ============================

# ========testcase2==========
A: .word 1, 2, 8, 2, 1
i: .word 5
B: .word 8, 2, 1, 4, 7
j: .word 5
strOutput: .string "Max length of common subarray: "
# output: Max length of common subarray: 3
# ============================

.text
.global _start
```

Console

```
Max length of common subarray: 3
```

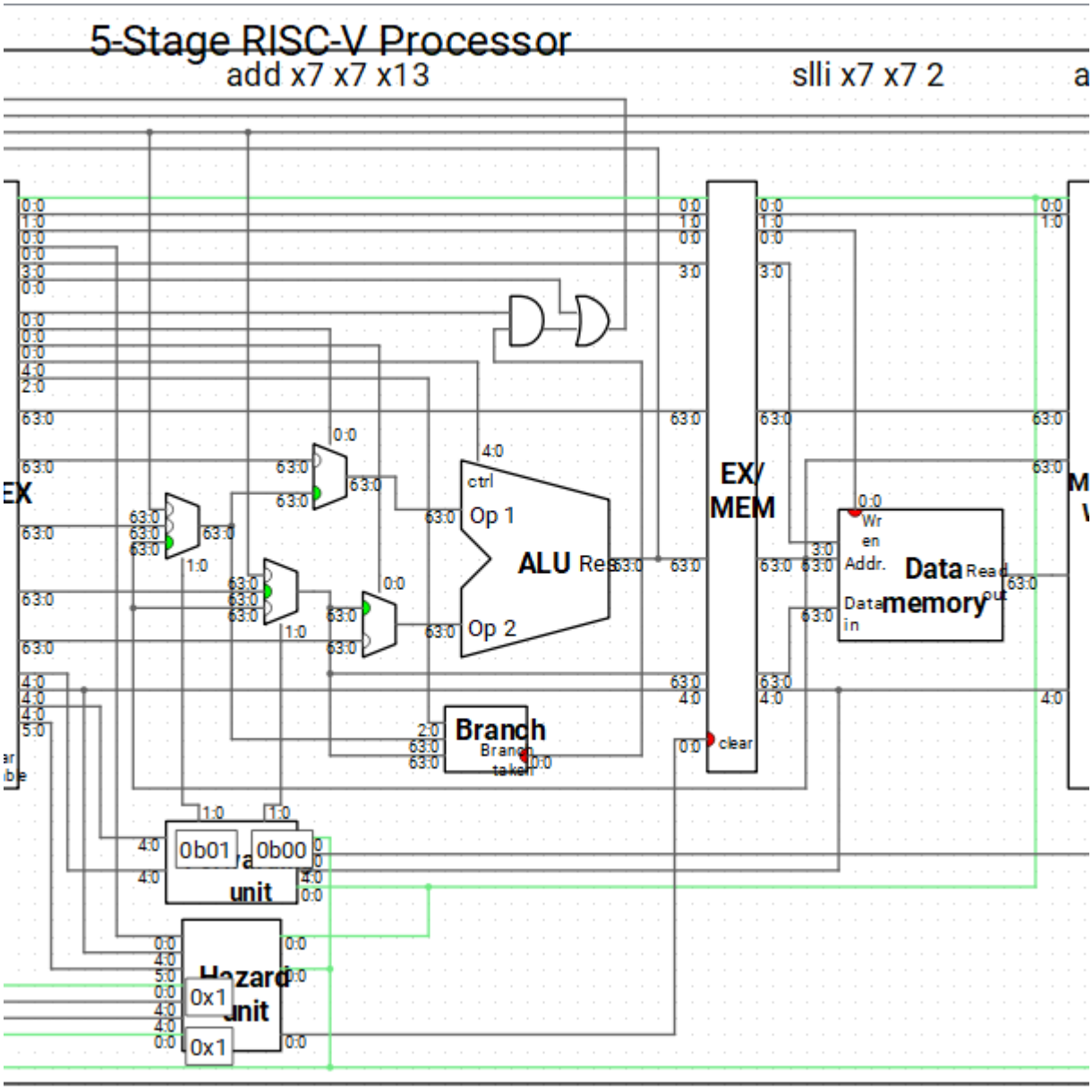
b. Flow Chart



2. Hazard in Your Code

- Type 1:

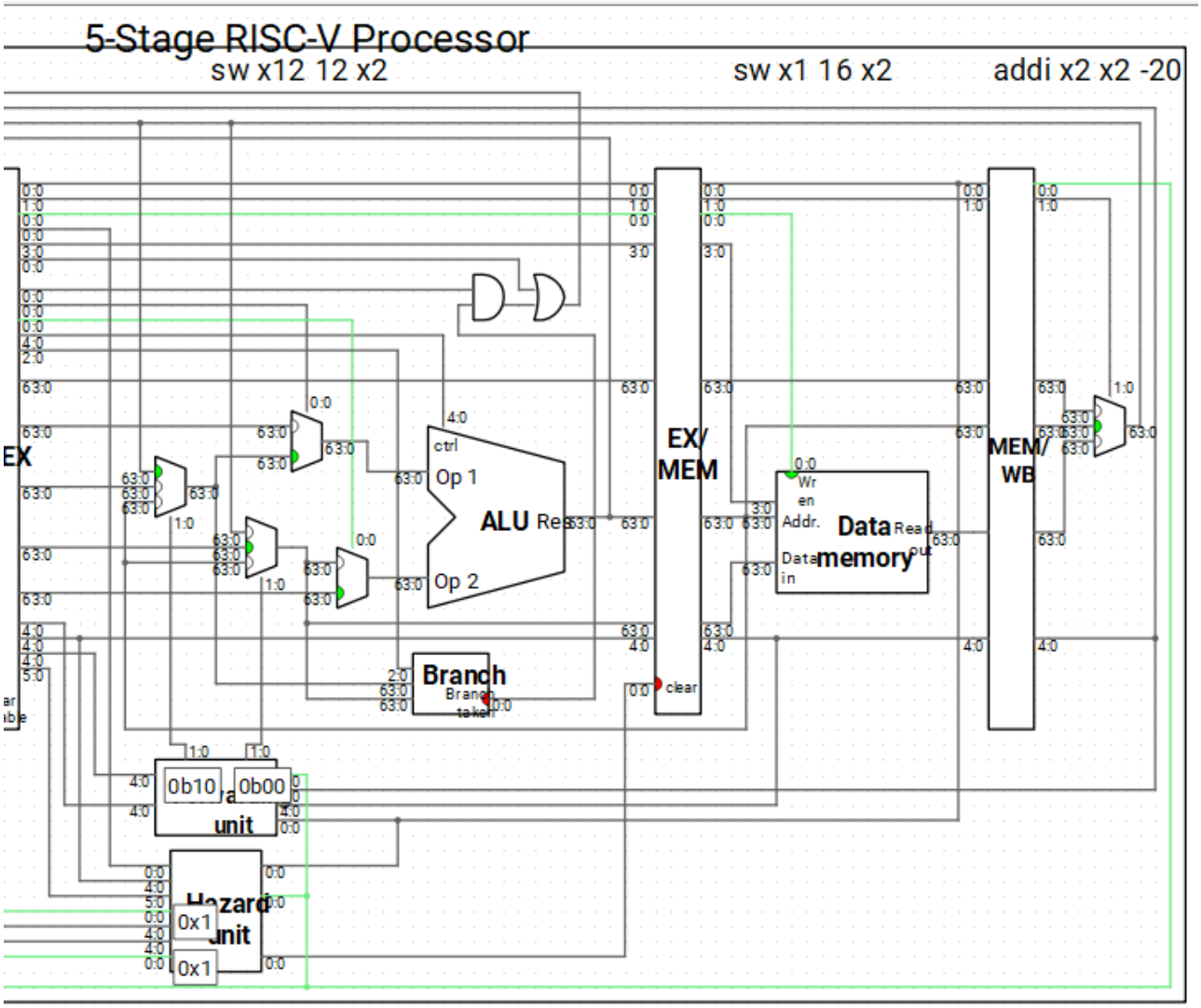
```
81      # count B[i-1] address
82      mv t2, a4
83      addi t2, t2, -1
84      slli t2, t2, 2
85      add t2, t2, a3
```



The register t2 is used to store the result of slli t2, t2, 2. However, t2 is also used in addi t2, t2, -1 as rs1. In Ripes, the processor detects dependency on MEM and EX stages for Type (1). Then, the Forwarding unit sets the control signal of MUX to 0b01 before rs1 to select the t2 value forwarded from the MEM stage to the EX stage.

- Type 2:

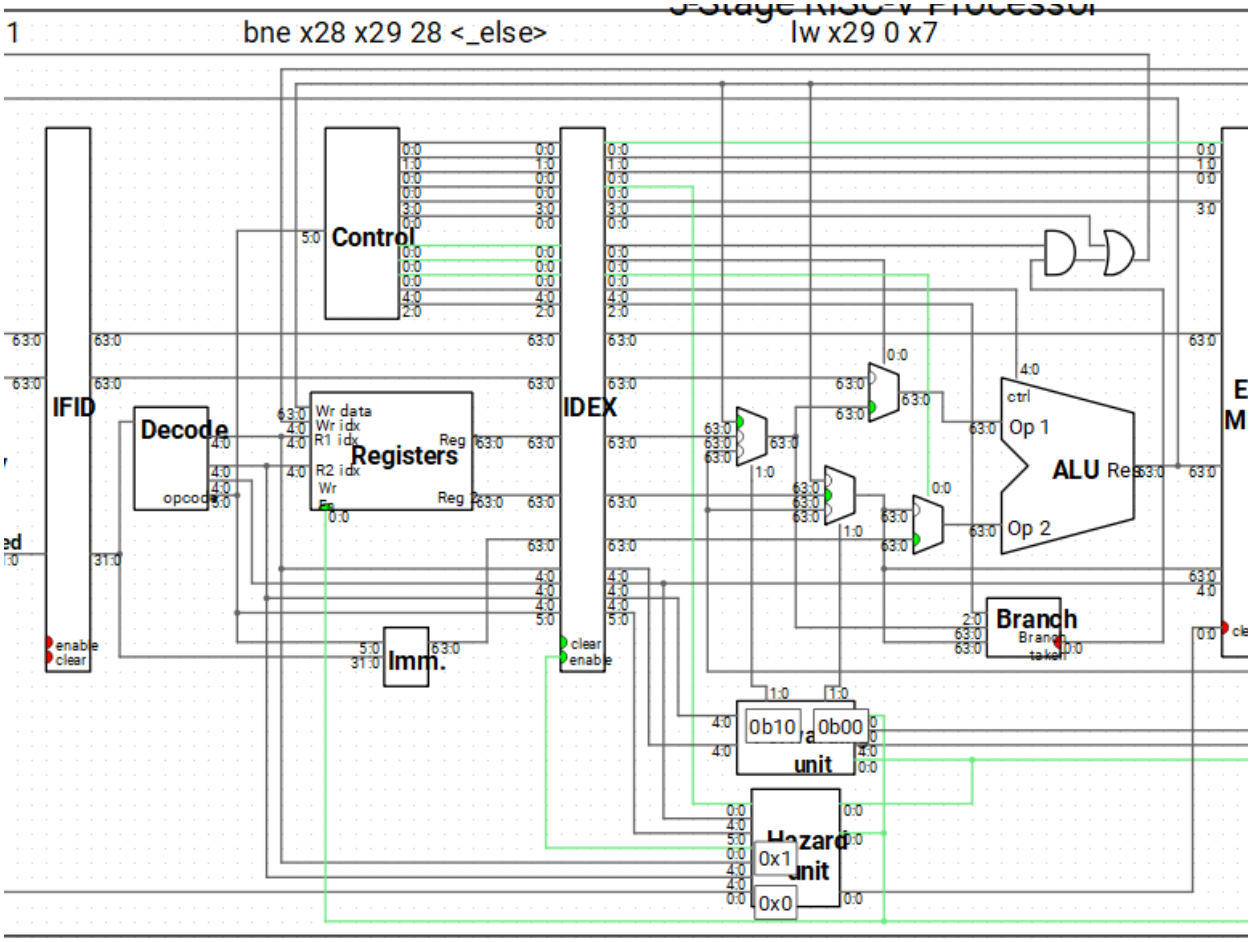
```
55 _LCS:
56     # save data
57     addi sp, sp, -20
58     sw ra, 16(sp) # save return address
59     sw a2, 12(sp) # save i
```

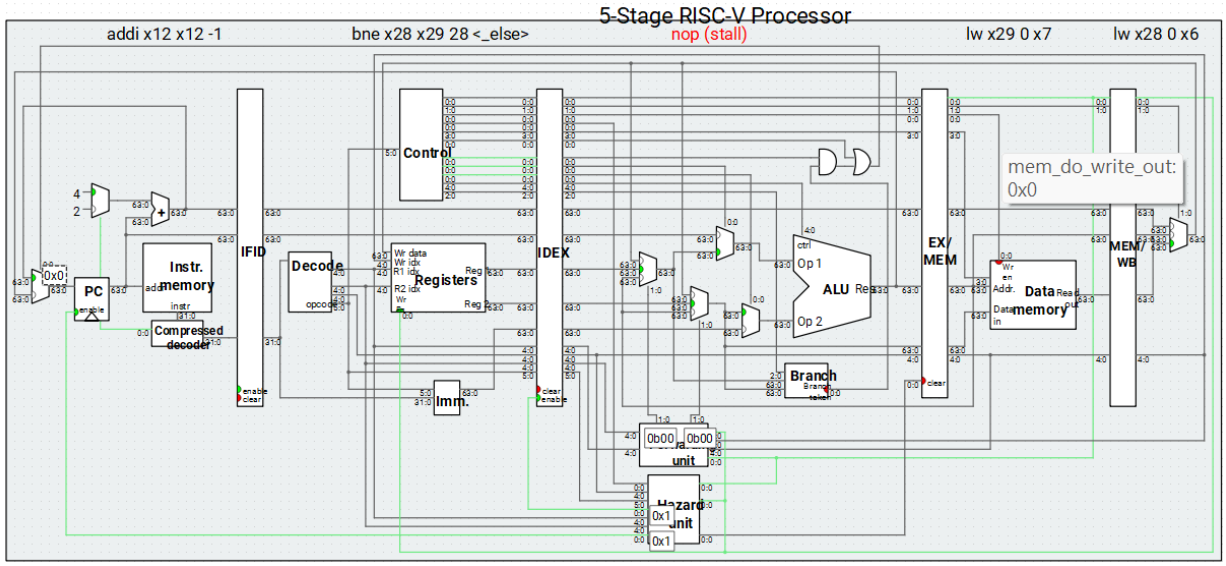


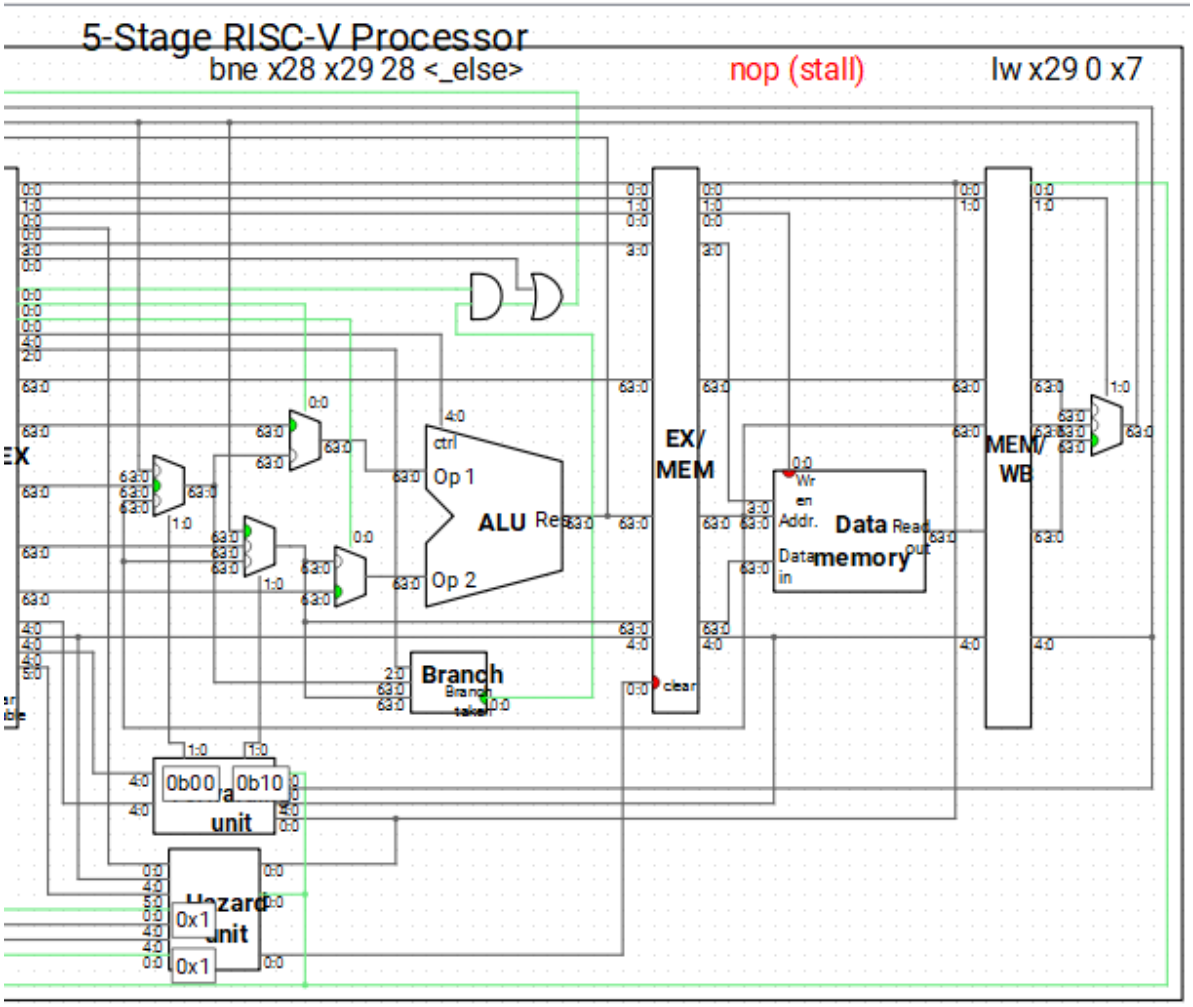
The register sp is used to store the result of addi sp, sp, -20. However, sp is also used in sw a2, 12(sp) as rs1. In Ripes, the processor detects dependency on WB and EX stages for Type (2). Then, the Forwarding unit sets the control signal of MUX to 0b10 before rs1 to select the sp value forwarded from the WB stage to the EX stage.

- Type 3:

```
87      # load A[i-1] to t3
88      lw t3, 0(t1)
89
90      # load B[j-1] to t4
91      lw t4, 0(t2)
92
93      # (A[i-1] != B[j-1]) => _else
94      bne t3, t4, _else
```



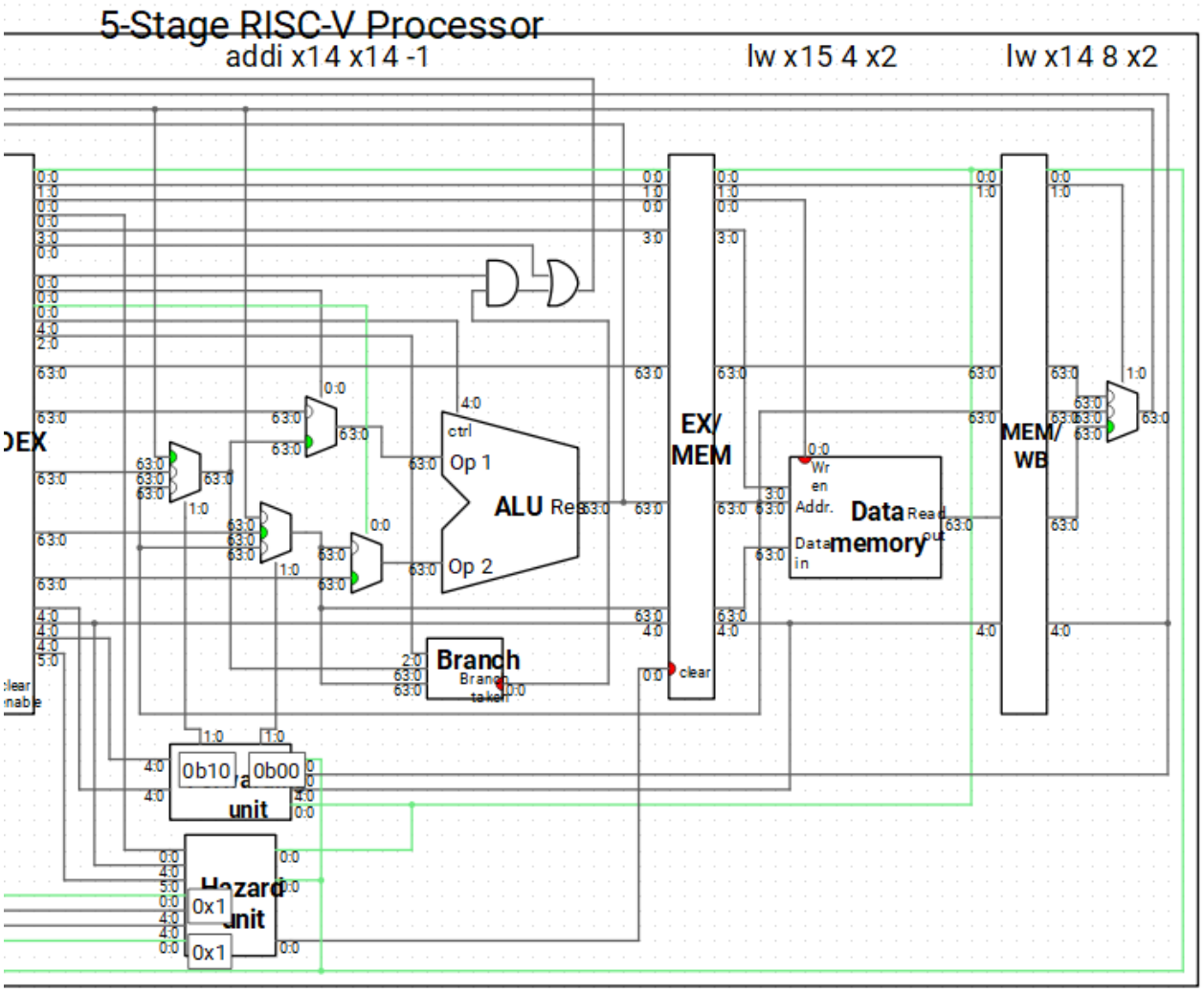




The register t4 is used to store the result of lw t4, 0(t2). However, t4 is also used in bne t3, t4, _else as rs2. In Ripes, the processor detects dependency on ID and EX stages for Type (3). Then, the Hazard unit sets the clear signal of ID/EX register to 1 and the enable signal of IF/ID register to stall a cycle. In the cycle after the next cycle while there is a bubble in Mem stage, the processor detects dependency on EX and WB stages. Then, the Forwarding unit sets the control signal of MUX to 0b10 before rs2 to select the t4 value forwarded from the WB stage to the EX stage.

- Type 4:

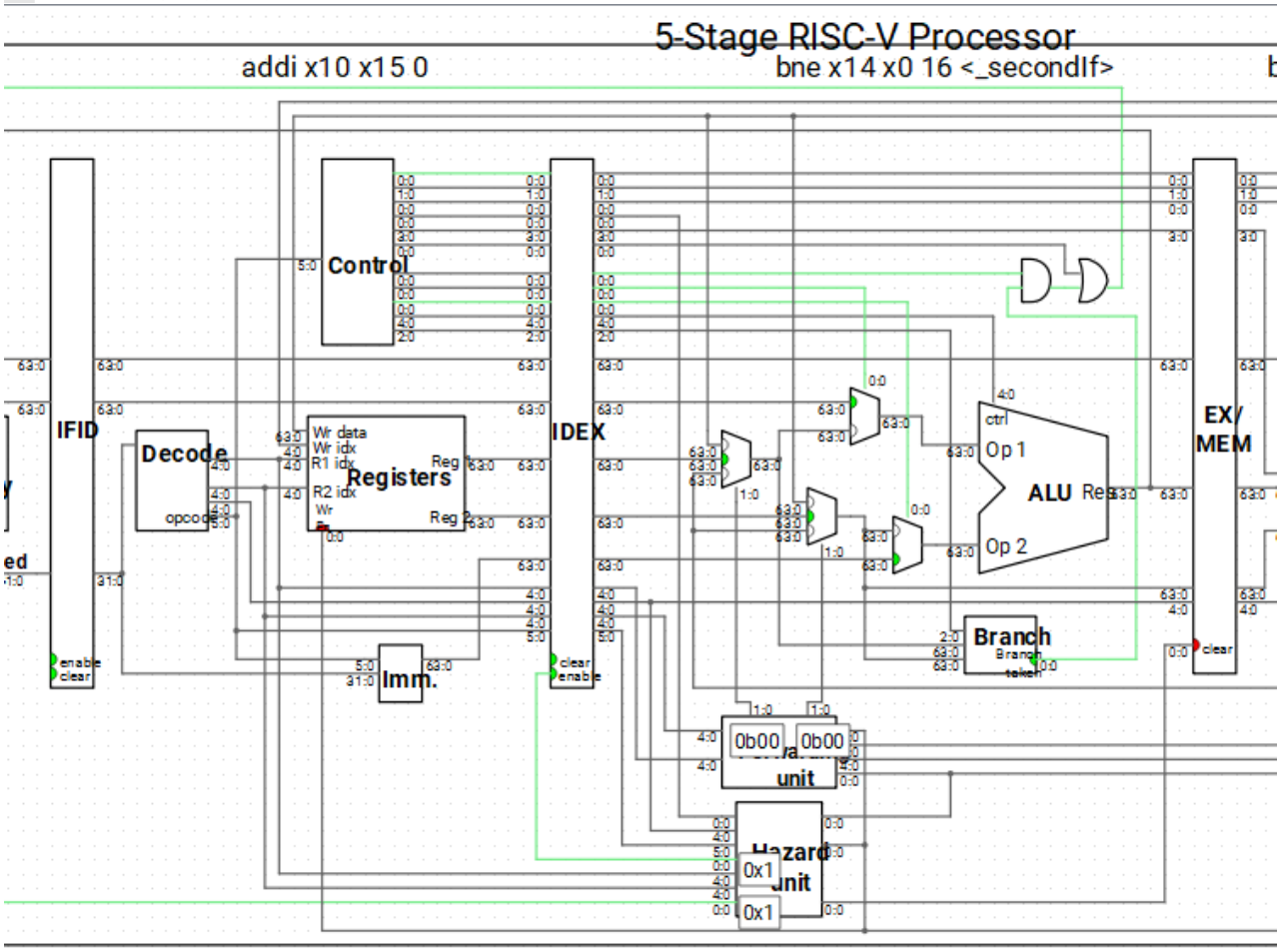
```
114     # restore the arguments
115     lw a2, 12(sp)
116     lw a4, 8(sp)
117     lw a5, 4(sp)
118
119     # b(t6) = LCS(i, j - 1, A, B, 0)
120     addi a4, a4, -1
```

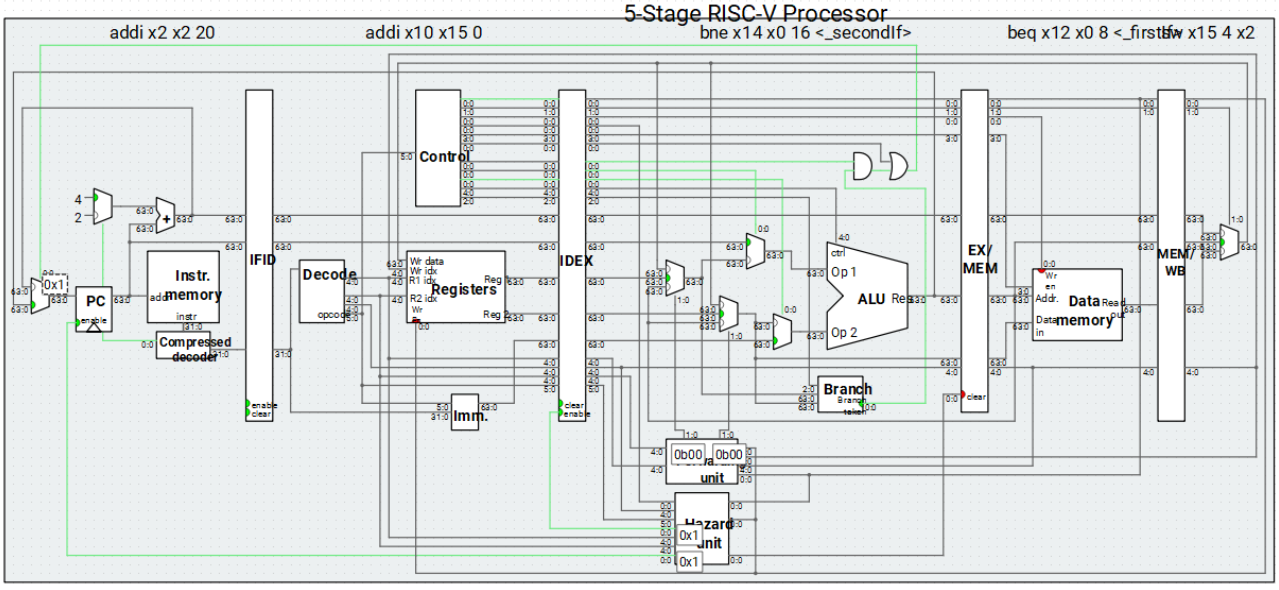


The register a4 is used to store the result of lw a4, 8(sp). However, a4 is also used in addi a4, a4, -1 as rs1. In Ripes, the processor detects dependency on WB and EX stages for Type (4). Then, the Forwarding unit sets the control signal of MUX to 0b10 before rs1 to select the a4 value forwarded from the WB stage to the EX stage.

- Type 5:

```
63      # (i == 0 || j == 0)
64      beq a2, zero, _firstIf # c
65      bne a4, zero, _secondIf #
66
67  _firstIf:
68      # return count
69      mv a0, a5
70      addi sp, sp, 20
71      jr ra
72
73
74  _secondIf:
75      # count A[i-1] address
76      mv t1, a2
77      addi t1, t1, -1
```





If bne a4, zero, _secondIf takes branch, then control hazard will happen. In Ripes, the processor detects dependency on EX stage for Type (5). Then, the Hazard unit sets the clear signals of IF/ID register and ID/EX register to 1 to flush the incorrect instructions. And the control signal of MUX is set to 1 before select the new PC address.