Intel Confidential

Grantley Platform CPU/QPI/Memory Reference Code Release Notes

March 31th, 2014
CRB BIOS Revision: 27.R03
Reference Code Revision: 0.96

Contents

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SUBTITLE – ReleaseNotes.txt
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; Intel Restricted Secret
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; Grantley-EP/EP4S CPU/QPI/Memory Reference Code
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; PURPOSE:
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; This is a revision history for the Grantley-EP/EP4S CPU/QPI/Memory
; Reference Code releases.
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Grantley Platform-EP/EP4S CPU/QPI/Memory Reference Code - Revision 0.96 (27.R03) – Production Candidate 2

Revision 0.96 - 27.R03

Notes:

- This is the Production Candidate Release for Grantley/Haswell-EP and EP4S Reference Code.

Potential issues and enhancements (under investigation)**:**

sighting.id	sighting.title
4987169	SPD CLK Changes with BLCK - fix needed for BLCK OC
4987234	HSX EN - A7 should be disabled in 3 channel configurations
4987335	Setting Thermal Throttling to OLTT is not working
4987392	MM 25.R00 LCK Ch boots mix TRR A/RFH Mode
4987459	HSX Clone: UCECC errors with CAP injection
4987468	HSX Clone: DDR3 UD4 ECC error due to new DDR4 PPR fixed data CMD training pattern
4987509	HSX Clone: MRC: Early Vref Training step should not be run with DDR3
4987510	HSX Clone: DDR4 QR and DDR3 8R LRDIMM CECC due to RxVREF margin loss when RMT enabled
4987528	{BIOS clone of HSX 4906119} Reset glitch on RDIMM (post register) may cause boot failure

Sighting fixes and enhancements: (fixes and enhancements since last RC release):

ID	RC	Title
CR_15572	YES	4987456: HSX Clone: DRAM RAPL DYNAMIC RANGE: Add BIOS option DRAM_RAPL_EXTENDED_RANGE
CR_15455	YES	4987468: HSX Clone: DDR3 UD4 ECC error due to new DDR4 PPR fixed data CMD training pattern
CR_15377	YES	4987444, 4987439: Using 25.R01 BIOS on 2S systems, the mmio_rule_3 register has different values between sockets
CR_15363	YES	4987437: Need MRC to always set imc_apm_override_enable=1 due to pcode pdwn_idle_cntr too low bug

Grantley Platform-EP/EP4S CPU/QPI/Memory Reference Code - Revision 0.90 (25.R01) – Production Candidate

Revision 0.90 - 25.R01

Notes:

- This is the Production Candidate Release for Grantley/Haswell-EP and EP4S Reference Code.

Potential issues and enhancements (under investigation)**:**

sighting.id	sighting.title
4168273	BIOS must lock down all sensitive registers in PCH config space before writing to new PDCWE opt-in bit
4986802	RAS: RANK Sparing and Mirror Fail over not working when EMCA and EMCACSMI Setup option is enabled
4987052	Program RCUTLCTRLCONFIG0_CR_R3GLERRCFG.MaskR3FatalError to 0xf
4987149	System may not be recoverable (it may be bricked) if power is pulled during Variable Reclaim operations
4987152	Selftest failed when D30 F3 is hidden
4987162	Add TXT S3 resume support in UP/MP case by calling LockConfig on BSP of all sockets
4987208	PKGC: Need to set QPI L1 as an entry criteria always
4987232	HSX Clone: Sparing SMI handler needs to disable patrol scrub before sparing and restore patrol scrub after complete
4987287	Low Margins seen for DDR3 QR DIMM's
4987378	PROMOTE from haswell_server: BIOS stopped with Fatal Error early in POST
4987380	MRC: W/A for 3DPC LRDIMM ZQCAL + CAP
4987382	MRC: Need dis_opp_cas=1 set for TRR/pTRR + ISOC enabled to avoid UCECC
4987437	HSX Clone: PRQ required: Need MRC to always set imc_apm_override_enable=1 due to pcode pdwn_idle_cntr too low bug
4987439	DisableCacheAsRam in CpuPei should not clear MMIO_RULE 7 on EX 3 on EP
4987444	ESCALATE from hexaii_hsx_mock:Using 25.R01 BIOS on 2S systems the mmio_rule_3 register has different values between sockets
4168273	BIOS must lock down all sensitive registers in PCH config space before writing to new PDCWE opt-in bit
4986802	RAS: RANK Sparing and Mirror Fail over not working when EMCA and EMCACSMI Setup option is enabled
4987420	PROMOTE from haswell_server: injecting UCE memory error with WHEA tools causes system to hang in SMI handler
4987418	PROMOTE from haswell_server: injecting LLC correctable error with emca causes system to soft hang
4987402	Implement work around for TI A3 DDR4 register CMD/CLK training failure
4987392	MM 25.R00 LCK Ch boots mix TRR A/RFH Mode
4987162	Add TXT S3 resume support in UP/MP case by calling LockConfig on BSP of all sockets

Sighting fixes and enhancements: (fixes and enhancements since last RC release):

ID	RC	Title
CR_15275	YES	4987382: MRC: Need dis_opp_cas=1 set for TRR/pTRR + ISOC enabled to avoid UCECC
CR_15274	YES	4987281: HSX Clone: Odin channel length difference exposes unplanned additional latency with 2:2. Need io_lat_io_comp += 2
CR_15229	YES	4987294: Need to keep MMIO_RULE to cover 64MB below 4GB (rule 3 on EP, rule 7 on EX)
CR_15203	YES	4987269: Warm Reset : DDR3 Lockstep does not restore CH3 TxDqs , TxDqDqs
CR_15148	YES	4987325: Restore lt lock config on S3 resume
CR_15145	YES	4987314: Isoch + TRR Mode A workaround
CR_15125	NO	4987327: Add ME9 PC build 9.1.0.1110 to BIOS PC image
CR_15141	YES	4987326: S3 Bootscript Defects
CR_15115	YES	4987088: S3 not restoring all needed registers
CR_15123	YES	4987315: Systems fail to boot with LRDIMM
CR_15053	YES	4987262: Need mh_output_en=1 set to allow TSOD polling to work correctly
CR_15047	YES	4986813: Production Release MRC will halt RDIMMs with non-production Registers Rev
CR_14972	YES	4987206: MRC Training: Cmd/Clk Training and RMT Cmd violate latest DDR4 Jedec spec for PPR Entry
CR_14971	YES	4987204: DDR4 UDIMM 2DPC CA VREF offset

Grantley Platform-EP/EP4S CPU/QPI/Memory Reference Code - Revision 0.84 (23.R02) – Beta Release 5

Revision 0.84 - 23.R02

Notes:

- This is the Beta Release for Grantley/Haswell-EP and EP4S Reference Code.

Potential issues and enhancements (under investigation)**:**

sighting.id	sighting.title
4166863	Memtest failure of secondary channel in mirrored mode causes CATERR
4986242	WHQL: Aztec City does not meet S3 resume time requirement. (Single Proc)
4986539	MRC: Phase shedding not programed when there is only one DRAM0 VR
4986802	RAS: RANK Sparing and Mirror Fail over not working when EMCA and EMCACSMI Setup option is enabled
4986927	CLONE from HSX: Refile 273405: During PkgC6/S3 exit CKE is unknown for a time window at VccpqPwrGood/PllLock assertion
4987013	MRC w/a for s4905517 (part2): W/A for TRR+PageTableAliasing doesn't cover all configs needed
4987192	ZQcal wa - pcode mbx channel mask not set correctly for all configs
4987201	MRC: Need thrt_allow_isoch=1 to avoid silent data corruption due to PRE sent during Powerdown
4987204	DDR4 UDIMM 2DPC CA VREF offset
4987206	[HSX] MRC Training: Cmd/Clk Training and RMT Cmd violate latest DDR4 Jedec spec for PPR Entry

Sighting fixes and enhancements: (fixes and enhancements since last RC release):

ID	RC	Title
CR_14574	YES	4987012: MRC: Page table aliasing bit should be set to 1 for some configs and option removed from customer setup options
CR_14573	YES	4986989: DDR4 RDIMM CLK RCOMP values not being set correctly
CR_14572	YES	4987013: W/A for TRR+PageTableAliasing doesn't cover all configs needed
CR_14571	YES	4986776: HSX LRDimm 2DPC 2133 Showing Huge RxVref Asymmetry
CR_14570	YES	4987038: Reading Board ID fails when using PDR region second time
CR_14523	YES	4986875: After PBO while in S3 SUT does will not return to S0 with Power Button
CR_14487	YES	4987010: DIMM Instability during first Jedec Init
CR_14482	YES	4986610: ESCALATE from hexaii_hsx_mock:POR: Isoc not supported on socket B3 (EN segment)
CR_14475	YES	4986922, 4986967: nvida card fails to resume S3 on Odin; S3 resume fail while disabling onboard VGA on Aztec CRB
CR_14469	YES	4986820: R0-C0 Dual socket configuration issue
CR_14450	YES	4986939: RCOMP_TYPE Bit conflict and incorrect variable used in code.
CR_14438	YES	4986978: Arandas LRDIMM fail to boot

CR_14435	YES	4986960: Kahuna System CatErred running hsxMemicalRAS with CAP injection sporadically
CR_14385	YES	4986782: ASPM being disabled in Linux b/c of wrong setting in ACPI tables
CR_14382	YES	4986775: PROMOTE from haswell_server: BIOS option for max paging size 2M is broken
CR_14368	YES	4986719: MM DDR3 UDIMM Memtest fail
CR_14358	YES	4986909: The HSX BUGECO 273245 is not implemented properly, impacts CRB build
CR_14331	YES	4986844: LRDIMM 3DPC/Encoded mode failing memtest after lockstep timing adjustment
CR_14330	YES	4986021: Memory controller register programming check mismatch
CR_14328	NO	4986398: MayanCity platform with add-in NICs with enabled legacy PXE OROMs got hung
CR_14317	YES	4985672: DIMM population rule not consistant with Grantley RC users' guide

Grantley Platform-EP/EP4S CPU/QPI/Memory Reference Code - Revision 0.83 (22.R01) – Beta Release 4

Revision 0.83 - 22.R01

Notes:

- This is the Beta Release for Grantley/Haswell-EP and EP4S Reference Code.

Potential issues and enhancements (under investigation)**:**

sighting.id	sighting.title
4165532	BDAT data is too large to fit into the current HOB
4166863	Memtest failure of secondary channel in mirrored mode causes CATERR
4985672	DIMM population rule not consistant with Grantley RC users' guide
4985793	Soft reset path for LRDIMM
4986128	Reference Code: MRC doesn't handle training failures
4986148	Memory error counter overflow causes both SMI and CSMI
4986242	WHQL: Aztec City does not meet S3 resume time requirement. (Single Proc)
4986539	MRC: Phase shedding not programed when there is only one DRAM0 VR
4986691	S3: Patrol Scrub Address is Incorrect on resume with only HA1 populated
4986766	MRC Training: GetMultiVref does not tolerate TxVref eye height < 8
4986776	HSX LRDimm 2DPC 2133 Showing Huge RxVref Asymmetry
4986800	RAS: Memory UCE Error didn't generate SMI when EMCA Setup option is disabled.
4986802	RAS: RANK Sparing and Mirror Fail over not working when EMCA and EMCACSMI Setup option is enabled
4986957	QPI RATIO changes based on PEG Ratio for Overclocking on HEDT
4987010	MRC: HSX Clone: EP R0 CH0 3DPC RA16 DIMM Instability during first Jedec Init
4987012	MRC: Page table aliasing bit should be set to 1 for some configs
4987013	MRC w/a for s4905517 (part2): W/A for TRR+PageTableAliasing doesn't cover all configs needed
4987045	MRC hangs when MT enable and DDR Init fail
4987055	MRC: HSX incorrectly has DIMM level power throttling enabled by default need MRC to disable
4987060	HSX Clone: CMD / ADDR training pattern may inadvertently enter PPR mode

Sighting fixes and enhancements: (fixes and enhancements since last RC release):

ID	RC	Title
CR_14475	YES	4986922, 4986967: nvidia card fails to resume S3 on Odin; S3 resume fail while disabling onboard VGA on Aztec CRB
CR_14382	YES	4986775: PROMOTE from haswell_server: BIOS option for max paging size 2M is broken
CR_14306	YES	4985793: Soft reset path for LRDIMM
CR_14295	YES	4986733: Odin spontaneous video fail while booting to RH 6.4
CR_14291	YES	4986617: Program Save state MSR for all threads
CR_14290	YES	4986840: Wrong bitwise operations in

		grantleysocketpkg\library\memoryqpiinit\mem\MemRAS.c & MemRecEnable.c
CR_14289	YES	4986839: Wrong bitwise operations in grantleysocketpkg\library\memoryqpiinit\mem\MemCmdClk.c
CR_14288	YES	4986838: Wrong bitwise operations in grantleysocketpkg\library\memoryqpiinit\mem\InitMem.c
CR_14281	YES	4986822 RCOMP in PkgC exit causing failures, BIOS needs to move Disabling PKGC Rcomp
CR_14275	YES	4986336: fixes for: Address Translation with Channel Hashing enabled and DDR4 open page secondary mapping
CR_14266	YES	4986584: RAS: eSMM support is incomplete
CR_14259	YES	4986833: JEDEC Single-Ended Clock Spec Violation on UDIMM
CR_14245	YES	4986886: MRC Training: DDR0_MA[17] missing from package delay table
CR_14229	YES	4165532: BDAT data is too large to fit into the current HOB
CR_14226	YES	4986858: Mayan, Aztec and Arandas fail to perform a warm reset or S3
CR_14224	YES	4986132: MRC failed RdDqDqs training after dimm/rank mapped-out
CR_14202	YES	4986767: Initial clock delays incorrect for LCC parts
CR_14079	YES	4986275: Fast Boot Paths need 3 month timeout
CR_14078	YES	4986685: Cannot set RAID Device ID to RSTe value in RC 0.80
CR_14075	YES	4986683: BIOS must not disable all MCs on a CPU when CPU is not populated with DIMMs
CR_13999	YES	4986548: MRC needs to apply SPD rounding rules and newer MR0 CL encodings
CR_13956	YES	4985932: Need RMT added to MRC cold fast boot

Grantley Platform-EP/EP4S CPU/QPI/Memory Reference Code - Revision 0.82 (20.R04) – Beta Release 3

Notes:

- This is the Beta Release for Grantley/Haswell-EP and EP4S Reference Code.
- **[Fixed] S3:** to perform S3, the user must disable Command Address Parity error checking. The BIOS default is that this feature is enabled (4905686).
- **[Fixed] C-State enabled OS:** To use SPS ME FW, Package C-states need to be disabled if you are booting a C-State enabled OS to avoid random hangs. The BIOS default setting is enabled (4905544).
- **Wellsburgs A-step silicon:** The v0.80 collateral does not support boot with Wellsburg A-step silicon. Customers that still have WBG-A0 silicon should remain on v0.79 code base.
- **[Fixed] DIMM information table:** DIMMINFO reporting in the serial message debug log (4986323, 4986484)
  - It has been found that reference code versions 0.78, 0.79, and 0.80 will not print the DIMMINFO table in the serial log if SDBG_MIN is included in the setting for serialDebugMsgLvl. This includes the SDBG_MIN+SDBG_MAX option.
  - It is recommended to avoid use of SDBG_MIN or SDBG_MIN+SDBG_MAX when running RMT, or if capturing the DIMMINFO table is otherwise desired.
  - This will be fixed in a future release of the reference code.
  - Note that the CRB BIOS uses the SDBG_MIN+SDBG_MAX value when choosing “Maximum” in the BIOS setup menu, so the DIMMINFO table will be missing in the serial output. This will be fixed in a future release of the CRB BIOS.

Potential issues and enhancements (under investigation):

sighting.id	sighting.title
4166841	MRC Rank disable is not functioning properly for slot 1
4166856	Write Fly By fails on Channel 1 after Rx Dq/Dqs fails on Channel 0
4166863	Memtest failure of secondary channel in mirrored mode causes CATERR
4985793	Soft reset path for LRDIMM
4985982	PROMOTE from presighting 454195 Micron-TI DDR4 1333 4Gb failed to boot
4986128	Reference Code: MRC doesn't handle training failures
4986132	Reference code: MRC failed RdDqDqs training after dimm/rank mapped-out
4986148	Bugeco 256630: Memory error counter overflow causes both SMI and CSMI
4986256	BIOS Mailbox: FAST_RAPL_NSTRIKE_PL2_DUTY_CYCLE (0x9d) isn't hooked up and doesn't have an option
4986310	HSX Clone: PerfWG: Recommend changing the BIOS default for QPI General Configuration for EP 2S to enable Early snoop
4986409	mirrorScrub should be enabled by default when mirror mode is enabled
4986429	W/A Incorrect: Memory: Chip select tristating too early after Self Refresh Entry
4986476	ESCALATE from hexaii_hsx_mock:C0: BIOS needs to set isoc registers differently on sockets 1..N
4986539	MRC: Phase shedding not programed when there is only one DRAM0 VR

4986547	CLONE from HSX: Clone from HSX Sighting:[C0] CAP Injection at 2133 2:2 results in memicals miscompares
4986550	ESCALATE from hexaii_hsx_mock:M0: Odin: pxpd00f0_perfctrlsts_0.vc1m_nosnoopopdis is 1 but should be 0 for isoc check
4986587	CPU RC distinguishes whether processor supports HT with wrong CPUID.(EAX=01h):EDX[28] function
4986648	MRC: Need to use pTRR + 2x refresh on all LRDIMM TRR configs
4986682	Investigation of NEM size increase to 3MB
4986683	PKGC Modification: BIOS must not disable all MCs on a CPU when CPU is not populated with DIMMs
4986695	DDR3 Row Hammer Free DIMM Checking
4986762	PKGC: BIOS needs to enable qpi clock gating by default
4986767	ESCALATE from hexaii_hsx_mock:SM3_2 / SM3_BIOS Fail w/ Memory Errors
4986791	Phase I- wrning message only ---production release MRC will only support CS-level memory Register and Buffer components
4986802	RAS: RANK Sparing and Mirror Fail over not working when EMCA and EMCACSMI Setup option is enabled
4986829	RAS: system hang on subsequent boot after injecting a memory uncorrectable error
4986833	HSX Clone: JEDEC Single-Ended Clock Spec Violation on UDIMM

Sighting fixes and enhancements: (fixes and enhancements since last RC release):

ID	RC	Title
CR_13897	YES	4167153: S3 MTRR programming not optimal
CR_13890	YES	4986537: eMCA ELOG contains insufficient information to be useful
CR_13889	YES	NO SIGHTING: HSX C0 ucode Patch mef306f2_0000000a
CR_13883	YES	4986593: Reference Code: incomplete implelemtation for EVMode
CR_13882	YES	4986695: DDR3 Row Hammer Free DIMM Checking
CR_13865	YES	4985795: Write fly by error handling
CR_13861	YES	4986624: disable memory PPD code in MRC
CR_13858	YES	4986655: HSX Clone: EX: Memic hangs with BT TO, TOR TO, and 3-Strike
CR_13841	YES	4986611: PerfWG: CRB BIOS needs to enable MMC bank XOR and HSX+ Amap
CR_13840	YES	4986522: HSX C0 NTB: BIOS should set NTB port as problematic(problematic_port_for_lock=1)
CR_13838	YES	4986248: CLONE from HSX: Malicious SW could negatively impact servers availability due to incorrect default value of IIO_CR_ERRPINDAT_0_5_2_CFG
CR_13836	YES	4986648: MRC: Need to use pTRR + 2x refresh on all LRDIMM TRR configs
CR_13691	YES	4986539: MRC: Phase shedding not programed when there is only one DRAM0 VR
CR_13688	YES	4986523: Enabling and disabling ISOCH has no effect on DRAM_POWER_INFO.DRAM_MIN_PWR
CR_13687	YES	4986014: HSX Clone: Crashdump 0x91 PECI completion code after an IERR injected with a real PCIe card
CR_13684	YES	4986411: BIOS sets Thermal Throttling "Disabled" to "OLTT"

CR_13681	YES	4986427: HSX Clone: CLONE ivytown: [PCIE_DMI]: SLD bit in uncerrsts not logged on DMI even though link is down
CR_13679	YES	4985755 poisoned_tlp_detect_mask bits are not set correctly wheter PoisonEnable is enabled/disabled
CR_13666	YES	4986369: [HSX C0] MRC: LRDIMM encoded chip select mode requires tcstagger register setting change
CR_13665	YES	4986340: Add Usb2PortLength call to Grantley PCH RC
CR_13647	YES	4986613: MRC Training: Advanced Centering Vref Eye Assumption Putting Dimms in Bad State
CR_13643	YES	4986469: MRC: DDR4 LRDIMM IDT A0 Buffer workarounds should be removed
CR_13642	YES	4986533: Grantley BIOS fail to boot when DIMM install at socket #1 only
CR_13641	YES	4986323: Need dimminfo turned on for serial output in CRB bios with minimal messages
CR_13601	YES	4986167: PROMOTE from haswell_server: ESX 5.5.0 GA reboots (shutdownbreak) during installation

Notes:

- This is the Beta Release for Grantley/Haswell-EP and EP4S Reference Code.
- **S3:** to perform S3, the user must disable Command Address Parity error checking. The BIOS default is that this feature is enabled (4905686).
- **C-State enabled OS:** To use SPS ME FW, Package C-states need to be disabled if you are booting a C-State enabled OS to avoid random hangs. The BIOS default setting is enabled (4905544).
- **Wellsburgs A-step silicon:** The v0.80 collateral does not support boot with Wellsburg A-step silicon. Customers that still have WBG-A0 silicon should remain on v0.79 code base.
- **DIMM information table:** DIMMINFO reporting in the serial message debug log (4986323, 4986484)
  - It has been found that reference code versions 0.78, 0.79, and 0.80 will not print the DIMMINFO table in the serial log if SDBG_MIN is included in the setting for serialDebugMsgLvl. This includes the SDBG_MIN+SDBG_MAX option.
  - It is recommended to avoid use of SDBG_MIN or SDBG_MIN+SDBG_MAX when running RMT, or if capturing the DIMMINFO table is otherwise desired.
  - This will be fixed in a future release of the reference code.
  - Note that the CRB BIOS uses the SDBG_MIN+SDBG_MAX value when choosing “Maximum” in the BIOS setup menu, so the DIMMINFO table will be missing in the serial output. This will be fixed in a future release of the CRB BIOS.

Potential issues and enhancements (under investigation):

sighting.id	sighting.title
4166841	MRC Rank disable is not functioning properly for slot 1
4166856	Write Fly By fails on Channel 1 after Rx Dq/Dqs fails on Channel 0
4166863	Memtest failure of secondary channel in mirrored mode causes CATERR
4168340	need to use 2x refresh for HSX B0 for Samsung Hynix or Elpida Mode A modules due to 4905103
4168666	Grantley not booting with 4GB on each processor
4168822	Disabling NUMA for Dimm on HA1 configuration will cause BIOS stuck at PublishHobData in PEI
4168833	DIMMs that fail memtest are not always disabled.
4168911	Enabling CLTT causes hang during Warm Resets
4169020	WARN_FPT_MINOR_MEM_TEST warning messages are missing DIMM and RANK information.
4985793	Soft reset path for LRDIMM
4985795	Reference Code: Write Fly By error handling for training failure
4985982	PROMOTE from presighting 454195 Micron-TI DDR4 1333 4Gb failed to boot
4986090	HSX Clone: Perf P-Limit - change perf_p_limit_threshold to 0xF
4986128	Reference Code: MRC doesn't handle training failures
4986132	Reference code: MRC failed RdDqDqs training after dimm/rank mapped-out
4986148	Bugeco 256630: Memory error counter overflow causes both SMI and CSMI

4986307	Multi-threaded MRC causing Low PPV yield ~75% with the latest BIOS is jeopardizing modulo transfer to the factory
4986310	HSX Clone: PerfWG: Recommend changing the BIOS default for QPI General Configuration for EP 2S to enable Early snoop
4986323	Need dimminfo turned on for serial output in CRB bios with minimal messages
4986348	HSX Clone: PkgC: QPI links not entering L1 during PkgC on a 1S system
4986359	Klocwork: Array 'SAD' of size 20 diddn't get detected to be value of -1
4986365	RX Vref tick size is printed as 4 mV in HSX logs should be 4.68 mV
4986370	DIMMMTR and mcMTR was not updated correctly
4986421	Reference Code: Aztec City hung at CP 0XB7 with SK Hynix 32GB dimm
4986429	W/A Incorrect: Memory: Chip select tristating too early after Self Refresh Entry
4986441	SDP: Memory Configuration reports DDR3 instead of DDR4
4986469	MRC: DDR4 LRDIMM IDT A0 Buffer workarounds should be removed
4986479	MRC: DRAM Turnarounds too high
4986507	MM DDR3 RDIMM Elpida memtest failed
4986525	CLONE from HSX: Clone from HSX Sighting:HSX DDR3 L-0 QEY9 shows incorrect DMFC up to 1066 expected is 1866
4986526	Cold fast boot does not work in multi threaded mode
4986533	Grantley BIOS fail to boot when DIMM install at socket #1 only.
4986539	MRC: Phase shedding not programed when there is only one DRAM0 VR
4986573	bios to pcode mbx disable command directs pcode to remove mc1 on lcc chop
4986587	CPU RC distinguishes whether processor supports HT with wrong CPUID.(EAX=01h):EDX[28] function
4986600	Reference code: hang at CP 0xB1 on Mayan City CRB DDR3 board.
4986604	BIOS is not setting the MC Disable mask before RST_CPL2
4986611	PerfWG: CRB BIOS needs to enable MMC bank XOR and HSX+ Amap
4986613	MRC Training: Advanced Centering Vref Eye Assumption Putting Dimms in Bad State
4986648	MRC: Need to use pTRR + 2x refresh on all LRDIMM TRR configs
4986655	HSX Clone: EX: Memic hangs with BT TO TOR TO and 3-Strike

Sighting fixes and enhancements: (fixes and enhancements since last RC release):

ID	RC	Title
CR_13518	YES	4986525: CLONE from HSX: Clone from HSX Sighting:HSX DDR3 L-0 QEY9 shows incorrect DMFC up to 1066, expected is 1866
CR_13517	YES	4986559: BIOS 19D13 can't set up lockstep with asymmetric config
CR_13506	YES	4986546: (W/A) ESCALATE from hexaii_hsx_mock:MT MRC - printf semaphore hang - Hang at postcode B0
CR_13474	YES	4986529, 4986527: 19.D10 BIOS Fails to boot on Lockstep CFG - caterr with MC UCERR's; DDR3 Lockstep config memory map setup incorrectly
CR_13473	YES	4986474, 4986507: HSX EN M0, EP M0, and EP C0 sometimes faile memtest with DDR3; MM DDR3 RDIMM Elpida memtest failed

CR_13453	YES	4986360: Support for NVDIMM on Grantley platforms
CR_13363	YES	4986250: BIOS settings for CAP x/ PkgC with MC PLL ON (for PkgC3/C6)
CR_13360	YES	4986457: HSX M0 reports error when DIMM on slot 1
CR_13336	YES	4169021: Request support to optimize/customize the BIOS releases for the Aztec City STHI to reduce the boot time down to the 30 second level
CR_13329	YES	4986429: Memory: Chip select tristating too early after Self Refresh Entry
CR_13328	YES	4986199: [Corrected] ESCALATE from hexaii_hsx_mock:[HSX C0] LRDIMM errors in 2DPC @2133 config
CR_13307	YES	4986307: Multi-threaded MRC causing hangs
CR_13306	YES	4986305: cnfg_500_nanosec setting needs updating for HSX
CR_13303	YES	4986405: PROMOTE from haswell_server: Change the BIOS default for maximum page table size to 1G and publish recommended setting for OS I&B
CR_13302	YES	4986403: MRC Training: Need change to RX strobe centering to improve UPM estimates
CR_13301	YES	4986388: GrantleySocketPkg: in 18.R01, HSW MCUs not the latest for A0h/B0h, include C0h
CR_13272	YES	4986341: MRC: smb_tsod_poll_rate.smb_tsod_poll_rate being incorrectly set to 128ms instead of expected 1ms
CR_13271	YES	4986170: Add enable/disable DLL reset funtionality and enable/disable RMT loop for vendor testing
CR_13270	YES	4986051: PCH sync up with clientsw: b4996808 PCH RPFN not functional
CR_13211	YES	4986318: MRC Should Remove CW Write for CAP Enabling on S3 Flow
CR_13210	YES	4986302: need to enable longodt feature in ddrio by default
CR_13209	YES	4986280: MRC: disable unused parity error receiver if udimm
CR_13206	YES	4986147: MRC: BIOS not setting LR-DIMM backside Vref and ODT according to SPD values
CR_13205	YES	4985973: MRC Training: DDR4 LRDIMM training steps do not support FPT
CR_13201	YES	4985806: MRC Training: DDR3 LRDIMM rank muliplication mode not working.
CR_13198	YES	4986350: Re-enable Phase Shedding by Default

Notes:

- This is the Beta Release 1 for Grantley/Haswell-EP and EP4S Reference Code.
- **S3:** to perform S3, the user must disable Command Address Parity error checking. The BIOS default is that this feature is enabled (4905686).
- **C-State enabled OS:** To use SPS ME FW, Package C-states need to be disabled if you are booting a C-State enabled OS to avoid random hangs. The BIOS default setting is enabled (4905544).
- **Wellsburgs A-step silicon:** The v0.80 collateral does not support boot with Wellsburg A-step silicon. Customers that still have WBG-A0 silicon should remain on v0.79 code base.
- **DIMM information table:** DIMMINFO reporting in the serial message debug log (4986323, 4986484)
  - It has been found that reference code versions 0.78, 0.79, and 0.80 will not print the DIMMINFO table in the serial log if SDBG_MIN is included in the setting for serialDebugMsgLvl. This includes the SDBG_MIN+SDBG_MAX option.
  - It is recommended to avoid use of SDBG_MIN or SDBG_MIN+SDBG_MAX when running RMT, or if capturing the DIMMINFO table is otherwise desired.
  - This will be fixed in a future release of the reference code.
  - Note that the CRB BIOS uses the SDBG_MIN+SDBG_MAX value when choosing “Maximum” in the BIOS setup menu, so the DIMMINFO table will be missing in the serial output. This will be fixed in a future release of the CRB BIOS.

Potential issues and enhancements (under investigation):

sighting.id	sighting.title
4166841	MRC Rank disable is not functioning properly for slot 1
4166856	Write Fly By fails on Channel 1 after Rx Dq/Dqs fails on Channel 0
4166863	Memtest failure of secondary channel in mirrored mode causes CATERR
4167481	C0 2:2 change required for BIOS
4167695	CPGC Implementation of Row Hammer DIMM Cell Test Tool
4168340	need to use 2x refresh for HSX B0 for Samsung Hynix or Elpida Mode A modules due to 4905103
4168360	Reference Code: request code change to use OEM/alternative 'freqTable' in MRC
4168666	Grantley not booting with 4GB on each processor
4168740	MC resets or shuts down when booting Win 2k8 or 2k12 with package c-states enabled
4168822	Disabling NUMA for Dimm on HA1 configuration will cause BIOS stuck at PublishHobData in PEI
4168833	DIMMs that fail memtest are not always disabled.
4169020	WARN_FPT_MINOR_MEM_TEST warning messages are missing DIMM and RANK information.
4985674	Enable per-bit RMT in CRB
4985793	Soft reset path for LRDIMM
4985795	Reference Code: Write Fly By error handling for training failure
4985806	MRC Training: DDR3 LRDIMM rank muliplication mode not working.
4985973	MRC Training: DDR4 LRDIMM training steps do not support FPT

4985982	PROMOTE from presighting 454195 Micron-TI DDR4 1333 4Gb failed to boot
4986057	EP early snoop workaround missing VNA credits reduction for B0 BIOS
4986128	Reference Code: MRC doesn't handle training failures
4986132	Reference code: MRC failed RdDqDqs training after dimm/rank mapped-out
4986146	PROMOTE from haswell_server: 17D55.PO1 BIOS not stable -- shuts down sporadically during S3 and resets.
4986147	MRC: BIOS not setting LR-DIMM backside Vref and ODT according to SPD values
4986148	Bugeco 256630: Memory error counter overflow causes both SMI and CSMI
4986165	17D58 Aztec City fail to return from S3
4986170	Feature Request: Add enable/disable DLL reset funtionality and enable/disable RMT loop for vendor testing
4986196	PCIE: Enable DLW Fix
4986256	BIOS Mailbox: FAST_RAPL_NSTRIKE_PL2_DUTY_CYCLE (0x9d) isn't hooked up and doesn't have an option
4986280	MRC: disable unused parity error receiver if udimm
4986293	CLONE from HSX: PUSH from ivytown: Patrol Scrub backpressure from PkgC causes BT TO
4986295	ESCALATE from hexaii_hsx_mock:C0: S3 Fails on configs running 2133Mhz memory
4986302	need to enable longodt feature in ddrio by default
4986307	Multi-threaded MRC causing Low PPV yield ~75% with the latest BIOS is jeopardizing modulo transfer to the factory
4986318	MRC Should Remove CW Write for CAP Enabling on S3 Flow
4986341	MRC: smb_tsod_poll_rate.smb_tsod_poll_rate being incorrectly set to 128ms instead of expected 1ms
4986348	HSX Clone: PkgC: QPI links not entering L1 during PkgC on a 1S system
4986350	Re-enable Phase Shedding by Default
4986370	DIMMMTR and mcMTR was not updated correctly
4986403	MRC Training: Need change to RX strobe centering to improve UPM estimates
4986405	PROMOTE from haswell_server: Change the BIOS default for maximum page table size to 1G and publish recommended setting for OS I&B
4986421	Reference Code: Aztec City hung at CP 0XB7 with SK Hynix 32GB dimm
4986429	W/A Incorrect: Memory: Chip select tristating too early after Self Refresh Entry

Sighting fixes and enhancements: (fixes and enhancements since last RC release):

ID	RC	Title
CR_12969	YES	4986219 (Aborted - Code changes reversed): HSX Clone: HSX EP: BT TO to BTID != 0x1FE/0x1FF while running PM Supercollider content
CR_13125	YES	4167695: CPGC Implementation of Row Hammer DIMM Cell Test Tool
CR_13101	YES	4986256: BIOS Mailbox: FAST_RAPL_NSTRIKE_PL2_DUTY_CYCLE (0x9d) isn't hooked up and doesn't have an option]
CR_13083	YES	4986295: S3 Fails on configs running 2133Mhz memory

CR_13082	YES	4986293: Patrol Scrub backpressure from PkgC causes BT TO
CR_13081	YES	4986284: Kahuna 1DPC system can't boot to 2133 without disabling Enforce POR
CR_13053	YES	4986278: System hanging at Lt Memory when only channels 2 and 3 are populated
CR_13031	YES	4986272: Setup Option needed to select HW vs Pcode Rcomp Control
CR_13025	YES	4986271: MRC Training: TxEq 3 point average truncation error
CR_13019	YES	4986085: PCH SATA RAID alternative ID option not work for IP CLEAN code
CR_13014	YES	4986225: ESCALATE from hexaii_hsx_mock:[HSX C0] LRDIMM 3DPC/encoded mode turnarounds not set properly
CR_13006	YES	NO SIGHTING: Disable phase shedding
CR_13004	YES	4985999: MRC Training: DDR3 LRDIMMs need inphi B0 WA
CR_13003	YES	4986159: Memory: Chip select tristating too early after Self Refresh Entry(updated)
CR_13002	YES	4986266: Hangs in BIOS w/ multi-threaded MRC enabled
CR_12996	YES	4985677: System Memory Poison in Setup menu should be grayed out when System Errors disabled
CR_12987	YES	4986247: C/A Parity Enable needs to happen before RCW disable
CR_12968	YES	4986218: C0 POE : s4168487 : QPI SAPM DLL values cannot change the l0p_window
CR_12962	YES	4986090, 4986174: HSX Clone: Perf P-Limit - change perf_p_limit_threshold to 0xF; BIOS: Perf p limit isn't setup in new format for C0
CR_12930	YES	4986239: 17R02 MiniBIOS fails in QPI initialization
CR_12922	YES	4986237: CMD Rcomps, Run once and then enable overrides
CR_12921	YES	4985987: System Hangs during Warm Reset when Memory Speed is set to 2133
CR_12918	YES	4986027: MRC w/a: Need to enabAle pTRR and 2x refresh for any DDR4 channels with >4 ranks with TRR modeA/B enabled
CR_12913	YES	4986134: Clock difference calculations used in turnarounds not accouting for wraparound
CR_12910	YES	4986198: MRC Training: EarlyCmdClk training needs to clear registers when complete
CR_12893	YES	4168604: Enable SAD A7 mode by default
CR_12889	YES	4986175: Remove "WBG s755 workaround" for WBG B1 silicon
CR_12880	YES	4166856: Write Fly By fails on Channel 1 after Rx Dq/Dqs fails on Channel 0
CR_12879	YES	4986168: C/A Parity Enable setting on DDR3 doesn't enable CAP error reporting
CR_12866	YES	4986000: CLTT - new correct sigma table values
CR_12865	YES	4986162, 4986163: Mismatch between BIOS and 3-sigma weight values for LRDIMMs; VR Phase Shedding not programmed correctly by BIOS for LRDIMMs
CR_12786	YES	4985827, 4985833: DRAM RAPL - dram_power_info.dram_min_pwr constant should scale to number of DIMMs installed; Invalid value of DRAM min power in the MSR 0x61C
CR_12785	YES	4985607, 4985707: MC is not booting when PROCHOT/MEMHOT is asserted; HSX Clone: C1/C1E does not have legacy functionality
CR_12775	YES	4168340: need to use 2x refresh for HSX B0 for Samsung, Hynix, or Elpida Mode A modules due to 4905103
CR_12768	YES	4168939: BIOS Request for WBG s4727769, HOST_CTRL_IDMA_REG[31]=1
CR_12732	YES	4986169: MRC Training: DDR4 LRDIMM backside ODT and Vref value changes

CR_12731	YES	4986173: MRC: Enable C/A Parity by default
CR_12728	YES	4986110: CMOS clearing for setup defaults not working after Variable module change
CR_12725	YES	4168911: Enabling CLTT causes hang during Warm Resets
CR_12724	YES	4986100: MRC: tcmrs.tmrd_ddr3 setting incorrect
CR_12715	YES	4986153: MRC Training: DDR4 LRDIMM TXVREF should not be PDA on backside
CR_12714	YES	4986101: MRC Training: DDR4 LRDIMM TXVREF kit table value off by 1
CR_12710	YES	4166863: Memtest Failure of secondary channel in mirrored mode causes CATERR
CR_12709	YES	4986015: MRC Training: CMDCLK training, after finding valid eye during initial shmoo, dump out of test
CR_12708	YES	4986154: MRC Training: DLL Reset messing up margins in RMT, changing flow
CR_12707	YES	4986159: Memory: Chip select tristating too early after Self Refresh Entry
CR_12699	YES	NO SIGHTING: Removed 4986078: MRC needs to enable comp override after initial rcomp is run
CR_12663	YES	4985599: PCH_SATA_TRACE_CONFIG is defined but not used
CR_12635	YES	4986027: Fix for RH workaround
CR_12585	YES	4985898: QPI Equalization Tuning Update for Kahuna (B0 Onward)
CR_12631	YES	4168737: DMAProtectionMemory Hang - Hynix UDIMM UE8
CR_12630	YES	4986118: Flip Tx and Rx 2D strobe centering
CR_12629	YES	4985867: MRC: pm_pdwn.pdwn_ck_mode setting restriction
CR_12616	YES	4985888: Fast warm resets on 2S Aztec City systems with RDIMMS in SKT0 C0 S0 and SKT1 C2 S0 hang at "100of the system memory tested OK" BIOS splash screen
CR_12599	YES	4986114: MRC Training: TxEq design changes in C0
CR_12596	YES	4985715: MRC: Enable pTRR by default for DDR3 configs
CR_12595	YES	4168651: Disable TRR on any channel that has a non-TRR DIMM installed
CR_12593	YES	4986027: MRC w/a: Need to enable pTRR and 2x refresh for any DDR4 channels with >4 ranks with TRR modeA/B enabled
CR_12586	YES	4985987: System Hangs during Warm Reset when Memory Speed is set to 2133
CR_12552	YES	4986023: MRC Training: DDR4 LRDIMM HW PBA ODT doesnt look correct.
CR_12550	YES	4985911: ESCALATE from hexaii_hsx_mock:MRC - LRDIMM mixed 3DPC/encoded mode + non-encoded channel hangs in MRC
CR_12549	YES	4986026: MRC: Set hasysdefeature.retrythreshold=1 (4 retries)
CR_12546	YES	4985982: PROMOTE from presighting 454195 Micron-TI DDR4 1333 4Gb failed to boot
CR_12545	YES	4985866: Custom Refresh Enable with Rate=20 does not cause 2x refresh
CR_12538	YES	4986013: MRC: XMP is broken
CR_12537	YES	4986012: MRC: Serial debug log fixes
CR_12536	YES	4986081: MRC: CMD Ron Target values need to be updated
CR_12535	YES	4985998: MRC Training: New WriteLeveling/Flyby initial PI code of 256 breaks DDR3 LRDIMMs
CR_12533	YES	4985965: MRC Training: Need to do TXVREF margining in non-PDA mode before TXVREF training is complete
CR_12532	YES	4986070: MRC: When Isoch and lockstep are both on, a channel/rank gets mapped out

CR_12531	YES	4986065: MRC needs to clear DISABLE_PERIODIC_RCOMP via b2p mailbox to enable periodic rcomp
CR_12530	YES	4986078: MRC needs to enable comp override after initial rcomp is run
CR_12930	YES	4986239: 17R02 MiniBIOS fails in QPI initialization

Grantley Platform-EP/EP4S CPU/QPI/Memory Reference Code - Revision 0.79 (17.R03) – Beta Release Candidate 3

Notes:

- This is the Beta Release Candidate 3 for Grantley/Haswell-EP and EP4S Reference Code.

1. RC and CRB BIOS V0.79 are known to have memory detection issue with non-ECC UDIMMs.

These issues will be addressed in Beta release.

2. RC and CRB BIOS V0.79 are known to fail Windows 2012 installation in UEFI mode.

The failing configuration was seen on Inca City with 4-HSX B0 and WBG B0 stepping with fully populated 3DPC. Windows 2012 UEFI installation hung at the windows logo screen.

The same installation works with 2DPC memory configuration (3rd dimm was removed).

These issues will be addressed in Beta release.

Potential issues and enhancements (under investigation):

sighting.id	sighting.title
4166346	Physical Presence Interface Extensions for VT VT-D TXT Enhancement Request
4166418	Reference Code: Use OEM/alternative 'odtValueTable' in MRC
4166682	[HSX_B0_PO] HSX Clone: IIO_SQUELCH Stuck High on Unconnected/unpopulated socket
4166841	MRC Rank disable is not functioning properly for slot 1
4166856	Write Fly By fails on Channel 1 after Rx Dq/Dqs fails on Channel 0
4166863	Memtest failure of secondary channel in mirrored mode causes CATERR
4167022	CLONE from BrickLand HSD#4031534: reset with 10.D02 bios
4167253	BIOS CSR error log clearing hides real silicon errors
4167481	C0 2:2 change required for BIOS
4167611	Enhancement request: The MRC FatalError Function [62 DAYS]
4167625	08_R01: Sparing mode can be set as enable w/one DIMM
4167700	2161755 - protocol gSmmHeciProtocolGuid is not installed in SMM memory.
4167723	HSX Clone: SC: Rand_Stress13b - IRP hang with Rd/Wr conflicts from multiple devices
4167767	WBG B0 PO - Mayan City is not detecting USB3 devices properly
4168177	MEMHOT Sense BIOS Knob does not work
4168320	HSX Clone: CBo PRQ Credit Overflow With All Cores Reporting 3-strike
4168340	need to use 2x refresh for HSX B0 for Samsung Hynix or Elpida Mode A modules due to 4905103
4168360	Reference Code: request code change to use OEM/alternative 'freqTable' in MRC
4168469	CLONE from HSX: DQS[NP] mux selects use incorrect latch enable
4168604	PerfWG ww24: Enable SAD A7 mode by default

4168740	MC resets or shuts down when booting Win 2k8 or 2k12 with package c-states enabled
4168743	multi thread MRC enable will result BIOS hang
4168776	CLONE from HSX: Setup time variation concern over the simple xover on dqstxen path
4168817	Cannot boot OS when setup sets Monitor MWait = Disabled and CPU C-State = Enabled
4168822	Disabling NUMA for Dimm on HA1 configuration will cause BIOS stuck at PublishHobData in PEI
4168833	DIMMs that fail memtest are not always disabled.
4168847	R2PCIe Setting Needed to Prevent System Slowdown or Softhang for HSX B0 Stepping
4168850	CLONE from HSX: Naitive mode DDR in 2:2 mode clock resync doesn't work for both Pkgc6 and mc parity error.
4168858	PerfWG: Change write major mode settings
4168939	BIOS Request for WBG s4727769 HOST_CTRL_IDMA_REG[31]=1
4168985	SAPM-DLL Avg Window Size Needs Tuning
4169020	WARN_FPT_MINOR_MEM_TEST warning messages are missing DIMM and RANK information.
4169032	PROMOTE from haswell_server: Unable to install Hyper-V in Windows Server 2012 on Mayan City
4985591	HSX Clone : " IO Reset is Causing Arandas to Fail"
4985599	WellsburgPkg: PCH_SATA_TRACE_CONFIG is defined but not used. Patsburg used it. Use or remove to avoid confusion
4985674	Enable per-bit RMT in CRB
4985760	MRC Training: DDR3 LRDIMM TA Register tcothp Overflow
4985793	Soft reset path for LRDIMM
4985795	Reference Code: Write Fly By error handling for training failure
4985799	MRC: Lockstep w/a needed for DDR3
4985818	IIO Sample code: request to correct IIO error bit definition
4985831	CLONE from HSX: DdrSelfRefreshClkQnn1H needs to be on a free-running clock if we're doing PkgC's in 2:2 mode
4985833	Invalid value of DRAM min power in the MSR 0x61C
4985863	Setting Memory Configuration->Multi-Threaded MRC=Enabled causes IERR during Memory Training
4985866	Custom Refresh Enable with Rate=20 does not cause 2x refresh
4985883	HSX Thermal Management : ASR AND SRT Options
4985884	Enabled RO=1 for Improved Remote P2P Performance
4985888	Fast warm resets on 2S Aztec City systems with RDIMMS in SKT0 C0 S0 and SKT1 C2 S0 hang at 100of the system memory tested OK" BIOS splash screen"
4985923	HSX Clone: PCIE: Isoch and VT-d on 1S config causes hangs
4985981	Platform XML files uneditable with shipping spsFITC.exe
4985982	PROMOTE from presighting 454195 Micron-TI DDR4 1333 4Gb failed to boot
4985998	MRC Training: New WriteLeveling/Flyby initial PI code of 256 breaks DDR3 LRDIMMs
4985999	MRC Training: DDR3 LRDIMMs need inphi B0 WA
4986011	PROMOTE from haswell_server: Isoc Flexcon Failure when IsocEn is Enable
4986014	HSX Clone: Crashdump 0x91 PECI completion code after an IERR injected with a real PCIe card
4986027	MRC w/a: Need to enabAle pTRR and 2x refresh for any DDR4 channels with >4 ranks with TRR

	modeA/B enabled
4986055	Set USB registers as indicated on USB BIOS guide Rev 11
4986056	BIOS must follow recommended USB sequences as indicated on USB BIOS guide Rev 11
4986057	EP early snoop workaround missing VNA credits reduction for B0 BIOS
4986066	BIOS w/a implemented on 4167910 needs to be removed
4986075	ESCALATE from hexaii_hsx_mock:BIOS fix for s762 and C0 sighting 4986057 bad on SK1 config on initial boot
4986078	[HSX_C0_PO] HSX Clone: MRC needs to enable comp override after initial rcomp is run
4986079	ESCALATE from hexaii_hsx_mock:BIOS Hangs when NTB is enabled
4986092	[HSX_C0_PO] remove BIOS WA for B0 255304
4986093	[HSX-C0-PO] remove B0 BIOS WA for hsd 272155
4986096	[HSX-C0-PO] fix B0 BIOS WA for hsd 272410
4986098	Reference Code: Intel CRB binary based on RC 0.78 hangs in MRC with Micron RDIMM
4986112	ESCALATE from hexaii_hsx_mock:C0 BIOS issues for isoc/ME
4986116	Set IIO_DFX_LCK_CTL.ntblck bit
4986124	HSX Clone: [C0 PO] Isoc: Vcm appears to be the only traffic getting priority at the HA
4986128	Reference Code: MRC doesn't handle training failures
4986132	Reference code: MRC failed RdDqDqs training after dimm/rank mapped-out
4986134	Clock difference calculations used in turnarounds not accouting for wraparound
4986148	Bugeco 256630: Memory error counter overflow causes both SMI and CSMI
4986168	C/A Parity Enable setting on DDR3 doesn't enable CAP error reporting
4986175	Remove WBG s755 workaround" for WBG B1 silicon."
4986176	[C0 PO] Post C0 fix TCO Comp settings
4986182	BIOS WA for IIO/QPI clock gating disable was implemented in CsrSapmCtl.c
4986198	MRC Training: EarlyCmdClk training needs to clear registers when complete
4986199	ESCALATE from hexaii_hsx_mock:[HSX C0] LRDIMM errors in 2DPC @2133 config
4986214	WBG B1 - add new device ID to properly recognize the latest chipset stepping
4986237	CMD Rcomps Run once and then enable overrides

Sighting fixes and enhancements: (fixes and enhancements since last RC release):

ID	RC	Title
CR_12539	YES	4986029: A0 HSX fail to boot starting with 17D45 and 16X11
CR_12453	YES	4168237: tRRD_L sets incorrectly @1333
CR_12490	YES	4985972: PCIe HSX UniPhy Recipe Updated to v7.00 (PCIe changes only)
CR_12482	YES	4986057: [C0 PO] EP early snoop workaround update for C0
CR_12161	YES	4168575 C0 PO: [HSX_C0_PO] Change to QPI Error signalling
CR_12415	YES	4985937: Expand SECPEI FV to use 2mb, remove 1mb limitation (Comment fix)
CR_12386	YES	4985784: QPI Equalization Tuning Update for Inca City (B0 Onward)
CR_12385	YES	4985758: QPI Equalization Tuning Update for Aztec City
CR_12374	YES	4985992: Set Rx-DQ delay register to 2 for nibbles 9-17 for X8 dimms

CR_12373	YES	4985975: ODT Comp=0 after VOC-Calibration when ECC is disabled
CR_12371	YES	4985887: MRC: ZQCal too close together during CPGC due to always_do_zq=1
CR_12369	YES	4985960: 2D strobe centering Vref level calculation changes
CR_12364	YES	NO SIGHTING: Include Initial HSX C-0 patch 0x01
CR_12363	YES	NO SIGHTING: Include HSX B-0 patch 0x12
CR_12194	YES	4985937: Expand SECPEI FV to use 2mb, remove 1mb limitation
CR_12193	YES	4985631: In specific situation platform requires power button or CMOS clear to start despite having PCH state after G3: S0 set in BIOS configuration
CR_12160	YES	4167253 C0 PO: BIOS CSR error log clearing hides real silicon errors
CR_12159	YES	4167166 C0 PO: [HSX_B0_PO] 4167166: [BSX_B0_PO] CLONE from HSX: OVL Error: cache allocation exceeds max cache!
CR_12158	YES	4166978 C0 PO: [HSX_B0_PO] HSX Clone: CBO TOR Timeout : QPI Credit w/a : Memory Stress with Early Snoop Enabled
CR_12157	YES	4166852 C0 PO: [HSX_B0_PO] HSX Clone: QPI EP : Enabling L1 is flagging CorErr 0x22 phy detected inband reset
CR_12156	YES	4166445 C0 PO: QPI link calibration timers: etoc = 14 & etdcc =12 for HSX A0
CR_12155	YES	4168125 C0 PO: QPIREUT_PH_STV.etdetectfwdclk set too low
CR_12154	YES	4168513 C0 PO: HSX Clone : HSX EX: QPI CFO Observed on Large Number of Ports
CR_12135	YES	4168340: need to use 2x refresh for HSX B0 for Samsung Hynix or Elpida Mode A modules due to 4905103
CR_12126	YES	4985935: HSX C0 readiness modification for WA: Row Hammer doesn't drain on link failure (4167167)
CR_12123	YES	NO_SIGHTING: Update for HSX C0 headers and latest BDX CSRs
CR_12118	YES	4168850: CLONE from HSX: Naitive mode DDR in 2:2 mode clock resync doesn't work for both Pkgc6 and mc parity error. - Update working for < HSX C stepping only.
CR_12115	YES	4985930: Common binary for HSX BDX
CR_12108	YES	4168529 HSX Clone: Need BIOS option to Disable Cores using physical id to WA HSX s4905198. Limit this to B0 and earlier stepping
CR_12046	YES	4985746: CLONE from HSX: OVL ERROR: OB TL sent data, but insufficient data
CR_12023	YES	4985618: Memory Scrub register is always enabled
CR_12021	YES	4985883: HSX Thermal Management : ASR AND SRT Options
CR_12020	YES	4985849: MRC Training: Display Training Results
CR_12019	YES	4985820: DDR3 Memtest failed
CR_12018	YES	4985785: MRC Training: Senseamp cal setting bad value of 0 when no transition found
CR_12017	YES	4985742: MRC: Implement Rx Timing Duty Cycle Training
CR_12016	YES	4985796: MRC Training: Enable Early Cmd/Clk for all DDR4
CR_12015	YES	4985887: MRC: ZQCal too close together during CPGC due to always_do_zq=1
CR_12014	YES	4985867: MRC: pm_pdwn.pdwn_ck_mode setting restriction
CR_12013	YES	4985811: MRC: Change t_ckev for DDR4 RDIMM

CR_12012	YES	4985851: MRC: rdimmtimingcntl.t_stab and rdimmtimingcntl2.t_ckoff should be set for UDIMMs
CR_12010	YES	4985831: CLONE from HSX: DdrSelfRefreshClkQnn1H needs to be on a free-running clock if we're doing PkgC's in 2:2 mode
CR_12009	YES	4985864: MRC Training: DDR Memtest currently does 2 loops, need to change to match Romley
CR_12008	YES	4167425: MRC: When COD is enabled, but memory is not behind each HA in the system, log a warning
CR_12006	YES	4985630: Sparing using BIOSNONSTICKYSCRATCHPAD5
CR_12004	YES	4985748: MRC Training: LRDIMM - Need to skip TXEQ training on subranks
CR_12003	YES	4985760: MRC Training: DDR3 LRDIMM TA Register tcothp Overflow
CR_12001	YES	4985791: MRC Training: DDR3 LRDIMM tcrwp.t_rwsr not set correctly
CR_12000	YES	4985756: MRC Training: DDR3 LRDIMM Register init not setting speed/freq correctly
CR_11999	YES	4985775: MRC Training: DDR3 LRDIMM Not setting ODT correctly per freq/speed
CR_11998	YES	4168681: MRC LRDIMM Training: Need all buffer training registers initialized to 0 during normal boot
CR_11995	YES	4985848: PchS3Support.c Assert is thrown after enable BIOS Guard in Aztec City
CR_11979	YES	4985609: MRC needs to tell Pcode if MC is disabled via fusing or mcmtr settings
CR_11914	YES	4985754: BIOS does not support WBG -A SKU
CR_11646	YES	4985711: HSX Clone: CLONE from HSX presighting.: CMD CTL scomp offset glitch
CR_11644	YES	4985704: MRC Training: Incorrect minimum in CLK difference between ranks calculation
CR_11643	YES	4985674: Enable per-bit RMT in CRB
CR_11640	YES	4168616: ESCALATE from hexaii_hsx_mock:LRDIMM Receive Enable Phase Training (MREP) shows bad results
CR_11639	YES	4168262: MRC GetMargins function does not tolerate a persistent correctable error
CR_11638	YES	4985655: OSR Override needs to disable pCode control
CR_11635	YES	4985773: MRC Training: CMD Normalization setup option does not work
CR_11634	YES	4985713: PROMOTE from haswell_server: ES2 QEYA (8C) do not achieve package C6 with BIOS 15.R02 (BETA Gate)
CR_11528	YES	4985736: MRC: Allow 2:2 mode to be automatically selected
CR_11510	YES	4985620: Change Gen 3 PCIe (8.0 GT/s) ctle_peak to 0x18 (24)
CR_11509	YES	4168811: PCIe Gen 2 Equalization Changes - EP
CR_11507	YES	4985644: MRC: LRDIMM Module Delay default disabled, needs to be auto
CR_11505	YES	4168676: MRC: Initial DDR3 LRDIMM Read to Write Timings need MDL added
CR_11504	YES	4166767: Enable CMD normalization training in BIOS
CR_11499	YES	4985617: Set Resistive Degeneration on DMI at 5.0Gbps Based on DCU_MODE
CR_11459	YES	4985699: MRC serial debug message clean up
CR_11437	YES	4985706: CRB Build not supporting Sleep states
CR_11423	YES	4985700: MRC: DDR4 LRDIMM Encoded Mode turnaround times not initialized
CR_11416	YES	4168461: HSX Clone: L0: QPI : QPI to LLC with specific cclk:uclk ratios broken .

CR_11415	YES	4985691: MRC: RfOn should be set to 0 after training completes on B0 and later steppings
CR_11403	YES	4985675: System soft hangs in USB ASL code on S3 resume
CR_11348	YES	4985629: MRC: Change error reporting for IDT PLL lock error in S3/warm reset flow
CR_11347	YES	4169038: MRC Training: RecEnable tCrap.t_rrd hardcoded to 4 for dual rank dimms
CR_11346	YES	4169037: MRC Training: Early Cmd/Clk bug, bad data in tCrap
CR_11321	YES	4168989: HSX Clone: d2cthresholden perf tuning CSR value update
CR_11320	YES	4168988: ESCALATE from hexaii_hsx_mock:QPI: qpierrdis.unc_mask can be set to 0x0.
CR_11319	YES	4168921: Turbo Power Limit MSR lock setup option doesnt work
CR_11318	YES	4168985: SAPM-DLL Avg Window Size Needs Tuning
CR_11317	YES	4168363: HSX BIOS is setting bit 31 (disable_pf_ack_bypass_path) of irp_misc_dfx0 CSR
CR_11316	YES	4168552: MRC: Clean up bw_limit_tf code to remove ISOCH check and disallow dramraplbwlimittf input of 0
CR_11308	YES	4168686: MRC: DDR3 TxVref per-bit margins railing on channels 0 and 2
CR_11302	YES	4169024: MRC Training: Need new TXVREF setting procedure for DDR DRAMS
CR_11301	YES	4168929: MRC Training: CMD Normalization Does Not Handle Negative Numbers
CR_11348	YES	4985629: MRC: Change error reporting for IDT PLL lock error in S3/warm reset flow
CR_11347	YES	4169038: MRC Training: RecEnable tCrap.t_rrd hardcoded to 4 for dual rank dimms
CR_11346	YES	4169037: MRC Training: Early Cmd/Clk bug, bad data in tCrap
CR_11321	YES	4168989: HSX Clone: d2cthresholden perf tuning CSR value update
CR_11320	YES	4168988: ESCALATE from hexaii_hsx_mock:QPI: qpierrdis.unc_mask can be set to 0x0.
CR_11319	YES	4168921: Turbo Power Limit MSR lock setup option doesnt work
CR_11318	YES	4168985: SAPM-DLL Avg Window Size Needs Tuning
CR_11317	YES	4168363: HSX BIOS is setting bit 31 (disable_pf_ack_bypass_path) of irp_misc_dfx0 CSR
CR_11316	YES	4168552: MRC: Clean up bw_limit_tf code to remove ISOCH check and disallow dramraplbwlimittf input of 0
CR_11308	YES	4168686: MRC: DDR3 TxVref per-bit margins railing on channels 0 and 2
CR_11302	YES	4169024: MRC Training: Need new TXVREF setting procedure for DDR DRAMS
CR_11301	YES	4168929: MRC Training: CMD Normalization Does Not Handle Negative Numbers

Notes:

- This is the Beta Release Candidate 2 for Grantley/Haswell-EP Reference Code.

Potential issues and enhancements (under investigation):

4165674	Reference Code: Request BIOS Ref Code to include failing Row and Col address information in the debug serial output during HW MEMTEST
4166377	Reference Code: request to have the number of spare ranks as an RC input parameter
4166418	Reference Code: Use OEM/alternative 'odtValueTable' in MRC
4166682	[HSX_B0_PO] HSX Clone: IIO_SQUELCH Stuck High on Unconnected/unpopulated socket
4167022	CLONE from BrickLand HSD#4031534: reset with 10.D02 bios
4167222	MRC should implement fast cold boot path
4167253	BIOS CSR error log clearing hides real silicon errors
4167261	07_R01: Platform is not returning from S1 state
4167481	C0 2:2 change required for BIOS
4167611	Enhancement request: The MRC FatalError Function [62 DAYS]
4167625	08_R01: Sparing mode can be set as enable w/one DIMM
4167700	2161755 - protocol gSmmHeciProtocolGuid is not installed in SMM memory.
4167723	HSX Clone: SC: Rand_Stress13b - IRP hang with Rd/Wr conflicts from multiple devices
4167808	Clone from Brickland - 3P unable to boot Trusted: 0d13 SINIT Reset - DPR is not locked
4168161	[HSX_B0_FE] DRAM Maintenance Feature translates SPD Byte 7 Incorrectly
4168177	MEMHOT Sense BIOS Knob does not work
4168213	MRC: Implement B0 based fix for PBA (the real PBA)
4168262	MRC GetMargins function does not tolerate a persistent correctable error
4168278	Register Control Word D needs to be set properly for C/A Parity]
4168320	HSX Clone: CBo PRQ Credit Overflow With All Cores Reporting 3-strike
4168340	need to use 2x refresh for HSX B0 for Samsung Hynix or Elpida Mode A modules due to 4905103
4168360	Reference Code: request code change to use OEM/alternative 'freqTable' in MRC
4168469	CLONE from HSX: DQS[NP] mux selects use incorrect latch enable
4168487	ESCALATE from hexaii_hsx_mock:QPI SAPM DLL values cannot change the l0p_window
4168568	CLONE from HSX: clock stop after selfrefresh will need to be delayed long enough to make sure alert is seen
4168603	PerfWG ww24: Enable MC bank XOR by default
4168604	PerfWG ww24: Enable SAD A7 mode by default
4168605	MRC: Disabling both empty channels on an iMC causes Ring RCSM to hang in the wait_blkack state during GV
4168666	Grantley not booting with 4GB on each processor

4168740	MC resets or shuts down when booting Win 2k8 or 2k12 with package c-states enabled
4168743	multi thread MRC enable will result BIOS hang
4168753	Reference Code: possible conflict of MRC status code
4168776	CLONE from HSX: Setup time variation concern over the simple xover on dqstxen path
4168803	HSX Clone: Vcm+Isoc Harasser with CEG rand +supercollider+CBDMA causing system to hang
4168817	Cannot boot OS when setup sets Monitor MWait = Disabled and CPU C-State = Enabled
4168822	Disabling NUMA for Dimm on HA1 configuration will cause BIOS stuck at PublishHobData in PEI
4168843	Add MRS printing back into MRC serial logging
4168847	R2PCIe Setting Needed to Prevent System Slowdown or Softhang for HSX B0 Stepping
4168850	CLONE from HSX: Naitive mode DDR in 2:2 mode clock resync doesn't work for both Pkgc6 and mc parity error.
4168888	mmcfg_base reads incorrect value
4168911	Enabling CLTT causes hang during Warm Resets.
4168930	MRC Training: RMT CMD Margins bug exposed by CMD Normalization
4169009	HSX Clone: <ES2 Gate>DRT: pkg_cstate fails to enter deep cstate with B0 patch 0xc
4169020	WARN_FPT_MINOR_MEM_TEST warning messages are missing DIMM and RANK information.
4985594	MRC: Min Debug Messages unexpected behavior with Xover 2:2 enabled
4985598	ESCALATE from hexaii_hsx_mock:Spontaneous reset from UC Patrol scrub errors during S3 flow
4985600	Setup: Memory Power Management (MPST support) causes CRB to reboot continuously
4985606	MRC Training: Incorrect minimum for DDR4 LRDIMM tRWDR
4985642	DDR4 LRDIMM asymmetric rank per channel config fails MDQS Coarse WL
4985648	HSX Clone: HSX not being setup to downgrade UCECC patrol scrub errors to CECCs in Mirror mode
4985674	Enable per-bit RMT in CRB
4985699	MRC serial debug message clean up
4985700	MRC: DDR4 LRDIMM Encoded Mode turnaround times not initialized
4985702	MRC Training: Add option for CMD Normalization
4985704	MRC Training: Incorrect minimum in CLK difference between ranks calculation
4985736	MRC: Allow 2:2 mode to be automatically selected
4985741	MRC Training: Change ODT activations for LRDIMM 3DPC/encoded mode
4985750	ESCALATE from hexaii_hsx_mock:MRC - LRDIMM hangs in CMD_CLK when configured in DP config
4985758	QPI Equalization Tuning Update for Aztec City
4985760	MRC Training: DDR3 LRDIMM TA Register tcothp Overflow
4985784	QPI Equalization Tuning Update for Inca City (B0 Onward)
4985793	Soft reset path for LRDIMM
4985795	Reference Code: Write Fly By error handling for training failure
4985797	MRC Training: CMD Normalization Changes
4985799	MRC: Lockstep w/a needed for DDR3
4985800	MRC Training: DDR4 LRDIMM and RDIMM need to skip CMD training on non-rank0 ranks per DIMM
4985801	MRC Training: DDR4 LRDIMM need to skip front side TXVREF training on non-rank0 ranks per DIMM
4985812	MRC Training: Senseamp Calibration logging is mixing up the nibbles.

4985820	ESCALATE from hexaii_hsx_mock:MM C4A1 DDR3 Memtest failed
4985831	CLONE from HSX: DdrSelfRefreshClkQnn1H needs to be on a free-running clock if we're doing PkgC's in 2:2 mode
4985883	HSX Thermal Management : ASR AND SRT Options
4985887	MRC: ZQCal too close together during CPGC due to always_do_zq=1
4985902	LRDIMM: Chip ID bits imporperly included in command/address parity calculations
4985908	MRC Training: LRDIMM PBA should issue BCW when all 9 data are the same.
4985909	MRC Training: 2-D strobe centering weight adjustment needed
4985910	MRC Training: Enable Duty Cycle Training by default
4985912	ESCALATE from hexaii_hsx_mock:MM C4A1 DDR3 Memtest fails in lockstep
4985922	MRC Training: JedecInit is restoring per dram vref values for DDR4 LRDIMM
4985923	HSX Clone: PCIE: Isoch and VT-d on 1S config causes hangs
4985939	MRC Training: CMD Normalization Not Checking CLK
4985960	2D strobe centering Vref level calculation changes
4985961	MRC: t_ccd being incorrectly set to same value as t_ccd_l
4985963	MRC Training: Jedec Init Reset Timer needs to be reduced
4985964	MRC: Move MRS print to after training is done
4985965	MRC Training: Need to do TXVREF margining in non-PDA mode before TXVREF training is complete
4985975	HSX Clone : " ODT Comp=0 after VOC-Calibration when ECC is disabled"
4985982	PROMOTE from presighting 454195 Micron-TI DDR4 1333 4Gb failed to boot
4985992	Set Rx-DQ delay register to 2 for nibbles 9-17 for X8 dimms
4985999	MRC Training: DDR3 LRDIMMs need inphi B0 WA
4986011	PROMOTE from haswell_server: Isoc Flexcon Failure when IsocEn is Enable
4986027	MRC w/a: Need to enable pTRR and 2x refresh for any DDR4 channels with >4 ranks with TRR modeA/B enabled

Sighting fixes and enhancements: (fixes and enhancements since last RC release):

ID	RC	Title
CR_12332	YES	4985598: Spontaneous reset from UC Patrol scrub errors during S3 flow
CR_12213	YES	4167222: MRC should implement fast cold boot path

Grantley Platform-EP/EP4S CPU/QPI/Memory Reference Code - Revision 0.77 (15.R03) – Beta Release Candidate 1

Notes:

- This is the Beta Release Candidate 1 for Grantley/Haswell-EP Reference Code.

Potential issues and enhancements (under investigation):

sighting.id	sighting.title
4165674	Reference Code: Request BIOS Ref Code to include failing Row and Col address information in the debug serial output during HW MEMTEST
4165893	RC should provide more informaiton to help customer identify where processor running when system hang.
4166377	Reference Code: request to have the number of spare ranks as an RC input parameter
4166418	Reference Code: Use OEM/alternative 'odtValueTable' in MRC
4167065	[HSX_B0_PO] HSX Clone: CLONE from HSX BugEco: Mode Register reads from inverted/mirrored side of rdimm/lrdimm is broken
4167290	QPI: MinRtid single pool mode
4167481	C0 2:2 change required for BIOS
4167611	Enhancement request: The MRC FatalError Function
4167625	08_R01: Sparing mode can be set as enable w/one DIMM
4167697	HSX MRC: Enable Xover 2:2 Mode for 2133 frequency
4167698	HSX MRC: Need BIOS Option for Xover 2:2 Mode
4167943	C/A Parity should not be enabled in MR5
4167974	[HSX_B0_FE] Register Control Word 8 needs to be set properly for C/A Parity
4167978	MRC: EarlyCmdClk Training needs some fixes.
4168161	[HSX_B0_FE] DRAM Maintenance Feature translates SPD Byte 7 Incorrectly
4168177	MEMHOT Sense BIOS Knob does not work
4168214	CLONE from HSX: HA can deadlock when SBO AD credits < 2 * AD_SNP egress credits
4168278	Register Control Word D needs to be set properly for C/A Parity]
4168288	imc#_c#_erf_ddr4_cmd_reg2 needs rdimm set to 1 when C/A parity is enabled
4168314	SDP: Windows Server 2012 reports DDR4 memory as DDR3 with speed 800MHz
4168329	DIMM therm event pin is not worked
4168340	need to use 2x refresh for HSX B0 for Samsung Hynix or Elpida Mode A modules due to 4905103
4168360	Reference Code: request code change to use OEM/alternative 'freqTable' in MRC
4168393	Setting NumaEn to disabled on 4S system the interleave list that's created for memory map is NUMA instead of UMA
4168395	DDR4 Training - TXEQ Training algorithms required to improve TX Voltage Margins
4168403	QPI Equalization Tuning Update for Mayan City (B0 Onwards)
4168463	qpireut_pm_r3.rxl0pexitrtrnalarmsel needs minimum value of 1 for QPI links to function properly

4168521	DDR Training - Add Imode Boost Swing Training to improve TX voltage margins
4168534	ESCALATE from hexaii_hsx_mock:Few Spare ranks not setup on Lockstep + Sparing configs
4168544	DDR Training: EarlyCMDClk needs to skip SRx8 DIMMs with older date codes
4168546	ESCALATE from hexaii_hsx_mock:t_cl setting violates jedec spec for some dimms at 1866 frequency
4168554	QPI HSX UniPhy Recipe Updated to v6.00 (QPI changes only)
4168568	CLONE from HSX: clock stop after selfrefresh will need to be delayed long enough to make sure alert is seen
4168605	MRC: Disabling both empty channels on an iMC causes Ring RCSM to hang in the wait_blkack state during GV
4168616	ESCALATE from hexaii_hsx_mock:LRDIMM Receive Enable Phase Training (MREP) shows bad results
4168650	MRC Training: Need to add code to move CLKS during early or late CmdClk training
4168686	MRC: DDR3 TxVref per-bit margins railing on channels 0 and 2
4168702	dimmmtr ddr3_dnsty and ddr3_width registers need to be set in customer bios
4168743	multi thread MRC enable will result BIOS hang
4168753	Reference Code: possible conflict of MRC status code
4168766	TxEq Training Changes
4168776	CLONE from HSX: Setup time variation concern over the simple xover on dqstxen path
4168795	ESCALATE from hexaii_hsx_mock:minRTID causing hangs on SF2B
4168814	ESCALATE from hexaii_hsx_mock:BIOS 14.D14 : Enabling minRTID bios knob causes boot hangs + CATERR
4168817	Cannot boot OS when setup sets Monitor MWait = Disabled and CPU C-State = Enabled
4168822	Disabling NUMA for Dimm on HA1 configuration will cause BIOS stuck at PublishHobData in PEI
4168843	Add MRS printing back into MRC serial logging
4168885	ESCALATE from hexaii_hsx_mock:RDIMMs with IDT B0 register RC0D not set correctly
4168888	mmcfg_base reads incorrect value
4168890	MRC: LRDIMMs do not work with early CTL CLK for 2DPC
4168906	Update for Rcomp Ron Codes to get desired resistance for B0
4168907	MRC: Need BIOS to check for invalid/not supported Samsung 2012 DDR4 1R RDIMMs
4168911	Enabling CLTT causes hang during Warm Resets.
4168919	Enable Early CMD-CLK by Default
4168929	MRC Training: CMD Normalization Does Not Handle Negative Numbers
4168948	HSX Clone: SK4D Hangs With MinCredit Enabled
4168962	HSX Clone: BIOS: implement s4905362/b272908 workaround
4168979	MRC: is_rdimm setting wrong for DDR4 RDIMMs affecting S3 CK voltage
4168988	ESCALATE from hexaii_hsx_mock:QPI: qpierrdis.unc_mask can be set to 0x0.
4169018	Enable TxEq training by default
4169020	WARN_FPT_MINOR_MEM_TEST warning messages are missing DIMM and RANK information.
4169024	MRC Training: Need new TXVREF setting procedure for DDR DRAMS
4169033	MRC: Add workaround for IDT B0 Register / PLL Lock failure
4169037	MRC Training: Early Cmd/Clk bug bad data in tCrap

4985608	MRC: Error reporting incorrect for IDT PLL workaround
4985629	MRC: Change error reporting for IDT PLL lock error in S3/warm reset flow
4985691	MRC: RfOn should be set to 0 after training completes on B0 and later steppings
4985699	MRC serial debug message clean up
4985700	MRC: DDR4 LRDIMM Encoded Mode turnaround times not initialized

Sighting fixes and enhancements: (fixes and enhancements since last RC release):

ID	RC	Title
CR_11226	YES	4168844: (Part 2) HSX Clone: False BT TO for 4S - BT entry 510 or 511
CR_11175	YES	4985608: MRC: Error reporting incorrect for IDT PLL workaround
CR_11172	YES	NO SIGHTING: Cleanup strings for space in MRCNORMAL FV
CR_11152	YES	4169009 Part2: HSX Clone: DRT: pkg_cstate fails to enter deep cstate with B0 patch 0xc
CR_11144	YES	4169037: MRC Training: Early Cmd/Clk bug, bad data in tCrap
CR_11143	YES	4169018: Enable TxEq training by default
CR_11120	YES	4169033: MRC: Add workaround for IDT B0 Register / PLL Lock failure
CR_11100	YES	4169009: HSX Clone: DRT: pkg_cstate fails to enter deep cstate with B0 patch 0xc
CR_11098	YES	4168554: QPI HSX UniPhy Recipe Updated to v6.00 (QPI changes only)
CR_11086	YES	4169043: 15d19 causes slow sata AHCI mode
CR_11046	YES	4168965: 2:2 DP MRC training failed
CR_11061	YES	4169029: 15_D22 Aztec, Kahuna, Arandas 2s fail to boot
CR_11027	YES	4168885: ESCALATE from hexaii_hsx_mock:RDIMMs with IDT B0 register RC0D not set correctly
CR_11025	YES	4167625 08_R01: Sparing mode can be set as enable w/one DIMM
CR_11017	YES	4168919: Enable Early CMD-CLK by Default
CR_11013	YES	4168979: MRC: is_rdimm setting wrong for DDR4 RDIMMs, affecting S3 CK voltage
CR_11011	YES	4168554: QPI HSX UniPhy Recipe Updated to v6.00 (QPI changes only)
CR_11004	YES	4168948: HSX Clone: SK4D Hangs With MinCredit Enabled
CR_10978	YES	4168534:ESCALATE from hexaii_hsx_mock:Few Spare ranks not setup on Lockstep + Sparing configs
CR_10963	YES	4168938: WBG, USB2 High Speed Disconnect Reference Voltage set to 600mV
CR_10962	YES	4167884: Consolidate PEI PchReset()
CR_10901	YES	4168297: PFAT (BIOS Guard) flash update support for CapsuleApp.efi
CR_10786	YES	4168909: Update reference code copy rights for 2013
CR_10761	YES	4168890: MRC: LRDIMMs do not work with early CTL CLK for 2DPC
CR_10536	YES	4165674: Reference Code: Request BIOS Ref Code to include failing Row and Col address information in the debug serial output during HW MEMTEST
CR_10532	YES	4168605: MRC: Disabling both empty channels on an iMC causes Ring RCSM to hang in the wait_blkack state during GV
CR_10530	YES	4168348: QPIRC BIOS knob QpiConfigTxWci not working as expected
CR_10526	YES	4168753: Reference Code: possible conflict of MRC status code
CR_10525	YES	4168800: Enable multi-threaded MRC by default

CR_10522	YES	4168738: MRC: Need to calculate turnaround times before RMT (postcode 0xb710)
CR_10520	YES	4168743: multi thread MRC enable will result BIOS hang
CR_10519	YES	4168686: MRC: DDR3 TxVref per-bit margins railing on channels 0 and 2
CR_10512	YES	4168765: Implement Imode Training
CR_10511	YES	4168760: DDR3 register "imc0_c0_tcrwp.t_rwsr" not set correctly in BIOS
CR_10510	YES	4168780: Enable PDA mode by default
CR_10508	YES	4168643: TxVref Centering has incorrect strobe to DRAM mapping
CR_10507	YES	4168649: MRC Training: Need to skip EarlyCmdClk for certain DIMMs
CR_10506	YES	4168756: Clear r3qctrl.flowq_vn1enable if VN1 does not need to be enabled and not early snoop for HSX C0
CR_10424	YES	4168678: HA to QPI and CBO to QPI credits not matching RTL settings for 2S ES, 15% BW shortfall
CR_10450	YES	4167255: Grantley stream sync to CP 1.20 common core
CR_10388	YES	4168742: MRC Training TXVREF non-pda rank margins not set correctly
CR_10384	YES	4168741: Add suport to CRB BIOS For memory using BCLK 100
CR_10379	YES	4168402, 4168403: QPI Equalization Tuning Update for Arandas and Mayan (B0 Onward)
CR_10378	YES	4168702: dimmmtr ddr3_dnsty and ddr3_width registers need to be set in customer bios
CR_10377	YES	4168650: MRC Training: Need to add code to move CLKS during early or late CmdClk training
CR_10374	YES	4168682: C/A Parity Enabling needs to set imc#_c#_mc#_dp_chkn_bit.en_rdimm_par_err_log=1 and dis_rdimm_par_chk=0
CR_10373	YES	4168311:QPI: Per Link Credit Reduce Not Working
CR_10369	YES	4168364 ACPI: Bit 3 in register 188h of IIO Root Ports is set during OS boot, but not restored during S3 resume
CR_10368	YES	4168558: Some isoc workarounds need to be applied for MeSegEn=1 (MESEG-only mode)
CR_10175	YES	NO_SIGHTING: MRC codesize reduction from serial mesage string changes
CR_10114	YES	4168471: SetupPlatform asserts when platform populated with DDR3 memory @ 800, 1066
CR_10110	YES	4167697: HSX MRC: Enable Xover 2:2 Mode for 2133 frequency
CR_10052	YES	4168604: Enable SAD A7 mode by default
CR_10051	YES	4168601: MRC Training: Early CTL/CLK not working properly for DDR3 and all DDR4 configs
CR_10044	YES	4168253: USB2, Need to change PLLCBTUNE register as Lynxpoint recommendation
CR_10025	YES	4168550: CKE mask being generated incorrectly
CR_10005	YES	4168586: RMT Pattern Length > 32k
CR_10001	YES	4168546: t_cl setting violates jedec spec for some dimms at 1866 frequency
CR_9991	YES	4168585: Put TxVref centering before RxVref Centering
CR_9989	YES	4168563: Enabling C/A Parity causes Training Failures
CR_9986	YES	4168595: MRC Training: GetMargins for CMD not checking range properly causing truncated margins
CR_9980	YES	4168591: MRC Training: PerCmdGroup CMD training is calling getMargins per rank instead of one time

Notes:

- This is an alpha release of Grantley/Haswell-EP Reference Code.

Known issues:

- None

Potential issues and enhancements (under investigation):

sighting.id	sighting.title
4166413	[HSX_B0_PO] CLONE from HSX: PUSH from ivytown: reading of RID values for non-existance IIO device/functions breaks PCIE header spec
4167284	RAS Sample Code: WHEA Memory Error Injection (6000009800)
4167506	08_R00: Hard disc missing installing RHEL 6.4
4167712	MSDEVFUNCHIDE is not locked
4167939	CLONE from wellsburg: CLONE from wellsburg: CLONE from lynx_point: LPT-REGR-BIOS: SATA LTR sending 0x880A active value when no sata drives are connected
4168323	HSX Clone: Socket 1 FIT patch load in COD causes RBT aliasing due to QPI Link Interleave not yet set up (1 Link case)
4168340	Need to use 2x refresh for HSX B0 for Samsung Hynix or Elpida Mode A modules due to 4905103
4168341	MayanCity CRB fails to install 32-bit Windows OS
4168360	Reference Code: request code change to use OEM/alternative 'freqTable' in MRC
4168384	Cannot install Windows 8 x86 (lose keyboard/mouse)
4168604	PerfWG ww24: Enable SAD A7 mode by default
4168616	ESCALATE from hexaii_hsx_mock:LRDIMM Receive Enable Phase Training (MREP) shows bad results
4168649	MRC Training: Need to skip EarlyCmdClk for certain DIMMs
4168666	Grantley not booting with 4GB on each processor
4165893	RC should provide more informaiton to help customer identify where processor running when system hang.
4166377	Reference Code: request to have the number of spare ranks as an RC input parameter
4166418	Reference Code: Use OEM/alternative 'odtValueTable' in MRC
4166810	[HSX_A0_FE] ESCALATE from hexaii_hsx_mock:S3 Resume BIOS Assert at PC 0XAF
4167199	PCH sample code generation errors
4167242	[BP_2013_WW4_GRNT] BIOS assertion Get BIOS ID from FV""
4167290	QPI: MinRtid single pool mode
4167353	SSATA Controller in RAID mode doesn't support hotplugs
4167381	MRC: LRDIMM needs write dq/delay training and multiple DQ delay settings for cycle training.
4167432	07_R02: Unable to install Win 2008 x86 because keyboard and mouse are not working
4167442	Request to set chicken bits 21 & 14 in XHCI MMIO +0x8094 to workaround: USBIF Compliancy Failure - Removing Interop Tree from LPT system causes intermittant BSOD

4167481	C0 2:2 change required for BIOS
4167576	MRC: EarlyCmdClk Training needs persistant parity signaling
4167577	Biosscratchpad1 not being set for DDR3 voltages
4167611	Enhancement request: The MRC FatalError Function
4167655	Add user configurable setup option for dynamic_perf_power_ctl.imc_apm_override_enable
4167697	HSX MRC: Enable Xover 2:2 Mode for 2133 frequency
4167698	HSX MRC: Need BIOS Option for Xover 2:2 Mode
4167700	Protocol gSmmHeciProtocolGuid is not installed in SMM memory.
4167705	Need support for CLI/GBT-XML in CRB BIOS as contingent plan for EPCSUtil
4167723	HSX Clone: SC: Rand_Stress13b - IRP hang with Rd/Wr conflicts from multiple devices
4167959	ESCALATE from hexaii_hsx_mock:alternate Amap Set to Enabled by default.
4167978	MRC: EarlyCmdClk Training needs some fixes.
4167997	HSX Clone: Unexpected PM Ack/Nak (0x13)
4168037	[HSX_B0_FE] VMSE_ERROR_MCDDC_DP_REG.ignore_vmse_err should be cleared when C/A Parity is enabled.
4168128	QPI: Change required for A0 HA/MC BGF Ptr seperation
4168131	Linux OS installation/boot hangs when XHCI
4168132	PCIe root port link speed Auto" setting"
4168155	C-states not working on GRNDCRB1.86B.000
4168161	[HSX_B0_FE] DRAM Maintenance Feature translates SPD Byte 7 Incorrectly
4168177	MEMHOT Sense BIOS Knob does not work
4168197	DCAHints Are Not Fully Enabled in B0 BIOS
4168214	CLONE from HSX: HA can deadlock when SBO AD credits < 2 * AD_SNP egress credits
4168224	DRAM Maintenance Feature should be Enabled for non-TRR DIMMs.
4168253	USB2 Need to change PLLCBTUNE register as Lynxpoint recommendation
4168278	Register Control Word D needs to be set properly for C/A Parity]
4168288	imc#_c#_erf_ddr4_cmd_reg2 needs rdimm set to 1 when C/A parity is enabled
4168311	QPI: Per Link Credit Reduce Not Working
4168333	Change to QPI Error signalling
4168343	MRC: Need pdwn_ck_mode set to tristate clock stop (value 1) by default for all DIMMs
4168356	MRC: C/A parity enabling issue
4168389	MRC: DDR4 LRDIMM Register and Data Buffer Spec Rev 0.92 Changes required
4168395	DDR4 Training - TXEQ Training algorithms required to improve TX Voltage Margins
4168396	Memory Frequency: 100Mhz Freq. multiples not supported in current BIOS.
4168397	0.75 Grantley OEM release fails to reset
4168403	QPI Equalization Tuning Update for Mayan City (B0 Onwards)
4168436	MRC: need code put back in that clears imc#_c#_tcrwp.t_rwsr for non DDR3 LRDIMM
4168449	Workaround settings required to avoid CATERR's for WBG ES2 samples in ww22
4168463	qpireut_pm_r3.rxl0pexitrtrnalarmsel needs minimum value of 1 for QPI links to function properly
4168471	SetupPlatform asserts when platform populated with DDR3 memory @ 800 1066
4168495	HSX Clone: SC: Completion starved at head of switch queue many MWr to loopback address with ACS bits cleared

4168532	Change DQ/CTL/CLK (Drive Strength) Rcomp target codes to 44
4168536	HSX Clone: Lockstep and TRR / Dram Maintanance cause CECCs
4168537	MRC: rxOffset.rxdqspsel needs to be restored to the correct value after Sense Amp Calibration
4168544	DDR Training: EarlyCMDClk needs to skip SRx8 DIMMs with older date codes
4168546	ESCALATE from hexaii_hsx_mock:t_cl setting violates jedec spec for some dimms at 1866 frequency
4168547	Spare Ranks should not be included in Patrol Scrub interval calculation
4168556	HSX-EP Grantley - Implement Register Spec 0.92 in MRC for RDIMM
4168558	Some isoc workarounds need to be applied for MeSegEn=1 (MESEG-only mode)
4168563	Enabling C/A Parity causes Training Failures
4168568	CLONE from HSX: clock stop after selfrefresh will need to be delayed long enough to make sure alert is seen
4168581	MRC: LateCmdClk training mixing up ranks on DR configs.
4168584	MRC: Write recovery for autoprecharge not set correct for DDR4 1333
4168585	Put TxVref centering before RxVref Centering
4168586	RMT Pattern Length > 32k
4168591	MRC Training: PerCmdGroup CMD training is calling getMargins per rank instead of one time
4168595	MRC Training: GetMargins for CMD not checking range properly causing truncated margins
4168601	MRC Training: Early CTL/CLK not working properly for DDR3 and all DDR4 configs
4168605	MRC: Disabling both empty channels on an iMC causes Ring RCSM to hang in the wait_blkack state during GV
4168622	MayanCity CRBBIOS fails to go to S1
4168623	MRC: Need to modulo Tx Per Bit Deskew Delay by 64 before writing back to picode CSR
4168629	PROMOTE from haswell_server: Enabling mirror mode causes 14.D02 to hang at Receive Enable training in CRB BIOS
4168648	MRC: Need to set mcsched_chkn_bit.ovrd_odt_to_io chicken bit for turnarounds on B-step and above
4168650	MRC Training: Need to add code to move CLKS during early or late CmdClk training
4168654	Reduce Memory reference code strings to reduce module size
4168664	Changes to EnableProcHot bios knob to allow selection of all prochot modes
4168674	MRC: Add w/a's per the M88DDR4 RCD/DB Sighting Report
4168682	C/A Parity Enabling needs to set imc#_c#_mc#_dp_chkn_bit.en_rdimm_par_err_log=1 and dis_rdimm_par_chk=0
4168702	dimmmtr ddr3_dnsty and ddr3_width registers need to be set in customer bios
4168703	MRC: Enable Agressive Turnaround Calculations
4168741	Add suport to CRB BIOS For memory using BCLK 100
4168742	MRC Training TXVREF non-pda rank margins not set correctly

Sighting fixes and enhancements: (fixes and enhancements since last RC release):

ID	RC	Title
CR_9966	YES	4168517: Lockstep Configs fail to boot
CR_9964	YES	NO SIGHTING: Sync QPIRC code with QpiRcSim0520 - Merge IVT RC code (35_L11) into HSX QPI RC SIM (to support one common code for IVT/HSX)
CR_9957	YES	4168568: clock stop after selfrefresh will need to be delayed long enough to make sure alert

		is seen
CR_9956	YES	4168584: MRC: Write recovery for autoprecharge not set correct for DDR4 1333
CR_9955	YES	4168583: Enable SenseAmp Training by Default
CR_9953	YES	4167576: MRC: EarlyCmdClk Training needs persistant parity signaling
CR_9952	YES	4168581: MRC: LateCmdClk training mixing up ranks on DR configs
CR_9951	YES	4168343: MRC: Need pdwn_ck_mode set to tristate clock stop (value 1) by default for all DIMMs
CR_9909	YES	4167250: MRC: Need LRDIMM backside RMT
CR_9907	YES	4168449: Workaround settings required to avoid CATERR's for WBG ES2 samples in ww22
CR_9851	YES	4168492: DRAM Power Info MSR has incorrect min and max values
CR_9839	YES	4168288: Do not enable CA Parity for UDIMMs
CR_9837	YES	4168545, 4168547: Scrub interval fixes
CR_9836	YES	4168541: 13_D09 Mayan City SRP Fails to Boot when a channel is fully populated
CR_9817	YES	4168310: Use of DDR4 Memory Weight Tables causes 2DPC memory configurations to reset during memtest on Kahuna systems
CR_9811	YES	4168537: MRC: rxOffset.rxdqspsel needs to be restored to the correct value after Sense Amp Calibration
CR_9810	YES	4168536: Lockstep and TRR / Dram Maintanance cause CECCs
CR_9806	YES	4168462: MRC: Need additional ODT assertion delay when CL - CWL > 1 for Reads
CR_9787	YES	4168406: MRC: All CMD groups are not being moved when being margined
CR_9785	YES	4168395: DDR4 Training - TXEQ Training algorithms required to improve TX Voltage Margins
CR_9746	YES	4168499: MRC: Need to change CAS2RCVEN and CAS2DRVEN calculations for Turnaround Timings
CR_9743	YES	4168215: MRC: Need to implement turnaround calculations for DDR3
CR_9738	YES	4168375: Lockstep & Adaptive Page Mode WA
CR_9721	YES	4168498: BIOS MRC: Enable Dynamic DDR Speed instead of forcing 1600 by default
CR_9716	YES	4168159: RMT Default pattern length needs to be increased from 1000 to 32767
CR_9715	YES	4168436: MRC: need code put back in that clears imc#_c#_tcrwp.t_rwsr for non DDR3 LRDIMM
CR_9690	YES	4167668: DDR3: Timing violation of t_mod and t_zqcs at 1867
CR_9689	YES	4166748: Not able to run CPGC test after BIOS post-code 0xb710
CR_9685	YES	4168430: Row hammer blocks bank address instead of bank group during TRR sequence
CR_9682	YES	4168396: Memory Frequency: 100Mhz Freq. multiples not supported in current BIOS.
CR_9561	YES	4167575: HSX MRC: DDR3 LRDIMMs ODT activation/values table needed
CR_9501	YES	4167959: ESCALATE from hexaii_hsx_mock:alternate Amap Set to Enabled by default.
CR_9496	YES	4168167: ESCALATE from hexaii_hsx_mock:MM BIOS POR check
CR_9494	YES	4165819: DDR: Need to implement Early CTL-CLK training
CR_9492	YES	4168401: MRC: JedecInit should come before senseamp
CR_9476	YES	4168272: Memory VR phase shedding - Hard coding to PS2 has VR thermal/rel issues: BIOS needs to set PS2/PS1 via configuration

CR_9471	YES	4168337: BIOS chose incorrect DIMM type for populating DIMM weights
CR_9456	YES	4168184 - WBG SATA and sSATA DTLE should be changed from 0x2 to 0x5
CR_9286	YES	4166418: Reference Code: Use OEM/alternative 'odtValueTable' in MRC
CR_9276	YES	4168329: DIMM therm event pin is not worked
CR_9260	YES	4165810: HSX IOT Memory Buffer Reservation
CR_9252	YES	4167634: Grantley Silicon reference code source contain non-ascii characters may cause build failure
CR_9234	YES	4168276 Add check for unsupported CPU steppings as well as illegal combinations
CR_9230	YES	4165364 Support for Debug Interface MSR (Requirement Change)
CR_9223	YES	4168275: Need customer option for PCPS/SPD and UFS
CR_9220	YES	4168161, 4168224: DRAM Maintenance updates
CR_9219	YES	4168317: Turnaround timings t_wwdd and t_wwdr need additional d clk in calculation
CR_9218	YES	4168318: Turnaround timings t_rwdd and t_rwdr need additional d clk in calculation
CR_9200	YES	4168321: HSX Clone: Socket 1 FIT patch load in COD causes RBT aliasing due to QPI Link Interleave not yet set up (2 Link case)
CR_9190	YES	4168319: MRC: DDR4 Register CKE Power Management is always disabled
CR_9188	YES	4167577: Biosscratchpad1 not being set for DDR3 voltages
CR_9178	YES	4165392 Need to support Cache QoS Enforcement (reqirement change)
CR_9177	YES	4168267: MRC: SenseAmp calibration needs RTT_PRK set to DISabled during calibration
CR_9175	YES	4168268: MRC: CPU side Termination not correct in DDR4 for SenseAmp calibration
CR_9174	YES	4168278: Register Control Word D needs to be set properly for C/A Parity]
CR_9169	YES	4168269: ESCALATE from hexaii_hsx_mock:L0: BIOS infinitely looping through memtest
CR_9161	YES	4167436: DDR3 Mode ODT should use 2 segments by setting segEn=3
CR_9160	YES	4167265: [HSX_B0_PO] HSX Clone: Clear longodtr2w in all datacontrol3 registers
CR_9159	YES	4167151: Alternate (HSX+) Address Map Needs to be Default for DDR4
CR_9068	YES	4168125,4167037(4032604): 1) QPIREUT_PH_STV.etdetectfwdclk set too low 2) CLONE from HSX: Clone from HSX Sighting:QPI EP: Rx AGC and Rx Vref train low on lanes 9&10 after BIOS boot
CR_9057	YES	4167074: Per Dram Addressable MRS exit for Rdimm/lrdimm inverted/mirrored side broken
CR_9055	YES	4167442: Request to set chicken bits 21 & 14 in XHCI MMIO +0x8094 to workaround: USBIF Compliancy Failure - Removing Interop Tree from LPT system causes intermittant BSOD
CR_9028	YES	4168178: WSel value should not be set by BIOS
CR_8994	YES	4168177: MEMHOT Sense BIOS Knob does not work
CR_8972	YES	4168239: MRC: t_xsdll setting for DDR4 needs to be updated
CR_8948	YES	4167685, 4167996: BIOS not programming VR PS correctly; DDR_RANKS_PRESENT incorrect values reported for Ch23
CR_8941	YES	4168202 MRC: DDR4 LRDIMM IDT Data Buffer A0 sightings report version 2013_04_15_1238
CR_8936	YES	4168217: DDR per bit training is broken
CR_8816	YES	4032594: HSX EX BO QPI CTLE0 sighting & sync up HSX qpi rc sim version 0425
CR_8813	YES	4167609: NTB-RP configuration WA_3875263 using PCIExpressWrite .vs. MmioWrite

CR_8802	YES	4167991: DDR Training: WL Coarse Flyby sweep sequence needs to be changed to start from lowest latency
CR_8781	YES	4168062: Incorrect VR to DIMM/Channel Mapping
CR_8774	YES	4168156: Clean up/remove/optimize serial debug messages
CR_8771	YES	4167576: MRC: EarlyCmdClk Training needs persistant parity signaling
CR_8770	YES	4167989: rfon WA needs to be kept in place for B0
CR_8769	YES	4167940: JKT/IVTwrbgfthresh Mirroring WA should be removed for HSX
CR_8768	YES	4168152: DDR Training - Enable Sense Amp Training by default
CR_8763	YES	4167882: Set IOLBCTL back to 0
CR_8761	YES	4167722: Need setup option to enable Eye Diagrams in RMT
CR_8759	YES	4168037: VMSE_ERROR_MCDDC_DP_REG.ignore_vmse_err should be cleared when C/A Parity is enabled.
CR_8758	YES	4168121: Lockstep fails memtest with data scrambling enabled due to selective_err_enb_chunk setting
CR_8757	YES	4167234: DQ/CA vref measured drops (as much as 9 mv) between even/odd code values
CR_8756	YES	4167338: ODT Not Asserting During CPGC PDA Control of TxVref in PDA Mode
CR_8755	YES	4168054: Need IOCOMP set to 15 for ch2/3 in 1HA mode

Notes:

- This is an alpha release of Grantley/Haswell-EP Reference Code.

Known issues:

- There is a known issue with this MiniBios running on Simics (4.6.73). In this environment, the MiniBios experienced a hang condition due to the following error. This issue was not seen in a real system environment.

```
N0.C0.D0.R0.S00: FAULTY_PARTS_TRACKING: Failed Receive Enable Pi
EvaluateFaultyParts ODT based eval expected
EvaluateFaultyParts status: 1

A warning has been logged! Warning Code = 0x30, Minor Warning Code = 0x14, Data = 0x0
Socket = 0 Channel = 0 DIMM = 0 Rank = 0

Warning has been upgraded to Fatal Error!
```

Potential issues and enhancements (under investigation):

sighting.id	sighting.title
4168355	MRC: EarlyCmdClk needs fixes to work on all ranks and improve efficiency.
4168351	MRC: writeRc (RCW) register writes not working when rank specified >0
4168350	CPGC V/A test improvements
4168340	need to use 2x refresh for HSX B0 for memory Mode A modules due to 4905103
4168329	DIMM therm event pin is not worked
4168323	HSX Clone: Socket 1 FIT patch load in COD causes RBT aliasing due to QPI Link Interleave not yet set up (1 Link case)
4168321	HSX Clone: Socket 1 FIT patch load in COD causes RBT aliasing due to QPI Link Interleave not yet set up (2 Link case)
4168319	MRC: DDR4 Register CKE Power Management is always disabled
4168318	Turnaround timings t_rwdd and t_rwdr need additional d clk in calculation
4168317	Turnaround timings t_wwdd and t_wwdr need additional d clk in calculation
4168298	QPI: Clear ES+Isoc bit in scratchpad3 when downgrading topology
4168288	imc#_c#_erf_ddr4_cmd_reg2 needs rdimm set to 1 when C/A parity is enabled
4168287	MRC: Need to set internalclockson=1 for A0 and B0 all the time (training and normal mode)
4168278	Register Control Word D needs to be set properly for C/A Parity]
4168269	ESCALATE from hexaii_hsx_mock:L0: BIOS infinitely looping through memtest
4168268	MRC: CPU side Termination not correct in DDR4 for SenseAmp calibration
4168267	MRC: SenseAmp calibration needs RTT_PRK set to DISabled during calibration
4168265	Disable SenseAmp Training by Default

4168229	GetMargins() Issues
4168227	PPDF enabled when bios knob set to disabled
4168224	DRAM Maintenance Feature should be Enabled for non-TRR DIMMs.
4168217	DDR per bit training is broken
4168214	CLONE from HSX: HA can deadlock when SBO AD credits < 2 * AD_SNP egress credits
4168202	MRC: DDR4 LRDIMM IDT Data Buffer A0 sightings report version 2013_04_15_1238
4168177	MEMHOT Sense BIOS Knob does not work
4168172	tcmr2shadow.two_mrs_en = 0 for RDIMMs
4168161	[HSX_B0_FE] DRAM Maintenance Feature translates SPD Byte 7 Incorrectly
4168156	Clean up/remove/optimize serial debug messages
4168152	DDR Training - Enable Sense Amp Training by default
4168128	QPI: Change required for A0 HA/MC BGF Ptr seperation
4168125	QPIREUT_PH_STV.etdetectfwdclk set too low
4168121	HSX Clone: Lockstep fails memtest with data scrambling enabled due to selective_err_enb_chunk setting
4168112	HSX Clone: R3QPI:0x10 & RxUUU:0x12 UNC QPI Link Errors
4168054	Need IOCOMP set to 15 for ch2/3 in 1HA mode
4167991	DDR Training: WL Coarse Flyby sweep sequence needs to be changed to start from lowest latency
4167989	rfon WA needs to be kept in place for B0
4167958	"HSX Clone : " DDR3 with Inphi registers failing training at 1333
4167900	QPI Fwdc Tx DCC wsel set incorrectly to 5 on B0
4167882	Set IOLBCTL back to 0
4167687	MRC: LRDIMM: Hynix QR initial LRDIMMs have 8 nibbles routed backwards need training averaged
4167681	MRC: Need WorkAround implemented for write leveling upper strobe issue/bug
4167611	Enhancement request: The MRC FatalError Function
4167610	Removing the 800MHz and 1067MHz frequency configurations for DDR4 from the BIOS Menu option
4167599	08_R01: Platform is not booting with mixed processor speed
4167577	Biosscratchpad1 not being set for DDR3 voltages
4167576	MRC: EarlyCmdClk Training needs persistant parity signaling
4167449	Clarification needed in RefCode and Docs for TXEQL/CTLEPEAK "all lane" vs "per lane" settings
4167338	HSX Clone: ODT Not Asserting During CPGC PDA Control of TxVref in PDA Mode
4167290	QPI: MinRtid single pool mode
4167269	NDR Completion with RTID 0 May Result in RTID Loss CA3S
4167251	HSX Clone: R3QPI Control Error with BIOS 07.D10 - BL Ingr Ptr Invalid - Temp WA
4167237	HSX Clone: PCODE: IO_BW_PLIMIT: The gv floor set by io_bw_plimit isn't consumed by hsx pcode
4167234	DQ/CA vref measured drops (as much as 9 mv) between even/odd code values
4167210	Page Policy: Idle Page Reset set to 8 for fixed open page mode
4167065	[HSX_B0_PO] HSX Clone: CLONE from HSX BugEco: Mode Register reads from inverted/mirrored side of rdimm/lrdimm is broken

4166960	[HSX_B0_PO] CLONE from HSX: MC: failing to return read data to HA causing HA checker to hang (Isoch page table alias bug)
4166854	QPI: 4SPO changes
4166810	[HSX_A0_FE] ESCALATE from hexaii_hsx_mock: S3 Resume BIOS Assert at PC 0XAF
4166772	ESCALATE from hexaii_hsx_mock: Disabling QPI Ports with BIOS causing OS hangs and CATERR's
4166713	HSX_PO: QPI: Only enable fanout in 4S ring and 2SEP COD
4166699	BIOS X19 failing incorrectly on a CBo mismatch. X14 passes
4166666	HSX Clone: Early Snoop hangs in BIOS
4166635	QPI HSX UniPhy Recipe Updated to v2.00 (QPI changes only)
4166597	Request to transition BSP to max non-Turbo earlier in POST
4166539	HSX_PO:QPI: Remove TxAlign programming and skip freq test on A0
4166526	HSX_PO: QPIRC:Isoc qpi_routing Increase Tor Timeouts New method for Cbo/Ha counting
4166522	[HSX_B0_PO] CLONE from HSX: Disable LLCMiss for DRd by default
4166492	[HSX_B0_PO] [HSX_A0_PO] CLONE from HSX: mem_rd prefetch with relaxed ordering passes mem_wr prefetch
4166440	MRC: Need to enable PA[7] mode
4166427	Tracking for 2S COD emulation bringup minibios fixes
4166394	BIOS should distribute CBO VNA credits based on physical not logical CBOID
4166388	1S-COD: BIOS must clear CBO_CR_CBO_COH_CONFIG_CFG.EGO
4166161	[HSX_A0_PO] CLONE from HSX: Config read to IIOMISCCTRL returns incorrect data in lock mode
4166126	[HSX_B0_PO] QPI: DCAEN
4166121	QPI: review for COD code
4166116	QPI: Meseg\Isoc pool change
4166088	QPI RC doesn't compile if MAX_SOCKET defined as 1
4165810	HSX IOT Memory Buffer Reservation

Sighting fixes and enhancements: (fixes and enhancements since last RC release):

ID	RC	Title
CR_8624	YES	4167885, 4167897,416790,4167908: Qpi changes made during HSX B0 PO
CR_8519	YES	4167978: MRC: EarlyCmdClk Training needs some fixes
CR_8515	YES	4167980: imc#_ddrcrcmdcontrols_cmds.ddr4modeenable needs set to 0 to enable C/A Parity
CR_8513	YES	4167974: Register Control Word 8 needs to be set properly for C/A Parity
CR_8511	YES	4167944: imc#_c#_erf_ddr4_cmd_reg2 needs to be setup when C/A Parity is enabled
CR_8509	YES	4167943: C/A Parity should not be enabled in MR5
CR_8499	YES	4167178: MRC hang due to intermittent SPD read errors
CR_8466	YES	4167909: BIOS Hangs at Post Code 0xBC when DRAM Maintenance Feature is enabled
CR_8436	YES	4167266: Request to expose Enable/Disable option for Relaxed Ordering
CR_8422	YES	4167757, 4167758 - Turn L0p and L1 enabled by default in setup
CR_8386	YES	4167942: MRC: DDR Package Delay Table not right for CTL and CLK signals

CR_8339	YES	4167174: MC unit fails to report self refresh indication on Package C-state entry flow when in MDLL off mode
CR_8337	YES	4167843: Update to DDR Comp Target Vref for B stepping
CR_8334	YES	4167880: GetMargins() railing on various DIMMs
CR_8332	YES	4167907: IOCOmp Latency requires increase to 14 to support 1HA on ch's 2 and 3
CR_8328	YES	4167779: MRC needs to use TX_PER_BIT_SETTLE_TIME = 40
CR_8303	YES	4167626: Need MRC to use mailbox command WRITE_PCU_MISC_CONFIG to disable rcomp
CR_8266	YES	4166780 Config_IOT_LLC disabled in CpuInit.c for HSX Power on
CR_8265	YES	4167282 [HSX_B0_PO] MMIO rule 3 is different across sockets - Update to CR_8234
CR_8256	YES	4167164: Weight values mismatch between BIOS and 3-sigma table
CR_8244	YES	HSD#4167600 - Changing SBSP to socket1 fails to boot
CR_8219	YES	4167050: Need sticky scratchpad bit set when DDR4 EEPROMs detected on cold boot (UPDATE)
CR_8170	YES	4167778 [HSX_B0_PO] Simics Grantley HSX-B0 config: Processorstartup uncore init bug
CR_8147	YES	4166592, 4166563, 4166483, 4166180: Remove A0 workarounds for B0
CR_8137	YES	4167608: MRC needs to enable comp override after initial rcomp is run
CR_8134	YES	4167265: Fix for Clear longodtr2w in all datacontrol3 registers (Fix based on feedback from Kevin)
CR_8132	YES	4166707: MRC needs to implement HSX B0 support for RH issue
CR_8051	YES	4166592, 4166618: DDR3/DDR4 identification to BIOS, Soft memtest cleanup
CR_8034	YES	4166938: Request a RC option setup.mem.allowCorrectableErrors for EvaluateFaulty
CR_8031	YES	4166952:QPI: set SYSTEM_CONFIGURATION.QpiLinkCreditReduce to default to per link
CR_8029	YES	4167265: Fix for Clear longodtr2w in all datacontrol3 registers
CR_8005	YES	4167649: DDR3 Dimms failing RxDqDqs
CR_8003	YES	4166143: Exit Self Refresh code needs to be fixed

Notes:

- This is a pre-alpha release of Grantley/Haswell-EP Reference Code.

Potential issues and enhancements (under investigation):

sighting.id	sighting.title
4168156	Clean up/remove/optimize serial debug messages
4168152	DDR Training - Enable Sense Amp Training by default
4168132	PCIe root port link speed "Auto" setting
4168128	QPI: Change required for A0 HA/MC BGF Ptr seperation
4168125	QPIREUT_PH_STV.etdetectfwdclk set too low
4168121	HSX Clone: Lockstep fails memtest with data scrambling enabled due to selective_err_enb_chunk setting
4168112	HSX Clone: R3QPI:0x10 & RxUUU:0x12 UNC QPI Link Errors
4168054	Need IOCOMP set to 15 for ch2/3 in 1HA mode
4167991	DDR Training: WL Coarse Flyby sweep sequence needs to be changed to start from lowest latency
4167989	rfon WA needs to be kept in place for B0
4167980	[HSX_B0_FE] imc#_ddrcrcmdcontrols_cmds.ddr4modeenable needs set to 0 to enable C/A Parity
4167974	[HSX_B0_FE] Register Control Word 8 needs to be set properly for C/A Parity
4167965	MRC: Need IOCOMP latency =14 for all channels/HA combinations as WA to margin issues
4167944	imc#_c#_erf_ddr4_cmd_reg2 needs to be setup when C/A Parity is enabled
4167943	C/A Parity should not be enabled in MR5
4167942	MRC: DDR Package Delay Table not right for CTL and CLK signals
4167940	JKT/IVTwrbgfthresh Mirroring WA should be removed for HSX
4167908	[HSX_B0_PO] Change BGF ptrsep settings to performance POR via bios/pcu mailbox
4167907	"HSX Clone : " IOCOmp Latency requires increase to 14 to support 1HA on ch's 2 and 3
4167900	QPI Fwdc Tx DCC wsel set incorrectly to 5 on B0
4167885	CLONE from HSX: HA can deadlock when SBO AD credits < 2 * AD_SNP egress credits
4167882	Set IOLBCTL back to 0
4167880	"HSX Clone : " GetMargins() railing on various DIMMs
4167843	Update to DDR Comp Target Vref for B stepping
4167779	HSX Clone: MRC needs to use TX_PER_BIT_SETTLE_TIME = 40
4167681	MRC: Need WorkAround implemented for write leveling upper strobe issue/bug
4167637	[HSX_B0_PO] CLONE from HSX: SenseAmpEn and OdtEn get stuck on when entering CKE powerdown immediately after a read
4167627	[HSX_B0_PO] Fix stepping revision checking in the MRC
4167608	[HSX_B0_PO] HSX Clone: MRC needs to enable comp override after initial rcomp is run

4167576	MRC: EarlyCmdClk Training needs persistant parity signaling
4167543	HSX Clone: BIOS needs to IOLBCTL=2
4167505	tcmr2shadow and tcmr0shadow are not being restored properly on fast boot / s3 flow
4167403	Reference Code: possible conflict of STS_ status code
4167388	HSX Clone: rcomp_timer.count=0x7ed0 causing mc pkgc fsm to hang in the pkgc_unforce_sr state
4167347	Disable Round Trip Latency to enable Training to address failing scenarios
4167342	MemPowerSave Mode causes CPGC Failures - No Boot
4167338	HSX Clone: ODT Not Asserting During CPGC PDA Control of TxVref in PDA Mode
4167290	QPI: MinRtid single pool mode
4167287	[HSX_A0_FE] BIOS Not Setting DDR3 TxVref Correctly
4167275	Commenting #define SERIAL_DBG_MSG in Reference Code is producing error when MiniBIOS is built
4167265	[HSX_B0_PO] HSX Clone: Clear longodtr2w in all datacontrol3 registers
4167264	MRC: Occasional fail on LRDIMM backside write cycle training
4167258	HSX Clone: POR Change: IBT-off Mode removed from POR. Remove from BIOS.
4167234	DQ/CA vref measured drops (as much as 9 mv) between even/odd code values
4167226	MRC memNvram structure clean up
4167225	MRC Multi-threaded mode is broken
4167210	Page Policy: Idle Page Reset set to 8 for fixed open page mode
4167178	[HSX_A0_FE] HSX Clone: MRC hang due to intermittent SPD read errors
4167174	[HSX_B0_PO] CLONE from HSX: MC unit fails to report self refresh indication on Package C-state entry flow when in MDLL off mode
4167091	MRC input items missing from max messages display
4167065	[HSX_B0_PO] HSX Clone: CLONE from HSX BugEco: Mode Register reads from inverted/mirrored side of rdimm/lrdimm is broken
4167057	HSX MRC: Requesting Setup Option for Turnaround Timing Calculation Enabling
4166976	Reference code: incorrect bit flag usage
4166952	QPI: set SYSTEM_CONFIGURATION.QpiLinkCreditReduce to default to per link
4166938	Reference Code: Request a RC option setup.mem.allowCorrectableErrors for EvaluateFaultyParts
4166934	Enable OSR by default
4166875	[HSX_B0_PO] B0 changes for CMD PI groupings
4166871	[HSX_B0_PO] B0 XOVER design changes for CMD fubs
4166862	STHI Aztec City Motherboards hangs at 0xB7h
4166846	MRC Training Failed with ECC OFF
4166810	[HSX_A0_FE] ESCALATE from hexaii_hsx_mock:S3 Resume BIOS Assert at PC 0XAF
4166802	[HSX_B0_PO] HSX Clone: HSX A0 PO: Self Refresh Commands do not push CS Low
4166729	Incorrect reporting of DDR speed in serial log
4166707	MRC needs to implement HSX B0 support for RH issue
4166641	BIOS Setup Menu does not have option to enable log of per bit margin data
4166631	[HSX_B0_PO] CLONE from HSX: Per Dram/Buffer addressable methodology does not work for LRDIMMs

4166502	Reference Code: MRC RC supporting VREF DCP device for DDR4
4166464	[HSX_B0_PO] MRC: Need to fix SenseAmp calibration for DDR4 due to silicon bug for A0
4166440	MRC: Need to enable PA[7] mode
4166377	Reference Code: request to have the number of spare ranks as an RC input parameter
4166358	'Auto' setting for ckeThrottling varies based on dimm type
4166143	Exit Self Refresh code needs to be fixed
4165893	RC should provide more informaiton to help customer identify where processor running when system hang.
4165820	[HSX_B0_PO] DDR: Need to implement Backside LR DIMM training

Sighting fixes and enhancements: (fixes and enhancements since last RC release):

ID	RC	Title
CR_7904	YES	4167637:SenseAmpEn and OdtEn get stuck on when entering CKE powerdown immediately after a read
CR_7903	YES	4167505: tcmr2shadow and tcmr0shadow are not being restored properly on fast boot / s3 flow
CR_7902	YES	4167627: Fix stepping revision checking in the MRC
CR_7901	YES	4167632: HSX B0 Xover changes impacting HSX A0 CMD margins
CR_7861	YES	4165955 & sync up HSX QPIRC 0322: EMC Request: Change Bus ratio, IO Ratio, MMIO ratio options to use base and limit.
CR_7805	YES	4167258: POR Change: IBT-off Mode removed from POR. Remove from BIOS
CR_7772	YES	4167543: BIOS needs to IOLBCTL=2
CR_7754	YES	4166414: HSX should have a mix of sparing and non-sparing mode in a system
CR_7753	YES	4167342: MemPowerSave Mode causes Failures - No Boot
CR_7605	YES	4032309: External QPIRC uses two define names for asm inc support & support hsx ex qpi ras
CR_7587	YES	4167347: Disable Round Trip Latency to enable Training to address failing scenarios
CR_7573	YES	4166915: DDR3 Micron DIMMs failing MRC training
CR_7571	YES	4166871: B0 XOVER design changes for CMD fubs
CR_7570	YES	4167050: MRC: Need sticky scratchpad bit set when DDR4 EEPROMs detected on cold boot
CR_7569	YES	4167388: rcomp_timer.count=0x7ed0 causing mc pkgc fsm to hang in the pkgc_unforce_sr state
CR_7561	YES	4032309:(Clone from HSX EX) External QPIRC uses two define names for asm inc support
CR_7559	YES	4167332: DRAM RAPL Baseline Mode 1 not default setting for DramRaplInit
CR_7556	YES	4167346 ProcessorStartupLib should expose PCD for code cache size for platform to configure
CR_7550	YES	4167368 Incorrect bus number used when accessing LEGACY_CSR_SAD_CONTROL
CR_7548	YES	4167332: DRAM RAPL Baseline Mode 1 not default setting for DramRaplInit
CR_7493	YES	4167264: MRC: Occasional fail on LRDIMM backside write cycle training
CR_7487	YES	4166738: Fast boot option not enabling fast boot reset flow
CR_7481	YES	4166922:ESCALATE from hexaii_hsx_mock:IIO: IIO disable enabling
CR_7460	YES	4167216: [HSX_A0_FE] ESCALATE from hexaii_hsx_mock:DRAM RAPL DP: DRAM RAPL Mode 1 not initialized on Socket 1
CR_7418	YES	4166999 Flex_Ratio CSR is not writable (not readable either for B0 step)

CR_7416	YES	4166843: Mixed x4 x8 dimms may cut off last strobe
CR_7414	YES	4167287: BIOS Not Setting DDR3 TxVref Correctly
CR_7413	YES	4166875: B0 changes for CMD PI groupings
CR_7393	YES	4167155:QPI CTLE Peaking Settings for B0 PO (All Board Designs)(reprogrom 1e instead of 0xf)
CR_7388	YES	4167214:QPIREUT_PH_CTR does not have Disable Auto Compliance bit set on HSX
CR_7376	YES	4167275: Commenting #define SERIAL_DBG_MSG in Reference Code is producing error when MiniBIOS is built
CR_7373	YES	4167057: Requesting Setup Option for Turnaround Timing Calculation Enabling
CR_7288	YES	4167252:[HSX Clone: R3QPI Control Error with BIOS 07.D10 - BL Ingr Ptr Invalid - Full WA]
CR_7256	YES	4166818: ESCALATE from hexaii_hsx_mock:BIOS: UFS disable option isn't working
CR_7255	YES	NO SIGHTING: Update to 4166934: Enable OSR by default
CR_7249	YES	4167227, 4167232: HSX Clone: MAILBOX_BIOS_CMD_DIMM_VR_PHASE_SHED incorrectly formatted; Verify and correct HSX-EP PCU2BIOS mailbox usage in power management code
CR_7244	YES	4166631: CLONE from HSX: Per Dram/Buffer addressable methodology does not work for LRDIMMs
CR_7209	YES	4167209: Patrol Scrub rate incorrectly set to 0 by default. Fatal errors when corrections occur.
CR_7197	YES	4167231: DDR3 Vdd not set correctly
CR_7192	YES	4167226: MRC memNvram structure clean up
CR_7191	YES	4167178: MRC hang due to intermittent SPD read errors
CR_7190	YES	4167225: MRC Multi-threaded mode is broken
CR_7177	YES	4166808, 4166648: MC Channel Hash Mode, Set page policy default to adaptive
CR_7158	YES	4166802: HSX Clone: HSX A0 PO: Self Refresh Commands do not push CS Low
CR_7146	YES	4167037:CLONE from HSX: Clone from HSX Sighting:QPI EP: Rx AGC and Rx Vref train low on lanes 9&10 after BIOS boot
CR_7144	YES	4167045: QPI HSX UniPhy Recipe Updated to v4.00 (QPI changes only)
CR_7141	YES	4167115: from hexaii_hsx_mock:PCode Still setting io_sa_config.qpi01_mask on UP systems
CR_7131	YES	4167155:QPI CTLE Peaking Settings for B0 PO (All Board Designs)
CR_7124	YES	4166846: MRC Training Failed with ECC OFF
CR_7123	YES	4167159: Memory controller timings violating JEDEC specs for DDR3
CR_7122	YES	4167180: CWL and Turnaround settings incorrect at 1333
CR_7121	YES	4167091: MRC input items missing from max messages display
CR_7109	YES	NO SIGHITNG: delete the code for "force L0r disabled if L0p disabled". HSX/IVT don't need this
CR_7108	YES	4167190:HSX Clone: QPI EP: FM1 : Warm resets causing QPI UNC 0x2 Drift Buffer alarm BEFORE Link Init
CR_7082	YES	4167137 Bios is using incorrect address for MMIO_TARGET_LIST_1_CBOBC_IOSAD_REG (HSX)
CR_7076	YES	4167077:ESCALATE from hexaii_hsx_mock:Enabling QPI Bitrate Knob in BIOS (Frequency Cap)
CR_7069	YES	4165797, 4166617: Channel A6 shift mode; Hard coded SPD data
CR_7067	YES	4165992, 4166432: Need to get RAPL and CLTT platform values; DDR4 support in MemWeight Tableand MemThroat.c file issue

Notes:

- This is a pre-alpha release of Grantley/Haswell-EP Reference Code.

Potential issues and enhancements: (under investigation)

sighting.id	sighting.title
4166377	Reference Code: request to have the number of spare ranks as an RC input parameter
4167065	HSX Clone: CLONE from HSX BugEco: Mode Register reads from inverted/mirrored side of rdimm/lrdimm is broken
4167338	HSX Clone: ODT Not Asserting During CPGC PDA Control of TxVref in PDA Mode
4166358	'Auto' setting for ckeThrottling varies based on dimm type
4166464	MRC: Need to fix SenseAmp calibration for DDR4 due to silicon bug for A0
4166502	Reference Code: MRC RC supporting VREF DCP device for DDR4
4166631	CLONE from HSX: Per Dram/Buffer addressable methodology does not work for LRDIMMs
4166729	Incorrect reporting of DDR speed in serial log
4166802	HSX Clone: HSX A0 PO: Self Refresh Commands do not push CS Low
4166833	Catastrophic temperature trip point
4166843	[HSX_A0_FE] CLONE from HSX: mixed x4 x8 dimms may cut off last strobe
4166846	MRC Training Failed with ECC OFF
4166868	[HSX_A0_FE] HSX Clone: BIOS fails to clear CR_RCOMP_TIMER.RCOMP bit in MC1 after first RCOMP
4166875	[HSX_B0_PO] B0 changes for CMD PI groupings
4166879	BIOS sighting fix for 4166398 incomplete mcbypassbgfthreshold not updated per pointer separation values
4166934	Enable OSR by default
4167005	[HSX_A0_FE] Round Trip Optimization Failure
4167046	[HSX_A0_FE] PCIe HSX UniPhy Recipe Updated to v4.00 (PCIe changes only)
4167091	MRC input items missing from max messages display
4167150	HSX Clone: CBDMA M2M+ROL traffic causes 3 strike (Ubox Lock FSM hang#3)
4167152	[HSX_A0_FE] Provide option to enable or disable Tx Vref PDA
4167155	QPI CTLE Peaking Settings for B0 PO (All Board Designs)
4167178	[HSX_A0_FE] HSX Clone: MRC hang due to intermittent SPD read errors
4167195	07_D10: Minibios is missing for Aztec city
4167204	4167204 :HSX Clone: Rckt: read tor timeout when under lock with oversubscribed tlb
4167214	QPIREUT_PH_CTR does not have Disable Auto Compliance bit set on HSX
4167225	MRC Multi-threaded mode is broken
4167226	MRC memNvram structure clean up
4167239	WBG B0 requires chicken-bit settings for keyboard

4167264	MRC: Occasional fail on LRDIMM backside write cycle training
4167317	QPI EP : L0p Control Parameters

Sighting fixes and enhancements: (fixes and enhancements since last RC release)

ID	RC	Title
CR_7288	YES	4167252:[HSX Clone: R3QPI Control Error with BIOS 07.D10 - BL Ingr Ptr Invalid - Full WA]
CR_7108	YES	4167190:HSX Clone: QPI EP: FM1 : Warm resets causing QPI UNC 0x2 Drift Buffer alarm BEFORE Link Init
CR_7076	YES	4167077:ESCALATE from hexaii_hsx_mock:Enabling QPI Bitrate Knob in BIOS (Frequency Cap)
CR_7041	YES	4167152: [HSX_A0_FE] Provide option to enable or disable Tx Vref PDA
CR_6978	YES	4167134: CheckRange() function not calculating correct parameter values
CR_6959	YES	4167059: BIOS GetMargins() Sometimes Returns Incorrect Results
CR_6958	YES	4167126 ProcessorStartupUncore.asm change to match HSX-B0 change of IIO_MMCFG_BASE and LIMIT address
CR_6953	YES	4165792: [HSX_A0_FE] Add Setup Option(s) - Page Table Aliasing
CR_6950	YES	4166267: Klocwork Issues 695, and 696
CR_6945	YES	4166976: CMD_CLK_TRAINING_EN bit field correction
CR_6944	YES	4167094: Scomp FSM fix
CR_6943	YES	4166914: Klockwork Issue: 845, 846
CR_6942	YES	4166907: Klockwork Issue - 824
CR_6934	YES	4167103 Core disable bug fix
CR_6926	YES	4167101:HSX Clone: SC: Credit loss between IRP and R2 interface from AD or AK traffic resulting in TOR TO and 100% stalling for lack of credits in ADQ
CR_6923	YES	4166901: Klockwork Issue: 847
CR_6891	YES	4166729: Incorrect reporting of DDR speed in serial log
CR_6877	YES	4167062, 4166868, 4166805: Disable MC clock gating if RCOMP is disabled; Clear RCOMP bit for MC1; Fix tech table loop
CR_6850	YES	4167023: VNA credit workaround required for A0 presi bug 241466
CR_6841	YES	4167044:4167042:Mayan and Arandas QPI TxEqs
CR_6817	YES	4166999 HSX flex_ratio CSR register not writable
CR_6803	YES	4166287: oppReadInWmm default value to be "Enabled"
CR_6802	YES	4166520 HSX_PO:core disable inifinite loop
CR_6801	YES	4166782: Need to re-enable ResetSystem call associated with LT Policy
CR_6797	YES	4166964: RMT Disable in BIOS options does not disable RMT
CR_6794	YES	4166786: RxVref Training Algorithm Using Incorrect Timing Offsets
CR_6784	YES	4166924: Add Setup Option: Bank XOR
CR_6782	YES	4165925: Add Setup Options(s) - Alternate Address Map
CR_6781	YES	4166934: Enable OSR by default
CR_6777	YES	4166358: 'Auto' setting for ckeThrottling varies based on dimm type
CR_6734	YES	4165820: DDR: Need to implement Backside LR DIMM training

CR_6730	YES	4166783:4166784:4166700:CATERR seen with BIOS X18 - using 14/16slice COD:Remove hardcoded 18slices
CR_6715	YES	4166818: ESCALATE from hexaii_hsx_mock:BIOS: UFS disable option isn't working
CR_6712	YES	4166883: set default of imcx_cx_chn_temp_cfg.thrt_allow_isoch to 1
CR_6689	YES	4166978:HSX Clone: CBO TOR Timeout : Memory Stress with Early Snoop Enabled
CR_6681	YES	4166269: Klocwork Issue-196
CR_6659	YES	4166263: Klocwork Issues: 212 and 213
CR_6658	YES	4167009: Enable DDR patrol scrubbing
CR_6657	YES	4166264: Klocwork Issue: 203
CR_6650	YES	4166641: BIOS Setup Menu does not have option to enable log of per bit margin data
CR_6647	YES	4167005: 4S: Memory failing to train - RTL Optimization Failure
CR_6645	YES	4166941:set egcritalwaysfirstdisable=1 in HA for *all* configs
CR_6644	YES	4166879: mcbypassbgfthreshold not updated per pointer separation values
CR_6642	YES	4166993: Enable BIOS for DDR-I/O CA buffer Ron to have 2 values, 18 ohms and 30 ohms
CR_6598	YES	4166850:ESCALATE from hexaii_hsx_mock:BIOS: 1S COD + Dir + HitMe 3 Strike
CR_6595	YES	4166961:HSX Clone: Running taprand alone on a DP system causes TOR timeout on Vcm Transaction
CR_6592	YES	4166768: Enable early CMD-CLK training in BIOS
CR_6589	YES	4166769: Enable Sense Amp training in BIOS
CR_6588	YES	4166262: Klocwork Issues: 215, 216 and 217
CR_6587	YES	4166766: Tx Vref updates
CR_6586	YES	4166266: Klocwork Issue: 202
CR_6585	YES	4166268: Klocwork Issues: 197
CR_6581	YES	4166862: STHI Aztec City Motherboards hangs at 0xB7h
CR_6557	YES	4166261: Klocwork Issues: 222 and 223
CR_6538	YES	4166255: Klocwork Issue: 178, 179, 180, 181
CR_6535	YES	4166256: Klocwork Issues: 185, 186, 187
CR_6530	YES	4166921:QPI: arandas, when s2 not present, system boots 3s chain.
CR_6527	YES	4166855:ESCALATE from hexaii_hsx_mock:PCIE: MCTP CATERRs when targeting remote socket
CR_6522	YES	4166715, 4166654: Memory timings not being calculated properly
CR_6521	YES	4166737: Set Scrambling Enabled as Default
CR_6474	YES	4166254: Klocwork issues - 175, 176, 177
CR_6470	YES	4166252: Klocwork Issue: 172
CR_6464	YES	4166704: COD and NUMA not visible to OS
CR_6453	YES	4166744: BDX: DDR4 roundtrip latency calculations
CR_6433	YES	4166877:QPI EP: qpierrdis.unc_mask is masking all qpi uncorrectable errors

Notes:

- This release is the pre-silicon sample code for Grantley/Haswell-EP Reference Code.

Known Issues:

- None

Potential Issues: (investigating)

- None

Sighting fixes and enhancements: (fixes and enhancements since last RC release)

ID	RC	Title
CR_6424	NO	Grantley Release 05_R00 Package
CR_6407	NO	4166681: Incorrect number of processors showing in Windows Device Manager
CR_6402	NO	4166869:QPI: enable d2c on 4sring.
CR_6401	NO	4166873:HSX Clone: CBO TOR Timeout : Concurrent CPU and ME traffic
CR_6398	NO	4166795: BIOS using 1n CMD timings on 2 DPC single rank UDIMMS
CR_6395	NO	4166478: Molette Bend ME FW for HSX PO
CR_6382	NO	4166099: Srat2.aslc breaks build when MAX_SOCKET < 4 (Partial Fix), COD\SRAT fixes from PO
CR_6381	NO	4166804: PPM data not output according to MAX_SOCKET
CR_6380	NO	4166706, 4166732: Add BIOS_ID and Platform ID to debug output before MRC
CR_6361	NO	4166830: BIOS D14 gets page fault in nonpaged area trying to run memrunner
CR_6357	NO	4166852:HSX Clone: QPI EP : Enabling L1 is flagging CorErr 0x22 phy detected inband reset
CR_6356	NO	4166854:QPI: 4SPO changes
CR_6354	NO	4166831: DIMMs in slot 1 causes failures
CR_6343	NO	4164769: Remove new files from ServerCommon package, need to be moved to override
CR_6335	NO	4166799 Wellsburg PchInit unmatched RestrictedBegin/RestrictedEnd tags
CR_6315	NO	4166824:QPI: fix CRB qpi rate options
CR_6310	NO	4166765: Enable 2133 capability in HSX BIOS
CR_6298	NO	4166755: ASPM is getting enabled on PCH Root Ports even if disabled in Setup.
CR_6297	NO	4166814: BIOS programming of cc_spare2 for Uniphy Clock disables
CR_6296	NO	4166457: Need to define/finalize PCode/BIOS interactions for IIO_DFX_BNDL_DISBL_REG
CR_6276	NO	4166781: PCIE - Mismatch in advertising link capability between lnkcap and lnkcap2 can cause legacy hardware(prior to 3.0 base PCIE spec) to train only to Gen1.
CR_6273	NO	4166750: ESCALATE from hexaii_hsx_mock:Isoc: VC1/VCp BIOS knobs are not working in BIOS X20/X21
CR_6264	NO	4166820: BIOS 05.d09 fails in MRC with UD4 on Mayan City

CR_6256	NO	4166457: Fix for Build Failure Under JKT
CR_6236	NO	4166457: Need to define/finalize PCode/BIOS interactions for IIO_DFX_BNDL_DISBL_REG
CR_6235	NO	4166776: PCIE slot power loss on warm reset
CR_6234	NO	4165760, 4165779, 4165806, 4165807, 4165833, 4165834, 4165874: Security password refresh issues
CR_6231	NO	NO SIGHTING: force QPI Link to 8.0GT if CRB platform and request speed is greater than 8.0G
CR_6229	NO	4166811: Implement "Enforce POR" setup option for memory
CR_6228	NO	4166764: Timing registers not set correctly when socket 1 does not have memory populated
CR_6227	NO	4166798: BIOS Setup In the Merge Trunk BIOS is Broken
CR_6226	NO	4166809: tRRD is being truncated to 8 bits
CR_6225	NO	4166768: Enable early CMD-CLK training in BIOS
CR_6224	NO	4166766: Enable Rx/Tx Vref training in BIOS
CR_6221	NO	4166786: RxVref Training Algorithm Using Incorrect Timing Offsets
CR_6214	NO	4166801 - Incorrect placement of RestrictedEnd tags causes build errors
CR_6209	NO	4166796: Rename PFAT binary file extension from .uni to .bin
CR_6203	NO	4166790, 4166714 - QpiMain.c file uses hard-coded value in SetupHtBase function/QPI: topology reduction not working in EP
CR_6169	NO	4166676: Pci64BitResourceAllocation knob not being honored for CBDMA base address
CR_6142	NO	4166501, 4166719: Merge Changes in from the Power-On Stream
CR_6140	NO	4166475, 4166688: Merging from the Power-On Stream
CR_6124	NO	4164394:Memory Dimm Isolation on Error
CR_6063	NO	4166557: HSX Clone: PCIE - Gen2/3 degraded width won't recover full width due to OC Done not being complete
CR_6043	NO	4166459: Add XHCI support in Grantley Trunk code
CR_6016	NO	4165457 - code for signal enabling - MCi_CTL2
CR_5482	NO	Grantley Release 03_R00 Package
CR_5431	NO	4166339: PCIe IIO Uplink Port No Longer Exists on HSX
CR_5430	NO	4166417: resolve mismatch between suggested ddrio register config and current MRC.ddrio.init code values
CR_5424	NO	4166183: Need certain training steps enabled by default, with BIOS setup option for others.
CR_5422	NO	4166467: Correct default values for Bits10-0 of HSX IIO_DFX_BNDL_DISBL_REG (refer HSD [4166457])
CR_5398	NO	4164172, 4165266: PFAT Support and Setup Menu item
CR_5395	NO	4166429: [HSX_A0_PO] CLONE from HSX: SAPM DLL: PCODE is not checking de-feature bit IO_FEATURE_DISABLE_ENABLE_SAPM_DLL
CR_5392	NO	4166458: PACKAGE_RAPL_LIMIT CSR renamed
CR_5386	NO	4166091, 4166340: Disable RCOMPs and set HA credit counts
CR_5383	NO	4166445 Addendum. HSX-a0 w/a -- QPI link calibration timers: etoc = 14 & etdcc =12
CR_5381	NO	4166443 01_D040 CRB External doesn't boot on Simics Grantley, DXE_ASSERT!: w:\grt01_d40_grtr\GrantleySocketPkg\Dxe\IioInit\IioGen3.c (1225): Bifurcation < = 4

CR_5378	NO	4166437: Advanced/earlyCMDCLK training changes needed due to SRX8 RDIMM problem.
CR_5377	NO	ADDENDUM to CR_5265: 4166237: PO values for RX_CTLE_PEAK_GEN1/2/3
CR_5376	NO	4166443: 01_D040 CRB External doesn't boot on Simics Grantley, DXE_ASSERT!: w:\grt01_d40_grtr\GrantleySocketPkg\Dxe\IioInit\IioGen3.c (1225): Bifurcation <= 4
CR_5371	NO	4166091, 4166141, 4166184: Periodic RCOMP WA and Added support for 4 VR's
CR_5370	NO	NO SIGHTING: Add rank interleave selection for Emulation
CR_5369	NO	4165796, 4165812, 4166285: Add C/A Parity setup option, Set PO DDR speed, Limit DDR4 to 1867
CR_5366	NO	4165776, 4165933: Set default SMB clk to 400K and add option to select 1M for DDR4
CR_5364	NO	4166453. HSX A0 WA - Do not program the home field of the QPIA2RCRCTRL register to a value greater than 0xe (the default)
CR_5363	NO	4166434: Issues found on multiple CPU/PPM setup options
CR_5355	NO	4166441: Simics errors when BIOS accesses byte/word CSRs via DWord
CR_5354	NO	4166427:Tracking for 2S COD emulation bringup minibios fixes
CR_5352	NO	4165817: Initializaton settings in BIOS for DDR training - ODT/VREF
CR_5347	NO	NO_SIGHTING: Round2 of PPM code resturct
CR_5333	NO	4166430: [HSX_A0_PO] CLONE from HSX: PMA_CR_SQUELCH_MASK needs to be set correctly for HW to complete PkgC entry
CR_5333	NO	4166430: [HSX_A0_PO] CLONE from HSX: PMA_CR_SQUELCH_MASK needs to be set correctly for HW to complete PkgC entry
CR_5331	NO	4166445 HSX-a0 w/a -- QPI link calibration timers: etoc = 14 & etdcc =12
CR_5323	NO	4166342:Change the GPIO register values settings for GP64 to GP67
CR_5322	NO	4166234: Entering Advanced menu causes HII corruption
CR_5316	NO	4166180: DDR DdrCrCtlTraining.CtlDrvSegEn field is missing in ddrctlcr readback logic
CR_5315	NO	4166396: BIOS is not reserving the IEDRAM which causes a failure when running on SVOS
CR_5310	NO	4166126:QPI: DCAEN
CR_5303	NO	4166369:WBG_PO SSE3 Recipe Non-Functional in Grantley Stream
CR_5290	NO	4166245: Simics command line window error messages - IIO Driver Portion
CR_5286	NO	4166422: HSW-EP : MemRas S3 support
CR_5285	NO	4166398: HA's MCCRDTTHRLD registers needs to be updated based on pointer separation values
CR_5284	NO	4166259: Klocwork Issues: 246, 247, 248, 249, 250, and 251
CR_5281	NO	4166318: Need initializaton settings in BIOS for DDR training - Package Delay Table
CR_5278	NO	4166258: Klocwork Issue: 256, and 754
CR_5274	NO	4166424: Part 2: [HSX_A0_PO] CLONE from HSX: Switch parity calculation zeroes TH bit in header so PCIDCAHint is not sent
CR_5269	NO	4164595: MESeg base and size initialization
CR_5268	NO	4166425: Part 2: CLONE from HSX: r2pcie logs spurious credit overflow errors during reset
CR_5267	NO	4166237: IIO workaround review list
CR_5265	NO	4166237: HSX Uniphy Recipe v0.6
CR_5240	NO	4165533: IIO does not support psuedo registers

Notes:

- This release is the pre-silicon sample code for Grantley/Haswell-EP Reference Code.

Known Issues:

- None

Potential Issues: (investigating)

- None

Sighting fixes and enhancements: (fixes and enhancements since last RC release)

ID	RC	Title
CR_939	NO	4165062: 32-bit Extended APIC ID support (ACPI 4.0 extensions) with BIOS option to force >8bit APIC ID value on VP
CR_737	NO	4164887: BIOS must configure the on-board graphics controller as the boot device when the motherboard is in Manufacturing-Mode.
CR_712	NO	416551, 4165620: DDR4 1.2v only support and MRC clean up
CR_710	NO	4165295: Setup option to relocate IOxAPIC in PCH.
CR_671	NO	4165524: DDR4 SPD Support
CR_668	NO	4165054: BIOS to support GPIO's detailed in the common core GPIO spreadsheet.
CR_667	NO	4164311: BIOS provides actual operating frequencies for all enabled CPUs in the system in setup
CR_635	NO	4164294: "PSMI Enable" setup option
CR_615	NO	4164993: Azalia VCp Optimizations Knob
CR_540	NO	4164721, 4164762: Support IDCODES/DEVID/RevID for WBG compatibility and algorithm for LPT RID translation to WBG
CR_537	NO	4164956: PilotIII (BMC) - Super IO support
CR_534	NO	4164547: BIOS should hand off control to OS with COM1 configured at 9600 n 8 1
CR_533	NO	4164576, 4164708: Port 80/84 postcode support and setup option for LPC and PCI bus redirection
CR_5320	NO	Grantley Release 02_R00 Package
CR_532	NO	4165624: Sense Amp Training
CR_530	NO	4164159: Crossover Calibration Training
CR_526	NO	4165623: MRC DDRIO API - Data
CR_5253	NO	4166411:Early Snoop not enabled in Sbo
CR_5247	NO	4166424: [HSX_A0_PO] CLONE from HSX: Switch parity calculation zeroes TH bit in header so PCIDCAHint is not sent
CR_5245	NO	4166425: CLONE from HSX: r2pcie logs spurious credit overflow errors during reset
CR_5239	NO	4164410: Error Logging

CR_5218	NO	4166421: OEM build error in PpmInitialize.c
CR_5217	NO	4166408: OEM build error with DxePlatform.inf
CR_5216	NO	4166406: OEM Build issue with undefined symbol V_PCH_LPTH_SATA_DEVICE_ID_D_RAID_SERVER in PciPlatform.c
CR_5215	NO	4166410: OEM build error with missing IpmiTransportProtocol
CR_5214	NO	4166407: OEM build error PatsburgPkg references in LastBootErrorLog.inf and WheaPlatformHooksLib.inf cause build issues
CR_5211	NO	4166107: QPI default for PO. Clean up OemMemoryQpiInit, Fix Minibios build due to SecOemLib
CR_5203	NO	4166416: Header files: Need add Sbo devices
CR_5198	NO	4166291 HSX -A0 w/a Reset Microcode does not properly report out LLC BIST errors
CR_5196	NO	4166412: DBG_MUX1_IIO_DFX_GLOBAL_REG Does Not Exist in HSX
CR_5196	NO	4166412: DBG_MUX1_IIO_DFX_GLOBAL_REG Does Not Exist in HSX
CR_5192	NO	4165036:Products that support ECC must log memory errors related to ECC in SEL
CR_5192	NO	4165036:Products that support ECC must log memory errors related to ECC in SEL
CR_5180	NO	4166385:4166379: isoc changes and Program Cbo_Coh_Config_CFG to match IVT settings
CR_5176	NO	4165901 WellsburgPkg code cleanup issue for 0.5 release.
CR_517	NO	4164326: Option to force system to boot to BIOS setup screen rather than requiring user to hit in a specific window of time
CR_5166	NO	4166373: BIOS needs to disable write-level training bit before updating TXGROUP
CR_5165	NO	4166397 OEM release build error with PchPlatformlPolicy.h and SetupPlatform.c
CR_5163	NO	4166362: Conversion from UINT8 to UINT16 is not correct for piCode's passed to GetSetDataGroup
CR_516	NO	4164535: Support for saving/restoring BIOS setup options to a file.
CR_5154	NO	4166343: Late command clock training fails due to num_cachelines programming error in BIOS
CR_5152	NO	4166013: MRC needs to disable 2cyc_byp before doing any cpgc activity and re_enable it before entering normal mode
CR_5151	NO	4166374:change ctle to 14
CR_515	NO	4165262: Report an error if DDR3 and DDR4 is found on Grantley
CR_5149	NO	4165818: DDR: Need to restore initial VREF for Sense Amp Training
CR_5148	NO	4166277, 4166186, 4166152, 4166192 - Setup related, remove CPU Only reset from RC
CR_5147	NO	4166320: MRC: Need initializaton settings in BIOS for DDR training - cmd_stretch (1n/2n/3n modes)
CR_5146	NO	4166238: HSX DDRIO initialization Flow Diagram
CR_5145	NO	4166096, 4166144: DDR: Need to Implement Conservative Turnaround Timing by PO
CR_5137	NO	4166323: missing restricted tags update
CR_5132	NO	4166374:QPI: initial txeq for PO
CR_5118	NO	4164769: Setup parameters for IPMI
CR_5114	NO	4166393: Invalid AML module name used when loading Processor Aggregator module
CR_5106	NO	4166360: PCIE NTB: pb23base and pb45base not set correctly
CR_5103	NO	4164857 and 4164543 : BIOS should not mask any errors in the system
CR_5092	NO	4166369, 4166372:WBG_PO SSE3 Recipe Non-Functional in Grantley Stream, Merge Remaining WBG Learnings From Grantley_PPO Stream To Grantley Stream

CR_5090	NO	4166282: [HSX_A0_PO] CLONE from HSX: Increase OC timer due to widened DCC calibration times
CR_5089	NO	4166366: [HSX_A0_PO] CLONE from HSX: PUSH from ivytown: With the VT-d denial of service fix enabled the PCIE TXN Layer does not return posted data credits
CR_5081	NO	4166383: Extra Global ASPM Setup Option in the PCIe Port Setup
CR_507	NO	4165084: Display firmware revision in setup
CR_5064	NO	4165786: PCIE: Port Naming Convention needs to change to Device Function
CR_5033	NO	4164582: Ref code ?Options? bits should be defined in a header file with comment
CR_5014	NO	4165662: BIOS need to support SPI Memory W25Q256FV
CR_5008	NO	4166365:4166367:NumSnpCreditsL0:Both HAs RTIDs being programmed as local in COD mode
CR_4984	NO	4164794: IIO PCIe Max Read Completion Combine Size
CR_4960	NO	4165824: PCIE: BIOS option for PCIRdCurrent/DRd.UC mode select
CR_4952	NO	4166314 QPI: phy recipe 0.0.6 (rx_ctle_peak not done yet, need kit update)
CR_4947	NO	4166310: CLONE from HSX: Conflict latency optimization still leads to data corruption
CR_4946	NO	4166218 Clarification of potentially duplicate BIOS knobs for isoc
CR_4945	NO	4166111: QPI: Need add change detect for MRC
CR_4932	NO	4165824: PCIE: BIOS option for PCIRdCurrent/DRd.UC mode select (CIPCTRL[0])
CR_4912	NO	4164217: Monroe - MPST table support
CR_4911	NO	4164193: IIO error configuration
CR_4909	NO	4164379: LLC size display
CR_4902	NO	4166048: CLONE from HSX: rpegr_ak_egress.ak_agent_queue.R_R2PCIE_EgressQueue_Overflow
CR_4901	NO	4165823: PCIE: Global Completion Timeout Options needed
CR_4898	NO	4164593, 4165377, 4165863, 4165934, 4165936: Rank Disable, New RCOMP mechanism, >255 Byte SPD support, Alternate Address Map
CR_4893	NO	4165822: PCIE: Global PCIE ASPM option needed
CR_4892	NO	4166321: PcieDeviceInit() in IioPortInit.c Broken Conditional
CR_4868	NO	4166316: Add Patch23 for HSX A0 PO
CR_4831	NO	No sighting: fix a "finding TXEQ value from TXEQ table" bug
CR_4828	NO	4166065:GrantleyPkg and GrantleySocketPkg have same package GUID in their .DEC file
CR_4826	NO	4165922:D77 4-socket doesn't boot with ASSERT w:\grt00_d77_grtr\MdeModulePkg\Core\Dxe\Mem\Pool.c(437): Tail->Signature == ((('p') | ('t' << 8)) | ((('a') | ('l' << 8)) << 16))
CR_4813	NO	4166284: SVOS isn't starting up it stays mapping tables
CR_4800	NO	No sighting: fix socket 2 link 1 TXEQ table
CR_4782	NO	4165829: Need a mechanism for limiting QPI max frequency on A0 super sku parts until max frequency has been officially enabled.
CR_4781	NO	4165825: Add BIOS option for QPI/TOR_TIMEOUT enable/disable
CR_4780	NO	4166209: Unmapped access to address 0xeeeeeeee
CR_4771	NO	4165752:BIOS to support Serial port baud rate at 9600 and 19200
CR_4770	NO	4166166: Update POR table
CR_4749	NO	4164265: Reserve Ways for OCLA (IOT) - Update for BIOS/VCU flow change

CR_4728	NO	4166189: Latest DDR3 emulation minibios causing pcode hang after warm reset
CR_4702	NO	4165950: 4164409: 4165007: EH clean up effort - Bring in the clean up changes to Grantley code base: APEI 4.1 for Error Handling: Add WHEA support to Grantley BIOS
CR_4692	NO	4166187: 01_D11 RESET: Simics is stoped by 01_D11 trying to reset bios.
CR_4676	NO	4166038: Request: Jump$ BIOS option to enter Jump$ loop after MRC
CR_4673	NO	4166110, 4166185: QPI: Per port CRC, per port L1, per port L0p
CR_4665	NO	4165367: Provide DIMM presence information to BMC using set fan control configuration command
CR_4654	NO	4166078: New BoardId for Storage platform, Emerald Point
CR_4650	NO	4166093: Internal Vref Enable in data FUB should use "SelfRefresh" instead of "CKEPwrDown"
CR_4649	NO	4166092: vref enabled too frequently in cmd fub
CR_4646	NO	4166068: Remove bypass mux in DDR xover
CR_4642	NO	4166169: CompUpdate between two reads or writes to the same rank overwrites XoverSel
CR_464	NO	4165348: Support Test Menu that comes from Client BIOS
CR_4620	NO	4165008: 4165950: 4166188: WHEA EINJ update: Error Handling/Logging Port from Brickland: CpuCsrAccess driver update
CR_4577	NO	4165514: Implements Intel TXT Server Bios Specification v1.2
CR_457	NO	4164785: IIO PCIE: ASPM (L0s+L1) support (control)
CR_4559	NO	4166037: Memory setting misprogrammed in latest 2HA emulation BIOS
CR_4547	NO	4166118: 4166053: QPI: Implement latest Phy recipe and link recipe from EV/CLONE from HSX: default value for IOVB_TX_IREF is incorrect -- is 2 and should be 0
CR_4524	NO	4166089: RatioLimit array size set too low causes compiler error for > 16 cores
CR_4520	NO	4165950 - Bring the Error Logging clean up changes from Brickland to Grantley
CR_4518	NO	4165950 - Bring the Error Logging clean up changes from Brickland to Grantley.
CR_4517	NO	4165950 - Bring the Error Logging clean up changes from Brickland to Grantley.
CR_4505	NO	4166167: Temporarily workaround the 2 CPU 8 Cores SKU boot issue with Simics
CR_4488	NO	4165386: ME9 FW image support requirements for Grantley platforms
CR_4465	NO	4166025, 4165951: [WBG AO PO] BIOS settings for WBG PO, update HCCPARAMS to fix XHCI config
CR_4455	NO	4166150: Misc. MRC changes from design/BIOS F2F
CR_4454	NO	4164163, 4164165: Per-bit Timing Deskew
CR_4441	NO	4165985: Need Perf P Limit support
CR_4439	NO	4164952:IPMI 2.0: POST Complete assert support
CR_4420	NO	4165894:HSX BIOS r2/r3 credit programming for PSMI
CR_4420	NO	4165894:HSX BIOS r2/r3 credit programming for PSMI
CR_4418	NO	4166140: Round Trip Latency Training
CR_4397	NO	4166109:4166135:QPI: Misc previosuly completed ARs from F2F review
CR_4379	NO	4164199: HSW eSMM changes for server
CR_4369	NO	4166105: Implement hardware based memory test and initialization
CR_4362	NO	4165991: VrMask always program without condition
CR_4358	NO	4165988: Add EET Override control

CR_4349	NO	Fixed 1S buffer credit support in IdentifySysConfigTypeHsx()
CR_4331	NO	4166074:4165361:QPI: Need to support COD (Cluster on Die) mode
CR_4294	NO	4165274: Moving SPS support from GrantleyRestrictedPkg to GrantleyPkg
CR_4293	NO	4164919, 4165271, 4165548: NM FW req. to turn cores off at boot-time; Set CPU perf. for POST; Removing ActiveCoreCount var.
CR_4292	NO	4165953: D87 does not set RST_CPL1 bit before WARM RESET
CR_4280	NO	NO_SIGHTING: QPI Setup syncup with Brickland
CR_4271	NO	4166072: Suplement to s4166021 (Update SPS ME support to the latest SPS ME-BIOS spec)
CR_4268	NO	4166047: Hotham 1.0 support in Grantley
CR_4266	NO	4265858: Late DDR CMD/CLK Training
CR_4232	NO	4166032: [ERB] Remove 'Restricted' Wellsburg DIDs
CR_4217	NO	4165993: Change Bandwidth scale per channel from per DIMM
CR_419	NO	4164802: CPU IIO: BIOS will provide a setup selection to Enable/Disable PCIe Extended Sync
CR_4187	NO	4166026: [ERB] PlatformIpmi.inf Depex build error in ERB (IP-free) build
CR_4177	NO	4165042: Put BIOS-ACM and SINIT-ACM in BIOS image
CR_417	NO	MemoryQpiInit.c Update
CR_4169	NO	4166021: Update SPS ME support to the latest SPS ME-BIOS spec
CR_4133	NO	4165463, 4165815, 4165871: Add option for Extended Tag Support, Isoch Coherency support, and Azalia VC1/VCP config
CR_4126	NO	4164475_4164476: Power Management: CLTT; Power Management: OLTT
CR_4113	NO	4165926: D69 bios fails in booting LCC 2 sockets 1 core 1 thread
CR_4112	NO	4165966 BIOS reports wrong number of cores in SSDV simulation
CR_4090	NO	Add runtime ASL code to issue commands to BMC to implement PowerMeter
CR_4072	NO	4165839: Manufacturing Mode: When Manufacturing Mode is ON setup menu is not displayed
CR_4045	NO	4164265 Config IOT/LLC - HSX VCU MAS Update
CR_4044	NO	4164251, 4164279: Scrub: Mirror scrub and LA Qual setting linked to setup options
CR_4039	NO	NO SIGHTING: MPM code sync with Romley-refresh and Brickland
CR_4030	NO	4165250: CPU replacement detection/DRAM_INIT_DONE message for SPS firmware
CR_4019	NO	3617091: BGF Tuning for DDR3-800
CR_399	NO	4164265 Reserve Ways for OCLA (IOT)
CR_3951	NO	4164265 Reserve Ways for OCLA (IOT) - Update to support HSX VCU Mailbox interface
CR_3948	NO	4164194:PCIe multicast
CR_3947	NO	4165932:Port PchSpi protocol from LPT client BIOs to WellsburgPkg
CR_394	NO	NO_SIGHTING: disable PchInt15 hook for SCU on PBG
CR_3936	NO	4165924: MRC: Support COD mode
CR_3924	NO	4165901:WellsburgPkg code cleanup issue for 0.5 Release
CR_3918	NO	4165930: Softsdv hangs with new PCH updates in release 81
CR_3912	NO	4165902, 4165903, 4165905, 4165906, 4165907, 4165908, 4165909: Cleanup for RC 0.5 External Release
CR_3904	NO	4165356:QPI: Need to support MCTP

CR_3897	NO	4165542, 4164295, 4164306, 4164147, 4164608, 4165013, 4165014, 4165015, 4165017, 4165019: Updated SPD, added Interleave and sparing support, and option to disable unused channels
CR_3891	NO	4164446: Power Management: HEDT overclock
CR_3890	NO	NO_SIGHTING:Qpi0904 sync. Fix route table programming
CR_3889	NO	4165761, 4165887: Unable to reset after accessing Advanced menu in Setup
CR_3875	NO	4165901 Wellsburg code cleanup issue for 0.5 release/
CR_3871	NO	4165726: Clone from HSX: Chicken bit for Per Core P-States
CR_3862	NO	No Sighting. Synch with LPT/Wellsburg client code.
CR_3835	NO	4165679 Update GPIO table based on the latest Grantley CCA GPIO revision.
CR_3833	NO	4164143 - RSTE 4.0
CR_3819	NO	4164444 - PERR Enable and 4165037-Add setup options - Poison
CR_3792	NO	4165731 Simics: BIOS hangs with 2s/18c/2t config
CR_3768	NO	4164269, 4164789: PCIE Lane Mask and TPH
CR_3762	NO	4164748: BIOS Reset test option should include also a setup option to test PCIE/DMI only or WBG PCIE/DMI only
CR_3757	NO	4165006 Add Setup Option: WHEA Error Handling enable/disable
CR_3732	NO	4165427 Patch23 Code Sync with Brickland CR_3574
CR_3729	NO	4164479: Power Management: UFS (Separate uncore frequency)
CR_3728	NO	4164877: Need to disabled channel and rank interleaving for EMULATION miniBIOS builds
CR_3723	NO	4164265 Reserve Ways for OCLA (IOT) - Update to support HSX VCU Mailbox interface
CR_3711	NO	4165482: Support disable OPTION ROM launch for each PCI-E Slot.
CR_3710	NO	Support disable OPTION ROM launch for each PCI-E Slot.
CR_3709	NO	Support disable OPTION ROM launch for each PCI-E Slot.
CR_3708	NO	4165866: Simics: D68 BIOS reports total memory incorrectly
CR_3694	NO	4165530: CPU stepping from BIOS for MCU display on MCU LCD
CR_3682	NO	4165802: Simics: More than 2 cores cause Assertion Lock->Lock = = EfiLockReleased
CR_3662	NO	4165862: Memory mapping bug
CR_3661	NO	4165861: Print dimmmtr to the debug log
CR_3650	NO	4165860: wpq_inorder_en needs to be set during DDR training
CR_3649	NO	4164165, 4165858, 4165859: 2D Rd Centering, Late CMD/CLK, and ZQ calibration
CR_3605	NO	4165800: HW_EMULATION flag causing grantley minibios hang in Simics
CR_36	NO	NO_SIGHTING: HA2 memory address map fix
CR_3506	NO	NO_SIGHTING: Port PchSpi driver to Client implementation code (H0084_52 label)
CR_3454	NO	NO_SIGHTING: Sync PCH Client code to label H0084_542
CR_345	NO	4165550: Boot hangs in QPIRC (new in D10)
CR_3404	NO	4165706:QPIRC: GRNTINT D39 in 4S config ends in QpiCoh.c
CR_3402	NO	4165717:Grantley 0.5 release: QPIRC: Review code and make sure it is ready for release
CR_3398	NO	4165442 HLV: Thermal Monitor Temperature Offset knob needed
CR_3375	NO	NO_SIGHTING: Clean up typos, add hot plug data & comments OemIioInit.c
CR_3353	NO	4165379, 4164224, 4164256, 4165378, 4165768: Added tPar_Recovery timings, MRC options, MR5

		shadow support and fixed DIMM speed reporting.
CR_3348	NO	4165767: D058 assertion in SoftGrantley due to IntelDebug implementation
CR_3335	NO	s4164101 - PCIe LTR
CR_3334	NO	4165755:Add scratch support to enable disable some key features for automated emuMinibios generation
CR_3333	NO	NO_SIGHTING: mmio routine cleanup and common definitions for MMCFG addresses
CR_3329	NO	4165748: Emulation: DDR4 failures w/ HSX-D044.3-EP-2S-HCC-2HA-1QPI-RDIMM-DDR4-4CH-1RANK-1GB
CR_331	NO	4165072: The BIOS needs to enable SMI on write to SLP_TYPE register.
CR_3307	NO	4164584 Support PCI Express AtomicOp Requests
CR_3282	NO	4165742: D49,D51 gets stuck in HSXEP2S-2C-1T Simulation
CR_3281	NO	4165504, 4165530: Display CPU stepping and BIOS version on Kahuna platform LCD
CR_3247	NO	4165716: Grantley 0.5 release: MRC code clean up
CR_3244	NO	4165364: Support for Debug Interface MSR
CR_3210	NO	NO_SIGHTING: Merge in MRC fixes from IVT
CR_3180	NO	4165720: Part of the sighting - Grantley 0.5 release: RAS: Clean up code ported from Brickland : Error log cleanup.
CR_3179	NO	NO_SIGHTING: Added 18C support in ACPI paltform
CR_3151	NO	4165483: BIOS shall lockdown backup BIOS blocks in flash using protection range registers
CR_3145	NO	4165371: Provide option for user to set fan PWM offset in BIOS SET UP menu and communicate this to BMC
CR_3138	NO	4165370, 4165366:BIOS updates the BMC?s system (SEL) time using Set SEL Time upon ACPI power state transitions;Inform ACPI set state change to BMC using Set ACPI power state cmd
CR_3136	NO	4165690:Nuvoton LPC SIO BIOS support for Aztec City - STHI
CR_3132	NO	4164298:Memory Page Reservation - User Configurable
CR_3131	NO	4164960:System Information Screen support
CR_3115	NO	4165733: Emulation miniBIOS fails push pop test with BIOS D44
CR_3066	NO	4164959: Dual video support
CR_3062	NO	4164962: SystemGUID (SYSGUID/GUID) support
CR_3055	NO	4165727:QPIRC: Sync 711 sim
CR_3043	NO	4164259: Bios knobs to program (alpha)s (alpha)f and C values
CR_3039	NO	4164903: Options to Disable system sleep states (individually) (pt.2)
CR_3029	NO	4165715: Grantley 0.5 release: Make sure DVP platform definition is within SV_HOOKS.
CR_3000	NO	4164173: platform-bifurcation, and equalization settings
CR_2996	NO	4164734: Porting SPS ME-BIOS implementation from Denlow
CR_2966	NO	4165708:QPIRC: Fix cpupciacess for 3rd qpi agent
CR_2959	NO	4165707:QPIRC: minibios fails to boot
CR_295	NO	CpuInit.c Sync, CoreDisable change etc.
CR_2917	NO	4164976:CPUSV: BIOS KNOB: Ability to enable/disable Isoc.
CR_2903	NO	4165700: 3 DIMMs per channel hangs in DDR training

CR_2902	NO	4165549 No 18-core support
CR_2901	NO	4165507 - Wellsburg to include 4-6 extra SATA ports (Setup options).
CR_2897	NO	NO_SIGHTING: Sync file names with Denlow ME
CR_2883	NO	NO_SIGHTING: Sync/Update IIO module with changes from Brickland
CR_2871	NO	4165673 BIOS need to provide a menu option to modify Function Disable 2 register.
CR_2870	NO	4164923: Add SetupOption(s) - Breakpoints, minor fix to previous commit
CR_2868	NO	No sighting - Synch PCH Client code to label H0079.
CR_2855	NO	4165699: MRC hangs when running with two DIMMs per channel
CR_2854	NO	4165698: Early CMD/CLK results overwritten
CR_2817	NO	4164160: Parity based CMD-CLK Training
CR_2816	NO	4165696:Synch to 5/20 headers
CR_2811	NO	4164997, 4165644: WellsburgPkg needs to be updated with PatsburgPkg Reset changes to support ResetSystemLib and update Yakima USB OC settings
CR_2777	NO	NO SIGHTING: Remove CR_1395 to solve HSD#4165687 - Latest Grantley BIOS asserts with Softsdv while reading CPUID
CR_2776	NO	4165693: Add support for DDR_TRAINING_EN emulation flag for Simics
CR_2770	NO	4164997: Onboard LAN support
CR_2738	NO	4165642, 4165643, 4165644:USB port and overcurrent pin assignment for Aztec City, Inca City and Yakima City
CR_2737	NO	4164923: Add SetupOption(s) - Breakpoints
CR_2724	NO	4165504: BIOS version displayed on LCD of the MCU_Card on Kahuna platform
CR_2718	NO	4165094: Default boot order defined
CR_2709	NO	NO_SIGHTING: Use HSX new FUSED_CORES register to read fused_cores_mask
CR_2701	NO	No Sighting: Update register EQU file for SEC phase CPU init code
CR_2661	NO	No Sighting: Pipe.c GetSbspSktId() bug fix
CR_2652	NO	No Sighting: Sync SetRstCpl function with Brickland (new HSX header files are now available)
CR_2651	NO	4165354:4165156:4165155:4164286:4164255:Sync latest QpiRcSim606
CR_2641	NO	4164265 Reserve Ways for OCLA (IOT) - Updated for HSX new requirements
CR_2640	NO	4164903: Options to Disable system sleep states (individually)
CR_2626	NO	4165677: BIOS simualtion flow for 2 HA's need to be implemented
CR_2622	NO	4165675: Memory training on channel 2/3 fails due to incorrect device number for DDRIO
CR_251	NO	4164712 WBG BIOS Shall inherit LPT configuration options and algorithms
CR_2406	NO	4165669: WellsburgPkg needs to be updated to the latest LPT client code label D75 and Remove PBG depedencies
CR_240	NO	4165449, 4165368, 4164945: Initial support for platform differentiation via board ID bits
CR_237	NO	Update CpuInit.c and related files by syncing with Romley/Brickland BIOS
CR_22	NO	Merge HSX Minibios Label 05, remove CPU Online related RAS drivers, update IIO\Error logging code\platform code to build with CSR header files
CR_202	NO	NO_SIGHTING: miscellaneous fixes for softsdv 1S boot
CR_189	NO	NO_SIGHTING: miscelleneous fixes for simics 1S boot

CR_1690	NO	4164945: MonoBIOS support (pt. 2)
CR_166	NO	Changed "NODE" to "SOCKET" in equate file
CR_151	NO	Sync-up ProcessorStartup folder files with Brickland D032
CR_1464	NO	NO_SIGHTING: Remove CR_1129 - CORE_PACKAGE_37651 Sync
CR_1395	NO	4164390: Cx State Autodemotion
CR_130	NO	Delete duplicate refcode files from Minibios folder to avoid confusion.
CR_1249	NO	4165598, 4165599, 4164581: EQ Setting Tables;EQ Setting Platform Hooks;QPI electrical params should be centralized in a well defined OEM file
CR_1248	NO	4164453, 4164653, 4165135, 4165181,4165182,4165224,4165453: QPI L1 Clock Gating;QPI L0r;Need ability to select QPI Port speed(s);L0p;L1;L0r;per-port L1 clock gating;
CR_1208	NO	4164945: MonoBIOS support
CR_1200	NO	4164487: Power Management: EET (Energy Efficient Turbo)
CR_1199	NO	4164515: Power Management: Pn/Pm clamping Pn/Pm selection for PROCHOT
CR_1187	NO	4164614, 4164612: Add setup option for Write buffer high water mark, EV MRC repeatability test
CR_1158	NO	4165505 WBG to add 4-6 SATA ports on SI
CR_1137	NO	4164943 Add SetupOptions - Patch & Patch 2/3 Load Option
CR_1135	NO	4165498: support Function and Port disable; Device disable
CR_1133	NO	4164508: Power Management: S3 support for Server
CR_1125	NO	4165430: HLV: SASV: BIOS knobs to program Latency MSRs.
CR_110	NO	NO_SIGHTING: MRC updates (DDR4, sense amp training, call table fix,..)
CR_1078	NO	4165655: BIOS to provide a setup option to hide/unhide devices on Wellsburg chipset
CR_1074	NO	4165657 NO_SIGHTING: EMULATION: miscalculation for DDR4 MR2 write latency; remove emulation hacks no longer needed
CR_1073	NO	4164987: All registers with RW-L attribute must be programmed
CR_1064	NO	4164221, 4164247, 4164252, 4164253, 4164254, 4164257, 4164916, 4164630: Added new setup options
CR_1057	NO	4164785: IIO PCIE: ASPM (L0s+L1) support (control) (pt.2)
CR_1042	NO	4164314: Display MaxEff/MaxNonTurbo
CR_1038	NO	NO_SIGHTING: DDR4 tweaks for emulation

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Notes:

- This release is the 1st pre-silicon sample code for Grantley/Haswell-EP.
- Boots with Simics.
- Pending requirements, WA for Platform PO.

Known Issues:

- None

Potential Issues: (investigating)

- None

Sighting fixes and enhancements: (fixes and enhancements since last RC release)

- None