AHB interface FIFO

User Guide

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Contents

1 Introduction

This document mainly describes the usage of the AHB interface FIFO IP. It works as AHB bus slave. So, it is used to facilitate user to connect FIFO to AHB bus.

The AHB interface FIFO IP supports the following features:

- Supports AHB interface protocols
- Supports two FIFO type : asynchronous FIFO and synchronous FIFO
- The interface type of Write port and Read port can be configured
- 32-bit AHB data buses
- FIFO data width can be configured
- FIFO address width can be configured
- Base Address can be configured

Device family support:

HME-M7

2 AHB interface FIFO Overview

2.1 Pin Description

Table 2-1 ***AHB interface FIFO Pin description***

Interface	Name	Direction	Width	Description
AHB interface signal	hclk	Input	1	AHB interface clock
	hresetn	Input	1	AHB interface reset, low active
	haddr	Input	32	AHB address bus
	hwrite	Input	1	AHB transfer direction: 1-write, 0-read
	hwdata	Input	32	AHB write data bus
	hrdata	Output	32	AHB read data bus
	hsel	Input	1	AHB slave select signal
	hready_out	Output	1	Transfer done output
	hresp	Output	1	Transfer response signal
	htrans	Input	2	AHB Transfer type signal, single or burst
	hsize	Input	3	AHB Transfer size signal
	hburst	Input	3	AHB Transfer type signal, increment or wrap
	ahb_fifo_int	Output	1	FIFO interrupt signal
FIFO port	clk	Output	1	Clock signal
	rst_n	Output	1	Reset signal, low active
	wclk	Output	1	Write clock signal
	rclk	Output	1	Read clock signal
	wrst_n	Output	1	Write reset signal, low active
	rrst_n	Output	1	Read reset signal, low active
	wclr	Output (optional)	1	Clear write pointer signal
	rclr	Output (optional)	1	Clear read pointer signal
	fifo_clr	Output (optional)	1	Hardware FIFO pointer clear signal
	wdata	Output	wr_dw	Write data signal
	rdata	Input	rd_dw	Read data signal
	wen	Output	1	Write enable signal
	ren	Output	1	Read enable signal
	almost_full	Input	1	Indicates that only one more write can be performed before the FIFO

				is full.
	almost_empty	Input	1	Indicates that the FIFO is almost empty and one word remains in the FIFO.
	prog_full	Input	1	This signal is asserted when the number of words in the FIFO is greater than or equal to the assert threshold. It is deasserted when the number of words in the FIFO is less than the threshold.
	prog_empty	Input	1	This signal is asserted when the number of words in the FIFO is less than or equal to the programmable threshold. It is de-asserted when the number of words in the FIFO exceeds the programmable threshold
	wfull	Input	1	FIFO full flag, active high
	rempty	Input	1	FIFO empty flag, active high
	wr_data_cnt	Input	wr_aw	Indicate how many data are stored in FIFO, in write clock domain
	rd_data_cnt	Input	rd_aw	Indicate how many data are stored in FIFO, in read clock domain
	prog_full_thresh	Output (optional)	wr_aw	Threshold value for the assertion and de-assertion of the programmable full flag.
	prog_empty_thresh	Output (optional)	rd_aw	Threshold value for the assertion and de-assertion of the programmable empty flag.
	prog_full_assert	Output (optional)	wr_aw	The upper threshold value for the programmable full flag, which defines when the signal is asserted.
	prog_full_negate	Output (optional)	wr_aw	The lower threshold value for the programmable full flag, which defines when the signal is de-asserted.
	prog_empty_assert	Output (optional)	rd_aw	The lower threshold value for the programmable empty flag, which defines when the signal is asserted
	prog_empty_negate	Output (optional)	rd_aw	The upper threshold value for the programmable empty flag, which defines when the signal is de-asserted.

Note: wr_aw means write port address width. rd_aw means read port address width. wr_dw means write port data width. rd_dw means read port data width.

2.2 Parameter Description

Table 2-2 ***AHB interface FIFO parameter description***

Name	Type	Value	Description
BASE_ADDR	integer	32'ha000_0000~ 32'hbfff_ffff or 32'hc000_0000~ 32'hdfff_ffff	The base address which can access the FIFO with AHB interface, 1K boundary.
WORK_MODE	integer	1/0	Indicates the FIFO type: 1-asynchronous FIFO 0-synchronous FIFO
WR_AHB_INF	integer	1/0	Indicates the write port interface type: 1-AHB interface 0-memory interface
RD_AHB_INF	integer	1/0	Indicates the read port interface type: 1-AHB interface 0-memory interface
WR_DATA_WIDTH	integer	<=32	Write port data width
RD_DATA_WIDTH	integer	<=32	Read port data width
WR_ADDR_WIDTH	integer	4~19	Write port address width
RD_ADDR_WIDTH	integer	4~19	Read port address width

2.3 Block Diagram

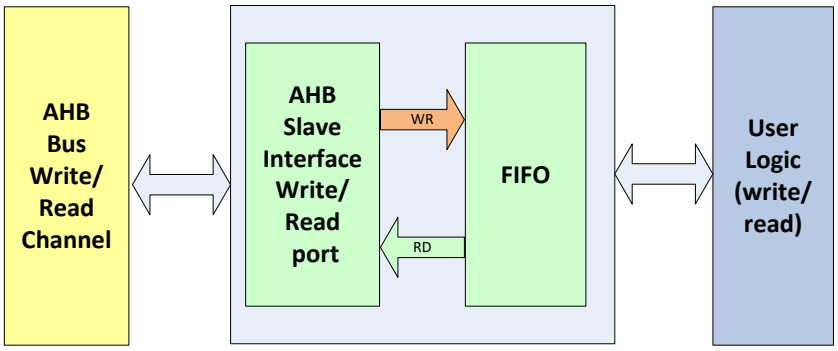

Figure 2-1(a) ***two types of interface FIFO block diagram***

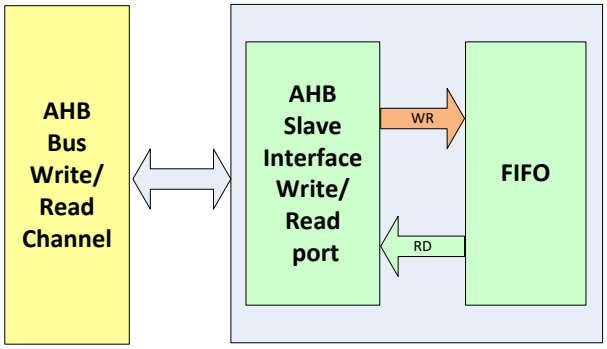

Figure 2-1(b) ***AHB interface FIFO block diagram***

The FIFO with AHB interface has two ports: write port and read port. If the FIFO works in the synchronous mode, the two ports can both be accessed by ARM or one accessed by ARM ,the other one accessed by FPGA logic. When the FIFO works in the asynchronous mode, only one port can be accessed by ARM and the other port can be accessed by FPGA logic.

3 AHB interface FIFO IP Usage

3.1 AHB interface FIFO operation timing diagram

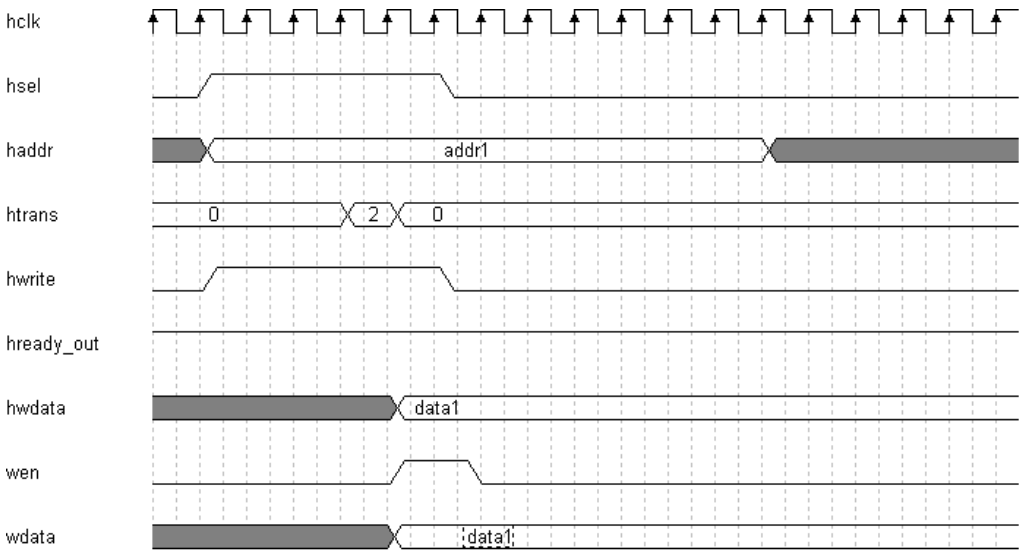

Figure 3-1 ***Basic write transfer***

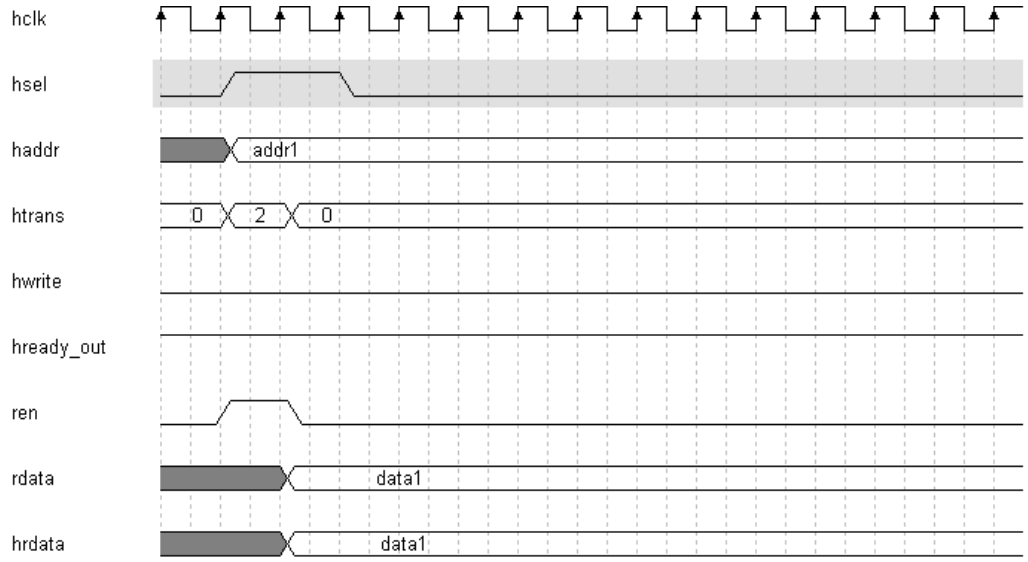

Figure 3-2 ***Basic read transfer***

In the figure 3-1, it is described how to transform the AHB bus signals to make them fit the FIFO write operation .The single transfer consists of one address cycle and one data cycle on the AHB bus side. When the trans signal is valid, the haddr and other control signals can be sampled and broadcasted to FIFO on the next

hclk rising edge.

In the figure 3-2, it is described how to transform the AHB bus signals to make them fit the FIFO read operation .The single transfer consists of one address cycle and one data cycle on the AHB bus side.

When the trans signal is valid, the haddr and other control signals can be sampled and broadcasted to FIFO on the next hclk rising edge. The read data from FIFO are routed directly back to the AHB.

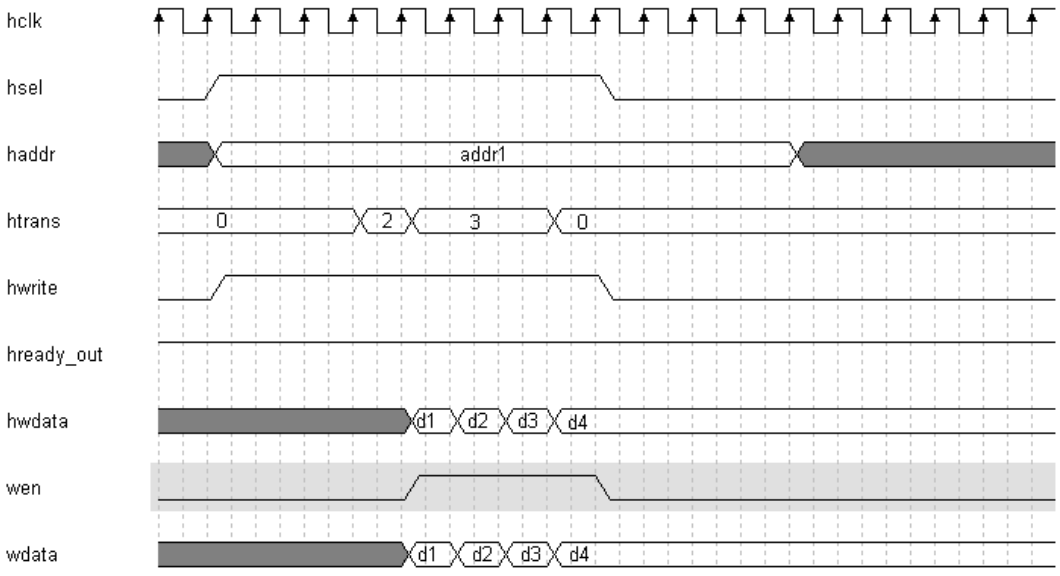

Figure 3-3 ***Burst writetransfer***

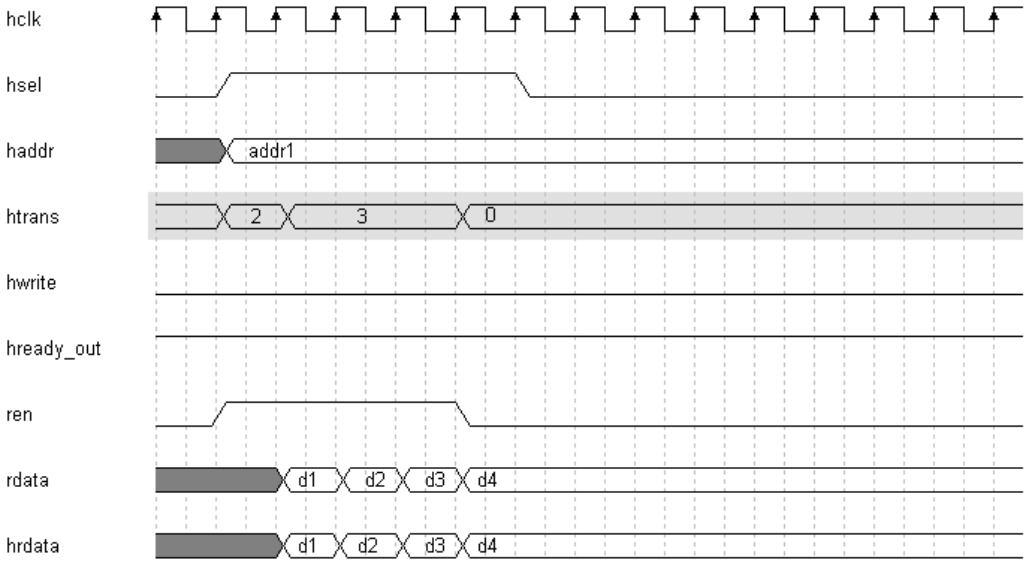

Figure 3-4 ***Burst read transfer***

3.2 AHB interface FIFO address mapping

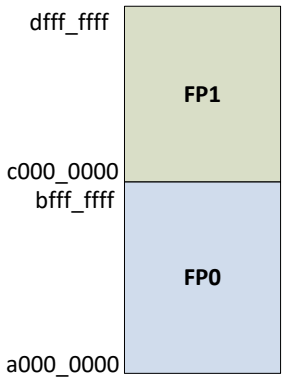

Figure 3-5 ***Address mapping***

The ARM Core provides two groups of AHB Bus signals,AHB0 and AHB1, so there are two memory space for user logic which are called as FP0 and FP1.It means that if you instantiate an ARM Core and choose the AHB0 , you must access your slaves on the address from a000_0000 to bfff_ffff, but if you connect the AHB interface FIFO to AHB1, the slaves can be accessed on the address from c000_0000 to dfff_ffff.
The Base Address can be configured by user, 1K boundary. The total space of FIFO data and registers is 64. The operation of writing data to FIFO or reading data from FIFO can be accomplished byy accessing the Base Address. The remain address space is for all the internal registers.

3.3 FIFO with AHB interface internal registers

The FIFO with AHB interface contains totally 12 internal registers: All these registers are shown below:

Table 3-1 ***All Internal Registers***

haddr	Registers	Comment	Access Type
BASE_ADDR+0x4	prog_full_thresh	Set the programmable full threshold value through ARM	R/W
BASE_ADDR+0x8	prog_empty_thresh	Set the programmable empty threshold value through ARM	R/W
BASE_ADDR+0xC	prog_full_assert	Set the programmable full assert value through ARM	R/W
BASE_ADDR+0x10	prog_empty_assert	Set the programmable empty assert value through ARM	R/W
BASE_ADDR+0x14	prog_full_negate	Set the programmable full negate value through ARM	R/W
BASE_ADDR+0x18	prog_empty_negate	Set the programmable empty negate value through ARM	R/W

BASE_ADDR+0x1c	fifo_ctrl_r	Set the value of fifo write/read pointer clear signal and all_int_enable signal	R/W
BASE_ADDR+0x20	fifo_int_enable_r	Set the value of separate int_enable signal	R/W
BASE_ADDR+0x24	fifo_status_r	Accessed by ARM to get the FIFO status	RO
BASE_ADDR+0x28	fifo_wr_data_cnt_r	Accessed by ARM to get the data number in write clock domain status	RO
BASE_ADDR+0x2c	fifo_rd_data_cnt_r	Accessed by ARM to get the data number in read clock domain status	RO
BASE_ADDR+0x30	fifo_int_status_r	Accessed by ARM to get the interrupt status	RO

- **FIFO with AHB interface IP internal register address description**

The base address of the FIFO with AHB interface IP is a parameter as shown in the above table and the internal registers' address are from BASE_ADDR + 0x4 to BASE_ADDR + 0x30.

- **FIFO with AHB interface IP internal register description**

- prog_full_thresh

The register has the same width with write port address width. If the port is generated through FIFO Wizard tool, the register can be accessed by ARM to set its value and read the same address to get the value.

- prog_empty_thresh

The register has the same width with read port address width. If the port is generated through FIFO Wizard tool, the register can be accessed by ARM to set its value and read the same address to get the value.

- prog_full_assert

The register has the same width with write port address width. If the port is generated through FIFO Wizard tool, the register can be accessed by ARM to set its value and read the same address to get the value.

- prog_empty_assert

The register has the same width with read port address width. If the port is generated through FIFO Wizard tool, the register can be accessed by ARM to set its value and read the same address to get the value.

- prog_full_negate

The register has the same width with write port address width. If the port is generated through FIFO Wizard tool, the register can be accessed by ARM to set its value and read the same address to get the value.

- prog_empty_negate

The register has the same width with read port address width. If the port is generated through FIFO Wizard

tool, the register can be accessed by ARM to set its value and read the same address to get the value.

- fifo_ctrl_r

The register is of 4 bit width: {fifo_clr, wclr, rclr, all_int_enalbe}, used to set the value of FIFO write/read pointer clear signal and all_int_enable. Set fifo_clr/wclr/rclr bit 1 will force clear FIFO in W/R clock domain, and set all_int_enable bit 1 will enable interrupt for FIFO.

- fifo_int_enable_r

The register is of 6 bit width: {prog_empty_IE, prog_full_IE, almost_empty_IE, almost_full_IE, rempty_IE, wfull_IE},used to enable 6 separate interrupt.

- fifo_status_r

The register is of 6 bit width: {prog_empty, prog_full, almost_empty, almost_full, rempty, wfull},used to get the FIFO status.

- fifo_wr_data_cnt_r

The register has the same width with write port address width. It is used to get the number of data stored in FIFO in write clock domain.

- fifo_rd_data_cnt_r

The register has the same width with read port address width. It is used to get the number of data stored in FIFO in read clock domain.

- fifo_int_status_r

The register is of 6 bit width: {prog_empty_I, prog_full_I, almost_empty_I, almost_full_I, rempty_I, wfull_I}, used to get interrupt status. It will be cleared to 0 as soon as it accessed by ARM.

3.4 Interrupt operation

The FIFO with AHB interface IP has six separate interrupt enable register and one all interrupt enable register. When they are enabled and one or more bits of the register fifo_status_r is 1, then the interrupt is generated. User can connect this interrupt request to any ARM's external interrupt input. And ARM will follow the normal interrupt handle procedure to handle IP's interrupt request.
ARM's external interrupt sources:

Table 3-2 ***ARM external interrupt sources***

Interrupt Serve Function	Type	Alternate Port	Description
Void FP0_IRQHandler(void)	I	fp_interrupt[0]	External interrupt 0
Void FP1_IRQHandler(void)	I	fp_interrupt[1]	External interrupt 1
Void FP2_IRQHandler(void)	I	fp_interrupt[2]	External interrupt 2
Void FP3_IRQHandler(void)	I	fp_interrupt[3]	External interrupt 3

Void FP4_IRQHandler(void)	I	fp_interrupt[4]	External interrupt 4
Void FP5_IRQHandler(void)	I	fp_interrupt[5]	External interrupt 5
Void FP6_IRQHandler(void)	I	fp_interrupt[6]	External interrupt 6
Void FP7_IRQHandler(void)	I	fp_interrupt[7]	External interrupt 7
Void FP8_IRQHandler(void)	I	fp_interrupt[8]	External interrupt 8
Void FP9_IRQHandler(void)	I	fp_interrupt[9]	External interrupt 9
Void FP10_IRQHandler(void)	I	fp_interrupt[10]	External interrupt 10
Void FP11_IRQHandler(void)	I	fp_interrupt[11]	External interrupt 11
Void FP12_IRQHandler(void)	I	fp_interrupt[12]	External interrupt 12
Void FP13_IRQHandler(void)	I	fp_interrupt[13]	External interrupt 13
Void FP14_IRQHandler(void)	I	fp_interrupt[14]	External interrupt 14
Void FP15_IRQHandler(void)	I	fp_interrupt[15]	External interrupt 15

4 Resource usage

Resource usage of the AHB interface FIFO IP on fuxi, with all optional flags(such as wr_data_cnt...)

Table 4-1 ***AHB interface FIFO IP resource usage***

Resource	DepthxWidth	LUTs	Regs
synchronous FIFO, write port and read port both AHB interface	512x32	324	184
synchronous FIFO, write port is AHB interface, read port connect with FP logic	512x32	338	184
synchronous FIFO, read port is AHB interface, write port connect with FP logic	512x32	333	183
asynchronous FIFO, write port is AHB interface, read port connect with FP logic	512x32	438	244
asynchronous FIFO, read port is AHB interface, write port connect with FP logic	512x32	466	243

5 Generate File Directory Structure

The AHB interface FIFO IP wizard generated file includes: source files (src), simulation files(sim) and example design files and related document. The detailed design directory structure is as below.

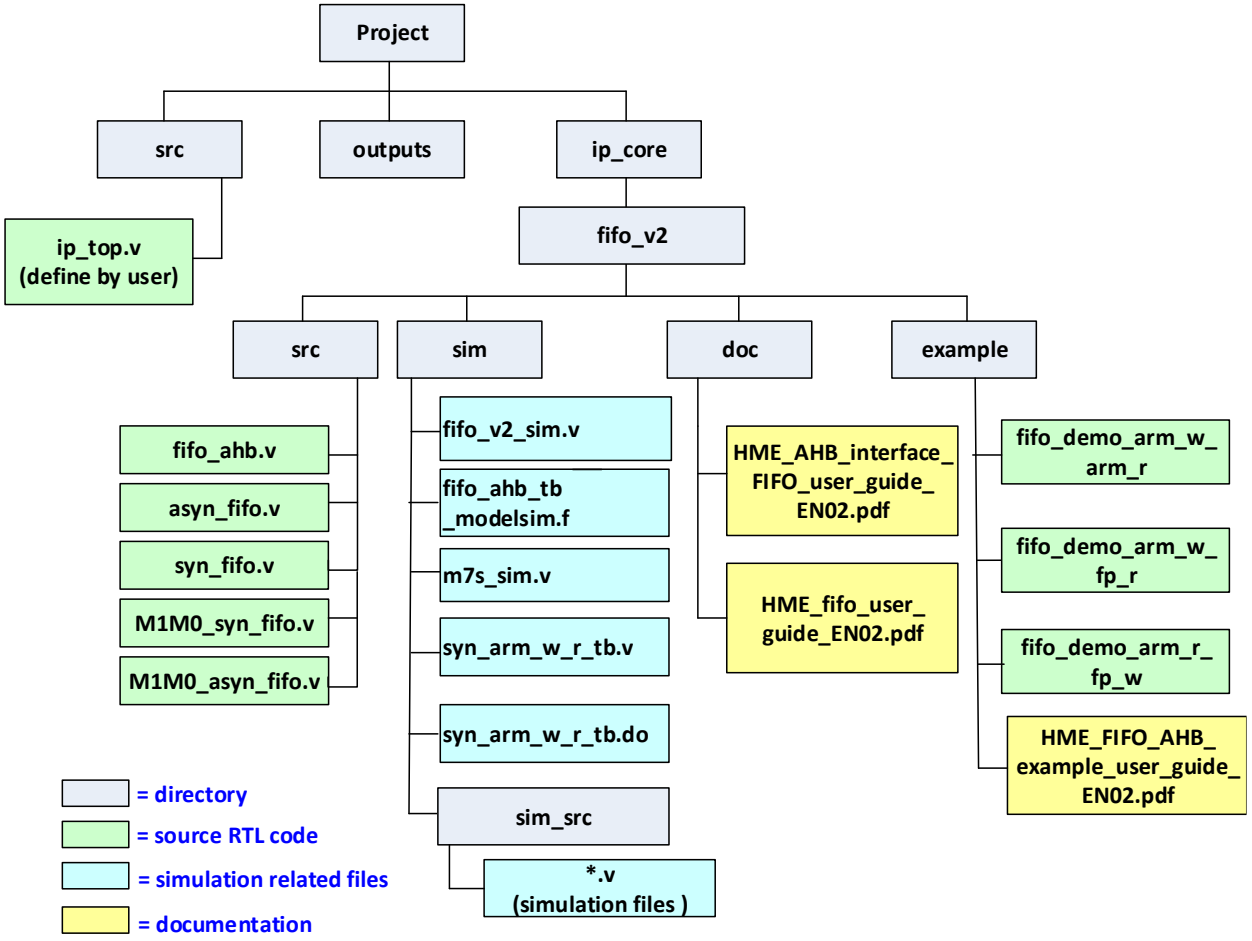

Figure 5-1 ***IP wizard generated file directory structure***

Table 5-1 ***Generated File Directory structure***

Directory	Description
src\	Directory for project source code, including IP wizard generate code.
ip_core\	The directory specially for all IPs
\fifo_v2	Directory for FIFO IP
\doc\HME_AHB_interface_FIFO_user_guide_EN02.doc	User guide for ahb interface FIFO IP
\doc\HME_fifo_user_guide_EN02.doc	User guide for FIFO IP (no ahb interface)
\src	IP Design RTL
fifo_ahb.v	The src of ahb interface FIFO IP

asyn_fifo.v	Asynchronous FIFO source code
syn_fifo.v	Synchronous FIFO source code
M1M0_syn_fifo.v	Synchronous FIFO source code for M0/M1 device
M1M0_asyn_fifo.v	Asynchronous FIFO source code for M0/M1 device
\sim	
\ syn_arm_w_r_tb.v	Testbench of ahb interface FIFO(arm write & arm read) IP
\ syn_arm_w_r_tb.do	Do script for Modelsim simulation (arm write & arm read)
\fifo_ahb_tb_modelsim.f	Modelsim simulation related files
\m7s_sim.v	Simulation file for M7 device
\fifo_v2_sim.v	Other RTL design files for fifo with AHB interface,
\sim_src	
*.v	Other RTL design files for simulation about AHB bus
\example	
fifo_demo_arm_r_fp_w.zip	AHB interface FIFO IP examples
fifo_demo_arm_w_arm_r.zip	
fifo_demo_arm_w_fp_r.zip	
HME_FIFO_AHB_example_user_guide_EN02.pdf	The guide of ahb interface FIFO

Revision History

Revision	Date	Comments
1.1	2018-03-26	Add AHB interface
2.0	2018-03-26	Add FWFT function