京微齐力
HERCULES MICROELECTRONICS

HME-H1D03 Family

FPGA

Data Sheet

Jun 2023

Hercules Microelectronics Co., Ltd.

Notes

Version Part Number

HME-H1(D03)DSE06

Contact Us

If you have any problems or requirements during using our product, please contact **Hercules Microelectronics Co., Ltd.,** or **your local distributors,** or send e-mail to sales@hercules-micro.com

Environmental Considerations

To avoid the harmful substances being released into the environment or harming human health, we encourage you to recycle this product in an appropriate way to make sure that most of the materials are reused or recycled appropriately. Please contact your local authorities for disposal or recycle information.

Warranty

The information in this document has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, Hercules Microelectronics Co., Ltd. reserves the right to discontinue or make changes, without prior notice, to any products herein to improve reliability, function, or design.
Hercules Microelectronics Co., Ltd. advises its customers to obtain the latest version of the relevant information to verify, before placing orders, that the information being relied upon is current.

The product introduced in this book is not authorized for use as critical components in life support devices or systems without the express written approval of Hercules Microelectronics Co., Ltd. As used herein: 1. Life support devices or systems are devices or systems that (a) are intended for surgical implant into the body or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user. 2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Revision History

The table below shows the revision history for this document.

Date	Version	Revision
Mar. 2019	1.0	Initial release.
Nov.2019	1.1	Add H1M03N3 part number Add W54 package information Modify W68 package information
Mar.2020	1.2	Delete L144 package information
July.2021	1.3	Delete W54 package information Delete W49 package information Add L128 package information
28 Dec, 2021	1.4	***Modify Ordering Information*** Commercial (0℃ to +85℃) Industrial (-40℃ to +100℃)
30 Jan, 2022	1.5	Add temperature details, TJ Correct product number
21 Mar, 2022	HME-H1(D03)DSE01	**Update format details** **Update pictures in Chapter 9** **Add the note about some packages without vendor logo**
13th Oct, 2022	HME-H1(D03)DSE02	Add STFBGA144(C144) package specification (9.2.5) Update Chapter 10 and 1.1
19th Jan, 2023	HME-H1(D03)DSE03	Correct the description of pin CDONE
27th Feb, 2023	HME-H1(D03)DSE04	Add H1D03N0 serial, and update Chapter 1.2 and Chapter 10
07th Apr, 2023	HME-H1(D03)DSE05	1-Add information of QFN56 package and update Chapter1.1, Chapter 1.2, Chapter 9, and Chapter 10 2-Modify Legends, adjust package order in Chapter 1.2 and Chapter 9.2, add printing picture and description in Chapter 10.3, and change format of NOTE
13 Jun, 2023	HME-H1(D03)DSE06	1- Correct Max User I/O of C144 package in H1D03N0, from *43(5)/8* to *68(12)/8* 2- Correct Max User I/O of C144 package in H1M03N0, from *49(12)/8* to *47(11)/8*

Table of Contents

Notes **1**

Revision History **2**

Table of Contents **3**

Before You Start **6**

About this Datasheet 6
HME-H1 Family FPGA Introduction 6
Legends 6

1 HME-H1D03 Series FPGA Features **8**

1.1 HME-H1 Family FPGA Feature Summary 9
1.2 Architecture Overview 10
1.3 System Connection Overview 10

2 FPGA **13**

2.1 Programmable Logic Block (PLB) 13
2.2 Embedded Memory Block 13
2.2.1 EMB18K Port Definitions 14
2.2.2 EMB18K Operations 15
2.2.3 EMB18K Operation Mode 16
2.2.4 Conflict Avoidance 19
2.3 DSP Block 19
2.3.1 DSP Primitive 19
2.3.2 DSP Usage Mode 21
2.4 Clock Resources 23
2.4.1 PLL 23
2.4.2 DLL 29

3 Input/output Blocks **30**

3.1 The I/Os During Power-On, Configuration, and User Mode 31

4 MCU **32**

4.1 8051 Instantiation 33
4.1.1 8051 Macro Primitive Description 33
4.2 Multiplex of P Port Pins 35
4.3 MCU Memory Map 35
4.4 External Memory Interface (EMIF) 36
4.4.1 Synchronous EMIF 36
4.4.2 EMIF Timing 37
4.5 SFR Interface 38
4.5.1 SFR Timing 38

5 SRAM **40**

5.1 SPRAM_8Kx32 SRAM Port Definitions 40
5.2 SPRAM_2Kx32 SRAM Port Definitions 40
6 MIPI 42
6.1 MIPI D-PHY Blocks 42
6.2 DSI Controller Core 42
7 Configuration and Debug 44
7.1 Configuration Modes and Pins 44
7.2 Configuration Process 45
7.3 Configuration Scheme 46
7.3.1 AS Mode 46
7.3.2 PS Mode 46
7.3.3 JTAG Mode 47
7.4 eFUSE 47
7.4.1 eFUSE field description 48
7.5 AES Security 48
8 DC & Switching Characteristics 49
8.1 DC Electrical Characteristics 49
8.1.1 Absolute Maximum Ratings 49
8.1.2 General Recommended Operating Conditions 50
8.1.3 Static Current on General Normal Operating Conditions 50
8.1.4 Power-On Specification 50
8.1.5 Recommended I/O Operating Conditions 51
8.1.6 Recommended MIPI Operating Condition 51
8.2 Switching Characteristics 53
8.2.1 Clock Performance 53
8.2.2 OSC Specifications 53
8.2.3 PLL Specifications 53
8.2.4 I/O Performance 54
8.2.5 PLB Performance 54
8.2.6 EMB18K Performance 54
8.2.7 DSP Performance 54
8.2.8 SRAM Performance 55
9 Pins and Package 56
9.1 Pins Definitions and Rules 56
9.2 Package Information 58
9.2.1 STFBGA144 Package Specifications 58
9.2.2 LQFP128 Package Specifications 59
9.2.3 QFN56 Package Specifications 60
9.2.4 WLCSP58 Package Specifications 61
9.2.5 WLCSP68 Package Specifications 62
9.2.6 WLCSP72 Package Specifications 63
10 Ordering Information 64
10.1 Part Number Conventions 64
10.2 Order Information 65

10.3 Chip Marking Spec 65

Before You Start

About this Datasheet

This datasheet is part of documentation for **HME-H1D03 FPGA devices**. It serves as a technical reference datasheet for you to be familiar with the HME-H1 family FPGA device's functions and characteristics.

For the detailed information of this family module, please go to http://www.hercules-micro.com.

If you have any questions or suggestions, please contact us at: support@hercules-micro.com.

HME-H1 Family FPGA Introduction

HME-H1D03 from Hercules-micro is a programmable video bridging device that supports a variety of protocols and interfaces for mobile image sensors and displays. It combines the extreme flexibility of an FPGA with the low power, 8051 MCU core, hardened MIPI D-PHY/controller and low cost and small footprint of an ASIC.

H1D03 supports video interfaces including MIPI®, MIPI DBI, CMOS camera and display interfaces, MIPI D-PHY, MIPI CSI-2, MIPI DSI, SubLVDS.

Hercules-micro provides many pre-engineered IP (Intellectual Property) modules for H1D03 by using these configurable soft core IPs as standardized blocks, hardened IPs and MCU, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

Interfaces on H1D03 provide a variety of bridging solutions for smart phone, tablets, wearables, VR, AR, Drone, Smart Home, HMI as well as adjacent ISM markets. The device is capable of supporting high-resolution, high-bandwidth content for mobile cameras and displays up to 2K.

Legends

Abbreviation	Full Name
AES	**A**dvanced **E**ncryption **S**tandard
APB	**A**dvanced **P**eripheral **B**us
AS	**A**ctive **S**erial
CCU	**C**ompare **C**apture **U**nit
CSI	**C**amera **S**erial **I**nterface
DPRAM	**D**ual **P**ort **R**AM
DC	**D**irect **C**urrent
DSP	**D**igital **S**ignal **P**rocessor
DLL	**D**elay-Locked **L**oop
DSI	**D**isplay **P**ixel **I**nterface
EMB	**E**mbedded **M**emory **B**lock
I2C	**I**nter-**IC** – a serial interface designed by Philips Semiconductors

Abbreviation	Full Name
ISP	**I**n **S**ystem **P**rogramming
ISR	**I**nterrupt **S**ervice **R**outine **U**nit
LE	**L**ogic **E**lement
LP	**L**ogic **P**arcel
LSB	**L**east **S**ignificant **B**it
MCU	**Micro C**ontrol **U**nit
MAC	**M**ultiply **A**ccumulate **C**ounter
MDU	**M**ultiplication-**D**ivision **U**nit
MSB	**M**ost **S**ignificant **B**it
MIPI	**M**obile **I**ndustry **P**rocessor **I**nterface
OCDS	**O**n-**C**hip **D**ebug **S**upport
OSC	Oscillator
PLB	**P**rogrammable **L**ogic **B**lock
PLL	**P**hase-**l**ocked **l**oop
PPI	**PHY-P**rotocol **I**nterface
PS	**P**assive **S**erial
SFR	**S**pecial **F**unction **R**egister
SPI	**S**erial **P**eripheral **I**nterface

This chapter briefly introduces HME-H1D03 family.

1 HME-H1D03 Series FPGA Features

FPGA

- SRAM-based FPGA Fabric
  - Up to 2K 6-input Look-up Tables, 4096 DFF-based registers
  - Performance up to 200MHz
- Embedded RAM Block Memory
  - 8 18Kbit programmable dual-port DPRAM memory
- Embedded DSPs block
  - 16 18x18 DSP (MAC) blocks or 32 12x9 DSP (MAC) blocks
- Clock Network
  - 8 de-skew global clocks
  - 1 +/-5% frequency accuracy after trimming OSC
  - 1 PLLs support frequency multiplication, frequency division, phase-shifting, de-skew
  - 6 external input clocks,
  - Dynamic clock management in system
- Two hardened 4-lane MIPI interfaces
  - Programmable transmit and receive D-PHY
  - 1.5Gb/s one lane, total 6 Gb/s per D-PHY
  - Programmable host and peripheral MIPI controller
- I/O
  - 3.3/2.5/1.8/1.5/1.2V LVTTL/LVCMOS general I/O
  - Programmable source synchronous I/O
    - Emulated MIPI D-PHY, LVDS Rx, LVDS Tx, BLVDS
    - Up to 1200 Mb/s per I/O

MCU

- Enhanced 8051 MCU
  - Reduced instruction cycle time (Up to 12 times in respect to standard 8051), frequency up to 80MHz
  - Compatible to 8051 instruction system
  - Support up to 8MB data/code memory extension
  - Support hardware 32/16-bit MDU
  - On-chip debugger system (OCDS)
  - 8-channel DMA
- Peripheral
  - 3 16-bit Timers
  - 1 I2C interface
  - 1 SPI interface
    Master rate up to 100Mb/s @200MHz
    Slave rate up to 25Mb/s @200MHz
  - 2 Full Duplex Serial Interfaces, the rate is up to 6.25Mb/s @200MHz
  - Enhanced hardware operation unit supports multiplication, division, skip and normalization.
- STOP, IDLE Mode Power Management

Memory

- Embedded SRAM Memory
  - 8Kx32b single-port SRAM
  - 2*2Kx32b single-port SRAM
  - Flexible memory configuration for FPGA or MCU

Configuration

- Configuration Mode
  - JTAG Mode
  - AS Mode
  - PS Mode
- JTAG Interface
  - JTAG Chip Configuration
  - JTAG 8051 Debugging

Security

- Encrypted Bitstream with 256-bit AES
- Protection against copying, overbuilding, cloning and tampering with both of customer's FPGA and 8051 firmware IP

- Applications examples
  - 2:1 MIPI DSI Display Interface Bridge
  - 2:2 MIPI DSI Display Interface Bridge
  - MIPI DSI to/from FPD-Link LVDS Display Interface Bridge
  - MIPI DSI to/from CMOS Display Interface Bridge

Package

- STFBGA144
- LQFP128
- QFN56
- WLCSP58
- WLCSP68
- WLCSP72

1.1 HME-H1 Family FPGA Feature Summary

Table 1-1 HME-H1 FPGA Feature Summary

Part Number		H1D03N0	H1D03N3	H1M03N0	H1M03N3
Programmable Logic Block (PLB)	Logic cells	3276	3276	3276	3276
	LUT6	2048	2048	2048	2048
	Register	4096	4096	4096	4096
Embedded Memory Block (EMB)	18Kb	8	8	8	8
	Max	144Kb	144Kb	144Kb	144Kb
DSP	18b*18b	16	16	16	16
PLL		1	1	1	1
DLL		2	2	2	2
OSC		1	1	1	1
MIPI	D-PHY	2	2	2	2
	DSI Controller	2	2	2	2
MCU	8051	1	1	1	1
	UART	2	2	2	2
	I2C	1	1	1	1
	SPI	2	2	2	2
	Timer	3	3	3	3
	DMA	1	1	1	1
SRAM	2K*32b	2	2	2	2
	8K*32b	1	1	1	1
	Total	48KB	48KB	48KB	48KB
SPI Flash		-	4Mb	-	4Mb
eFuse		2x512b	2x512b	2x512b	2x512b
pSRAM		-	-	128Mb(1x8M*16b)	64Mb(2x4M*8b)
Package (unit: mm)		Max User I/O (LVDS pair)/MIPI lane			
C144(6x6x0.94, 0.5 pitch)		68(12)/8		47(11)/8	
L128(16x16 x1.2, 0.5 pitch)		58(12)/8			
Q56(5.0x5.0x0.55, 0.3 pitch)			17(5)/8		
W58(3.9x3.3x0.55, 0.4 pitch)			20(3)/8		
W68(4.0x4.6x0.55, 0.5 pitch)					21(7)/8
W72(3.9x3.3x0.55, 0.4 pitch)			34(10)/8		

1.2 Architecture Overview

The HME-H1 FPGA architecture consists of programmable functional tiles and an enhanced 8051 system. The PLBs, IOBs, EMB, DSPs and PLLs make up the FPGA. The enhanced 8051 and SRAM can make up the MCU system. The EMB and DSP can be called as special function block (SFB).

- Programmable Logic Blocks (PLBs) contain RAM-based Look-Up Tables (LUT-6) to implement logic and storage elements that can be used as flip-flops. PLBs can be programmed to perform a wide variety of logical functions as well as to store data.
- Embedded Memory Block provides data storage in the form of 18K bit dual-port blocks.
- DSPs accept two 18-bit binary numbers as inputs and calculate the product. The DSP block includes special DSP multiply-accumulate blocks.
- Phase (PLL) blocks provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase shifting clock signals.
- Input/Output Blocks (IOBs) control the flow of data between the I/O pins and the internal logic of the device. Each IOB supports bidirectional data flow plus 3-state operation.
- The monocycle enhanced 8051 CPU is used as central processing unit, whose instruction set is compatible with standard ASM51 completely.
- The embedded SRAM can be used as the 8051 coding and data memory or for FPGA embedded memory.
- The MIPI D-PHY and DSI controller can be used as MIPI interface to connect the CSI and DSI devices.

These elements are organized as shown in figure below.

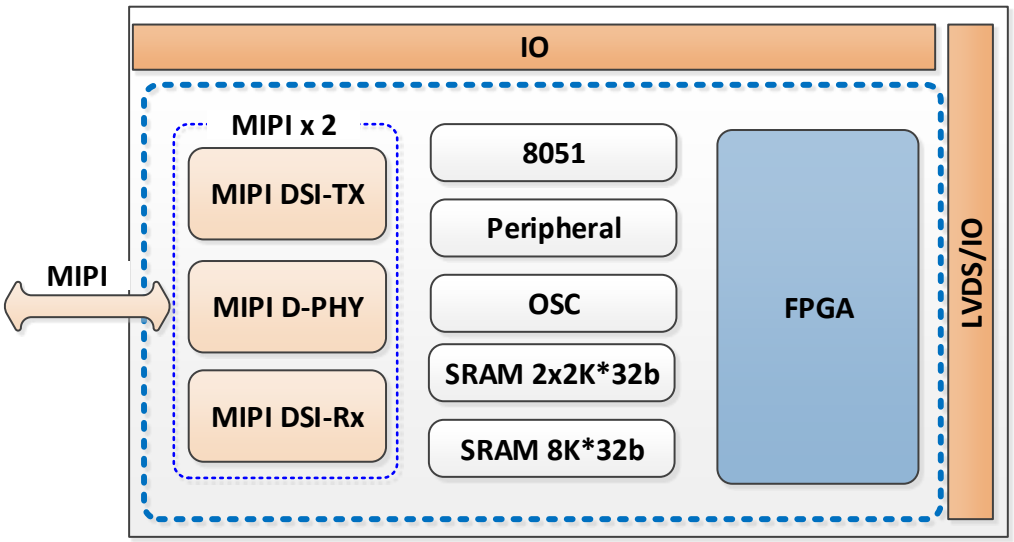


Figure 1-1 HME-H1 FAMILY Architecture

1.3 System Connection Overview

The H1D03 device is comprised of enhanced 8051 processor, embedded peripherals, SRAM, CCB, Clock

block, MIPI PHY and controller which are interconnected via the routing resources to the FPGA. This chapter only describes the system level functions which are special for the HME-H1C03 family device. The enhanced r8051xc2 core, peripherals, MIPI and Clock block are described in other User Guide and App Notes documents.

The system connection diagram is shown in figure below.

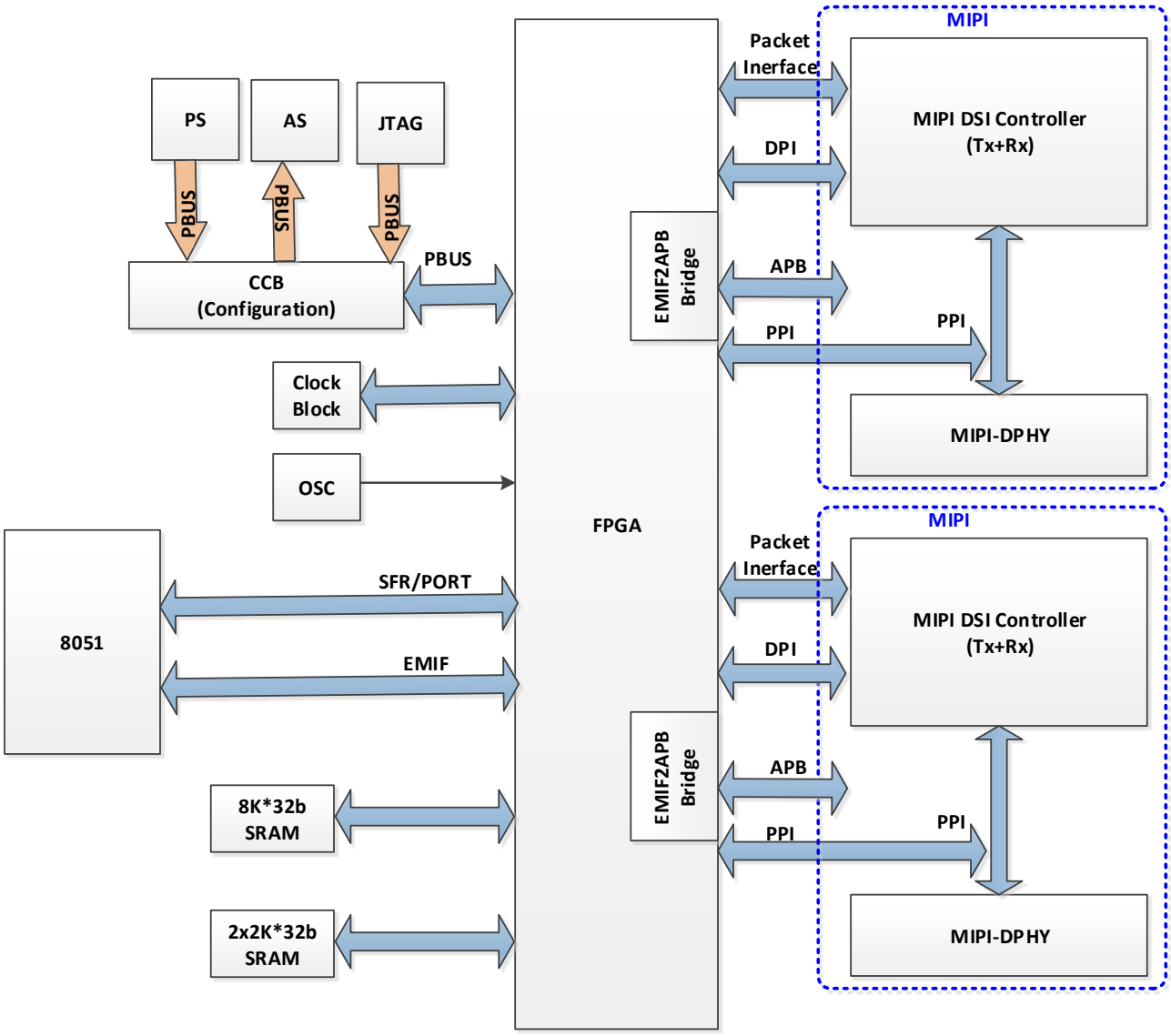


Figure 1-2 System Connection Diagram

The embedded 8Kx32b or 2Kx32b SRAM can be used as 8051's code and data memory via the EMIF interface, the two blocks can constitute an 8051 MCU system.

User can use the Fuxi IP wizard to instantiate the MCU IP and make the peripherals connected to FPGA. All the peripherals such as UART, SPI, I2C, Ports, timers and interrupts and so on then can be used by the system.

The standard 8051 MCU has 128 bytes of Special Function Registers, and there are some SFRs which are not be occupied by the peripherals. Users can use the SFR interface and these free SFRs to extend their customized peripherals or IPs which then can be programmed as the hard peripherals.

The FPGA can transfer the data via the MIPI D-PHY's PPI interface which is also connected to DSI controller.

The FPGA can configure the DSI controller via the APB interface and communicate with DSI controller via the Packet interface. The FPGA can receive the CSI data from the sensor or drive the DSI display through the DSI controller and D-PHY.

2 FPGA

The HME-H1 FAMILY FPGA consists of up to 256 PLBs, 16 EMB9K blocks, 16 18x18 DSPs, 1 PLL and 5 banks I/O. This chapter describes these element blocks.

2.1 Programmable Logic Block (PLB)

The Programmable Logic Block (PLB) is the fabric basic logic tile that is composed of LE and Xbar. The PLB is the basic tile of the fabric. Their organization is shown in the figure below. One LE contains eight interconnected Logic Parcels (LP). The LE constitutes the main logic resource for implementing synchronous as well as combinatorial circuits.

The Xbar switches and passes the signals between the tile elements.

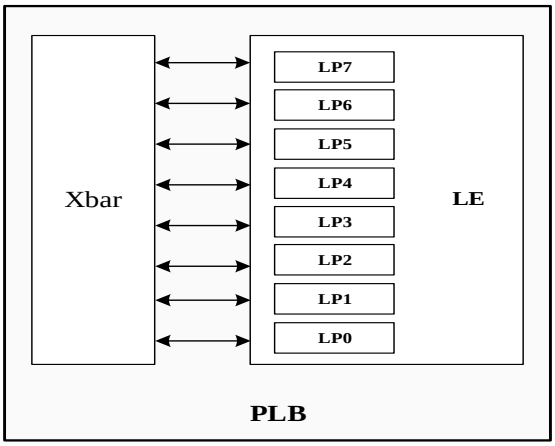


Figure 2-1 PLB Schematic Diagram

The LP is the basic programmable logic element, and has the following elements in common to provide logic and arithmetic functions:

- One 6-input LUT function generators
- Two register elements
- Carry, cascade, shift and arithmetic logic

2.2 Embedded Memory Block

HME-H1 family device supports embedded memory block (EMB), which is organized as one column of EMB18K. EMB18K module is a true dual-port memory that permits independent access to the common EMB block. Each port has its own dedicated set of data, control, and clock lines for synchronous read and write

operations.

EMB18K provides the features as below:

- 18 Kbits
- EMB18K can be used as four 4.5 Kb or two 9 Kb EMB independently
- Mixed clock mode
- A, B data width configured independently
- Support write/read first or through output mode
- Bypass or register output
- Configurable normal RAM or FIFO mode
- One 64-bit Error Correction Coding block is provided per EMB18K
- Initialization file to pre-load memory content in RAM and ROM modes
- Three Memory Modes available
  - emb_tdp
  - emb_sdp
  - emb_sp

2.2.1 EMB18K Port Definitions

The dual-port primitive EMB18K signals are defined in the following table.

Table 2-1 *EMB18K Port Definition*

Port Name	Type	Width	Description
clka	I	1	Input clock for port A
cea	I	1	Chip enable for port A
wea	I	1	Write enable for port A
aa	I	12	Address line for port A
da	I	18	Data input for port A
clkb	I	1	Input clock for port B
ceb	I	1	Chip enable for port B
web	I	1	Wire enable for port B
ab	I	12	Address line for port B
db	I	18	Data input for port B
q	O	18	Memory data q output
wq_in	I	9	Input from paired EMB5K for wide true dual port mode
wq_out	O	9	Output to paired EMB5K for wide true dual port mode

Table 2-2 *EMB18K Parameters*

Parameters	Type	Description
modea_sel	string	Port a usage mode setting: 256x18, 512x9, 1kx4, 2kx2, 4kx1, wtdp (wide true dual port) Default: 256x18
modeb_sel	string	Port b usage mode setting: 256x18, 512x9, 1kx4, 2kx2, 4kx1, wtdp (wide true dual port) Default: 256x18
porta_wr_through	string	Bypassing of write data from write port to read port enable for port a, true or false Default: false
portb_wr_through	string	Bypassing of write data from write port to read port enable for port b, true or false Default: false
init_file	string	EMB initial file Default: “” (No initial file)
operation_mode	string	EMB working mode, just for simulation true_dual_port, single_port, simple_dual_port
porta_data_width	string	EMB port a data width
portb_data_width	string	EMB port b data width

2.2.2 EMB18K Operations

Writing data to and accessing data from the EMB18K are synchronous operations that take place independently on each of the two ports.

When the we and ce signals enable the active edge of clk, data at the d input bus is written to the EMB18K location addressed by the lines. There are two write actions which are selected by wr_through parameter. The write data is also passed to q output bus if the wr_through is true during the writing process. The q output bus value will be the previous read output value during the writing process if the wr_through is false. The two operation waveforms are shown in below figures.

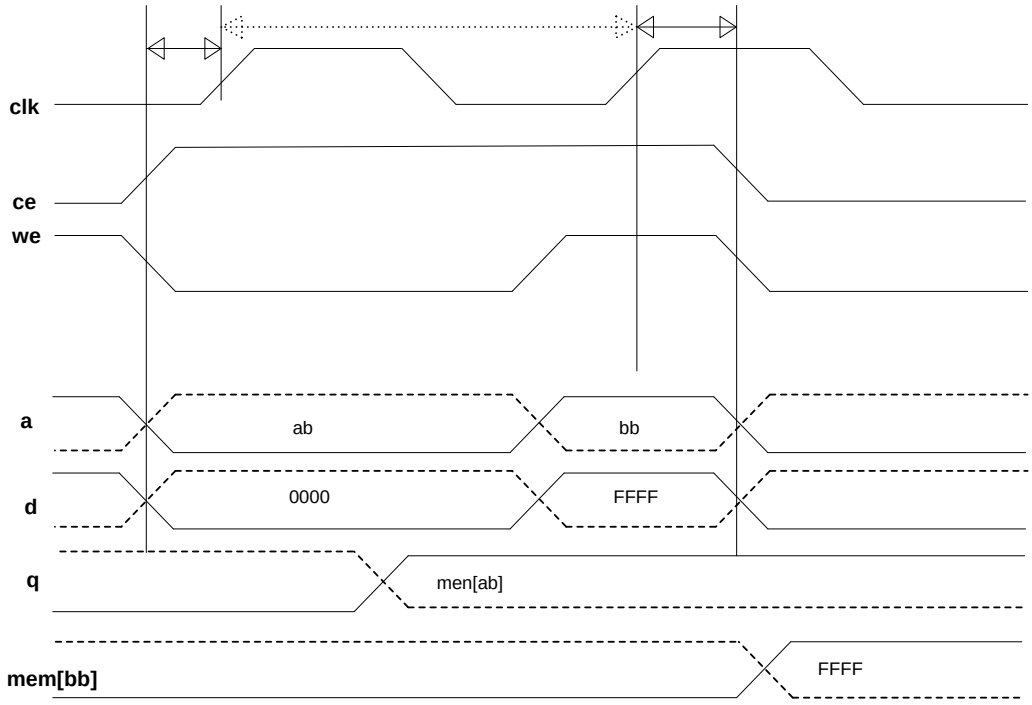


Figure 2-2 wr_through is false Waveform

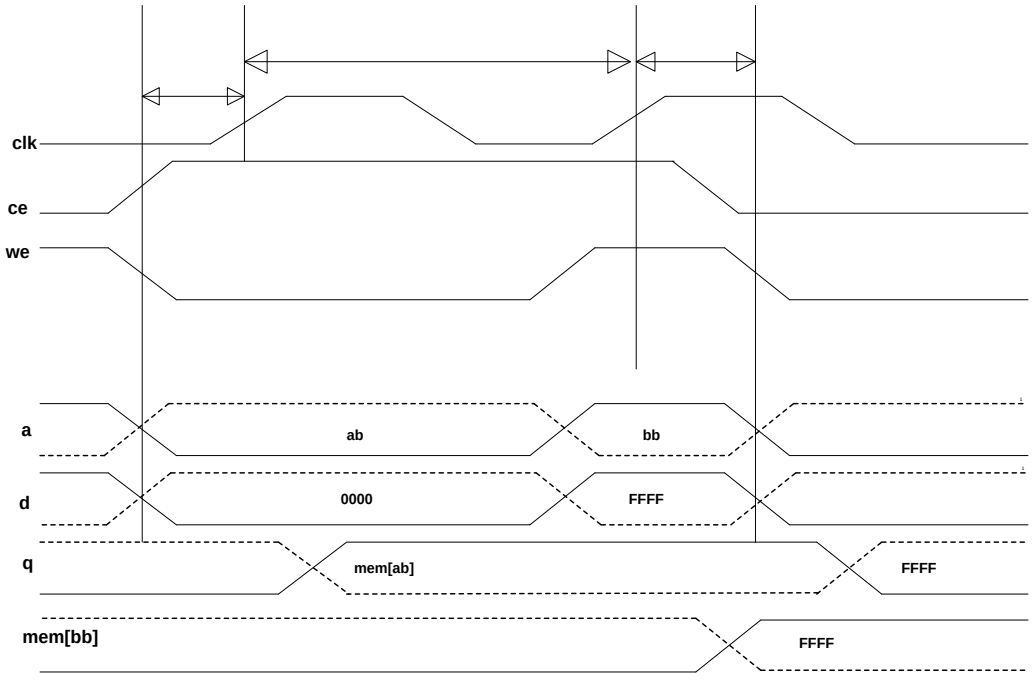


Figure 2-3 wr_through is true Waveform

2.2.3 EMB18K Operation Mode

EMB18K True Dual-port

EMB18K supports any combination of dual-port operation: two read ports, two write ports, or one read and one write at different clock frequencies. The following figure shows true dual-port memory configuration.

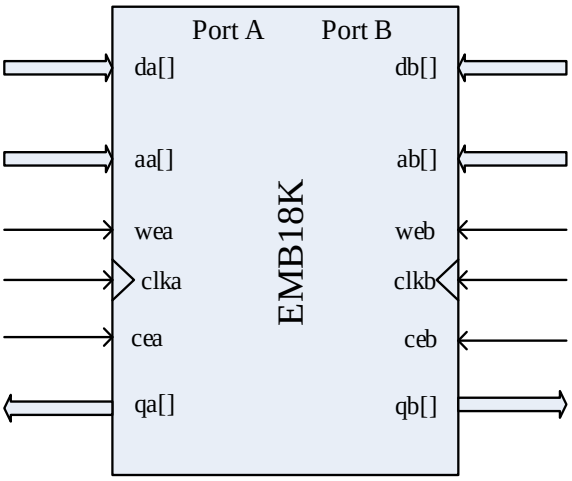


Figure 2-4 True Dual-port Memory Mode

Table 2-3 Port Descriptions of True Dual-port Memory Mode

Port Name	Type	Description
aa (b)	Input	Port A (B) Address.
da (b)	Input	Port A (B) Data Input.
qa (b)	Output	Port A (B) Data Output.
wea (b)	Input	Port A (B) Write Enable. Data is written into the dual-port SRAM upon the rising edge of the clock when both wea (b) and cea (b) are high.
cea (b)	Input	Port A (B) Enable. When cea (b) is high and wea (a) is low, data read from the dual-port SRAM address aa (b). If cea (b) is low, qa (b) retains its value.
clka (b)	Input	Port Clock.

EMB18K Simple Dual-port

EMB18K also supports simple dual-port memory mode: one read port while one write port. The following figure shows simple dual-port memory configuration.

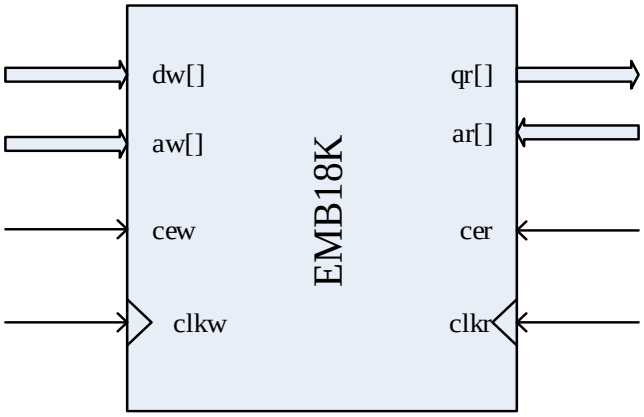


Figure 2-5 Simple Dual-port Memory Mode

Table 2-4 Port Descriptions of Simple Dual-port Memory Mode

Port Name	Type	Description
dw	Input	Write Data
aw	Input	Write Address
clkw	Input	Write Clock
cew	Input	Write Port Enable. Active high.
qr	Output	Read Data
ar	Input	Read Address
cer	Input	Read Enable. Active high
clkr	Input	Read Clock

Table 2-5 Simple Dual-port Configurations

W Port	Read Port						
	4K×1	2K×2	1K×4	512×8	512×9	256×16	256×18
4K × 1	√	√	√	√			
2K × 2	√	√	√	√			
1K × 4	√	√	√	√			
512 × 8	√	√	√	√			
512 × 9					√		
256 × 16	√	√	√	√		√	
256 × 18							√

EMB18K Single-port

EMB18K also supports single-port memory mode as shown in the figure below.

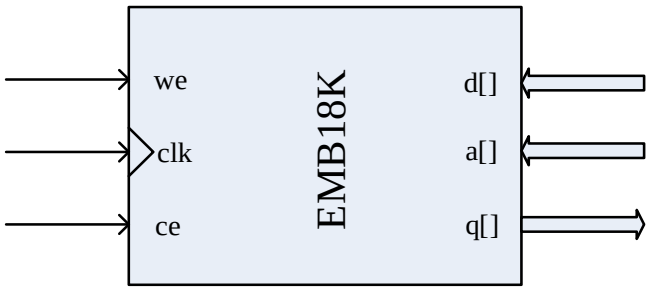


Figure 2-6 Single-port Memory Mode

Table 2-6 Pin Description of Single-port Memory Mode

Port Name	Type	Description
d	Input	Write Data
a	Input	Write Address.
we	Input	Write Enable. Active high.
clk	Input	Write Clock.
ce	Input	Port Enable. Active high.
q	Output	Read Data

Table 2-7 Single-port Configuration

Port						
4K×1	2K×2	1K×4	512×8	512×9	256×16	256×18

2.2.4 Conflict Avoidance

In the dual-port memory mode, both ports can access any memory address at any time. When both ports access the same address, the read and write behavior should observe certain clock timing restrictions. These restrictions are applicable to both synchronous and asynchronous clocks.

2.3 DSP Block

The HME-H1 family devices have one column of 8 DSP MAC tiles. Within the DSP column, a single DSP tile is combined with extra logic and routing.

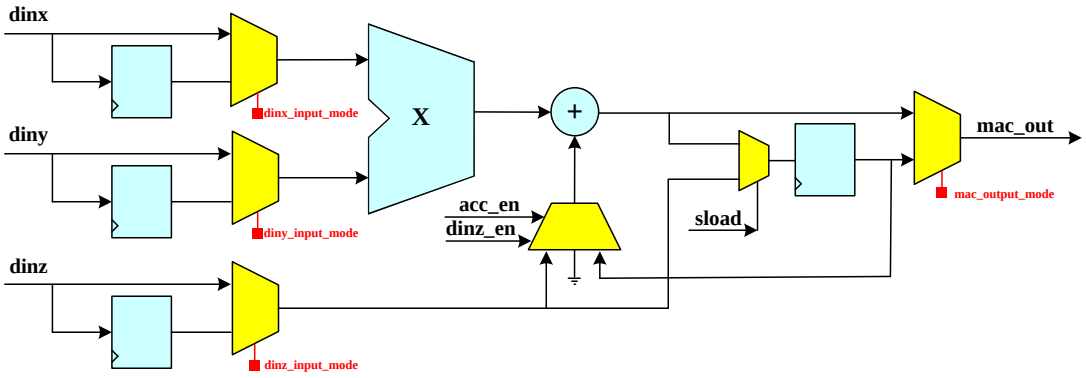


Figure 2-7 DSP Block

DSP tile contains an 18 x 18 two's complement multiplier and a 40-bit sign-extended accumulator, a function that is widely used in digital signal processing (DSP). Programmable pipelining of input operands, intermediate products, and accumulator outputs enhances throughput.

DSP provides features as below:

- 18 x 18 two's-complement multiplier with a full-precision 36-bit result
- Flexible 40-bit post-accumulator with optional registered accumulation feedback
- Dynamic user-controlled operating modes to adapt DSP functions from clock cycle to clock cycle
- Registers, ensuring maximum clock performance and highest possible sample rates with no area cost
- One DSP support 2 independent 12 x 9 multiplier with 21-bit accumulator

2.3.1 DSP Primitive

The following figure shows DSP (MAC) block.

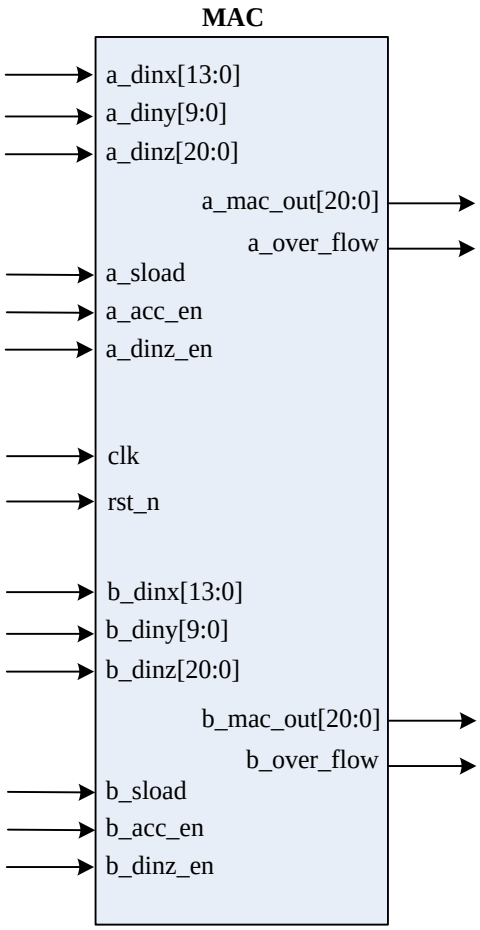


Figure 2-8 MAC Block

Table 2-8 Port Definition

Port	Direction	Width	Description
a_dinx[13:0]	I	14	Multiplicand inputs from ixbar to mult A MSBs, 6 bit LSBs for usage in 18x18 mode.
b_dinx[13:0]	I	14	Multiplicand inputs from ixbar to mult B MSBs.
a_diny[9:0]	I	10	Multiplier input from ixbar to mult A, LSBs of multiplier input in 18x18 mode.
b_diny[9:0]	I	10	Multiplier input from ixbar to mult B, MSBs of multiplier input in 18x18 mode.
a_dinz[20:0]	I	21	Ixbar and bypass inputs to mult A post add and post add LSBs in 18x18 mode.
b_dinz[20:0]	I	21	Ixbar and bypass inputs to mult B post add and post add MSBs in 18x18 mode.
a_sload	I	1	sloadA, when asserted directly loads the post add input into the accumulator.
b_sload	I	1	sloadB, when asserted directly loads the post add input into the accumulator.
a_acc_en	I	1	Accumulator A enable.
a_dinz_en	I	1	Post adder A enable.
b_acc_en	I	1	Accumulator B enable.

Port	Direction	Width	Description
b_dinz_en	I	1	Post adder B enable.
a_mac_out[20:0]	O	21	Outputs to oxbar mult A.
b_mac_out[20:0]	O	21	Outputs to oxbar mult B.
a_overflow	O	1	mulA Overflow flag.
b_overflow	O	1	mulB Overflow flag.
clk	I	1	Clock input.
rstn	I	1	Reset input, Active low.

Table 2-9 Parameter Table

Parameters	Type	Description
mode_sel	string	MAC working mode select, default: 000.
signed_sel	string	Set signed/unsigned multiplication, true or false, default: true.
adinx_input_mode	string	a_dinx input mode setting: bypass or register, default: bypass.
adiny_input_mode	string	a_diny input mode setting: bypass or register, default: bypass.
adinz_input_mode	string	a_dinz input mode setting: bypass or register, default: bypass.
amac_output_mode	string	a_mac_out output mode setting: bypass or register Default: bypass.
bdinx_input_mode	string	b_dinx input mode setting: bypass or register, default: bypass.
bdiny_input_mode	string	b_diny input mode setting: bypass or register, default: bypass.
bdinz_input_mode	string	b_dinz input mode setting: bypass or register, default: bypass.
bmac_output_mode	string	b_mac_out output mode setting: bypass or register, Default: bypass.

2.3.2 DSP Usage Mode

The DSP can be used as two dependent 12x9 A-MAC and B-MAC or one 18x18 MAC function. These MACs have the same functions is shown as Figure 2-7. The HME Fuxi deals with use input width and maps to 12x9 A-MAC and B-MAC or one 18x18 MAC automatically.

Table 2-10 Port Description

Port name	Type	Description
clk	Input	Clock, posedge active.
rstn	Input	Reset, active low.
dinx	Input	Multiplier input (Range: 2~18).
diny	Input	Multiplier input (Range: 2~18).
dinz	Input	Input (Range: 2~40).
sload	Input	Accumulate load.
acc_en	Input	Accumulate enable, active high.
dinz_en	Input	Adder enable, active high.
mac_out	Output	Output (Range: 2~40).
overflow	Output	Overflow, 1 overflow; 0 not active high.

Note: *The acc_en and dinz_en both are not active if they are both high.*

Table 2-11 Parameter Description

Parameter	Type	Description
signedx_sel	string	“true” dinx input type is signed “false” dinx input type is unsigned
signedy_sel	string	“true” diny input type is signed “false” diny input type is unsigned
signedz_sel	string	“true” dinz input type is signed “false” dinz input type is unsigned
dinx_input_mode	string	" bypass " input directly to multiplier; " register " input via register
diny_input_mode	string	" bypass " input directly to multiplier; " register " input via register
dinz_input_mode	string	" bypass" input directly; " register" input via register
mac_output_mode	string	" bypass" mac output directly; " register" mac output via register

The x * y multiplier output will be an unsigned result only when both the x and y are unsigned, otherwise the x * y multiplier output will be a signed and two’s complement result. The mac_out will be an unsigned result only when both the dinz and multiplier output are unsigned, otherwise the mac_out will be a signed and two’s complement result.

Multiplier

The following figure describes that the DSP is used as a multiplier which outputs the dinx * diny result.

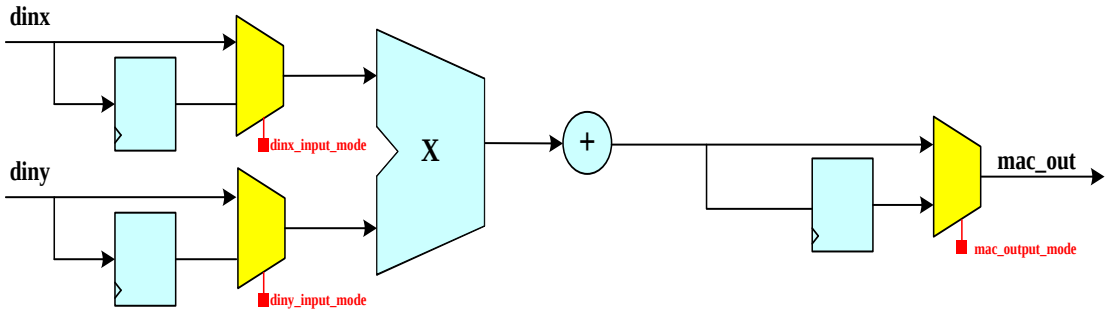


Figure 2-9 Multiplier

Multiplier and adder

The following figure describes that the DSP is used as a multiplier and adder which output the dinx * diny + dinz result.

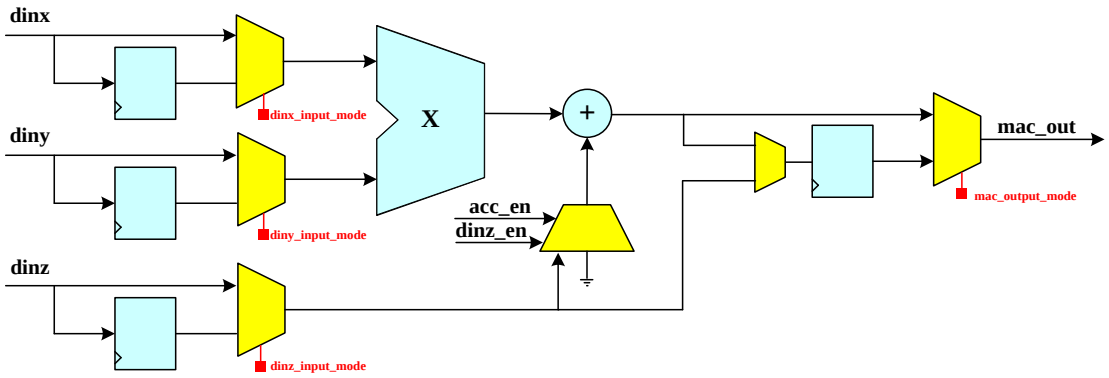


Figure 2-10 Multiplier and Adder

Multiplier and Accumulator

The following figure describes that the DSP is used as a multiplier and adder which output the dinx * diny + $mac\_out_{(n-1)}$ result.

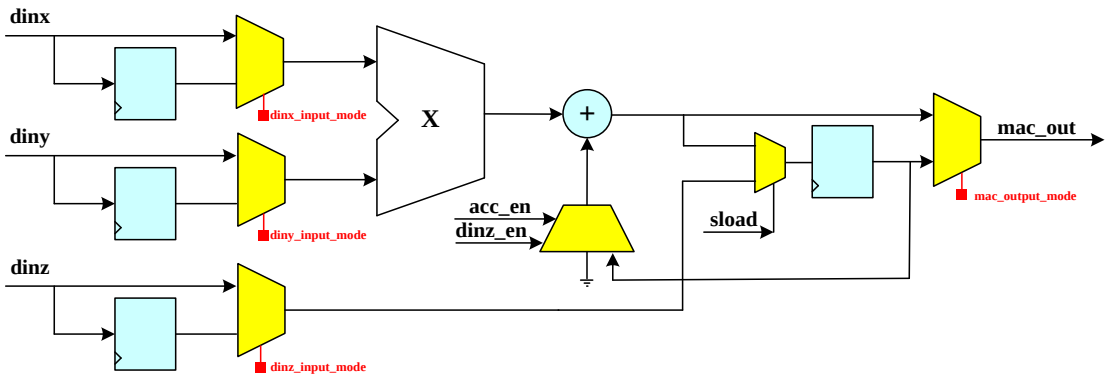


Figure 2-11 Multiplier and Accumulator

2.4 Clock Resources

The HME-H1 family devices provide abundant clock lines to address the different clocking requirements of high fanout, short propagation delay, and extremely low skew. Global clocks are often driven from the PLLs, DLLs, and clock input pins.

2.4.1 PLL

HME-H1 devices have four phase-locked loop (PLL) that provide robust clock management and synthesis for device clock controllers, external system clock management, and I/O interfaces.

The dedicated clock pin, XIN and OSC (internal configuration oscillator) and FPGA logic feed the left PLL's reference clock input and the PLL can generate 6 clock outputs which can as global clocks for the device.

Features

- Input frequency: 10~600MHz

- PFD input frequency: 10 ~ 200MHz
- Output frequency: 1.17 ~ 600MHz
- VCO operating rang: 600 ~ 1200MHz
- Fixed VCO quadrant phase shift: 0°, 45°, 90°, 135°, 180°, 225°, 270°, 315°
- Power-down mode
- PLL 6 outputs
- Lock detector and lock output
- A fractional divisor (non-integer) divider support
- De-skew mode
- Switch over
- Dynamic phase shift
- Dynamic frequency reconfigure

Block Diagram

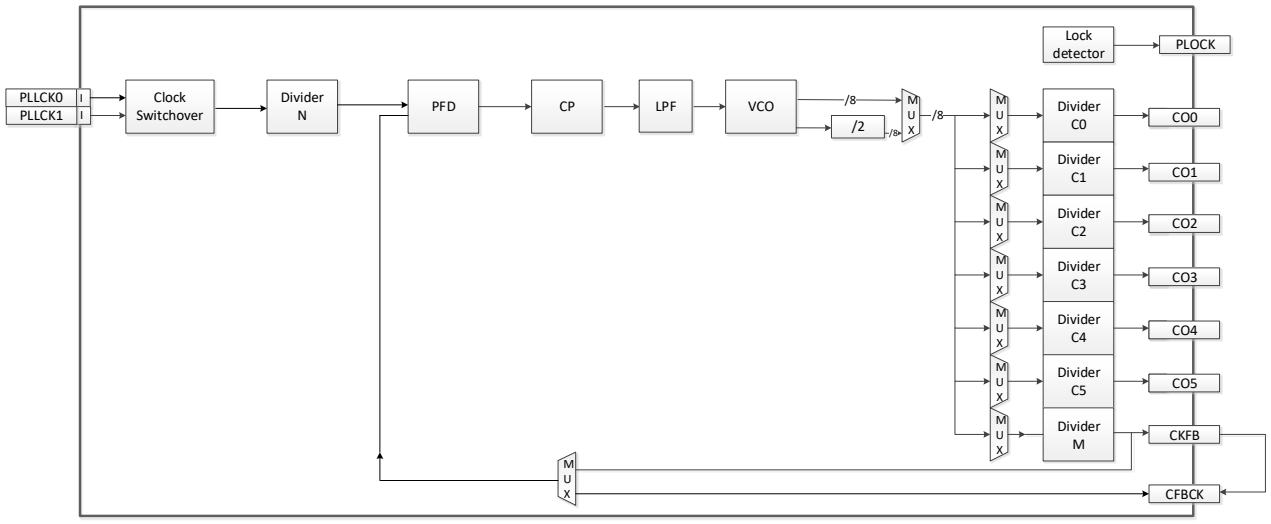


Figure 2-12 PLL Blcok diagram

Description

This PLL is a general purpose, high-performance PLL-based clock generator. It is designed to operate with low jitter and low power consumption.

For wide output frequency range, four VCO operating ranges are provided setting by 2bits. This PLL has programmable output frequency, which ranges from 10MHz to 1250MHz configured using a 8-bit input divider(DIVN), a 8-bit feedback divider(DIVM), a 3-bit post-VCO divider(DIVMP), a 1-bit feedback-VCO divider(DIVFB) and four 8-bit output dividers(DIVCx). Around 50% duty cycle of output clocks can be achieved by enabling the output divider. It can also be used as a clock buffer through a bypass mode. A full

power-down mode is also available.

There are two types operation modes: frequency synthesize and deskew modes.

Frequency synthesize Mode

The PLL's frequency synthesize mode block diagram is shown below.

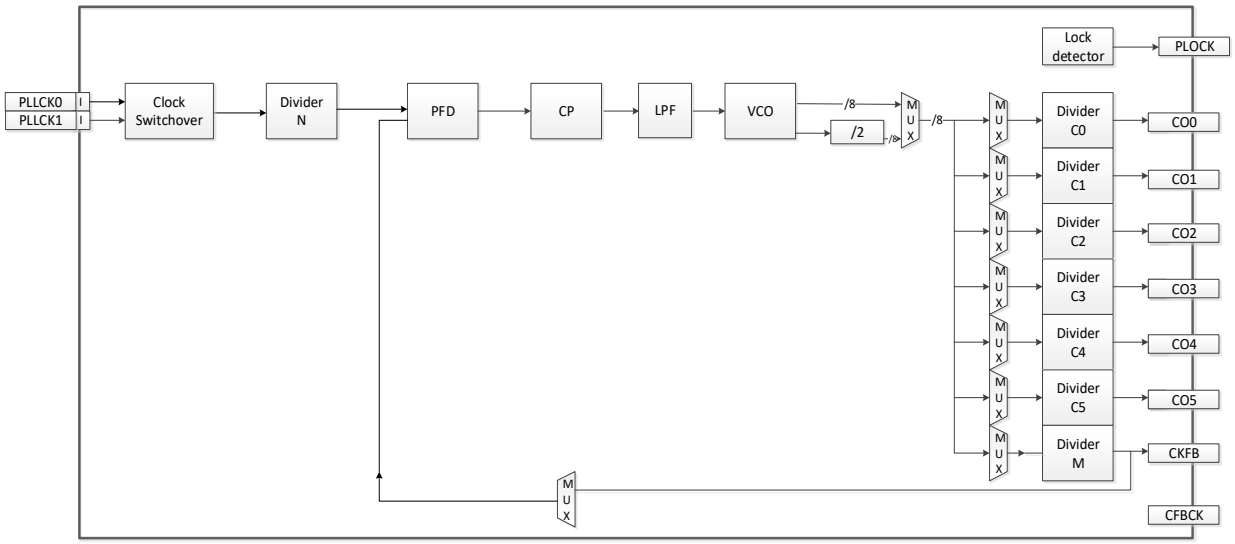


Figure 2-13 The PLL block diagram in frequency synthesize mode

The output clock frequency Fcon is programmable through the divider setting of DIVN[7:0], DIVM[7:0], DIVMP[2:0],DIVFB and DIVCx[7:0].

$$Fcox = Fin \cdot \frac{Nfb \cdot Nm}{Nmp \cdot Nn \cdot Ncox} \quad (x=0,1,2,3,\ldots5)$$

$$Fvco = Fin \cdot \frac{Nfb \cdot Nm}{Nn}$$

Input divider value Nn=DIVN[7:0]+1

Feedback divider value Nm=DIVM[7:0]+1

Feedback-VCO divider value Nfb=DIVFB+1

Output divider value Ncox=DIVCx[7:0]+1

Frequency synthesize mode provides better jitter performance because clock feedback into the PFD does not pass through as much circuitry.

Deskew Mode

The PLL's frequency deskew mode block diagram is shown below.

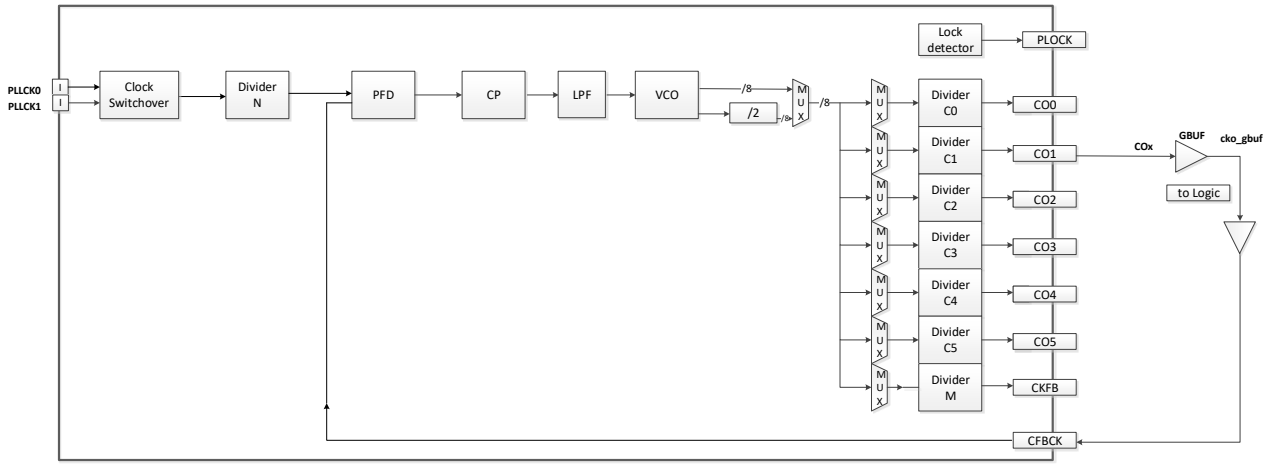


Figure 2-14 PLL Block Diagram in Deskew Mode

The PLL feedback path source is a global or regional clock network, minimizing clock delay to registers for that clock type and specific PLL output.

The output clock frequency Fcox is:

$$Fcox = Fin \cdot \frac{Nm \cdot Nco0}{Nn \cdot Ncox} \quad (x=0,1,2,3)$$

$$Fvco = Fin \cdot \frac{Nm \cdot Nmp \cdot Nco0}{Nn}$$

The PLL support up to three different deskew modes. Each mode allows clock multiplication and division, phase shifting.

Source-Synchronous Mode

If the data and clock arrive at the same time at the input pins, the phase relationship between the data and clock remains the same at the data and clock ports of any I/O element input register.

Source-synchronous mode compensates for delay of the clock network used, including any difference in the delay between the following two paths:

- Data pin to I/O element register input
- Clock input pin to the PLL phase-frequency detector input

Phase Relationship between Data and Clock in Source-Synchronous Mode

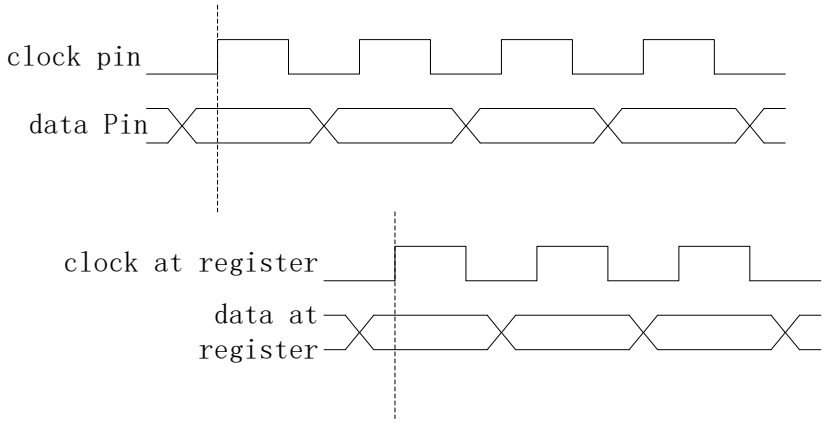


Figure 2-15 The phase relationship between data and clock in source-synchronous mode

Normal Mode

An internal clock in normal mode is phase-aligned to the input clock pin. The external clock output pin has a phase delay relative to the clock input pin if connected in this mode.

In normal mode, the PLL fully compensates the delay introduced by the Gclk-ctrl network.

Phase Relationship between Data and Clock in Normal Mode

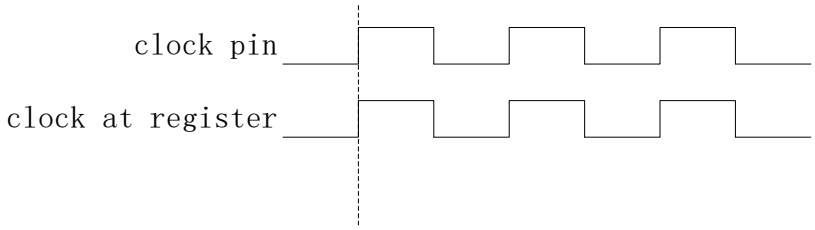


Figure 2-16 The phase relationship between data and clock in normal mode

Zero Delay Buffer (ZDB) Mode

In zero delay buffer (ZDB) mode, the external clock pin is phase-aligned with the clock input pin for zero delay through the device.

When using this mode, use the same I/O standard on the input clock and output clocks to guarantee clock alignment at the input and output pins.

Phase Relationship between Data and Clock in Zero Delay Buffer (ZDB) Mode

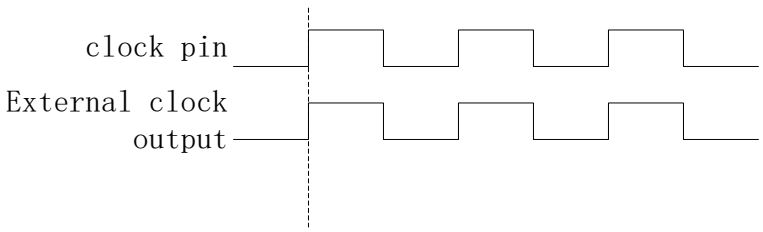


Figure 2-17 Phase relationship between data and clock in ZDB mode

Bypass Mode

Fin is buffered directly to Cox, bypassing the PLL without power-down the internal loop of PLL.

Power-down Mode

The entire PLL cell is powered down internally, and Cox is set to 0. A Tlock time (pull-in and lock time) is required for the PLL to when switching from Power-down Mode to Normal Mode (Frequency synthesize Mode or Deskew Mode).

Output clock delay implementation

Output clock delay is used to implement a robust solution for clock delays. It is implemented with a combination of the VCO multi-phase outputs and the counter starting time. The VCO multi-phase outputs and counter starting time are the most accurate methods of inserting delays, because they are purely based on counter settings, which are independent of process, voltage, and temperature.

Output clock delay is consisted of fine tune and coarse tune. Fine tune using VCO multi-phase taps, and coarse tune using counter starting time.

Dynamic phase shift

The dynamic phase shift feature allows the phase of individual outputs to be dynamically adjusted relative to each other and reference clock. Each output and feedback divider can be individually selected for phase shifting. This feature simplifies the interface and allows to quickly adjust output delay by changing output clock phase shift in real time.

Fractional divider

Fractional divider feature allows a fractional (non-integer) divider in the CO0 output path. The resolution of the fractional divide is 1/8 or 0.125 and the minimum value support to 2.625. This feature effectively increasing the number of synthesizable frequencies by a factor of eight only in the CO0 output path.

When using the fractional divider, the dynamic phase shifting feature will not be supported in the CO0 output path and vice versa.

Clock Switchover

The clock switchover feature allows the PLL to switch between two reference input clocks. Use this feature for clock redundancy or for a dual-clock domain application, such as a system that turns the redundant clock if the previous clock stops running. Output clock can be manually selected or automatically switch. Use the switchover circuitry for switching from ck0 to ck1 running at the same frequency. For example, in applications that requires a redundant clock with the same frequency as the reference clock.

The PLL is a general-purpose, high-performance PLL-based clock generator, which serves as a frequency synthesizer for a wider frequency range. It can also be used as a clock buffer through a bypass mode. The PLL has programmable output frequency that ranges from 1.17 MHz to 600 MHz configured using an 8-bit input divider (DIVN), an 8-bit feedback divider (DIVM), a 1-bit VCO-post divider (DIVFB) and six 8-bit output

dividers (DIVCx).

The PLL has the dynamic phase shift feature that allows the phase of individual outputs to be dynamically adjusted relative to each other and reference clock. Each output and feedback divider can be individually selected for phase shifting. This feature simplifies the interface and allows to quickly adjust the output delay by changing the output clock phase shift in real time.

The PLL also has a triangular modulation that can generate a spread-spectrum clock.

2.4.2 DLL

The DLL takes input reference clock that ranges from 200 MHz to 600 MHz, and generates a multi-phase clock that has the same frequency as the reference clock. Each delay of the multi-phase clock is in 360°/16=22.5° increments. The DLL is designed specifically to support the high performance interfacing requirements of LVDS devices.

This chapter lists the details of input/output blocks of HME-H1D03 family.

3 Input/output Blocks

The Input/output Block (IOB) provides a programmable, bidirectional interface between the I/O pin and the FPGA internal logic.

All I/O pins are organized into banks that include the general I/O banks, LVDS I/O banks. Each bank has several common VDDIO output supply-voltage pins, which also powers certain input buffers. The bank0/1/2 are LVDS I/O banks which can also support general single-end I/O. The bank3/4 are only general single-end I/O.

The bank3/4 I/O provides the features as below:

- Support LVTTL/ LVCMOS 33/25/18 IO standards
- Pull-Up resistor support
- Fixed driving strength
- DDR/SDR support

The bank0/1/2 LVDS I/O provides the features as below:

- Support LVTTL 33/25/18 IO standards
- Support LVCMOS 33/25/18/15/12 IO standards
- support 2/4/8/12/16mA driving strength;
- Programmable pull-up/pull-down/bus-keeper;
- Programmable slew rate control;
- Support LVDS/BLVDS/subLVDS input; CML/LVPECL/TMDS without termination; MIPI D-PHY
- Programmable differential termination
- Programmable differential driving strength
- 1200Mbps data rate
- DDR/SDR support
- ISERDES (DDR 1:N & SDR 1:N/2, N=2, 4, 6, 8, 10, 12, 14, 16)
- OSERDES (DDR N:1 & SDR N/2:1, N=2, 4, 6, 8, 10, 12, 14, 16)

3.1 The I/Os During Power-On, Configuration, and User Mode

With no power applied to the FPGA, all I/Os are in a high-impedance state. The VCCINT and VCCIO supplies may be applied in any order. Before power-on can finish, VCCINT, AVDD, VCCIO must have reached their respective minimum recommended operating levels. At this time, all I/O drivers also will be in a high-impedance state. After configuration, those I/Os to which signals have been assigned go active while all unused I/Os remain in a high-impedance state.

This chapter shows 8051 instantiation, multiplex of P port pins, MCU memory map, EMIF and SFR interface of HME-H1D03 family.

4 MCU

MCU Subsystem is composed of 80 MHz enhanced 8051 processor, embedded peripherals, SRAM and other components which are interconnected via the Xbar or hardware connection. This chapter only describes the MCU system and functions which are special for the HME-H1D family device.

The MCU features are listed as follows:

- **Enhanced 8051MCU**
  - Reduced instruction cycle, 12 times in respect of standard 8051 MIPS, up to 200 MHz
  - Compatible 8051 instruction system
  - On-chip debugger system (OCDS), online JTAG debugging
  - Up to 8M data/code memory
- **Extend memory interface**
  - Data/code unified addressing, flexible memory configuration
  - Flexible chip inside and outside memory expand (EMIF)
- **Peripheral**
  - 1 MDU
  - 3 16-bit Timers, Timer 2 can be used as capture unit
  - 1 16-bit Watch Dog Timer
  - 1 I2C/SMBus Interface
  - 1 SPI Interface
  - 2 Full Duplex Asynchronous Series Ports
  - 8-channel DMA
- **Suspend, Idle Mode Power Management**

The figure below describes the functions of MCU and connections between MCU and FPGA.

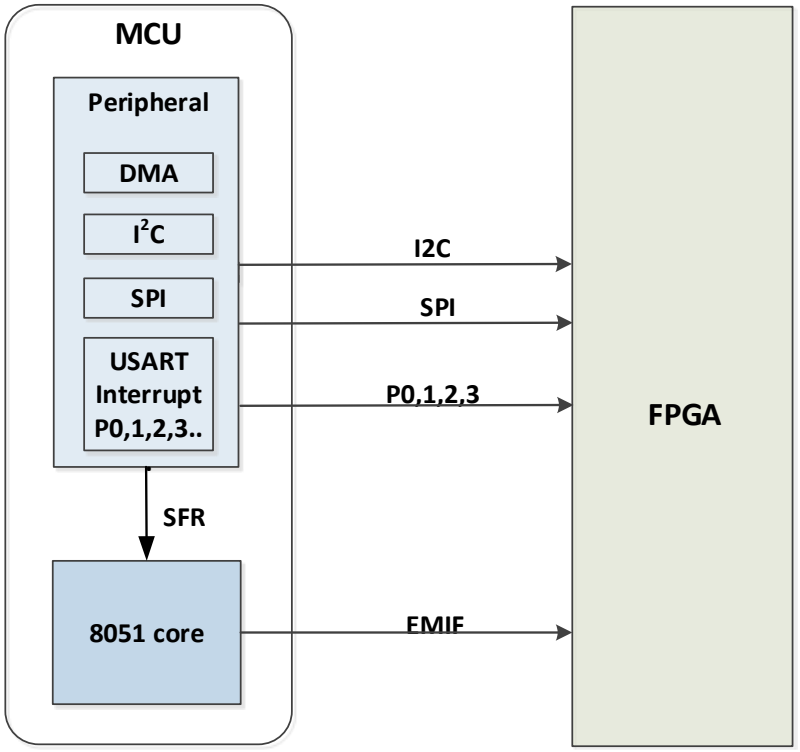


Figure 4-1 MCU System Diagram

4.18051 Instantiation

In the view of a user design, the 8051 IP is considered to be a macro block as other IP, which will be instantiated in the RTL code of the user design. The 8051 tile also contains Xbar that is used to connect with other tiles.

4.1.1 8051 Macro Primitive Description

Table 4-1 8051 Port Definition

Name	Type	Bus size	Description
Global Interface			
clkcpu	I	1	MCU 8051 clock, come from MCU GBUF or internal OSC.
clkcpuen	O	1	Be low when CPU is in STOP and IDLE mode.
clkperen	O	1	Be low when CPU is in IDLE mode.
resetn	I	1	MCU reset, active low.
ro	O	1	MCU core reset output.
swd	I	1	Start Watchdog Timer input. High level on this pin during reset starts the Watchdog Timer immediately after reset is released.
SPI Interface			
scki	I	1	Serial clock input.
scko	O	1	Serial clock output.
scktri	O	1	Serial clock tri-state enables.
ssn	I	1	Slave select input.

Name	Type	Bus size	Description
misoi	I	1	“Master input / slave output” input pin.
misoo	O	1	“Master input / slave output” output pin.
misotri	O	1	“Master input / slave output” tri-state enable.
mosii	I	1	“Master output / slave input” input pin.
mosio	O	1	“Master output / slave input” output pin.
mositri	O	1	“Master output / slave input” tri-state enables.
spssn	O	8	Eight slave select output.
I2C Interface			
scli,	I	1	Serial clock input.
sdai,	I	1	Serial data input.
sclo,	O	1	Serial clock output.
sdao,	O	1	Serial data output.
General I/O			
port0i	I	8	8-bit input port.
port0o	O	8	8-bit output port.
port1i	I	8	8-bit input port, combine with int2-7, ccu, t2, rxd1.
port1o	O	8	8-bit output port, combine with ccu, txd1.
port2i	I	8	8-bit input port.
port2o	O	8	8-bit output port.
port3i	I	8	8-bit input port, combine with int0-1, rxd0, t0, t1.
port3o	O	8	8-bit output port, combine with txd0, rxd0o.
EMIF/SFR Interface			
memack	I	1	Memory acknowledges.
memdatai	I	8	Memory data input.
memdatao	O	8	Memory data output.
memaddr	O	23	Memory address.
memwr	O	1	Memory write enable.
memrd	O	1	Memory read enable.
sfrack	I	1	SFR acknowledges.
sfrdatai	I	8	SFR data input.
sfrdatao	O	8	SFR data output.
sfraddr	O	7	SFR address.
sfrwr	O	1	SFR write enable.
sfrrd	O	1	SFR read enable.
Hold Interface			
hold	I	1	Hold mode request, active high.
holda	O	1	Hold mode acknowledge signal.
intoccur	O	1	Interrupt occurs in hold mode signal.
waitstaten	O	1	Wait state indicator, active low when 8051 performs a wait cycle.

Table 4-2 Parameter Table

Parameters	Type	Description

program_file	String	Mcu/8051 program file: *.hex.

4.2 Multiplex of P Port Pins

Some function modules, such as: external interrupt1, USART0, USART1, Timer 0~2, and Compare – Capture Unit, share pins with port1 and port3. The following shows the details.

Table 4-3 Port Pin Multiplex

Name	Type	Polarity Bus size	Alternate Port	Description
External Interrupts Inputs				
int0	I	Low/Fall	port3i[2]	External interrupt 0
int1	I	Low/Fall	port3i[3]	External interrupt 1
int2	I	Fall/Rise	port1i[4]	External interrupt 2
int3	I	Fall/Rise	port1i[0]	External interrupt 3
int4	I	Rise	port1i[1]	External interrupt 4
int5	I	Rise	port1i[2]	External interrupt 5
int6	I	Rise	port1i[3]	External interrupt 6
int7	I	Rise	port1i[6]	External interrupt 7
Serial 0 Interface				
rxd0i	I	1	port3i[0]	Serial 0 receive data
rxd0o	O	1	port3o[0]	Serial 0 transmit data
txd0	O	1	port3o[1]	Serial 0 transmit data or receive clock in mode 0
Serial 1 Interface				
rxd1	I	1	port1i[0]	Serial 1 receive data
txd1	O	1	port1o[1]	Serial 1 transmit data
Timers Inputs				
t0	I	Fall	port3i[4]	Timer 0 external input
t1	I	Fall	port3i[5]	Timer 1 external input
t2	I	Fall	port1i[7]	Timer 2 external input
t2ex	I	Fall	port1i[5]	Timer 2 capture trigger
Compare – Capture Unit				
cc(0)	I	Rise/Fall	port1i[0]	Compare/Capture 0 input
cc(1)	I	Rise	port1i[1]	Compare/Capture 1 input
cc(2)	I	Rise	port1i[2]	Compare/Capture 2 input
cc(3)	I	Rise	port1i[3]	Compare/Capture 3 input
Ccubus[0]	O	1	port1o[0]	Compare/Capture 0 Output
Ccubus[1]	O	1	port1o[1]	Compare/Capture 1 Output
Ccubus[2]	O	1	port1o[2]	Compare/Capture 2 Output
Ccubus[3]	O	1	port1o[3]	Compare/Capture 3 Output

4.3 MCU Memory Map

The 8051 MCU core can extend both Program Memory and External Data Memory (independently) up to 8

MB by means of dedicated page address register. But HME-H1 family ORs the 8051 write and read program and external data signals to one write and read signals, this makes the program and external data memory share the memory space. The program memory is up to increase from address 0, and the reset and interrupt vectors are stored in the low memory.

NOTE Users must separate program memory space from external data memory space, do not make them overlapped.

The parameter program file is used to locate the 8051 firmware *.hex file which will be the part of the initialized data and is added to configuration file.

The following figure describes the HME-H1 family MCU memory map which includes the FP extend memory.

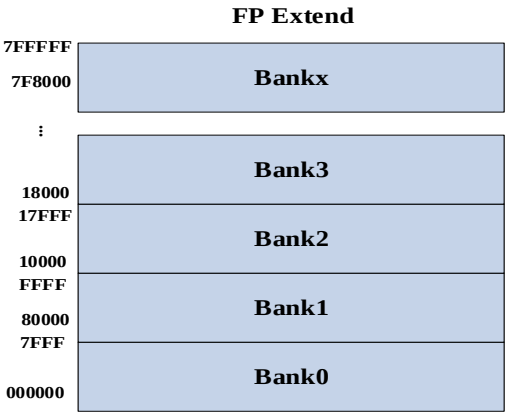


Figure 4-2 MCU Memory Map

4.4 External Memory Interface (EMIF)

EMIF is used to extend the MCU memory, with the address 00000~7FFFFF, which can be used by Fabric.

The HME-H1 family provides synchronous EMIF for Fabric extended memory.

4.4.1 Synchronous EMIF

The Fabric extended memory uses the same clkcpu as the 8051 clock. The signals are connected directly to Fabric.

The synchronous EMIF connection with fabric is shown as in figure below:

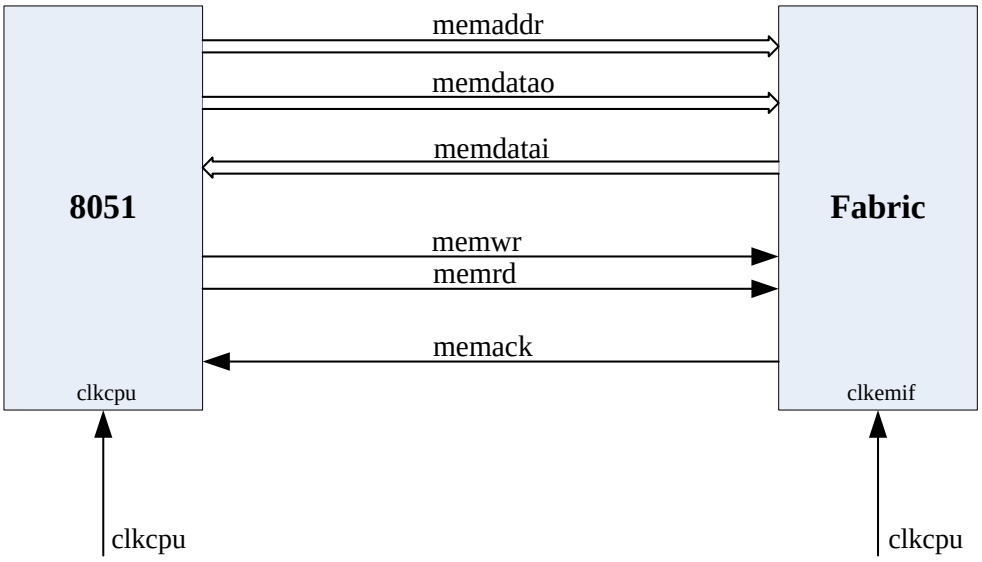


Figure 4-3 EMIF Extension

4.4.2 EMIF Timing

Control signals of “memrd”, “memwr” and “memack” are in the clkcpu domain and generated on the posedge clkemif. The “memrd”, “memwr”, “memack” control signals and “memaddr”, “memdatao” bus will be held if there is no valid “memack” to be sent to 8051 core. Both “memrd “and “memwr” will be invalid when “memack” changes to be low, and either “memaddr” or “memdatao” will be delayed for several periods.

In read cycle, Fabric places the read data to “memdatai” bus and does not output a valid “memack” after one or several cycles until the fabric data is ready after the “memrd” is asserted. EMIF read waveform is shown in the following figure.

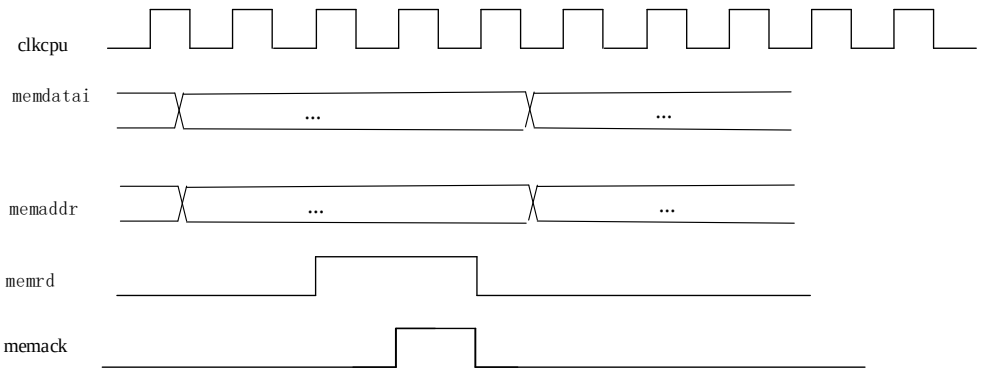


Figure 4-4 EMIF Read Waveform

In write cycle, when the “memwr” is asserted, Fabric writes the “memdatao” to the extended memory and sends a valid “memack” to 8051 on the next cycle.

EMIF write waveform is shown in the following figure:

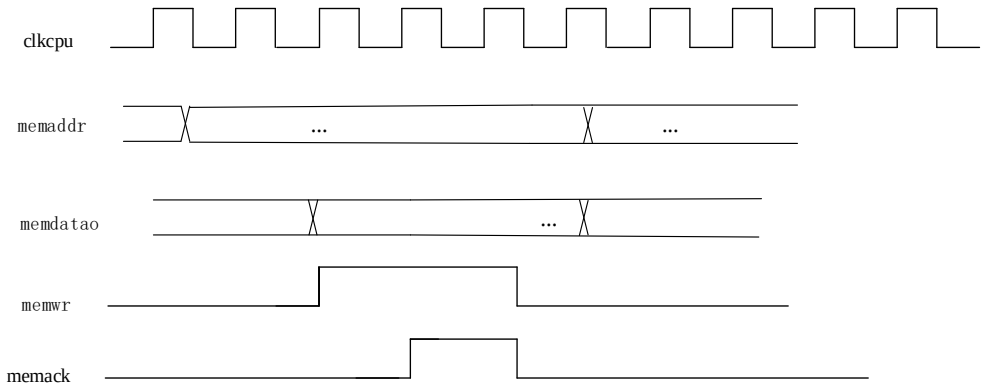


Figure 4-5 EMIF Write Waveform

4.5 SFR Interface

The HME-H1 family provides synchronous SFR interface for Fabric extended SFR. The SFR interface signals are connected directly to Fabric.

The synchronous SFR connection with fabric is shown as in figure below:

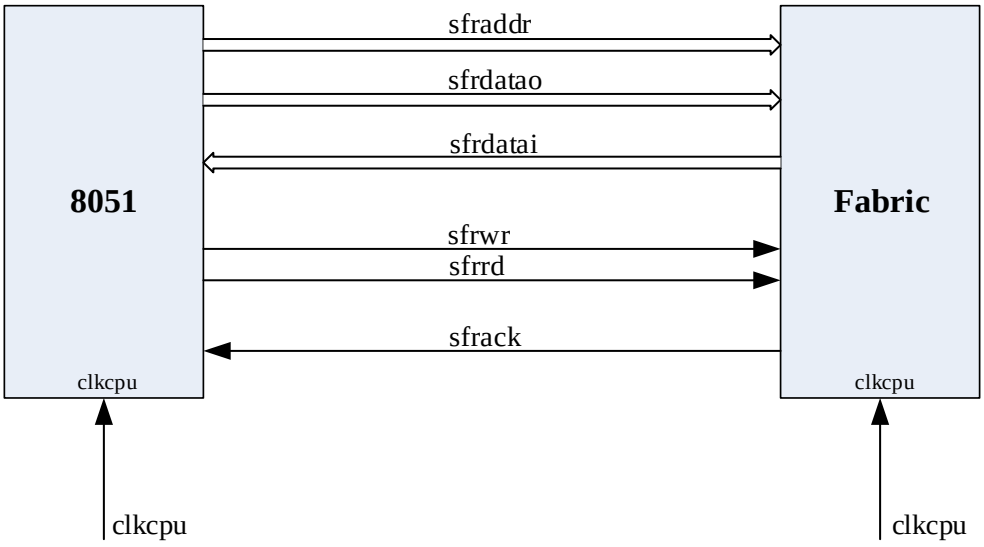


Figure 4-6 SFR Extension

4.5.1 SFR Timing

Control signals of “sfrrd”, “sfrwr” and “sfrack” are in the clkcpu domain and generated on the posedge clkcpu. The “sfrrd”, “sfrwr”, “sfrack” control signals and “sfraddr”, “sfrdatao” bus will be held if there is no valid “sfrack” to be sent to 8051 core. Both “sfrrd “and “sfrwr” will be invalid when “sfrack” changes to be low, and either “sfraddr” or “sfrdatao” will be delayed for several periods.

In read cycle, Fabric places the read data to “sfrdatai” bus and does not output a valid “sfrack” after one or several cycles until the fabric data is ready after the “sfrrd” is asserted. SFR read waveform is shown in the following figure.

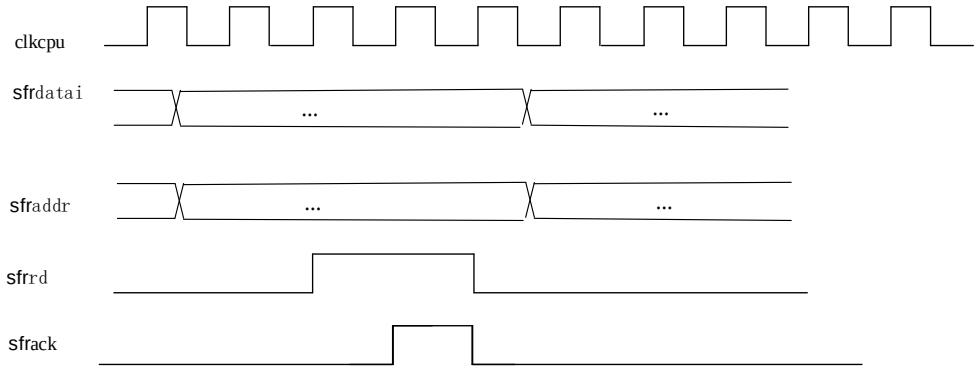


Figure 4-7 SFR Read Waveform

In write cycle, when the “sfrwr” is asserted, Fabric writes the “sfrdatao” to the extended memory and sends a valid “sfrack” to 8051 on the next cycle.

SFR write waveform is shown in the following figure:

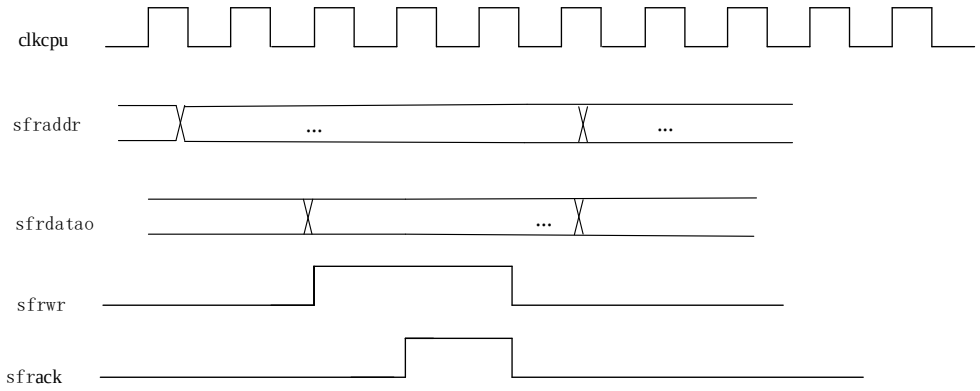


Figure 4-8 SFR Write Waveform

This chapter introduces port definitions of 8Kx32 and 2Kx32 SRAMs.

5 SRAM

HME-H1D03 family device contains an embedded SPRAM. There are two types of synchronous SPRAM, one is 8Kx32b, the other is 2Kx32b. The two SPRAM which are connected to FPGA can be used as memory by FPGA or 8051 MCU via the FPGA's logic and routing resources.

5.1 SPRAM_8Kx32 SRAM Port Definitions

The single-port primitive SPRAM signals are defined in the table below.

Table 5-1 SPRAM_8Kx32 SRAM Port Definition

Port Name	Type	Width	Description
clk	I	1	Input clock for SRAM, posedge active
ceb	I	1	Chip enable for SRAM, active low
web	I	1	Write enable for SRAM, active low
beb	I	4	Byte enable for SRAM, active low
addr	I	13	Address line for SRAM
datai	I	32	Data input for SRAM
datao	o	32	Input clock for SRAM

Table 5-2 SRAM Parameters

Parameters	Type	Description
init_file	string	SPRAM initial file, the suffix name is .dat or .hex Default: “”

5.2 SPRAM_2Kx32 SRAM Port Definitions

The single-port primitive SPRAM signals are defined in the table below.

Table 5-3 SPRAM_2Kx32 SRAM Port Definition

Port Name	Type	Width	Description
clk	I	1	Input clock for SRAM, posedge active
ceb	I	1	Chip enable for SRAM, active low
web	I	1	Write enable for SRAM, active low
addr	I	11	Address line for SRAM
datai	I	32	Data input for SRAM
datao	o	32	Input clock for SRAM

Table 5-4 SRAM Parameters

Parameters	Type	Description
init_file	string	SPRAM initial file, the suffix name is .dat or .hex Default: “”

This chapter lists details of MIPI D-PHY blocks and DSI controller core of HME-H1D03.

6 MIPI

6.1 MIPI D-PHY Blocks

The left side of the device includes two hard MIPI D-PHY quads. The D-PHY can be configured to support both camera interface (CSI-2) and display interface (DSI) applications. Below is a summary of the features supported by the hard D-PHY quads.

- Transmit and Receive compliant to D-PHY Revision 1.1
- High-Speed (HS) and Low-Power (LP) mode support (including built-in contention detect)
- Up to 6 Gb/s per quad (1500 Mb/s data rate per lane)
- Dedicated PLL for Transmit Frequency Synthesis
- Dedicated Serializer and De-Serializer blocks for fabric interfacing
- Supports continuous clock mode or low power clock mode

6.2 DSI Controller Core

The DSI Controller Core provides a flexible, high-performance, easy-to-use Mobile Industry Processor Interface (MIPI) Display Serial Interface (DSI) controller.

Key features include:

- Implements all three DSI Layers (Pixel to Byte packing, Low Level Protocol, Lane Management)
- Support for Command and Video Modes
- Host and Peripheral versions
- Scalable data lane support, 1 to 4 Data Lanes
- bidirectional support on lane 0
- Supports High Speed and Low Power operation
- Support for all DSI data types and formats
- Virtual Channel support
- Supports ULPS mode
- Full Low-Level Protocol Error and Contention detection and reporting

- Supports continuous and non-continuous Clock Lane operation
- Supports multiple packets per transmission
- Support for all three Video Mode packet sequences
  - Non-Burst Mode with Sync Pulses
  - Non-Burst Mode with Sync Events
  - Burst mode
- Support for bus turnaround signaling
- Flexible packet based user interface
  - APB interface (status and control)
- Supports PHY Protocol Interface (PPI) compatible MIPI D-PHYs
- MIPI Alliance Specification for Display Serial Interface Version 1.3.1 compliant

This part introduces details of configuration modes and pins, process, scheme, eFuse and AES Security of HME-H1D03 family.

7 Configuration and Debug

HME-H1 devices are configured by loading application-specific configuration data (Bitstream) into internal memory. HME devices must be configured each time when they are powered-up because their configuration memory are volatile.

7.1 Configuration Modes and Pins

The bitstream is loaded into the device through special configuration pins. These configuration pins serve as the interface for a number of different configuration modes:

There are 3 configuration modes: JTAG, AS and PS mode which are defined by three dedicated MSEL1/0 and JM_B pins. The three pins values are latched for mode selection when the devices are power on or reset. The configuration modes are described in table below.

Table 7-1 Configuration Mode

Mode	Direction	Description
(MSEL1, MSEL0)	Input	Configuration mode select. Default value: pull down 00B. The pin value will be latched for mode selection when the devices are power on or reset. 00B : AS Mode and clock is from internal OSC 01B : PS Mode 10B : reserved 11B : AS Mode while clock is from external pin
JM_B	Input	JTAG pin mode. The default value is pull up 1. The pin value will be latched for mode selection when the devices are power on or reset. 1: TCK/TDI/TDO/TMS pins are no JTAG functions, only user I/Os. 0: TCK/TDI/TDO/TMS pins are only used as JTAG functions.

Table 7-2 Configuration Pins

SPI serial configuration Pins		
SCK	Input/output	In passive serial configuration mode, SCK is a clock input used to clock configuration data from external device source into device. In active serial configuration mode, SCK is a clock output from device. The pin can be used as regular user I/Os after configuration.
mosi	Input/output	Data Output when in AS mode, data input when in PS mode.The pin can be used as regular user I/Os after configuration.

SPI serial configuration Pins		
miso_busyout	Input/output	Data Input when in AS mode, data output when in PS mode.The pin can be used as regular user I/Os after configuration.
csn	output or input	Chip select output to enable a SPI Flash in AS mode or input as a device select PS mode. The pin can be used as regular user I/Os after configuration.
hold	output	Hold output for SPI Flash
wp	output	Write protect output for SPI Flash
Dedicated Configuration Pins:		
CDONE	output	This is a dedicated configuration status pin; the pin will output low during configuration and output high when configuration succeeds. The pin can be used as regular user I/Os after configuration.
CRST_N	input	Chip global reset input. Active low.
Dedicated Pins: JTAG		
TCK	input	TCK Input Boundary-Scan Clock.
TDI	input	TDI Input Boundary-Scan Data Input.
TDO	output	TDO Output Boundary-Scan Data Output.
TMS	input	TMS Input Boundary-Scan Mode Select.

7.2 Configuration Process

The whole configuration process includes these procedure:

- ❒ Power Up
- ❒ Reset
- ❒ Initialization
- ❒ Configuration
- ❒ User Mode

If the device is powered up from the power-down state, VDD_CORE, AVDD (for the Efuse and internal power) must be powered up to the appropriate level for the device to exit from POR.

After power up, HME devices go through POR. During POR, the device resets, holds CDONE low, and tri-states all user I/O pins. When the device exits POR, all user I/O pins continue to tri-state. While CRST_N is low, the device is in reset. When CRST_N goes high, the device enters the initialization step. In HME devices, the initialization clock source is the internal oscillator. The device provides itself with enough clock cycles for proper initialization to clear the configuration memory.

When the initialization is finished, the device is ready to receive configuration data and the configuration stage starts. After the configuration data is accepted and CDONE goes high, HME device will enter user mode.

The POR circuit monitor the Power up/down voltage level and will generate the POR signal when the trigger point condition is met.

7.3 Configuration Scheme

7.3.1 AS Mode

HME download cable can operate the SPI Flash by the JTAG indirectly.

The following figure describes the AS configuration scheme using JTAG indirectly.

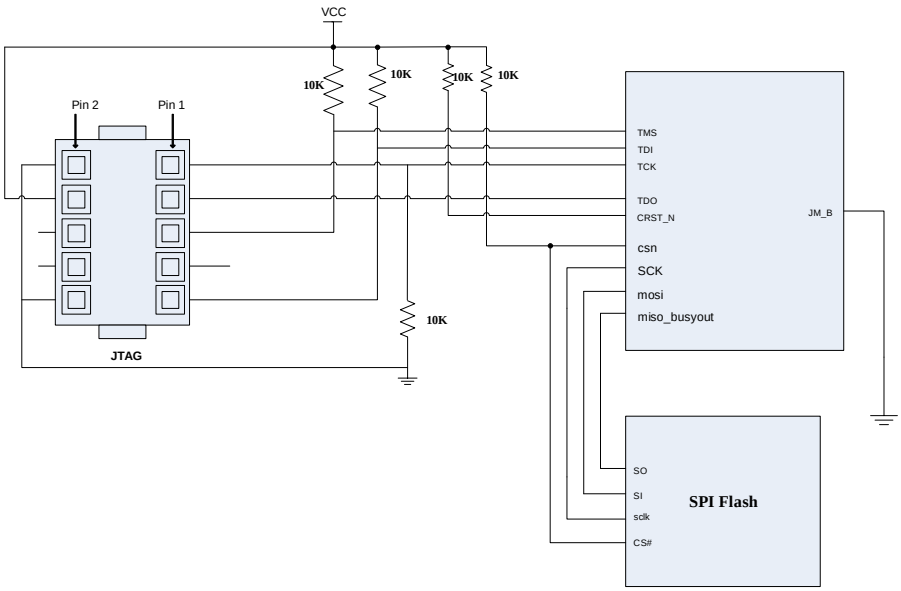


Figure 7-1 AS Configuration using JTAG

7.3.2 PS Mode

In the PS mode, HME-H1 family works as slave device, receive configuration data from external master controller passively. SPI Master can't read configuration data from HME-H1 family, so the PS master or HME cable can't operate the H1's embedded Efuse which must be programmed by JTAG.

The figure below describes HME-H1 family in PS configuration.

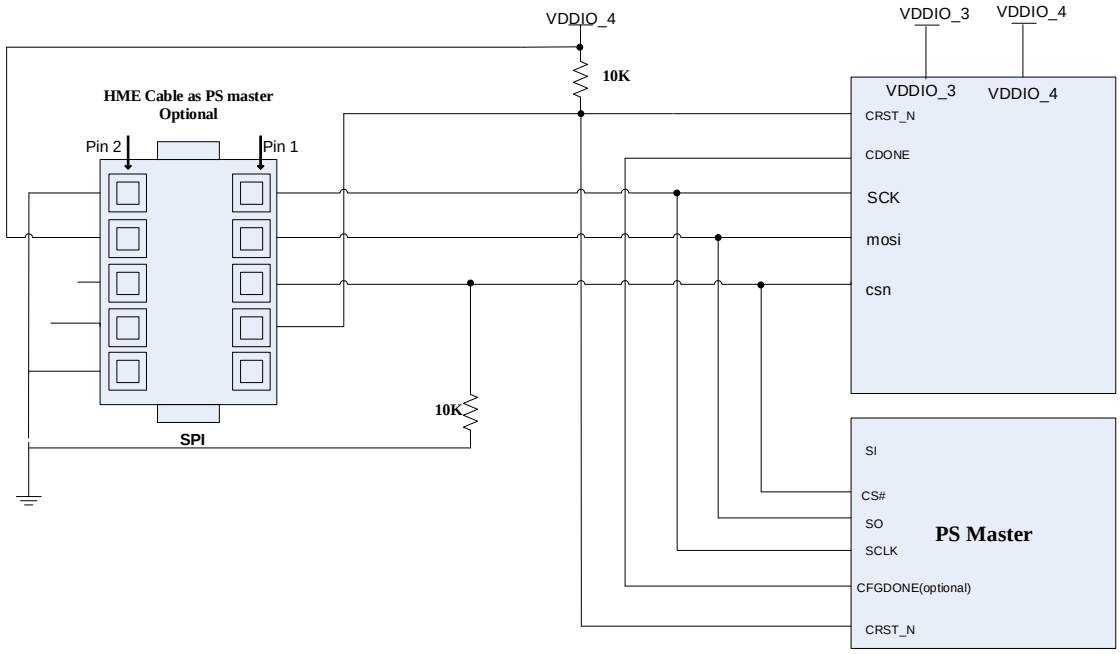


Figure 7-2 PS Configuration

7.3.3 JTAG Mode

There are two JTAG devices inside HME-H1 family for fabric debugging and configuration.

JTAG interface can access and debug configuration and program H1's embedded Efuse.

The figure below describes HME-H1 family in JTAG configuration.

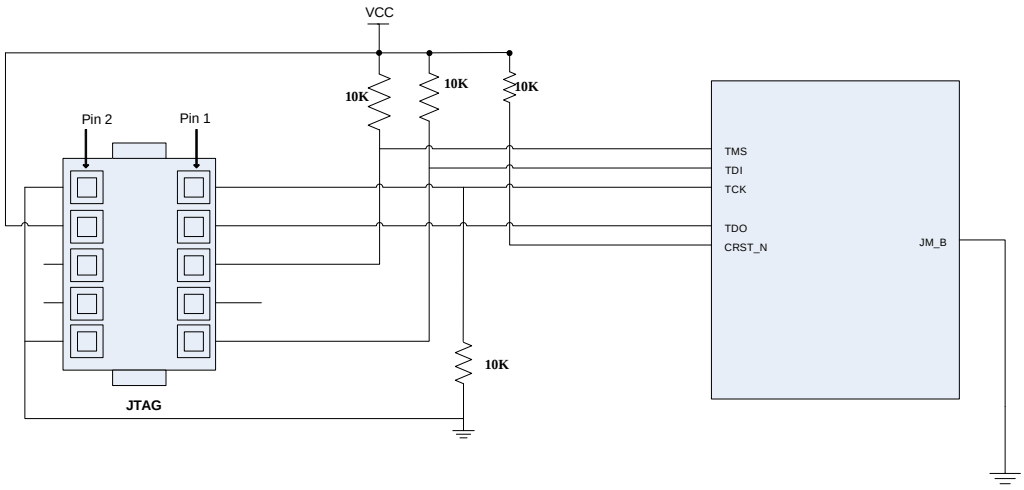


Figure 7-3 JTAG Configuration

7.4 eFUSE

HME-H1 has one 1024 bit eFUSE which is a One Time Program electrically programmable fuses memory. The eFuse can store the 256 bit AES key and 128bit initiation vector for bitstream decryption and other configuration setting data.

Using Fuxi tool E-Fuse Burner can program the eFUSE via HME download cable.

7.4.1 eFUSE field description

Table 7-3 eFUSE field

Bit	Description
Reserved region	
1023:416	Reserved
User region	
415:408	Crc check for user region[7:0]
407:387	User data. which can be operated by pbus master.
386:384	User_efuse_lock_bit
383:256	Initial vector[127:0]
255:0	AES key[255:0]

7.5 AES Security

Advanced Encryption Standard (AES) is a specification for the encryption of electronic data. The AES algorithm is adopted to encrypt the configuration bitstream using a 256-bit key. The HME-H1 family will decrypt the encrypted bitstream using the 256-bit key which is stored in Efuse. The configuration will success if the two 256-bit keys are matching, otherwise the configuration will fail and the device can't work.

The encryption and decryption process is shown in figure below.

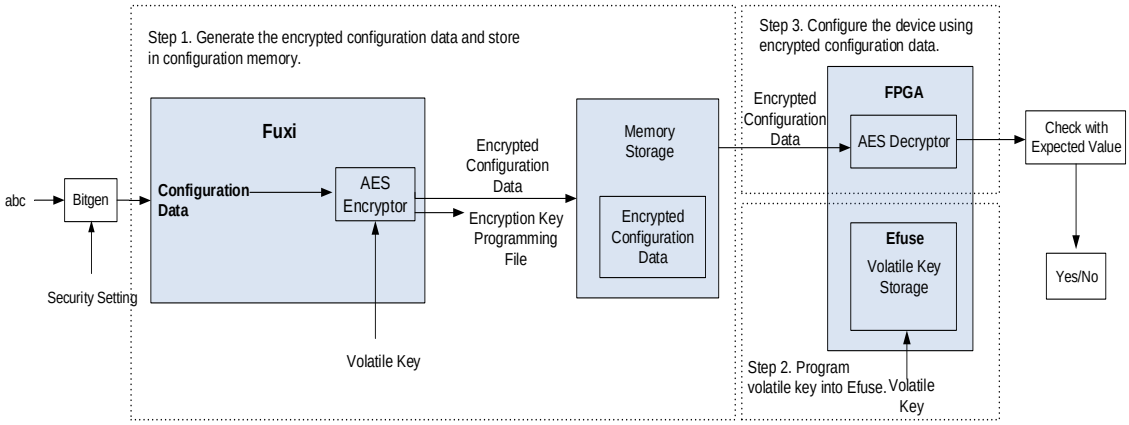


Figure 7-4 Encryption and Decryption Process

This chapter introduces DC and switching characteristics of HME-H1D03 family.

8 DC & Switching Characteristics

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **The following information applies unless otherwise noted: AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.** All parameters representing voltages are measured with respect to GND.

8.1 DC Electrical Characteristics

8.1.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 8-1 Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Max	Units
VDD_CORE	Internal supply voltage		-0.5	1.32	V
VDDIO_X	I/O driver supply voltage		-0.5	3.75	V
AVDD	Internal Efuse,LDO supply voltage		-0.5	3.75	V
OSC_VDD	Internal OSC supply voltage		-0.5	1.32	V
mipix_VDDA	MIPI supply voltage		-0.5	1.32	V
mipi_VDDPLL	MIPI PLL supply voltage		-0.5	1.32	V
VIN	Voltage applied to all User I/O pins and dual-purpose pins	Driver in a high-impedance state	-0.5	3.75	V
	Voltage applied to all Dedicated pins		-0.5	3.75	V
VESD	Electrostatic Discharge Voltage	Human body model	0	±2000	V
		Charged device model	-	±500	V
		Machine model	-	±200	V
TJ	Junction temperature		-40	125	°C
TSTG	Storage temperature		–55	125	°C

8.1.2 General Recommended Operating Conditions

Table 8-2 General Recommended Operating Conditions

Symbol	Description	Min	Nominal	Max
TJCOM	Junction temperature	-40°C	25°C	125°C
VDD_CORE	Internal supply voltage	0.98V	1.2V	1.26V
AVDD	Internal Efuse,LDO supply voltage	2.25V	2.5V	2.75V
OSC_VDD	Internal OSC supply voltage	1.08V	1.2V	1.26V
mipix_VDDA	MIPI supply voltage	1.08V	1.2V	1.26V
mipi_VDDPLL	MIPI PLL supply voltage	1.08V	1.2V	1.26V
VDDIO_3/4	I/O supply voltage @ 3.3V	2.97V	3.3V	3.63V
	I/O supply voltage @2.5V	2.25V	2.5V	2.75V
	I/O supply voltage @1.8V	1.62V	1.8V	1.98V
VDDIO_0/1/2	I/O supply voltage @ 3.3V	2.97V	3.3V	3.63V
	I/O supply voltage @2.5V	2.25V	2.5V	2.75V
	I/O supply voltage @1.8V	1.62V	1.8V	1.98V
	I/O supply voltage @1.5V	1.35V	1.5V	1.65V
	I/O supply voltage @1.2V	1.08	1.2V	1.32V

8.1.3 Static Current on General Normal Operating Conditions

Table 8-3 Static Current on General Normal Operating Conditions

Symbol	Description	Min	Nominal	Max
Static_Current_Core_1p2	VDD_CORE static current @1.2V/25°C	2.5mA	3.0mA	3.5mA
Static_Current_bank012_2p5	Bank0/1/2 static current @2.5V/25°C	-2.6uA	10uA	15uA
Static_Current_bank012_1p8	Bank0/1/2 static current @1.8V/25°C	-7.1uA	-5uA	1uA
Static_Current_bank3	Bank3 static current @2.5V/25°C	-4.0uA	0.1uA	4uA
Static_Current_bank4	Bank4 static current @2.5V/25°C	0uA	10uA	15uA

8.1.4 Power-On Specification

Table 8-4 Supply Voltage Thresholds for Power-On Reset

Symbol	Description	Min	Max
VDD_CORET	Threshold for the VDD_CORE supply	0.71V	
AVDDT	Threshold for the VCCIO supply	1.57 V	

Table 8-5 Supply Voltage Ramp Rate

Symbol	Description	Min	Max
VDD_CORER	Ramp rate from GND to valid VDD_CORE supply level	200ns	10ms
AVDDR	Ramp rate from GND to valid AVDD supply level	200ns	10ms
tCFGR	VDD_CORE and AVDD threshold to configuration allowed	1ms	

8.1.5 Recommended I/O Operating Conditions

Table 8-6 Single-ended I/O Standard Input DC Specifications

I/O Standard	VDDIO_X (V)			Vref (V)			Vil (V)	Vih (V)
	Min	Typ	Max	Min	Typ	Max	Max	Min
3.3V LVTTL and LVCMOS	3.135	3.3	3.465	-	-	-	0.8	2
2.5V LVTTL and LVCMOS	2.375	2.5	2.625	-	-	-	0.7	1.7
1.8V LVTTL and LVCMOS	1.71	1.8	1.89	-	-	-	0.35 x VDDIO_X	0.65 * VDDIO_X
1.5V LVCMOS	1.425	1.5	1.575	-	-	-	0.35 x VDDIO_X	0.65 * VDDIO_X
1.2V LVCMOS	1.140	1.2	1.26				0.35 x VDDIO_X	0.65 * VDDIO_X

Table 8-7 Single-ended I/O Standard Output DC Specifications

I/O Standard	Test Conditions		Voltage Threshold	
	Iol (mA)	Ioh (mA)	Maximum Vol (V)	Minimum Voh (V)
3.3V LVTTL	4	-4	0.4	2.4
3.3V LVCMOS	0.1	-0.1	0.4	Vccio – 0.4
2.5V LVTTL and LVCMOS	1	-1	0.4	Vccio – 0.4
1.8V LVTTL and LVCMOS	2	-2	0.45	Vccio – 0.45
1.5V LVTTL and LVCMOS	2	-2	25% Vccio	75% Vccio
1.2V LVTTL and LVCMOS	6	-6	0.4	Vccio-0.4

Table 8-8 Differential I/O Standard Input DC Specifications

I/O Standard	Vccio (V)			Vid (V)			Vicm (V)		
	Min	Typ	Max	Min	Min	Max	Min	Typ	Max
LVDS	2.375	2.5	2.625	0.1	0.35	0.6	0.1	1.25	2.0
miniLVDS	2.375	2.5	2.625	0.2	0.4	0.6	0.2	1.25	2.0
BLVDS	2.375	2.5	2.625	0.1				1.25	

Table 8-9 Differential I/O Standard Output DC Specifications

I/O Standard	Vod (mV)			Delta(Vod) (mV)		Vocm (V)		
	min	typ	max	min	max	min	typ	max
LVDS	250	350	600		50	1.075	1.25	1.425
miniLVDS	300	450	600		50	1.0	1.2	1.4
BLVDS*		600				1.075	1.25	1.425

8.1.6 Recommended MIPI Operating Condition

Table 8-10 MIPI D-PHY I/Os

Symbol	Description	Min	Typ	Max	Unit
Receiver					
High Speed					
VCMRX	Common-Mode Voltage HS Receive Mode	70	-	330	mV
VIDTH	Differential Input High Threshold	-	-	70	mV
VIDTL	Differential Input Low Threshold	-70	-	-	mV
VIHHS	Single-ended input High Voltage	-	-	460	mV
VILHS	Single-ended input Low Voltage	-40	-	-	mV
VTERM-EN	Single-ended Threshold for HS Termination Enable	-	-	450	mV
ZID	Differential Input Impedance	80	100	125	Ω
Low Power					
VIH	Logic 1 Input Voltage	880	-	-	mV
VIL	Logic 0 Input Voltage, not in ULP Stage	-	-	550	mV
VIL-ULPS	Logic 0 Input Voltage, in ULP Stage	-	-	300	mV
VHYST	Input Hysteresis	25	-	-	mV
Transmitter					
High Speed					
VCMTX	HS Transmit Static Common Mode Voltage	150	200	250	mV
VOD	HS Transmit Differential Voltage	140	200	270	mV
VOHHS	HS Single-ended Output High Voltage	-	-	360	mV
ZOS	Single-ended Output Impedance	40	50	62.5	Ω
△ZOS	Signle-ended Output Impedance Mismatch	-	-	10	%
Low Power					
VOH	Output High Voltage	1.1	1.2	1.3	V
VOL	Output Low Voltage	-50	-	50	mV
ZOLP	Output Impedance in LP Mode	110	-	-	Ω

Table 8-11 Quiescent Current Requirements

Symbol	Description	Device	Typical(1)	Maximum(2)	Units
ICOREQ	Quiescent VDDCORE supply current for whole device.		2		mA

Note:

(1) The numbers in this table are based on the conditions set forth in General Recommended Operating Conditions.

(2) Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. Typical values are characterized using typical devices at room temperature (TJ of 25°C at VDDCORE *= 1.2V).The FPGA is programmed with a "blank" configuration data file (i.e., a design with no functional elements instantiated).The maximum limits are tested for each device at the respective maximum specified junction temperature and at maximum voltage limits with MAX* VDDCORE *and VCCIO.*

8.2 Switching Characteristics

Timing parameters and their representative values are selected for inclusion below either because they are important as general design requirements or they indicate fundamental device performance characteristics.

8.2.1 Clock Performance

Table 8-12 Recommended Operating Frequency of Global Clock

Symbol	Max Frequency	Units
GCLK	600	MHz

Table 8-13 Recommended Operating Frequency of MCU Clock

Symbol	Max Frequency	Units
MCU clock	80	MHz

Table 8-14 *Recommended Operating Frequency of JTAG Clock*

Symbol	Max Frequency	Units
TCK	60	MHz

Table 8-15 Recommended Operating Frequency of PS Clock

Symbol	Max Frequency	Units
SCK	60	MHz

8.2.2 OSC Specifications

Table 8-16 OSC Specifications

Symbol	Description	Min	Typ	Max	Unit
Fout	Output clock freq.		80		MHz
T_{dt}	Output clock duty cycle	45	50	55	%
Tjit	Jitter performance		0.1		UIPP

8.2.3 PLL Specifications

Table 8-17 PLL Specifications

Symbol	Description	Min	Typ	Max	Unit
Fin	Input clock freq.	10		600	MHz
Fpfd	PFD input freq.	10		200	MHz
Fvco	VCO operation freq.	600		1200	MHz
Fout	Output freq.	1.17		600	MHz
Tlock	Lock time			200	us
Duty	Output clock duty cycle	45	50	55	%
N	Input divider	1		256	--
M	Loop divider	1		256	--
C0~C5	Output divider	1		256	--

Symbol	Description	Min	Typ	Max	Unit
Ndly	Output clock delay	0		255	--
Terr	Static phase error	-10		10	Degree
Trst	External reset time		50	100	ns
Tcalib	Calibration time	32		160	us

8.2.4 I/O Performance

Table 8-18 Recommended Operating Frequency of I/O

IO Standard	Description	Max Frequency
LVCMOS/LVTTL	VDDIO=1.2v	100 MHz
LVCMOS/LVTTL	VDDIO=1.5v	160 MHz
LVCMOS/LVTTL	VDDIO=1.8v	200 MHz
LVCMOS/LVTTL	VDDIO=2.5v	250 MHz
LVCMOS/LVTTL	VDDIO=3.3v	250 MHz
LVDS	VDDIO= 2.5V	600 MHz
miniLVDS	VDDIO= 2.5V	600 MHz

8.2.5 PLB Performance

Table 8-19 Recommended Operating Frequency of PLB

Symbol	Description	Speed		Units
		Min	Max	MHz
CNT16	16 bit counter performance @ recommended operating condition.		450	
CNT24	24 bit counter performance @ recommended operating condition.		400	

8.2.6 EMB18K Performance

Table 8-20 Recommended Operating Frequency of EMB5K

Symbol	Description	Speed		Units
		Min	Max	MHz
EMB18K	EMB18K using register path		248	
	EMB18K not using register path		200	

8.2.7 DSP Performance

Table 8-21 Recommended Operating Frequency of DSP

Symbol	Description	Speed		Units
		Min	Max	MHz
DSP	DSP using register path.		248	
	DSP not using the register path.		200	

8.2.8 SRAM Performance

Table 8-22 Recommended Operating Frequency of SRAM

Symbol	Description	Speed		Units
		Min	Max	MHz
SRAM	2K*32b and 8K*32b.		248	

9 Pins and Package

9.1 Pins Definitions and Rules

Table 9-1 Pins Definitions and Rules

Pin Name	Direction	Description
User I/O Pins		
IOXX_#	inout	user I/O pin
Multi-Function Pins		
IOXXX/ZZZ_#		Multi-function pins are labeled IOXXX/ZZZ_#, where ZZZ represents one or more of the following functions in addition to being general purpose user I/O. If not used for their special function, these pins can be user I/O.
Multi-Function Pins: SPI serial configuration Pins		
SCK	Input/output	In passive serial configuration mode, SCK is a clock input used to clock configuration data from external device source into device. In active serial configuration mode, SCK is a clock output from device. The pin can be used as regular user I/Os after configuration.
mosi	output	Data Output when in AS mode, data input when in PS mode. The pin can be used as regular user I/Os after configuration.
miso_busyout	Input	Data Input when in AS mode, data output when in PS mode. The pin can be used as regular user I/Os after configuration.
csn	output or input	Chip select output to enable a SPI Flash in AS mode or input as a device select PS mode. The pin can be used as regular user I/Os after configuration in AS mode.
hold	output	Hold output for SPI Flash
wp	output	Write protect output for SPI Flash
Multi-Function Pins: Configuraiton Pins		
CDONE	output	This is a dedicated configuration status pin; the pin will output low during configuration and output high when configuration succeeds. The pin can be used as regular user I/Os after configuration.
MSEL1/0	Input	Configuration mode select. Default value: pull down 00B. The pin value will be latched for mode selection when the devices are power on or reset. 00B : AS Mode and clock is from internal OSC

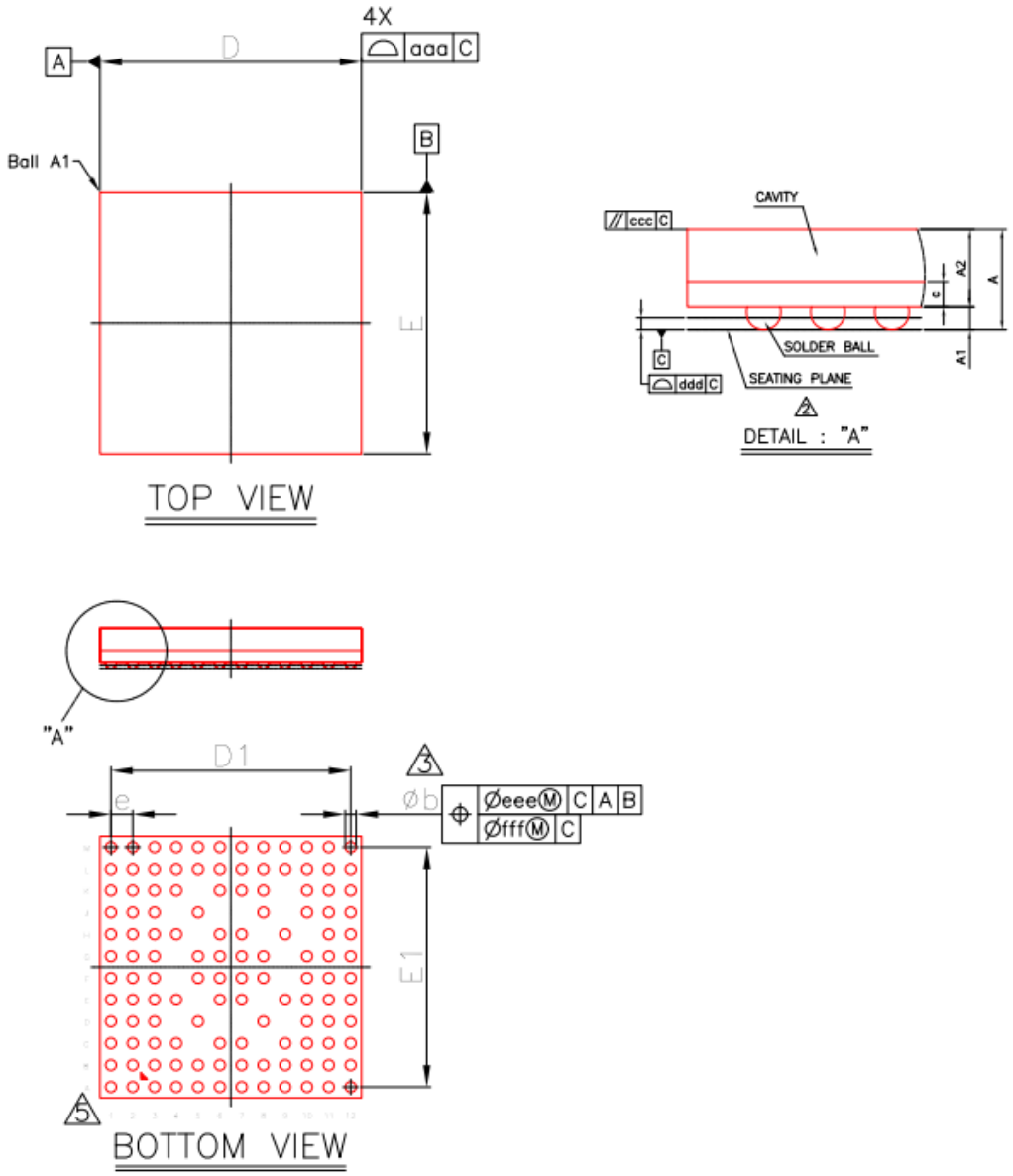
Pin Name	Direction	Description
		01B : PS Mode 10B : reserved 11B : AS Mode while clock is from external pin
Multi-Function Pins: Clock Pins		
CLKX	input	These clock pins connect to Global Clock Buffers. These pins become regular user I/Os when not needed for clocks.
Dedicated Pins: JTAG		
JM_B	Input	JTAG pin mode. The default value is pull up 1. The pin value will be latched for mode selection when the devices are power on or reset.
TCK	input	TCK Input Boundary-Scan Clock.
TDI	input	TDI Input Boundary-Scan Data Input.
TDO	output	TDO Output Boundary-Scan Data Output.
TMS	input	TMS Input Boundary-Scan Mode Select.
Dedicated Pins: JTAG		
CRSTn	input	Chip global reset input. Active low.
Dedicated Pins: MIPI Pins		
mipix_VSSA	N/A	MIPI analog ground
mipix_VDDA	N/A	MIPI analog power,1.2V
mipi_VDDPLL	N/A	MIPI PLL power,1.2V
mipi_VSSPLL	N/A	MIPI PLL ground
mipix_CKP	Input/Output	MIPI differential P clock
mipix_CKN	Input/Output	MIPI differential N clock
mipix_DPY	Input/Output	MIPI lane 0~3 P data
mipix_DNY	Input/Output	MIPI lane 0~3 N data
Dedicated Pins: Power		
VDDIO_X	N/A	Digital power for IO. Along with all the other VCCO pins in the same bank. 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V are selectable.
VDD_CORE		Digital power for core.1.2V.
AVDD		Analog power for PLL and eFuse, The range is from 1.8V to 3.3V. The power voltage is connected to 2.5V when the JTAG program the eFuse.
OSC_VDD	N/A	OSC power, 1.2V
OSC_VSS	N/A	OSC ground
VSS_CORE	N/A	core ground
VSS_IO	N/A	IO ground

***Note*:**

(1) AVDD *should connect to the pin6 of HME JTAG cable for Efuse Programming.*

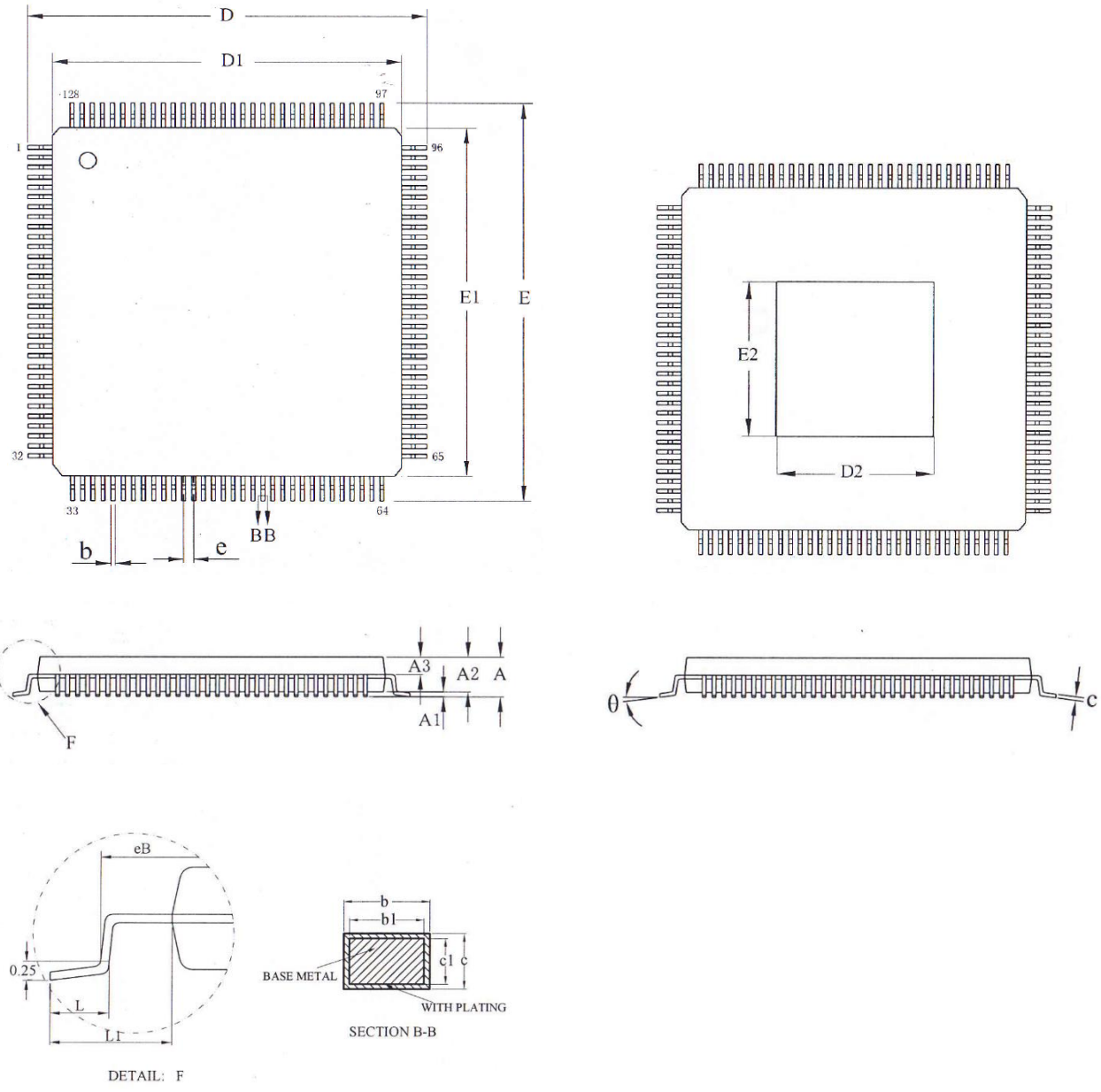
9.2 Package Information

9.2.1 STFBGA144 Package Specifications



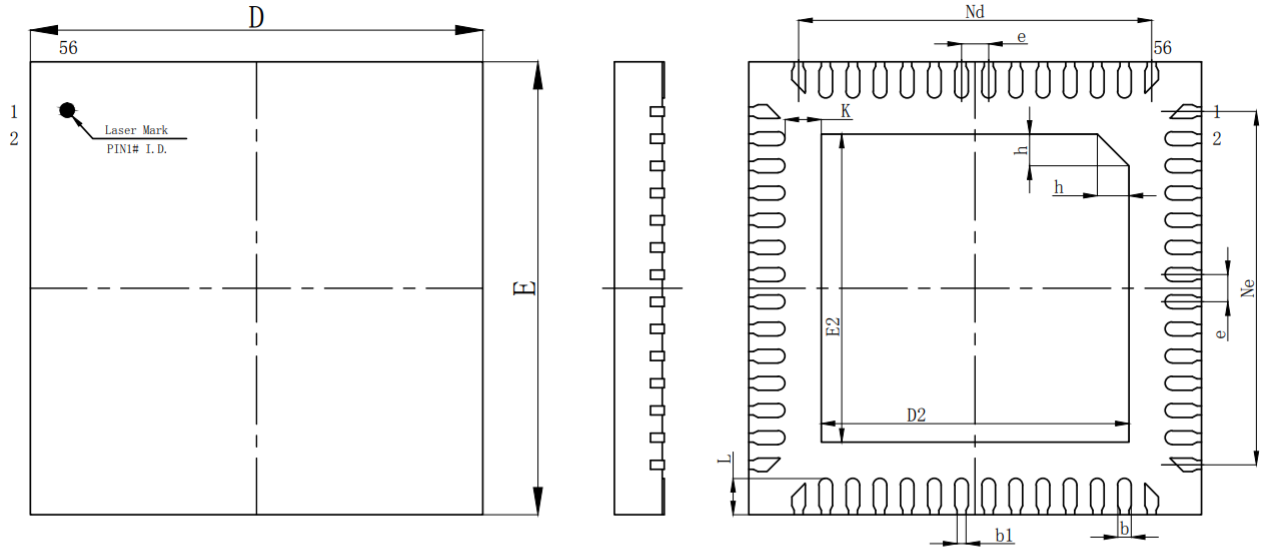
Symbol	Common Dimensions（mm）			Symbol	Common Dimensions（mm）		
	Min.	Nom.	Min.		Min.	Nom.	Max.
A	0.87	0.94	1.01	e	---	0.50	---
A1	0.10	0.15	0.20	b	0.20	0.25	0.30
A2	0.74	0.79	0.84	aaa	0.15		
c	0.22	0.26	0.30	ccc	0.10		
D	5.90	6.00	6.10	ddd	0.08		
E	5.90	6.00	6.10	eee	0.15		
D1	---	5.50	---	fff	0.05		
E1	---	5.50	---	MD/ME	12/12		

9.2.2 LQFP128 Package Specifications



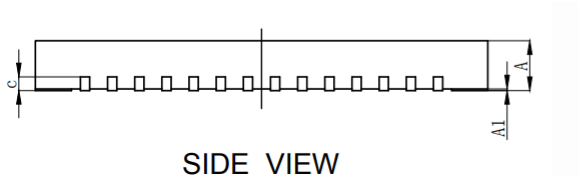
Symbol	Common Dimensions（mm）			Symbol	Common Dimensions（mm）		
	Min.	Nom.	Min.		Min.	Nom.	Min.
A	-	-	1.60	E	15.80	16.00	16.20
A1	0.05	-	0.15	E1	13.90	14.00	14.10
A2	1.35	1.40	1.45	E2	4.95 REF		
A3	0.59	0.64	0.69	D2	4.95 REF		
b	0.14	-	0.22	eB	15.05	-	15.35
b1	0.13	0.16	0.19	e	0.40BSC		
c	0.13	-	0.17	L	0.45	-	0.75
c1	0.12	0.13	0.14	L1	1.00 REF		
D	15.80	16.00	16.20	Θ	0°	3.5°	7°
D1	13.90	14.00	14.10				

9.2.3 QFN56 Package Specifications



TOP VIEW

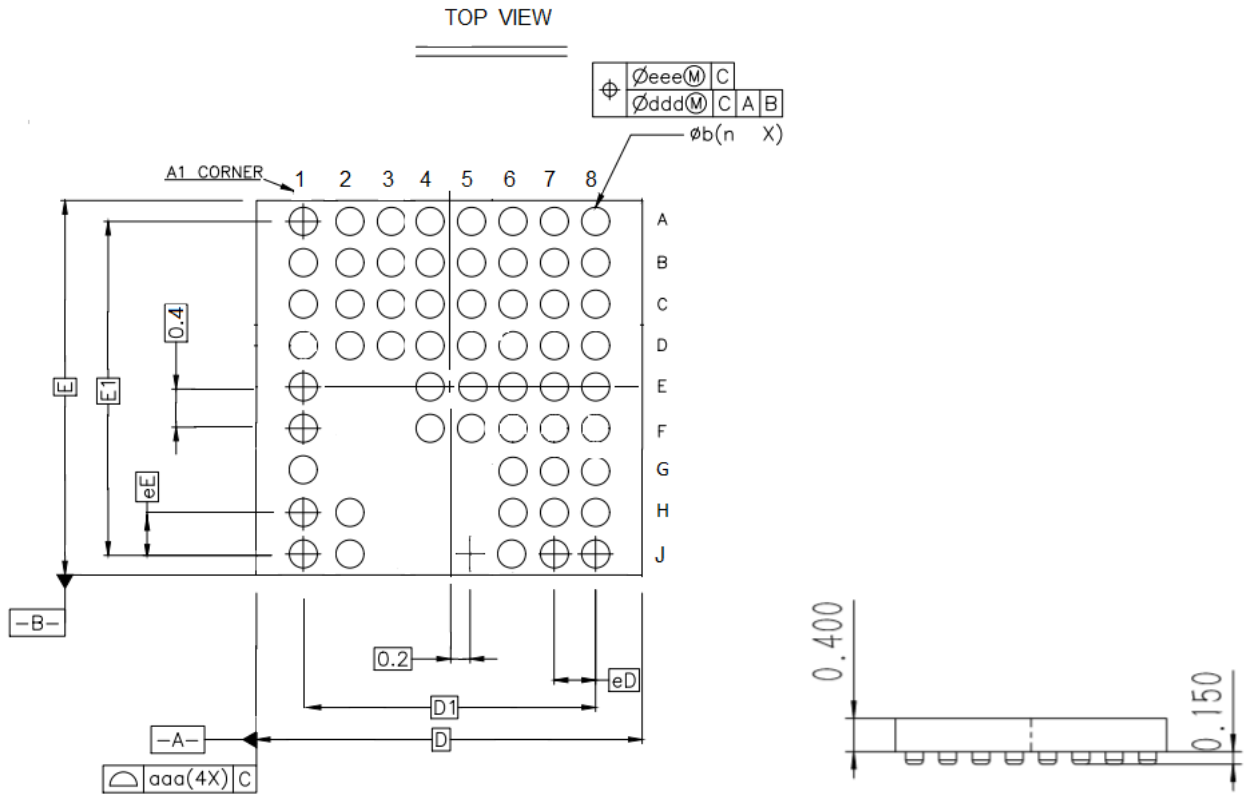
BOTTOM VIEW



SIDE VIEW

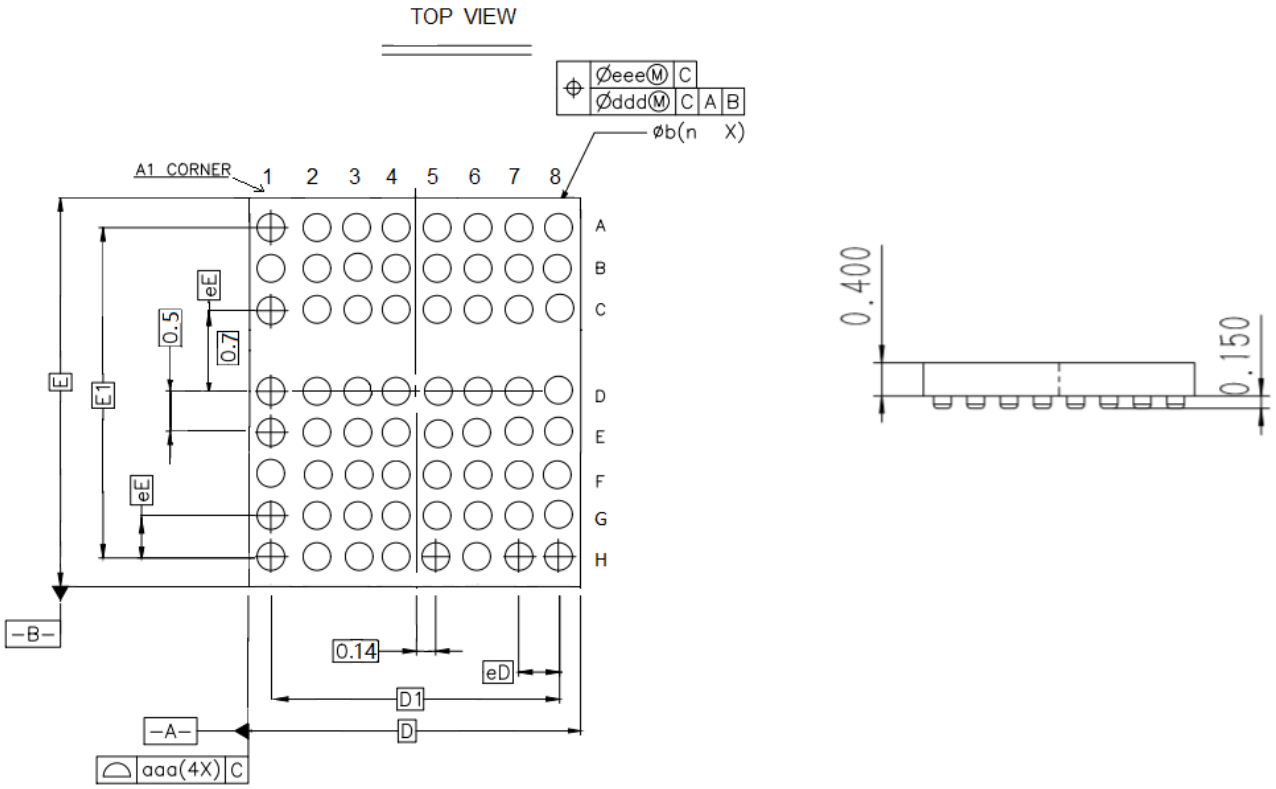
Symbol	Dimensions（mm）		
	Min.	Nom.	Max.
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.10	0.15	0.20
b1		0.10REF	
c		0.152REF	
D	4.90	5.00	5.10
D2	3.30	3.40	3.750
e		0.30BSC	
Ne		3.90BSC	
Nd		3.90BSC	
E	4.90	5.00	5.10
E2	3.30	3.40	3.50
L	0.35	0.40	0.45
K	0.35	0.40	0.45
h	0.30	0.35	0.40

9.2.4 WLCSP58 Package Specifications



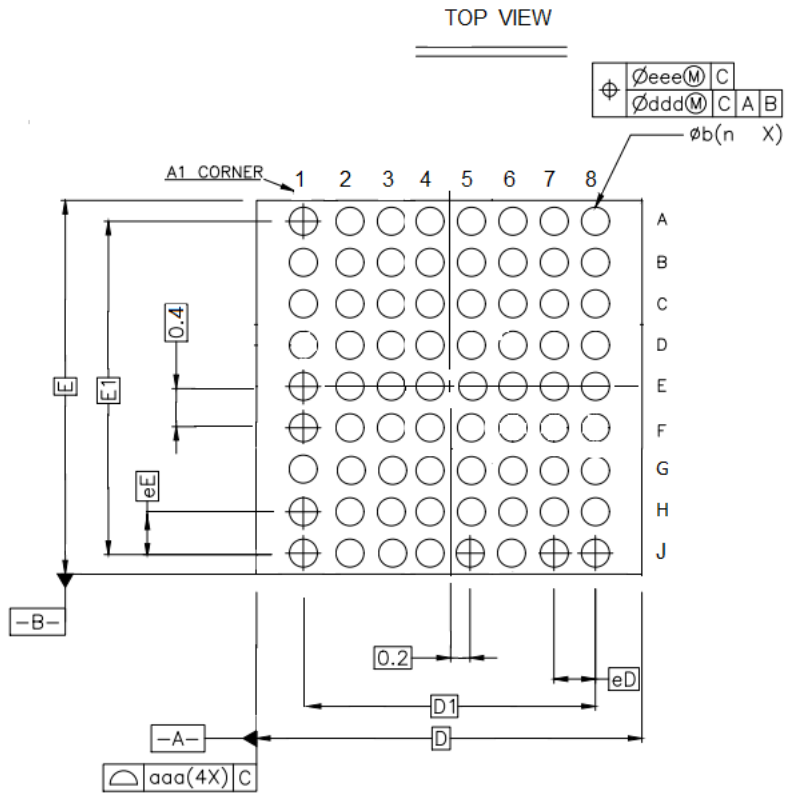
	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOM.	MAX.
Total Thickness	~~A~~	–	0.400	–
Stand Off	~~A1~~	–	0.15	–
Wafer Thickness (Molding)	~~A2~~	0.285 ±		0.020
Si Die Thickness	~~A3~~	0.285		REF
Body Size	D	3.255		BSC
	E	3.984		BSC
Ball Diameter (Size)		0.210		
Ball/Bump Width	b	0.240	0.270	0.300
Ball/Bump Pitch	eD	0.400		
	eE	0.400		
Ball/Bump Count	n	72		
Edge Ball Center to Center	D1	2.8		BSC
	E1	3.200		BSC
Package Edge Tolerance	aaa	0.035		
Coplanarity ~~(whole wafer)~~	ccc	0.030		
Ball/Bump Offset (Package)	ddd	0.150		
Ball/Bump Offset (Ball)	eee	0.080		

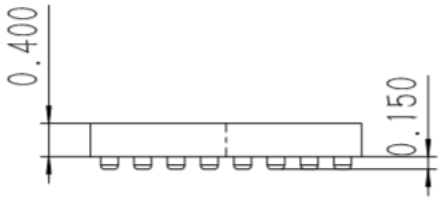
9.2.5 WLCSP68 Package Specifications



Item	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOM.	MAX.
Total Thickness	A	-	0.400	-
Stand Off	A1	-	0.150	-
Body Size	D		4.000 BSC	
	E		4.561 BSC	
Ball Diameter(Size)			0.215	
Ball/Bump Width	b	0.185	0.215	0.245
Ball/Bump Pitch	eD		0.500	
	eE		0.500	
			0.700	
Ball/Bump Count	n		64	
Edge Ball Center to Center	D1		3.715 BSC	
	E1		3.915 BSC	
Package Edge Tolerance	aaa		0.035	
Ball/Bump Offset(Package)	ddd		0.150	
Ball/Bump Offset(Ball)	eee		0.080	

9.2.6 WLCSP72 Package Specifications





	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOM.	MAX.
Total Thickness	~~A~~	–	0.400	–
Stand Off	~~A1~~	–	0.15	–
Wafer Thickness (Molding)	~~A2~~	0.285 ± 0.020		
SI Die Thickness	~~A3~~	0.285 REF		
Body Size	D	3.255 BSC		
	E	3.984 BSC		
Ball Diameter (Size)		0.210		
Ball/Bump Width	b	0.240	0.270	0.300
Ball/Bump Pitch	eD	0.400		
	eE	0.400		
Ball/Bump Count	n	72		
Edge Ball Center to Center	D1	2.8 BSC		
	E1	3.200 BSC		
Package Edge Tolerance	aaa	0.035		
Coplanarity ~~(whole wafer)~~	ccc	0.030		
Ball/Bump Offset (Package)	ddd	0.150		
Ball/Bump Offset (Ball)	eee	0.080		

This chapter shows details of ordering information.

10 Ordering Information

10.1 Part Number Conventions

All part numbers have the following conventions:

Table 10-1 Part number conventions

Vendor	Product Series	Device Type	LUT Density	NVM Density	Package Type	Temperature Range	Speed Grade
HME-	H1	D	03	N3	W72	C	7

Vendor

- ❒ CME former vendor marker
- ❒ HME latest vendor marker

Product Series

- ❒ H1 Hercules 1 family

Device Type

- ❒ D FPGA + DSP + MCU
- ❒ M FPGA + MCU + SDRAM/PSRAM

LUT Density

- ❒ 03 3K LUTs

Configuration NVM (SPI-flash) Option

- ❒ N0 Without internal SPI-flash
- ❒ N3 With 4Mb internal SPI-flash

Package Type: <type><#>

- ❒ L Low profile quad flat package (LQFP)
- ❒ W Wafer Level Chip Scale (WLCSP)
- ❒ C STFBGA
- ❒ Q QFN
- ❒ # Pin number (58 for 58pin, 72 for 72pin…)

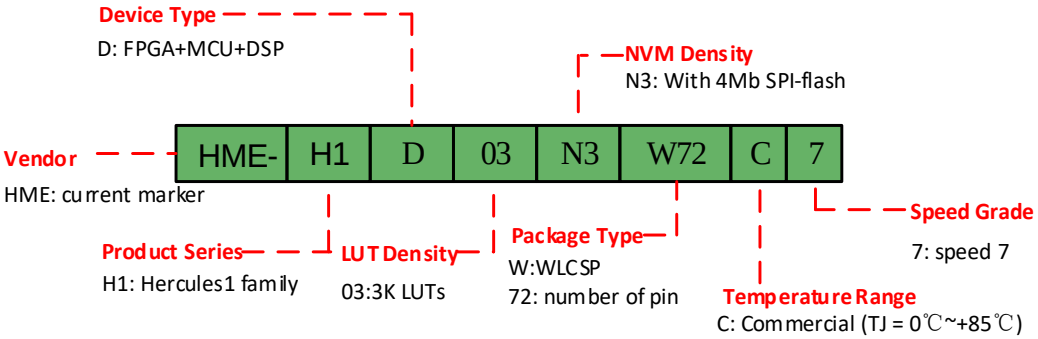
Temperature Range

- ❒ C Commercial (TJ = 0℃ to +85℃)
- ❒ I Industrial (TJ = -40℃ to +100℃)

Speed Grade

- ❒ # Speed (7 for speed 7, 6 for speed 6, …)

Example: **HME - H1 D 03 N3 W72 C 7**



10.2 Order Information

Table 10-2 Order information of H1D03 family

Product	Order P/N	Grade
H1D03N3W72C7	H1D03N3W72	Commercial
H1D03N3W72I7	H1D03N3W72I	Industrial
H1D03N3W58C7	H1D03N3W58	Commercial
H1M03N3W68C7	H1M03N3W68	Commercial
H1D03N0L128C7	H1D03N0L128	Commercial
H1D03N0L128I7	H1D03N0L128I	Industrial
H1M03N0C144C7	H1M03N0C144	Commercial
H1M03N0C144I7	H1M03N0C144I	Industrial
H1D03N0C144C7	H1D03N0C144	Commercial
H1D03N0C144I7	H1D03N0C144I	Industrial
H1D03N3Q56C7	H1D03N3Q56	Commercial
H1D03N3Q56I7	H1D03N3Q56I	Industrial

10.3 Chip Marking Spec

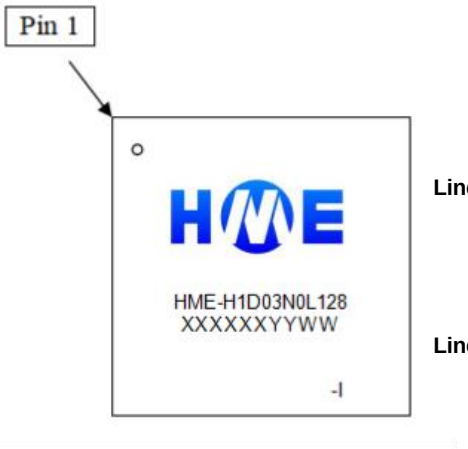
1) "C7" will not be marked. That default is commercial grade.

2) If "-I" is marked on the chip, that means industrial grade.

3) CME and HME are both official markers, please feel free to use.

4) As dimension limitations, there will be no vendor logo on chips in W58, W68, W72 and Q56.

Sample Marking:

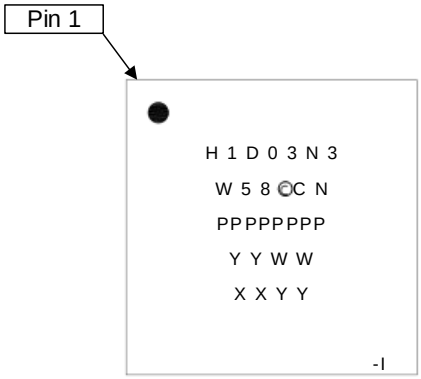


Line 4, Wafer Lot Number(first 6 bits) + Date Code
XXXXXXYYWW
YYWW(Actual Assembly Work Week)
e.g.
YY(Yearly 2015)---15
WW(Weekly 18) ---18
Line 5, Temperature Range
-I: Industrial
Empty for Commercial

Figure 10-1 General printing of H1D03 family

The paintings on H1D03N3W58, H1D03N3W72, H1D03N3W72I, and H1M03N3W68 are shown as follow.

H1D03N3W58



Line 3, PPPPPPPP
First 6 bits, Silicon Lot No
Last 2 bits, Silicon Series No
Line 4, YYWW
Date Code, Actual Assembly Work Week
e.g.
YY(Yearly 2023)——23
WW(Weekly 18)——18
Line 5, XXYY
XX—— Unit X-Coordinate on silicon
YY——Unit Y-Coordinate on silicon
Line 6, Temperature Range
I——Industrial
Empty—— Commercial

Figure 10-2 Specific printing of H1D03 family