HDL-Wideband-PFB-Lab-Test

Tags

Design Files

Simulink file

https://github.com/liuweiseu/snap_hdl_tut/blob/master/snap_hdl_pfb_v2.slx

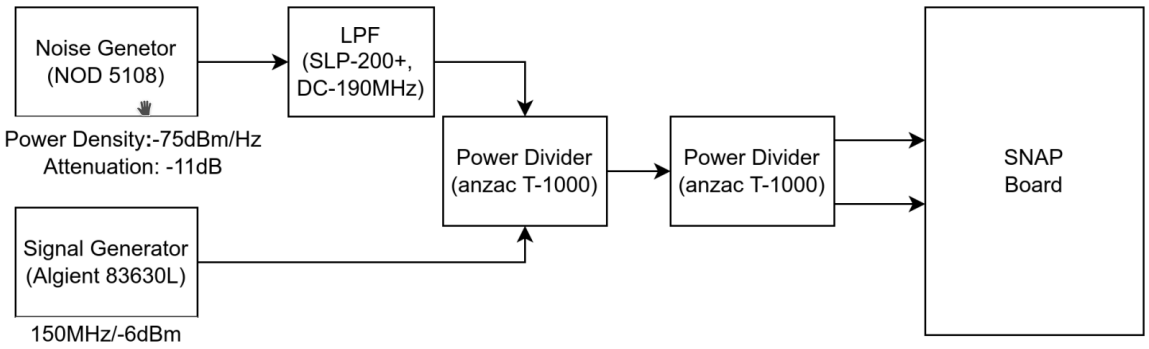
Python script

https://github.com/liuweiseu/snap_scripts/blob/master/ipynb/snap_hdl_pfb.ipynb

Note: Please make sure you use the correct branch of mlib_devel, casper_dspdevel and casperfpga mentioned in the ipynb.

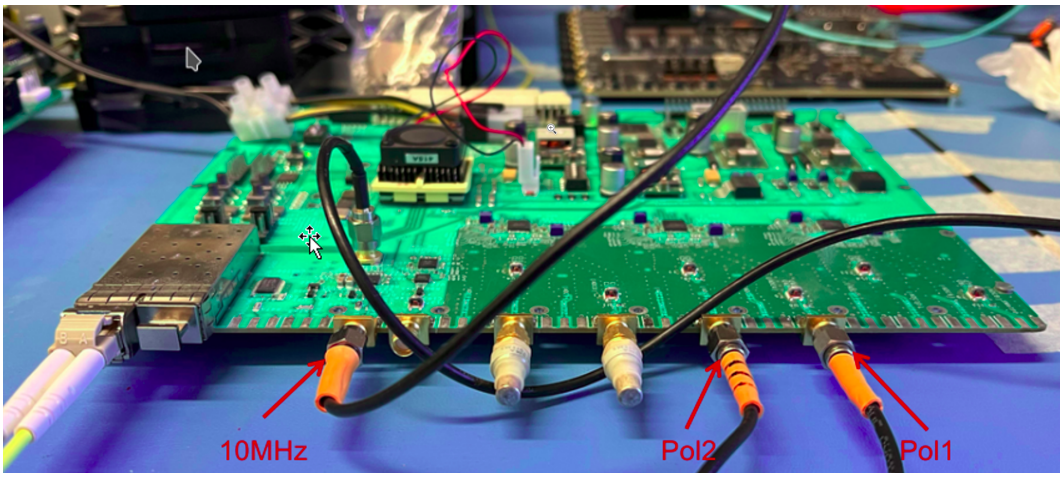
SNAP set up

Signal Chian



ADC mode

- Sampling Freq: 500MSps



Input signal

Noise generator

- PN: NOD 5108
- Attenuation: -11dB

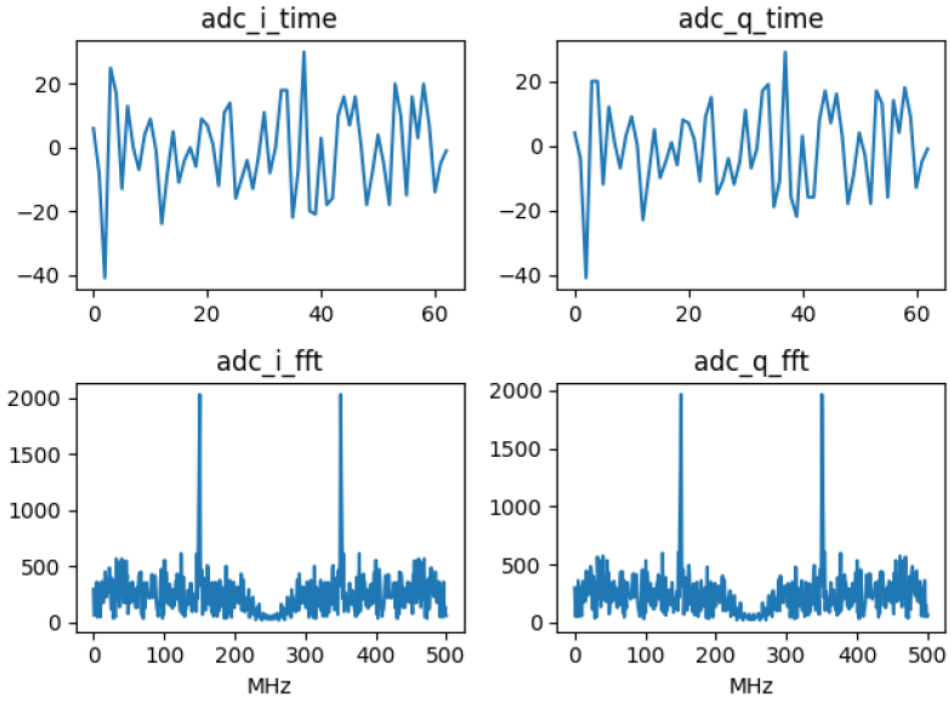
Signal generator

- PN: aGILENT 83630L
- Freq: 150MHz
- Amp: -6dBm

Test result

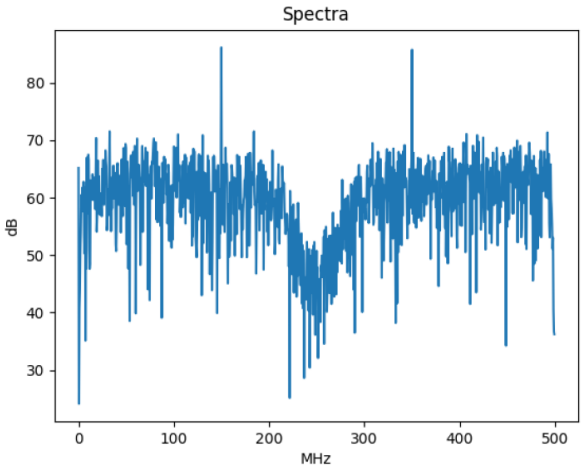
ADC RMS

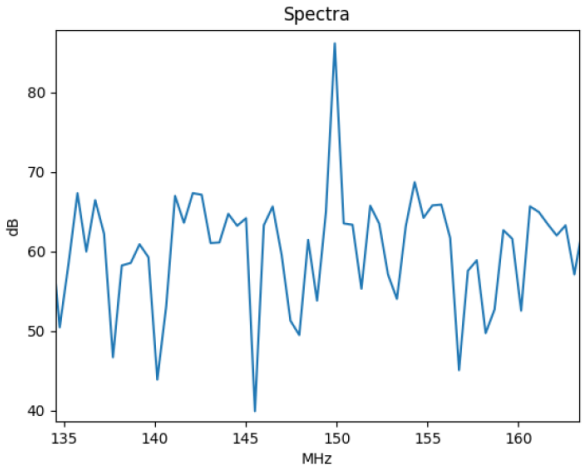
```
************************************
SNAP Board IP:  192.168.2.100
************************************
 Fabric Clock Freq : 250.311637 MHz
      RMS of ADC_I : 13.911762
      RMS of ADC_Q : 13.503327
```



Wideband PFB test result

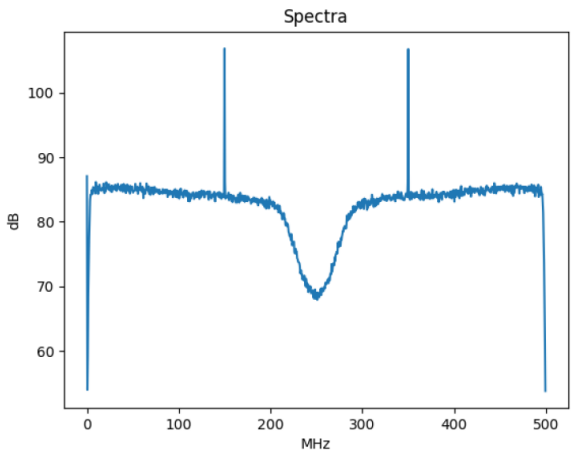
- acc_num = 1

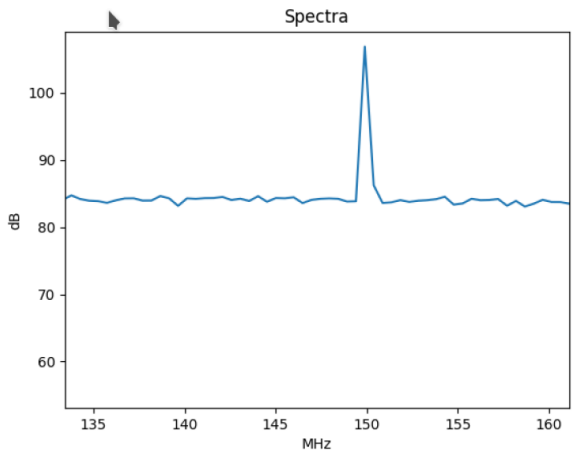




- acc_num = 128

  sig power: 107.3; noise power:84.5—> SNR: **23.8dB**.





The frequency resolution is:

$$500MHz/1024 = 488.28kHz$$

In theory, the power of noise is:

$$-75 + 10log(488.28 * 10^3) - 11 = -29.11dBm$$

The signal amp is -6dBm, so the SNR should be **23.11dB**, which is almost the same as the result we got in the lab.