# HDL-Wideband-PFB-Lab-Test

Tags



# Design Files

## Simulink file

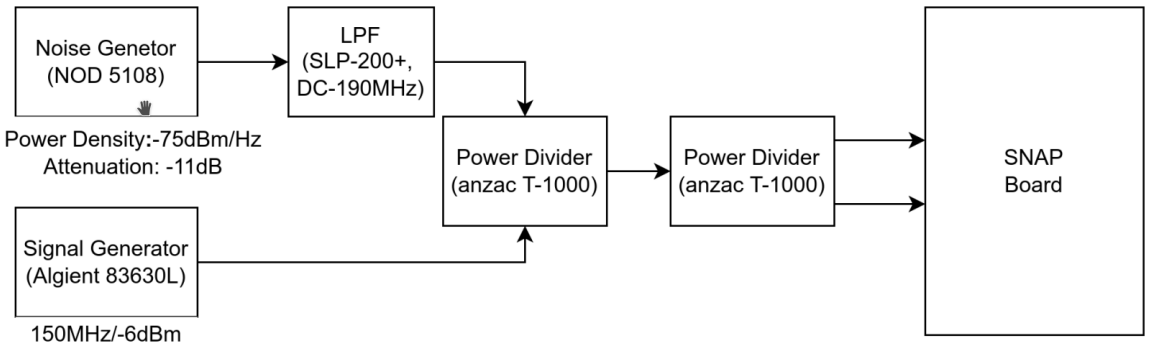
https://github.com/liuweiseu/snap_hdl_tut/blob/master/snap_hdl_pfb.slx

## Python script

https://github.com/liuweiseu/snap_scripts/blob/master/ipynb/snap_hdl_pfb.ipynb

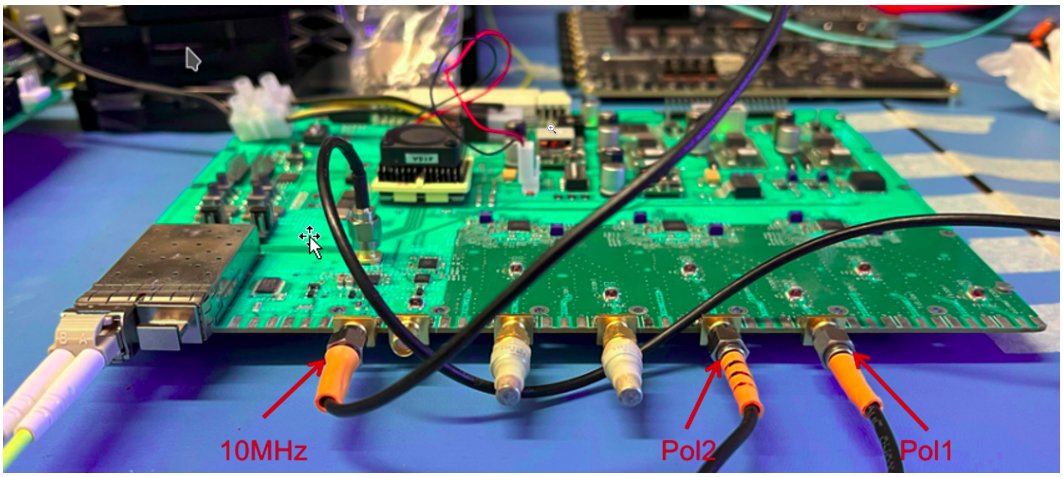
# SNAP set up

## Signal Chian




## ADC mode

- Sampling Freq: 500MSps




## Input signal

### Noise generator

- PN: NOD 5108
- Attenuation: -11dB

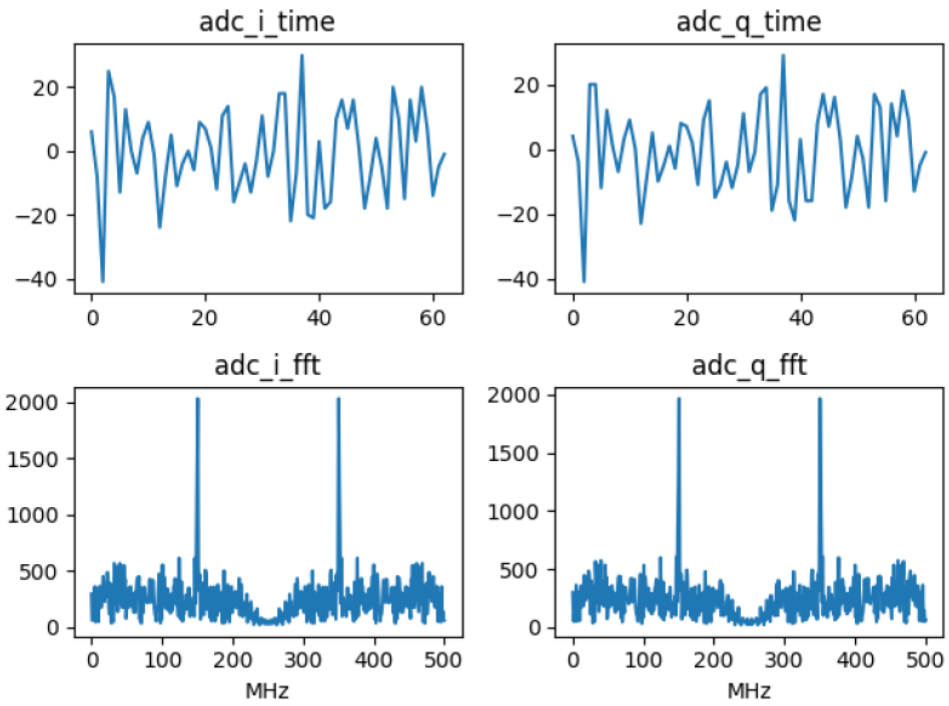
### Signal generator

- PN: aGILENT 83630L
- Freq: 150MHz
- Amp: -6dBm

# Test result

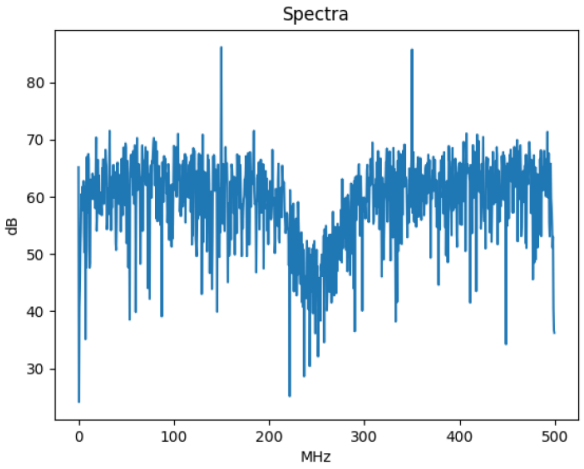
## ADC RMS

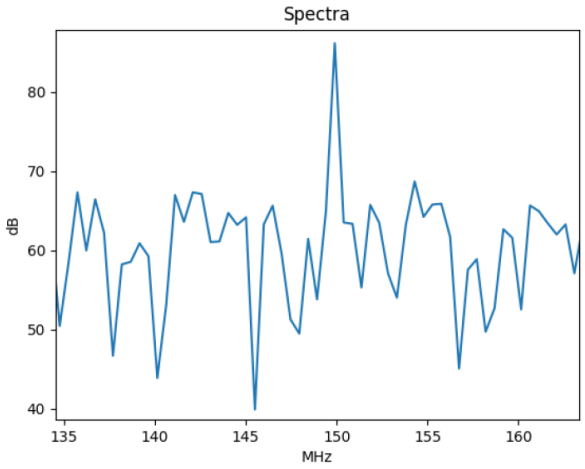
```
************************************
SNAP Board IP:  192.168.2.100
************************************
 Fabric Clock Freq : 250.311637 MHz
      RMS of ADC_I : 13.911762
      RMS of ADC_Q : 13.503327
```




## Wideband PFB test result

- acc_num = 1




- acc_num = 128