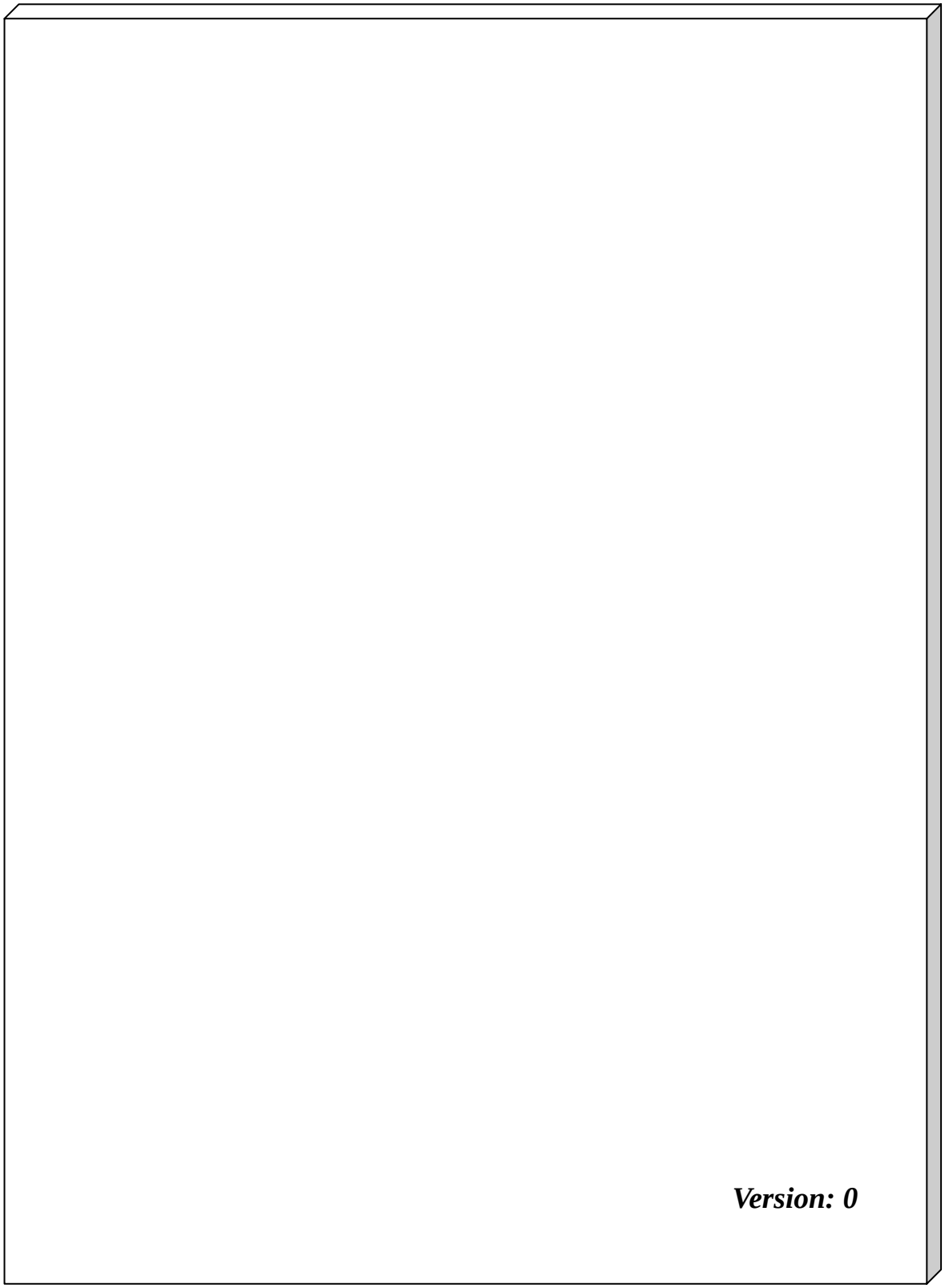

20/Aug/2014

MODULE NO. :

GMD13002 SERIES

CUSTOMER P/N:

VERSION NO.	CHANGE DESCRIPTION	DATE
0	ORIGINAL VERSION	2014/08/20

DATE: 2014/08/20

DATE: 2014/08/20

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1. FUNCTIONS & FEATURES

- LCD TYPE:

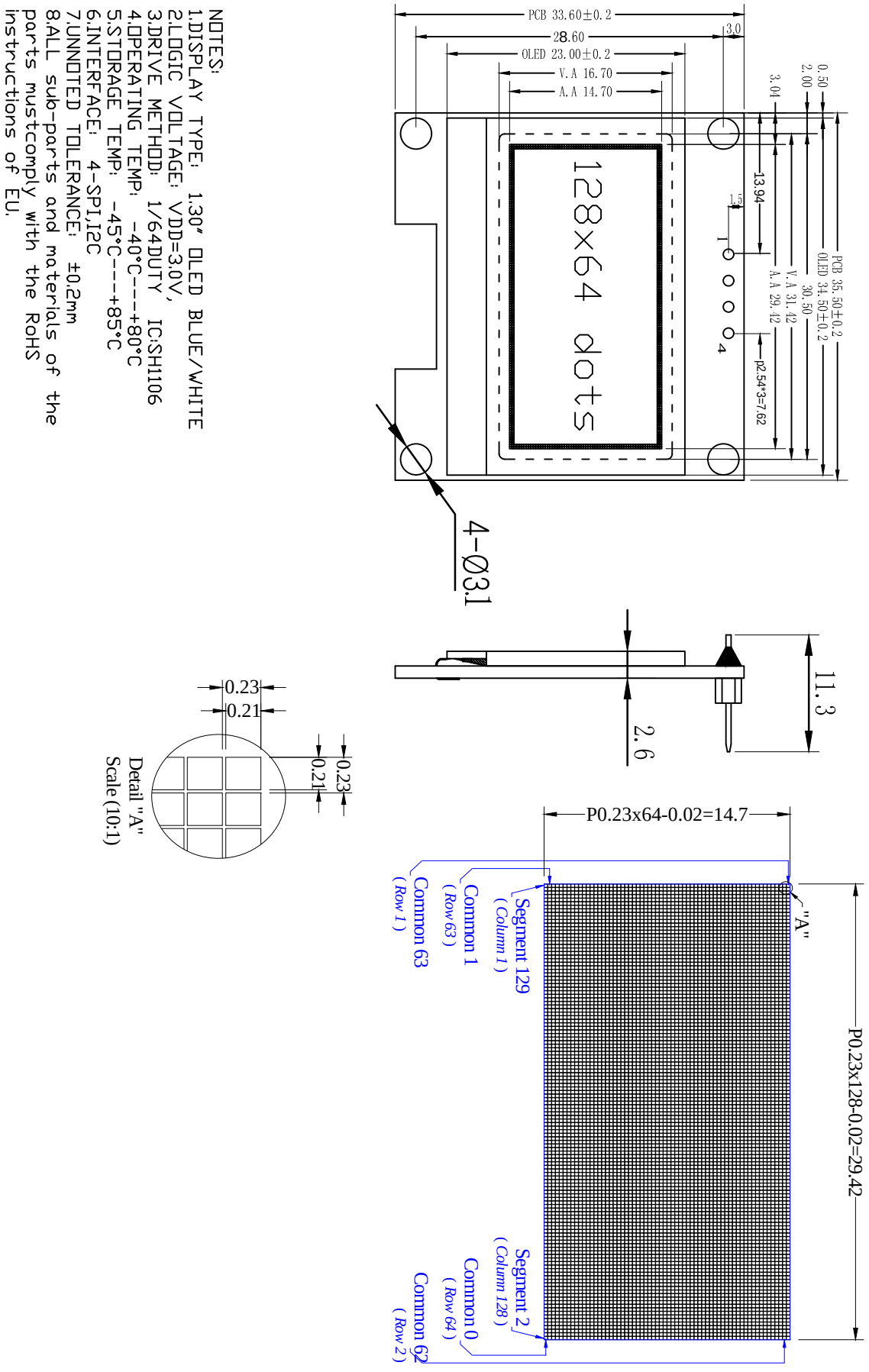
MODULE MODEL	LCD TYPE	REMARK
2864KLBLG03	1.30" OLED Passive Matrix White	

- Driving Scheme : 1/64 Duty,
- Viewing direction : 6 O'clock
- Drive IC : SH1106
- Power Supply Voltage : 3.0V
- V_{CC} : 12.0V
- Interface :IIC
- RoHS Compliant

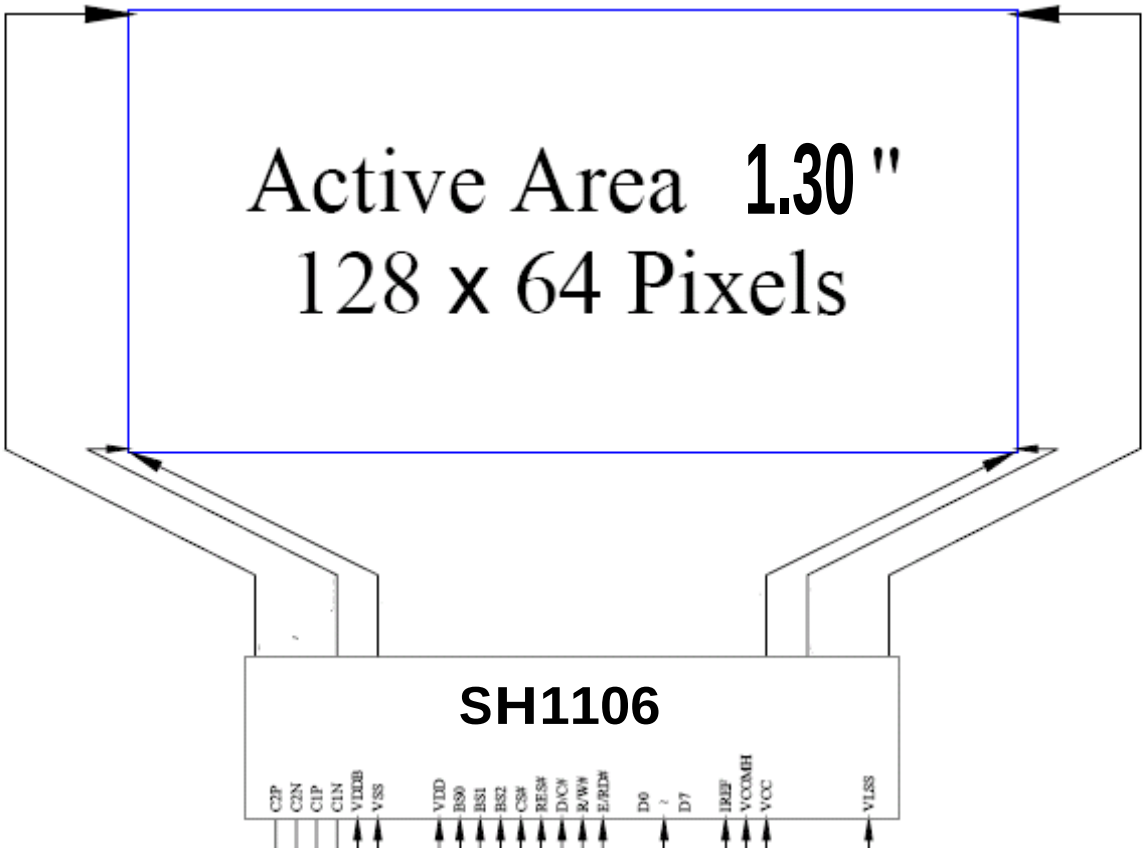
2. MECHANICAL SPECIFICATIONS

- Module Size : 35.50x33.70x2.60(max)mm
- Viewing Area : 31.42(L) x 16.70 (W) mm
- Active Area : 29.42 (L) x 14.70 (W) mm
- Dot Pitch : 0.23 (W) x 0.23 (H) mm
- Dot Size : 0.21(W) x 0.21(H) mm

3. EXTERNAL DIMENSIONS (unit: mm)



4. BLOCK DIAGRAM



5. PIN ASSIGNMENT

PIN	SYMBOL	Descriptions
1	GND	Ground of Logic Circuit
2	VDD	Power Supply for Logic
3	SCK	Serial clock input.
4	SDA	Serial data input.

电话：18923720150 邮箱：2355526548@qq.com

6. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V_{DD}	-0.3	4	V	1, 2
Supply Voltage for Display	V_{CC}	0	16	V	1, 2
Supply Voltage for DC/DC	*V_{BAT}*	*-0.3*	*5*	*V*	*1, 2*
Operating Temperature	T_{OP}	-40	85	°C	
Storage Temperature	T_{STG}	-40	85	°C	3
Life Time (120 cd/m^2)		10,000	-	hour	4
Life Time (80 cd/m^2)		30,000	-	hour	4
Life Time (60 cd/m^2)		50,000	-	hour	4

Note 1: All the above voltages are on the basis of "V_{SS} = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: V_{CC} = 12.0V, T_a = 25°C, 50% Checkerboard.
Software configuration follows Section 4.4 Initialization.
End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

7. ELECTRICAL CHARACTERISTICS

7.1. Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness (V_{CC} Supplied Externally)	L_{br}	Note 5	100	-	-	cd/m^2
Brightness (V_{CC} Generated by Internal DC/DC)	*L_{br}*	*Note 6*	*90*	*110*	*130*	*cd/m^2*
C.I.E. (Blue)	(x) (y)	C.I.E. 1931	0.12 0.22	0.16 0.26	0.20 0.30	
Dark Room Contrast	CR		-	2000:1	-	
Viewing Angle			-	Free	-	degree

* Optical measurement taken at V_{DD} = 2.8V, V_{CC} = 12V & *8V*.
Software configuration follows Section 4.4 Initialization.

7.2. DC CHARACTERISTICS

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	V_{DD}		1.65	2.8	3.3	V
Supply Voltage for Display (Supplied Externally)	V_{CC}	Note 5 (Internal DC/DC Disable)	-	12	-	V
Supply Voltage for DC/DC	*V_{SAT}*	*Internal DC/DC Enable*	*3.5*	*-*	*4.2*	*V*
Supply Voltage for Display (Generated by Internal DC/DC)	*V_{CC}*	*Note 6 (Internal DC/DC Enable)*	*6.4*	*-*	*9*	*V*
High Level Input	V_{IH}	I_{OUT} = 100μA, 3.3MHz	0.8×V_{DD}	-	V_{DD}	V
Low Level Input	V_{IL}	I_{OUT} = 100μA, 3.3MHz	0	-	0.2×V_{DD}	V
High Level Output	V_{OH}	I_{OUT} = 100μA, 3.3MHz	0.9×V_{DD}	-	V_{DD}	V
Low Level Output	V_{OL}	I_{OUT} = 100μA, 3.3MHz	0	-	0.1×V_{DD}	V
Operating Current for V_{DD}	I_{DD}		-	180	300	μA
Operating Current for V_{CC} (V_{CC} Supplied Externally)	I_{CC}	Note 7	-	23	32	mA
Operating Current for V_{SAT} (V_{CC} Generated by Internal DC/DC)	*I_{SAT}*	*Note 8*	*-*	*45*	*50*	*mA*
Sleep Mode Current for V_{DD}	$I_{DD, SLEEP}$		-	1	5	μA
Sleep Mode Current for V_{CC}	$I_{CC, SLEEP}$		-	2	10	μA

Note 5 & *6*: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.

Note 7: V_{DD} = 2.8V, V_{CC} = 12V, IREF=910K 100% Display Area Turn on.

Note 8: V_{DD} = 2.8V, V_{CC} = 8V, IREF=560K *100% Display Area Turn on.*

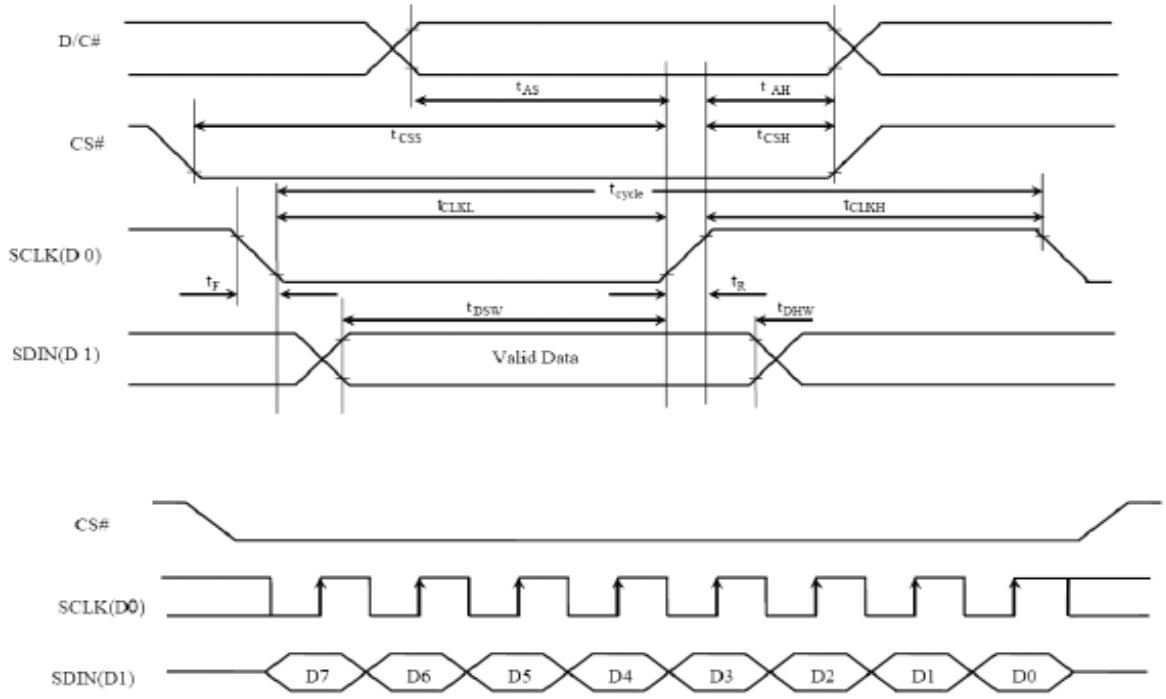
* Software configuration follows Section 4.4 Initialization.

7.3.AC CHARACTERISTICS

3.3.3.1 Serial Interface Timing Characteristics: (4-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns

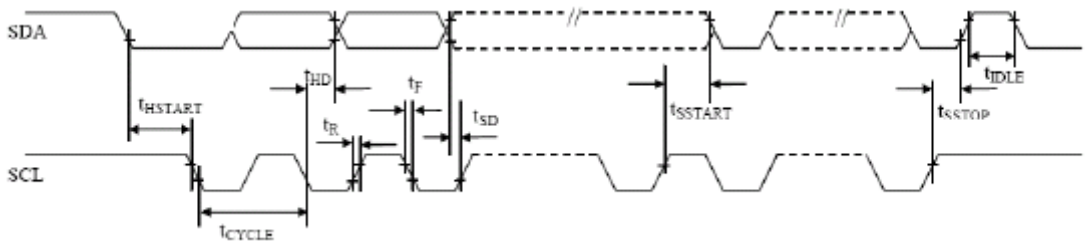
* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)



1 I^2C Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	μs
t_{HSTART}	Start Condition Hold Time	0.6	-	μs
t_{HD}	Data Hold Time (for "SDA_{OUT}" Pin)	0	-	ns
	Data Hold Time (for "SDA_{IN}" Pin)	300		
t_{SD}	Data Setup Time	100	-	ns
t_{SSTART}	Start Condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	μs
t_{SSTOP}	Stop Condition Setup Time	0.6	-	μs
t_R	Rise Time for Data and Clock Pin		300	ns
t_F	Fall Time for Data and Clock Pin		300	ns
t_{IDLE}	Idle Time before a New Transmission can Start	1.3	-	μs

* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)



8. COMMANDS

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
1. Set Column Address 4 lower bits	0	1	0	0	0	0	0	Lower column address				Sets 4 lower bits of column address of display RAM in register. (POR = 00H)
2. Set Column Address 4 higher bits	0	1	0	0	0	0	1	Higher column address				Sets 4 higher bits of column address of display RAM in register. (POR = 10H)
3. Set Pump voltage value	0	1	0	0	0	1	1	0	0	Pump voltage value		This command is to control the DC-DC voltage output value. (POR=32H)
4. Set Display Start Line	0	1	0	0	1	Line address						Specifies RAM display line for COM0. (POR = 40H)
5. The Contrast Control Mode Set	0	1	0	1	0	0	0	0	0	0	1	This command is to set Contrast Setting of the display. The chip has 256 contrast steps from 00 to FF. (POR = 80H)
Contrast Data Register Set	0	1	0	Contrast Data								
6. Set Segment Re-map (ADC)	0	1	0	1	0	1	0	0	0	0	ADC	The right (0) or left (1) rotation. (POR = A0H)
7. Set Entire Display OFF/ON	0	1	0	1	0	1	0	0	1	0	D	Selects normal display (0) or Entire Display ON (1). (POR = A4H)
8. Set Normal/ Reverse Display	0	1	0	1	0	1	0	0	1	1	D	Normal indication (0) when low, but reverse indication (1) when high. (POR = A6H)
9 Multiplex Ration Mode Set	0	1	0	1	0	1	0	1	0	0	0	This command switches default 63 multiplex mode to any multiplex ratio from 1 to 64. (POR = 3FH)
Multiplex Ration Data Set	0	1	0	*	*	Multiplex Ratio						
10. DC-DC Control Mode Set	0	1	0	1	0	1	0	1	1	0	1	This command is to control the DC-DC voltage DC-DC will be turned on when display on converter (1) or DC-DC OFF (0). (POR = 8BH)
DC-DC ON/OFF Mode Set	0	1	0	1	0	0	0	1	0	1	D	

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
11. Display OFF/ON	0	1	0	1	0	1	0	1	1	1	D	Turns on OLED panel (1) or turns off (0). (POR = AEH)
12. Set Page Address	0	1	0	1	0	1	1	Page Address				Specifies page address to load display RAM data to page address register. (POR = B0H)
13. Set Common Output Scan Direction	0	1	0	1	1	0	0	D	*	*	*	Scan from COM0 to COM [N - 1] (0) or Scan from COM [N -1] to COM0 (1). (POR = C0H)
14. Display Offset Mode Set	0	1	0	1	1	0	1	0	0	1	1	This is a double byte command which specifies the mapping of display start line to one of COM0-63. (POR = 00H)
Display Offset Data Set	0	1	0	*	*	COMx						
15. Set Display Divide Ratio/Oscillator Frequency Mode Set	0	1	0	1	1	0	1	0	1	0	1	This command is used to set the frequency of the internal display clocks. (POR = 50H)
Divide Ratio/Oscillator Frequency Data Set	0	1	0	Oscillator Frequency				Divide Ratio				
16. Dis-charge / Pre-charge Period Mode Set	0	1	0	1	1	0	1	1	0	0	1	This command is used to set the duration of the dis-charge and pre-charge period. (POR = 22H)
Dis-charge /Pre-charge Period Data Set	0	1	0	Dis-charge Period				Pre-charge Period				
17. Common Pads Hardware Configuration Mode Set	0	1	0	1	1	0	1	1	0	1	0	This command is to set the common signals pad configuration. (POR = 12H)
Sequential/Alternative Mode Set	0	1	0	0	0	0	D	0	0	1	0	
18. VCOM Deselect Level Mode Set	0	1	0	1	1	0	1	1	0	1	1	This command is to set the common pad output voltage level at deselect stage. (POR = 35H)
VCOM Deselect Level Data Set	0	1	0	VCOM (β X V_{REF})								
19. Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Read-Modify-Write start.
20. End	0	1	0	1	1	1	0	1	1	1	0	Read-Modify-Write end.
21. NOP	0	1	0	1	1	1	0	0	0	1	1	Non-Operation Command
22. Write Display Data	1	1	0	Write RAM data								
23. Read Status	0	0	1	BUSY	ON/ OFF	*	*	*	0	0	0	
24. Read Display Data	1	0	1	Read RAM data								

Note: Do not use any other command, or the system malfunction may result.

9. FUNCTIONAL SPECIFICATION

9.1 Commands

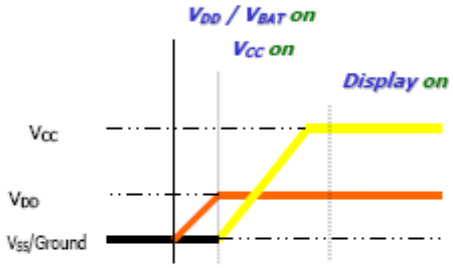
Refer to the Technical Manual for the SH1106

9.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

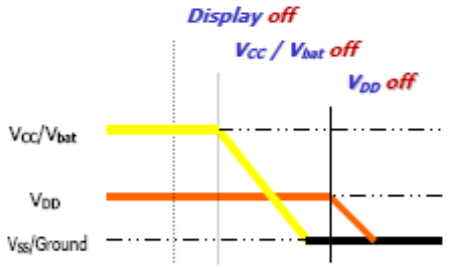
9.2.1 Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}/ V_{BAT}
6. Delay 100ms
   (When V_{CC} is stable)
7. Send Display on command



9.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC} / V_{BAT}
3. Delay 100ms
   (When V_{CC} / V_{BAT} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



Note 13:

1) Since an ESD protection circuit is connected between V_{DD} and V_{CC} inside the driver IC, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF.
2) V_{CC} / V_{BAT} should be kept float (disable) when it is OFF.
3) Power Pins (V_{DD}, V_{CC}, V_{BAT}) can never be pulled to ground under any circumstance.
4) V_{DD} should not be power down before V_{CC} / V_{BAT} power down.

9.3 Reset Circuit

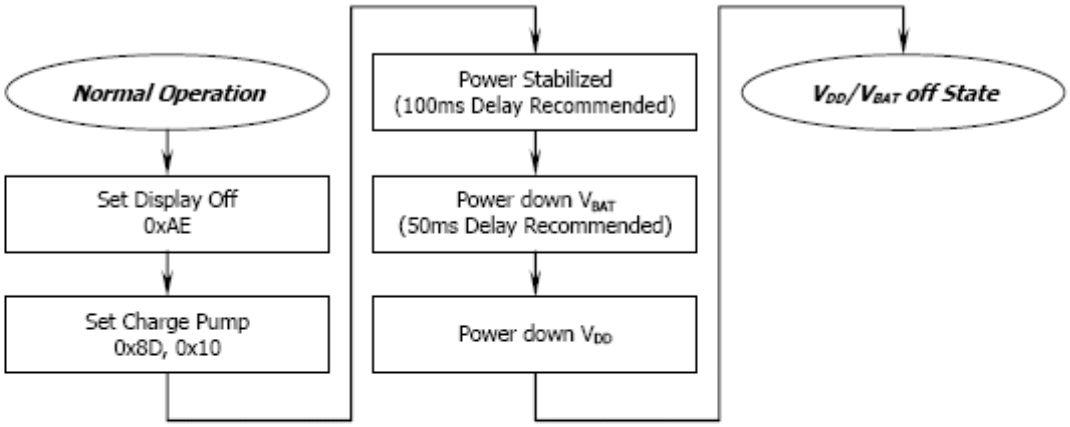
When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 128×64 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to colum address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

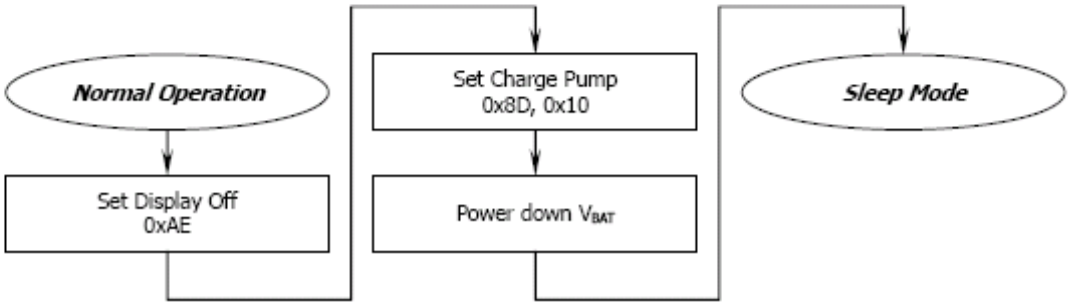
9.4 Actual Application Example

If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

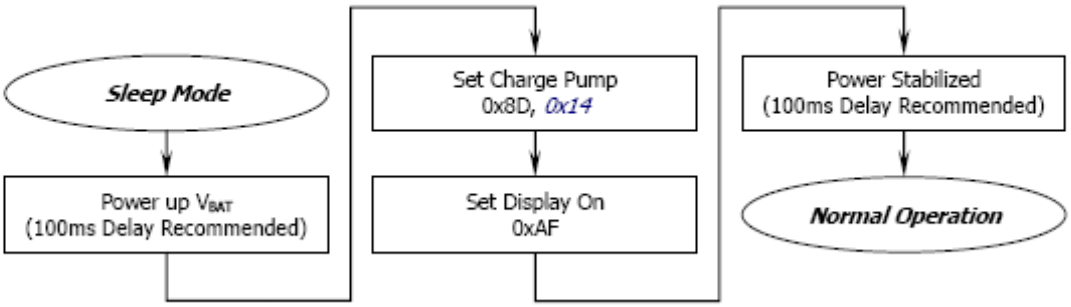
<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>



10. MODULE ACCEPT QUALITY LEVEL (AQL)

10.1 AQL Standard Value: Critical Defect =0.1, Major Defect=0.65; Minor Defect =2.5.

10.2 Inspection Standard: MIL-STD-105E Table Normal Inspection Single Sampling Level II

11. RELIABILITY TEST.

11.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	70°C, 240 hrs	The operational functions work.
Low Temperature Operation	-40°C, 240 hrs	
High Temperature Storage	85°C, 240 hrs	
Low Temperature Storage	-40°C, 240 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 120 hrs	
Thermal Shock	-40°C ⇔ 85°C, 24 cycles 60 mins dwell	

* The samples used for the above tests do not include polarizer.
* No moisture condensation is observed during tests.

11.2 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

12. QUALITY DESCRIPTION & APPLICTION NOTE

Please refer to "General Inspection Criteria" document.