



User Manual UM3244

DT5720

2/4 Channel 12bit 250 MS/s Digitizer

Rev. 10 - May 26th, 2017

Purpose of this Manual

This document contains the full hardware description of the DT5720 CAEN digitizer and their principle of operating as **Waveform Recording Digitizer** (basing on the hereafter called "**waveform recording firmware**").

The reference firmware revision is: **4.14_0.14**.

For any reference to registers in this user manual, please refer to document [RD1] on the digitizer web page.

For any reference to DPP firmware in this user manual, please refer to documents [RD2] present on the firmware web page.

Change Document Record

Date	Revision	Changes
-	00-9	Old manuals are available on request (see Chap. Technical Support).
May 26 th , 2017	10	Revised layout and improved text.

Symbols, Abbreviated Terms and Notation

ADC	Analog-to-Digital Converter
AMC	ADC & Memory Controller
DAQ	Data Acquisition
DAC	Digital-to-Analog Converter
DC	Direct Current
LVDS	Low-Voltage Differential Signal
PLL	Phase-Locked Loop
ROC	ReadOut Controller
TTT	Trigger Time Tag
USB	Universal Serial Bus

Reference Documents

- [RD1] UM5961 – 720 Registers Description.
- [RD2] UM2088 – DPP-PSD User Manual.
- [RD3] GD2512 – CAENUpgrader QuickStart Guide.
- [RD4] GD2817 – How to make coincidences with CAEN digitizers.
- [RD5] UM1935 – CAENDigitizer User & Reference Manual.
- [RD6] AN2472 – CONET1 to CONET2 migration.
- [RD7] GD2783 – First Installation Guide to Desktop Digitizers & MCA.
- [RD8] UM2091 – CAEN WaveDump User Manual.
- [RD9] GD2484 – CAENScope Quick Start Guide.
- [RD10] UM5960 – CoMPASS User Manual.

All CAEN documents can be downloaded at: <http://www.caen.it/csite/LibrarySearch.jsp>

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MADE IN ITALY: We stress the fact that all the boards are made in Italy because in this globalized world, where getting the lowest possible price for products sometimes translates into poor pay and working conditions for the people who make them, at least you know that who made your board was reasonably paid and worked in a safe environment. (this obviously applies only to the boards marked "MADE IN ITALY", we cannot attest to the manufacturing process of "third party" boards).



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1 Introduction

The Mod. DT5720 is 2/4 Channel 12 bit 250 MS/s Desktop Waveform Digitizer with 2 V_{pp} input dynamic range on single ended MCX coaxial connectors (see Tab. 1.1). The DC offset is adjustable via a 16-bit DAC on each channel in the ±1 V range.

Considering the sampling frequency and bit number, these digitizers are well suited for mid-fast signals as the ones coming from liquid or inorganic scintillators coupled with PMTs or Silicon Photomultiplier.

A common acquisition trigger signal (common to all the channels) can be fed externally via the front panel TRG-IN input connector or via software. Alternatively, each channel is able to generate a self-trigger when the input signal goes under/over a programmable threshold. The trigger from one board can be propagated out of the board through the front panel GPO .

During the acquisition, data stream is continuously written in a circular memory buffer. When the trigger occurs, the digitizer writes further samples for the post trigger and freezes the buffer that can be read by one of the provided readout links.

Each channel has a SRAM digital memory (see Tab. 1.1 for the available memory size options) divided into buffers of programmable size (1 ÷ 1024). The readout (from USB or Optical link) of a frozen buffer is independent from the write operations in the active circular buffer (ADC data storage).

Two modes are supported for the event storage in the board memories: Standard mode and Pack2.5 mode (see Sec. Event structure).

DT5720 features front panel CLK-IN connector as well as an internal PLL for clock synthesis (50 MHz oscillator) from internal/external references.

The board houses USB 2.0 and optical link interfaces. USB 2.0 allows data transfers up to 30 MB/s. The Optical Link interface (CAEN proprietary CONET protocol) is capable of transfer rate up to 80 MB/s and offers daisy chain capability. Therefore, it is possible to connect up to 8 ADC modules to a single A2818 Optical Link Controller, or up to 32 using a 4-link A3818 version (Mod. A2818/A3818, see Tab. 1.1).

In addition to the waveform recording firmware, CAEN provides for this digitizer the Digital Pulse Processing firmware (DPP) for the Pulse Shape Discrimination (DPP-PSD) [RD2], which combines the functionalities of a digital QDC (charge integration) and discriminator of different shapes for particle identification. These special firmware make the digitizer an enhanced system for Physics Applications.

Board Model		Description
DT5720B	4 Ch.	4 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, SE
DT5720C	2 Ch.	12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, SE
DT5720D	4 Ch.	12 bit 250 MS/s Digitizer: 10MS/ch, C20, SE
DT5720E	2 Ch.	12 bit 250 MS/s Digitizer: 10MS/ch, C20, SE
DPP Firmware		Description
DDP-PSD 2/4ch	DDP-PSD Digital Pulse Processing for Pulse Shape Discrimination (2/4ch x720)	
Related Products		Description
A2818	A2818 – PCI Optical Link (Rhos compliant)	
A3818A	A3818A – PCIe 1 Optical Link	
A3818B	A3818B – PCIe 2 Optical Link	
A3818C	A3818C – PCIe 4 Optical Link	
Accessories		Description
A318	SE to Differential Clock Adapter	
A654	Single Channel MCX to LEMO Cable Adapter	
A654 KIT4	4 MCX TO LEMO Cable Adapter	
A654 KIT8	8 MCX TO LEMO Cable Adapter	
A659	Single Channel MCX to BNC Cable Adapter	
A659 KIT4	4 MCX TO BNC Cable Adapter	
A659 KIT8	8 MCX TO BNC Cable Adapter	
AI2730	Optical Fibre 30 m simplex	
AI2720	Optical Fibre 20 m simplex	
AI2705	Optical Fibre 5 m simplex	
AI2703	Optical Fibre 30 cm simplex	
AY2730	Optical Fibre 30 m duplex	
AY2720	Optical Fibre 20 m duplex	
AY2705	Optical Fibre 5 m duplex	

Tab. 1.1: Table of models and related items

2 Block Diagram

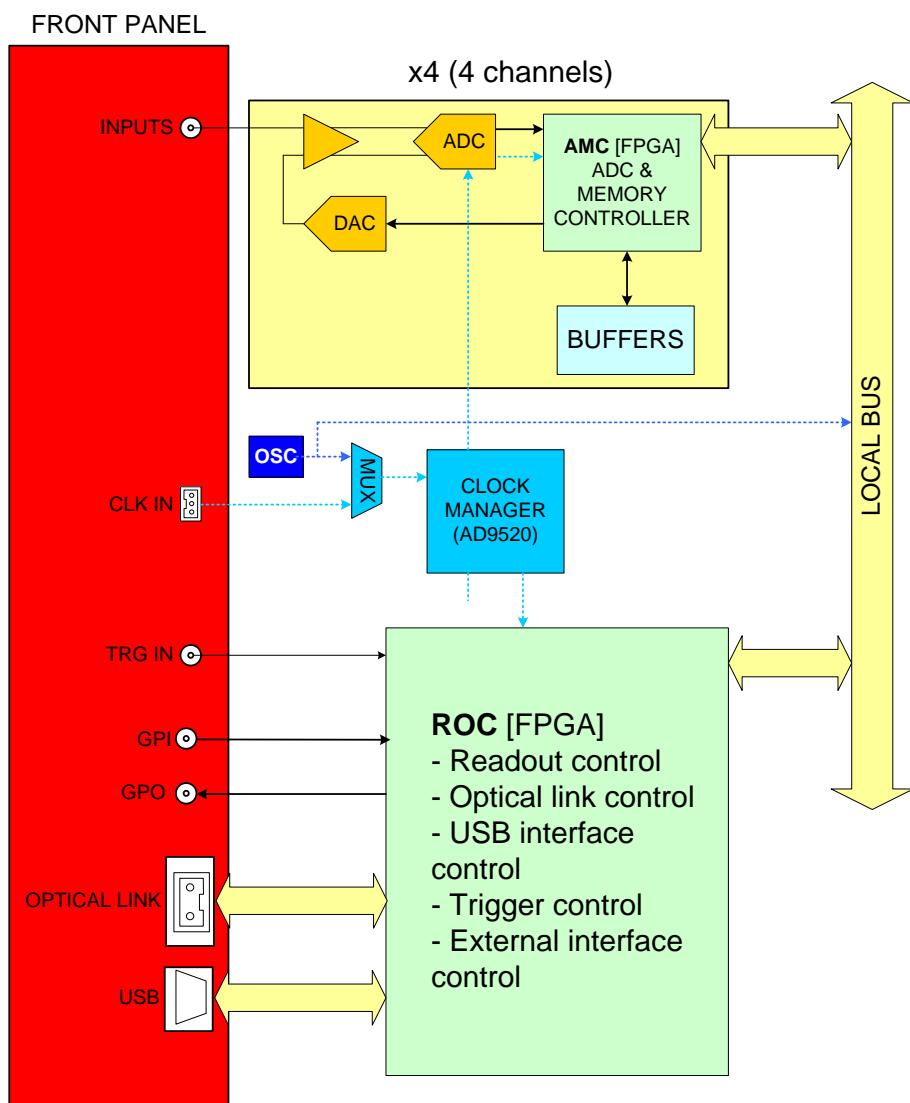


Fig. 2.1: Block Diagram

3 Technical Specifications

GENERAL	Form Factor: 154x50x164 mm ³ (WxHxD) Desktop	Weight 675 g	
ANALOG INPUT	Channels 2/4 channels Single ended	Connector MCX	Bandwidth 125 MHzMHz
	Impedance (Z_{in}) 50 Ω	Full Scale Range (FSR) 2 V _{pp}	Offset Programmable DAC for DC offset adjustment on each channel in the full range (± 1 V).
		Abs Max Rating 6 V _{pp} (with V _{rail} max +6 V or -6 V for any DAC offset value)	
DIGITAL CONVERSION	Resolution 12 bits	Sampling Rate 250 MS/s simultaneously on each channel	
SYSTEM PERFORMANCE	ENOB 10.14 (64 kS Buffer)	THD 74.1 dB	SIGMA 0.95 LSB rms (64 kS Buffer, open input)
	SINAD 62.85 dB	SFDR 82.0 dB	
ADC SAMPLING CLOCK GENERATION	Clock source: internal/external On-board programmable PLL provides generation of the main board clocks from an internal (50 MHz local Oscillator) or external (front panel CLK-IN connector) reference		
DIGITAL I/O	CLK-IN (AMP Modu II) AC coupled differential input clock LVDS, ECL, PECL, LVPECL, CML (single ended NIM/TTL to differential adapter available by A318 accessory) Jitter < 100 ppm requested	GPO (LEMO) General purpose digital output NIM/TTL, R _t = 50 Ω	
	TRG-IN (LEMO) External trigger digital input NIM/TTL, Z _{in} = 50 Ω	GPI (LEMO) SYNC/START General purpose digital input NIM/TTL, Z _{in} = 50 Ω	
MEMORY	1.25M sample/ch or 10M sample/ch (see Tab. 1.1) Multi Event Buffer divisible into 1 ÷ 1024 Independent read and write access Programmable event size and pre/post trigger		
TRIGGER	Trigger Source - <i>Self-trigger</i> : channel over/under-threshold for common (waveform recording firmware) or individual (DPP firmware only) trigger generation - <i>External-trigger</i> : common trigger by TRG IN connector or individual by LVDS connector (DPP firmware only) - <i>Software-trigger</i> : common trigger by software command	Trigger Propagation TRG-OUT programmable digital output	
		Trigger Time Stamp <i>Waveform recording FW</i> : 31-bit counter – 16 ns resolution - 17 s range; 48 bit fw extension <i>DPP-PSD</i> : 32-bit counter – 4 ns resolution - 17 s range; 47 bit fw extension; 64 bit sw extension	

ADC & MEMORY CONTR.	Altera Cyclone EP1C20 (one FPGA serves 1 channel)	
COMMUNICATION INTERFACE	Optical Link CAEN CONET proprietary protocol Up to 80 MB/s transfer rate Daisy-chain: it is possible to connect up to 8 or 32 ADC modules to a single Optical Link Controller (respectively A2818 or A3818)	USB USB 2.0 compliant Up to 30 MB/s transfer rate
SUPPORTED FIRMWARE	DPP-PSD for the Pulse Shape Discrimination	
FIRMWARE UPGRADE	Firmware can be upgraded via USB/Optical Link	
SOFTWARE	General purpose C libraries, configuration tools, readout software (Windows® and Linux® support). LabVIEW™ VIs and demos for Windows® only	
POWER CONSUMPTIONS	1.5A @ +12V (Typ.)	

Tab. 3.1: Specification table

4 Packaging and Compliancy

The unit is a Desktop module housed in an alloy box (weight: 675 g) with the following dimensions:

154 W x 50 H x 164 L mm³ (connectors not included)

154 W x 50 H x 171 L mm³ (including connectors).



Fig. 4.1: Model view

CAUTION: to manage the product, consult the operating instructions provided.



**A POTENTIAL RISK EXISTS IF THE OPERATING INSTRUCTIONS ARE
NOT FOLLOWED!**

CAEN provides the specific document “Precautions for Handling, Storage and Installation”, available in the documentation tab of the product’s web page, that is mandatory to read before operating with CAEN equipment.

5 Power Requirements

DT5720 module is powered by the external AC/DC stabilized power supply provided with the digitizer and included in the delivered kit.

The DT5720 typical power consumption is 1.5 A (@ +12 V).



Note: Using a different power supply source, like battery or linear type, it is recommended the source to provide +12 V and, at least, 2 A in case of DT5720; the power jack is a 2.1 mm type, a suitable cable is the RS 656-3816 type (or similar)



Fig. 5.1: AC/DC power supply provided with the module

6 Cooling Management

Starting from revision 4 of the hardware (readable at 0xF04C address of the Configuration ROM), the DT5720 features an automatic fan speed control to guarantee an appropriate cooling in consequence of internal temperature variations. The automatic control is managed by the ROC FPGA firmware from revision 4.4 on.

The user can manually set the fan speed through the bit[3] of the Fan Speed Control register.

Hardware revision \geq 4 and ROC FPGA firmware revision \geq 4.4:

- Bit[3] = 0 (default) sets the automatic fan speed control;
- Bit[3] = 1 sets HIGH the fan speed.

Hardware revision < 4 and ROC FPGA firmware revision < 4.4:

- Bit[3] = 0 (default) sets LOW the fan speed;
- Bit[3] = 1 sets HIGH the fan speed.

7 Panels Description

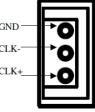


Fig. 7.1: Front panel view



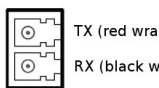
Fig. 7.2: Rear panel view

Front Panel

ANALOG INPUT		
	FUNCTION Input connectors from CH0 to CH3 receive the input analog signals.	MECHANICAL Specs Series: MCX connectors. Type: CS 85MCX-50-0-16. Manufacturer: SUHNER Suggested plug: MCX-50-2-16 type. Suggested cable: RG174 type.
CLOCK IN		
	FUNCTION Input and output connectors for the external clock.	MECHANICAL Specs Series: AMPMODU connectors. Type: 3-102203-4 (3-pin). Manufacturer: AMP Inc.
PINOUT 		
GPO 		
	FUNCTION General purpose programmable digital output connector to propagate: <ul style="list-style-type: none"> • the internal trigger sources; • the channel probes (i.e. signals from the mezzanines); • GPI signal according to register addresses 0x8110 and 0x811C, or • the motherboard probes (i.e. signals from the motherboard), like the Run signal, ClkOut signal, ClockPhase signal, PLL_Unlock signal or Busy signal according to register address 0x811C. ELECTRICAL Specs Signal level: NIM or TTL. Requires 50 Ω termination.	MECHANICAL Specs Series: 101 A 004 connectors. Type: DLP 101 A 004-28. Manufacturer: FISCHER. Alternatively: Type: EPL 00 250 NTN. Manufacturer: LEMO.

TRG-IN	FUNCTION Digital input connector for the external trigger.	MECHANICAL Specs Series: 101 A 004 connectors. Type: DLP 101 A 004-28. Manufacturer: FISCHER. Alternatively: Type: EPL 00 250 NTN. Manufacturer: LEMO.
	ELECTRICAL Specs Signal level: NIM or TTL. Input impedance (Z_{in}): 50 Ω.	

GPI	FUNCTION General purpose programmable input connector. Can be used to reset the time stamp (see Sec. Reset, Clear and Default Configuration) or to start/stop the acquisition.	MECHANICAL Specs Series: 101 A 004 connectors. Type: DLP 101 A 004-28. Manufacturer: FISCHER. Alternatively: Type: EPL 00 250 NTN. Manufacturer: LEMO.
	ELECTRICAL Specs Signal level: NIM or TTL. Input impedance (Z_{in}): 50 Ω.	

OPTICAL LINK PORT	FUNCTION Optical LINK connector for data readout and flow control. Daisy chainable. Compliant with Multimode 62.5/125 μm cable featuring LC connectors on both sides.	MECHANICAL Specs Series: SFF Transceivers. Type: FTLF8519F-2KNL (LC connectors). Manufacturer: FINISAR.
	ELECTRICAL Specs Transfer rate: up to 80 MB/s.	PINOUT  TX (red wrap) RX (black wrap)

LINK LEDs (GREEN/YELLOW): right LED (GREEN) indicates the network presence, while left LED (YELLOW) signals the data transfer activity.

USB PORT	FUNCTION USB connector for data readout and flow control.	MECHANICAL Specs Series: USB connectors. Type: 787780-2 (B-Type). Manufacturer: AMP Inc.
	ELECTRICAL Specs Standard: compliant with USB 2.0 and USB 1.0. Transfer rate: up to 30 MB/s.	

USB LINK LED (GREEN): indicates the USB communication is active.

DIAGNOSTICS LEDs	
	<p>DTACK (GREEN): indicates there is a read/write access to the board; PLL LOCK (GREEN): indicates the PLL is locked to the reference clock; PLL BYPS (GREEN): not used; RUN (GREEN): indicates the acquisition is running (data taking). See Sec. Acquisition Run/Stop; TRG (GREEN): indicates the trigger is accepted; DRDY (GREEN): indicates the event/data is present in the Output Buffer; BUSY (RED): indicates all the buffers are full for at least one channel.</p>

Rear Panel

SPARE LINK		
		FUNCTION
Auxiliary connector reserved for CAEN usage.		MECHANICAL Specs
ELECTRICAL Specs N/A		Series: Header connectors. Type: 7610-5002-5+5. Manufacturer: 3M.

DC INPUT		
		FUNCTION
Input connector for the desktop Digitizer main power supply from the external AC/DC adapter.		MECHANICAL Specs
ELECTRICAL Specs Typ. Input voltage: +12 VDC.		PINOUT
		

IDENTIFYING LABEL	
	<p>FUNCTION A blue label on the Desktop rear panel indicates:</p> <ul style="list-style-type: none"> - the model; - the serial number (S/N); - the symbol of the CE conformity marking.

8 Functional Description

Analog Input Stage

Input dynamic is 2 V_{pp} . In order to preserve the full dynamic range with unipolar input signal, positive or negative, it is possible to add a DC offset by means of a 16 bit DAC, which is up to $\pm 1 \text{ V}$. The input bandwidth ranges from DC to 125 MHz (with 2nd order linear phase anti-aliasing low pass filter).

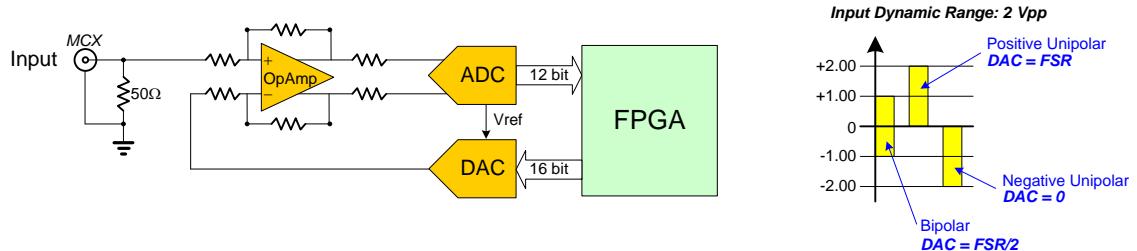


Fig. 8.1: Analog input diagram

DC Offset Individual Setting

Setting the DC offset for channel n requires a write access at register addresses 0x1n98. Writing at 0x8098, the DC offset will apply to all channels at once. Refer to [RD1] for more details.

Clock Distribution

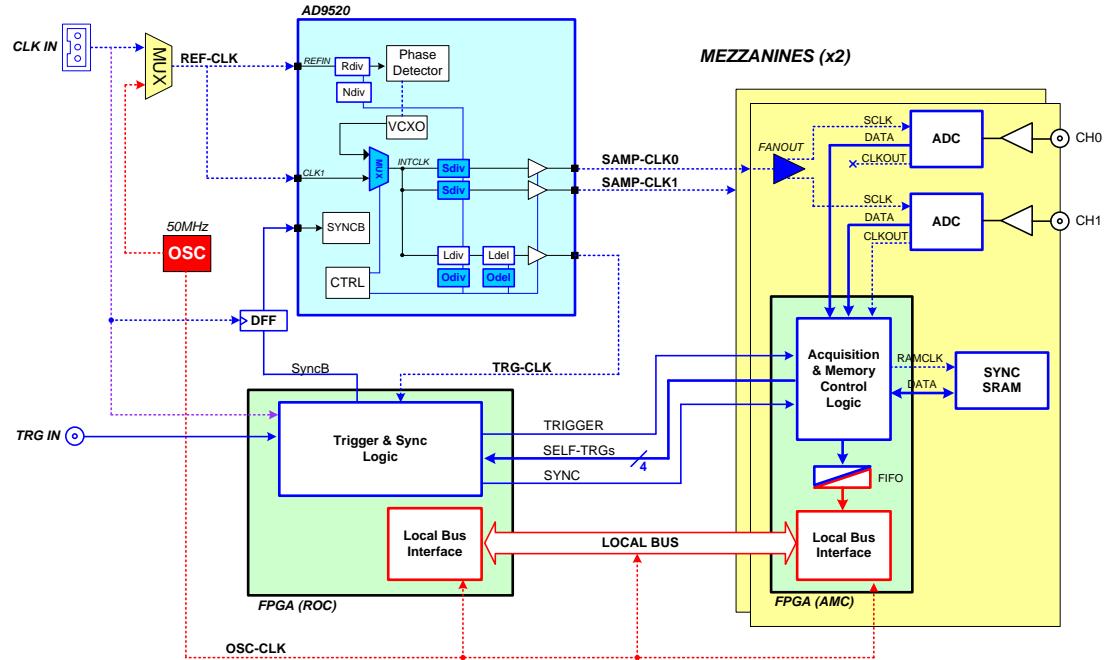


Fig. 8.2: Clock distribution diagram

The clock distribution of the module takes place on two domains: OSC-CLK and REF-CLK.

OSC-CLK is a fixed 50-MHz clock coming from a local oscillator which handles USB, Optical Link and Local Bus, that takes care of the communication between motherboard and mezzanines (see red traces in Fig. 8.2).

REF-CLK handles ADC sampling, trigger logic, and acquisition logic (samples storage into RAM, buffer freezing on trigger) through a clock chain. REF-CLK can be either an external (via the front panel CLK-IN connector) or an internal (via the 50-MHz local oscillator) source. In the latter mode, OSC-CLK and REF-CLK will be synchronous (the operation mode remains the same).

REF-CLK clock source selection can be done by writing bit[6] of register 0x8100 [RD1] between the following modes:

- INT mode (default) means REF-CLK is the 50 MHz of the local oscillator (REF-CLK = OSC-CLK);
- EXT mode means REF-CLK source is the external frequency fed on CLK-IN connector.

The external clock signal must be differential (LVDS, ECL, PECL, LVPECL, CML) with a jitter lower than 100 ppm (see Chap. **Technical Specifications**). CAEN provides the A318 cable to adapt single ended signals coming from an external clock unit into the differential CLK-IN connector (see Tab. 1.1).

The DT5720 is equipped with a phase-locked-loop (PLL) and clock distribution device, AD9520. It receives the REF-CLK and generates the sampling clock for ADCs and the mezzanine FPGA (SAMP-CLK0 and SAMP-CLK1), as well as the trigger logic synchronization clock (TRG-CLK) and the output clock (CLK-OUT).

AD9520 configuration can be changed and stored into non-volatile memory. Changing the AD9520 configuration is primarily intended to be used for external PLL reference clock frequency change (see Sec. **PLL Mode**). The DT5720 locks to an external 50 MHz reference clock with default AD9520 configuration.

Refer to the AD9520 datasheet for more details:

http://www.analog.com/static/imported-files/data_sheets/AD9520-3.pdf

(in case the active link above does not work, copy and paste it on the internet browser)

PLL Mode

The Phase Detector within the AD9520 device allows to couple REF-CLK with an internal VCXO, which provides the nominal ADCs frequency (250 MS/s).

As introduced in Sec. **Clock Distribution**, the source of the REF-CLK signal (see Fig. 8.2) can be external on CLK-IN front panel connector or internal from the 50 MHz local oscillator.

The following options are allowed:

1. 50 MHz internal clock source - this is the standard operation mode: the AD9520 dividers do not require to be reprogrammed (the digitizer works in the AD9520 default configuration). The clock source selection bit (bit[6] of 0x8100 [**RD1**]) is in default INT mode. REF-CLK = OSC-CLK.
2. 50 MHz external clock source - in this case, the clock source is taken from an external device; the AD9520 dividers do not need to be reprogrammed as the external frequency is the same as the default one. The clock source selection bit (bit[6] of 0x8100 [**RD1**]) must be set in EXT mode. CLK-IN = REF-CLK = OSC-CLK.
3. External clock source different from 50 MHz - the clock source is externally provided as in point 2, but the AD9520 dividers must now be reprogrammed to lock the the VCXO to the new REF-CLK in order to provide out the nominal sampling frequency at 250 MS/s. The clock source selection bit (bit[6] of 0x8100 [**RD1**]) must be set in EXT mode. CLK-IN = REF-CLK ≠ OSC-CLK.

If the digitizer is locked, the PLL-LOCK front panel LED must be on.



Note: the user who wants to work as in point 3, please contact CAEN (see Chap. **Technical Support**) indicating the required reference clock frequency, to check its feasibility and then receive the PLL programming file. The “Upgrade PLL” function in CAENUpgrader software tool can be used to update the digitizer PLL [**RD3**].

Reducing the Sampling Frequency

In case the board is required to work at a sampling frequency (SAMP-CLK) lower than the nominal, it can be achieved by reprogramming the AD9520 dividers. REF-CLK can be configured as in Sec. **PLL Mode**. Not all the frequencies are admitted and a lower frequency limit must be considered, due to the internal electronics. Please contact CAEN (see Sec. **Technical Support**) to check the feasibility.

Trigger Clock

The TRG-CLK logic works at 125 MHz, equal to the sampling frequency: TRG-CLK = SAMPL-CLK.

Acquisition Modes

Acquisition Run/Stop

The acquisition can be started and stopped in different ways, according to bits[2:0] of register 0x8100 [**RD1**]:

- SW CONTROLLED (bits[1:0] = 00): Start and Stop take place by software command. Bit[2] = 0 means stopped, while bit[2] = 1 means running.
- GPI CONTROLLED (bits[1:0] = 01): bit[2] = 1 arms the acquisition and the Start is issued as the GPI signal is set high and the Stop occurs when it is set low. If bit[2] = 0 (disarmed), the acquisition is always off.
- FIRST TRIGGER CONTROLLED (bits[1:0] = 10): bit[2] = 1 arms the acquisition and the Start is issued on the first trigger pulse (rising edge) on the TRG-IN connector. This pulse is not used as a trigger; actual triggers start from the second pulse on TRG-IN. The Stop acquisition must be SW controlled (i.e. reset of bit[2]).

Acquisition Triggering: Samples and Events

When the acquisition is running, a trigger signal allows to:

- store a 31-bit counter value of the Trigger Time Tag (TTT).
The counter (representing a time reference), like the Trigger Logic Unit (see Fig. 8.2), operates at a frequency of 125 MHz (i.e. 8 ns, that is to say 2 ADC clock cycles). Due to the way acquired data is written into the board internal memory (i.e. in 4-sample bunches), the TTT counter is read every 2 trigger logic clock cycles, which means the trigger time stamp resolution results in 16 ns (i.e. 62.5 MHz). Basing on that, the LSB of the TTT is always "0";
- increment the EVENT COUNTER;
- fill the active buffer with the pre/post-trigger samples, whose number is programmable via register address 0x8114 [**RD1**]; the acquisition window width (also referred to as record length) is determined via register addresses 0x800C and 0x8020; then, the buffer is frozen for readout purposes, while the acquisition continues on another buffer.

An event is therefore composed by the trigger time tag, pre- and post-trigger samples and the event counter.

Overlap between “acquisition windows” may occur (a new trigger occurs while the board is still storing the samples related to the previous trigger); this overlap can be either rejected or accepted (programmable via software).

If the board is programmed to accept the overlapping triggers (by writing at register address 0x8000 [**RD1**]), as the overlapping trigger arrives, the current active buffer is filled up, then the samples storage continues on the subsequent one. In this case, not all events will have the same size (see Fig. 8.3).

A trigger can be refused for the following causes:

- Acquisition is not active.
- Memory is FULL and therefore there are no available buffers.
- The required number of samples for building the event pre-trigger is not reached yet; this happens typically as the trigger occurs too early either with respect to the RUN Acquisition command (see Sec. **Acquisition Run/Stop**) or with respect to a buffer emptying after a Memory FULL status (see Sec. **Acquisition Synchronization**).
- The trigger overlaps the previous one and the board is not enabled for accepting overlapped triggers.

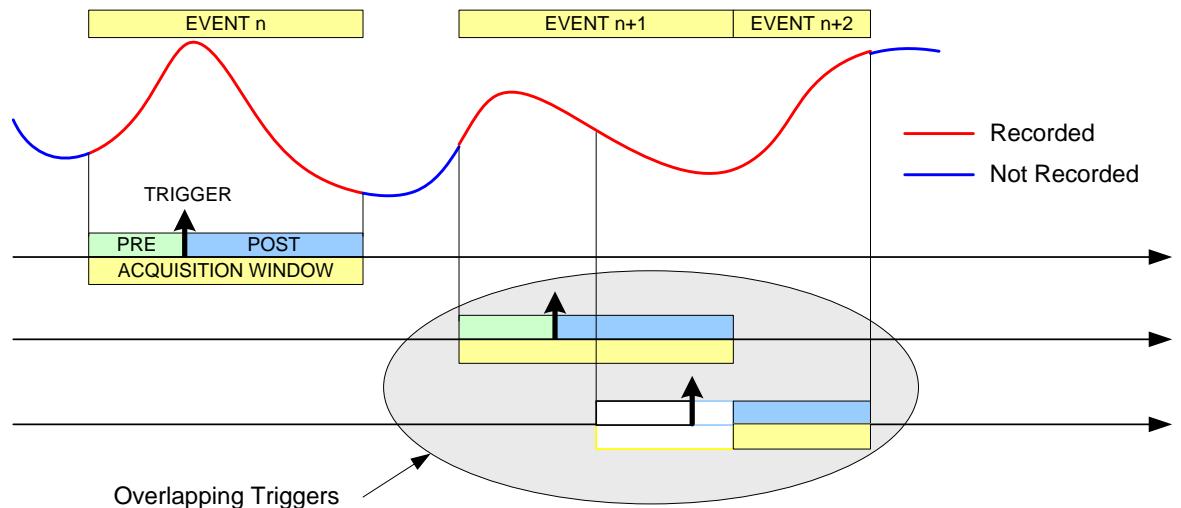


Fig. 8.3: Trigger Overlap

As a trigger is refused, the current buffer is not frozen and the acquisition continues writing on it. The EVENT COUNTER can be programmed in order to be either incremented or not. If this function is enabled, the EVENT COUNTER value identifies the trigger number sent (but the event number sequence is lost); if the function is not enabled, the EVENT COUNTER value coincides with the sequence of buffers saved and readout.

Multi-Event Memory Organization

Each channel of the DT5720 features a SRAM memory to store the acquired events. The memory size in the standard event storage mode is 1 MS (1.25 MS in Pack2.5 mode) or 8 MS (10 MS in Pack2.5 mode), according to the board version (see Tab . 1.1). The channel memory can be divided in a programmable number of buffers, N_b (N_b from 1 up to 1024), by the register address 0x800C [RD1], as described in Tab. 8.1.



Note: in case of Pack2.5 reading mode, values must be multiplied by 5/4.

Register Value	Number of Buffers (N_b)	Size of one Buffer	
		SRAM 1.25 MB/ch (1 MS)	SRAM 10 MB/ch (8 MS)
0x00	1	1.25 MB/ch (1 MS)	10 MB/ch (8 MS)
0x01	2	640 kB/ch (512 kS)	5 MB/ch (4 MS)
0x02	4	320 kB/ch (256 kS)	2.5 MB (2 MS)
0x03	8	160 kB/ch (128 kS)	1.25 MB/ch (1 MS)
0x04	16	80 kB/ch (64 kS)	640 kB/ch (512 kS)
0x05	32	40 kB/ch (32 kS)	320 kB/ch (256 kS)
0x06	64	20 kB/ch (16 kS)	160 kB/ch (128 kS)
0x07	128	10 kB/ch (8 kS)	80 kB/ch (64 kS)
0x08	256	5 kB/ch (4 kS)	40 kB/ch (32 kS)
0x09	512	2.5 kB/ch (2 kS)	20 kB/ch (16 kS)
0x0A	1024	1.25 kB/ch (1 kS)	10 kB/ch (8 kS)

Tab. 8.1: Buffer organization of 720 family series. For each value of buffer size it is reported the memory size and the number of samples of one buffer, where $k = 1024$ and $M = 1024 \cdot 1024$.

Having 1 MS memory size as reference, this means that each buffer contains $1M/N_b$ samples (e.g. $N_b = 1024$ means 1024 samples in each buffer).

Custom size events

In case an event size less than the buffer size is needed, the user can set the N_{LOC} value at register address 0x8020 [RD1], where N_{LOC} is the number of memory locations. The size of the event is so forced to be according to the formula:

$$1 \cdot N_{LOC} = 4 \cdot N_{Sample} \text{ (normal mode)}$$

$$1 \cdot N_{LOC} = 5 \cdot N_{Sample} \text{ (Pack2.5 mode)}$$

When $N_{LOC} = 0$ the custom size is disabled.



Note: The value of N_{LOC} must be set in order that the relevant number of samples does not exceed the buffer size and it must not be modified while the acquisition is running. Even using the custom size setting, the number of buffers and the buffer size are not affected by N_{LOC} , but they are still determined by N_b .

The concepts of buffer organization and custom size directly affect the width of the acquisition window (i.e. number of the digitized waveform samples per event). The Record Length parameter defined in CAEN software (such as WaveDump and CAENScope introduced in Chap. **Software Tools**) and the `Set/GetRecordLength()` functions of the CAENDigitizer library (see Sec. **Libraries**) rely on these concepts.

Event structure

The event can be readout via USB or Optical Link; data format is 32-bit long word (see Fig. 8.4).

An event is structured as:

- **Header** (four 32-bit words)
- **Data** (variable size and format)

Header

The Header consists of four words including the following information:

- **EVENT SIZE** (bits[27:0] of 1st header word) is the total size of the event, i.e. the number of 32-bit long words to be read.
- **BOARD FAIL FLAG** (bit[26] of 2nd header word) implemented from ROC FPGA firmware revision 4.5 on (reserved otherwise), it is set to “1” in consequence of a hardware problem (e.g. PLL unlocking). The user can collect more information about the cause by reading at register address 0x8104 and contact CAEN Support Service if necessary (see Chap. **Technical Support**).
- **TRG OPTIONS** (bits[23:8] of 2nd header word); starting from revision **4.6** of the ROC FPGA firmware (reserved otherwise), these 16 bits can be programmed to provide trigger information according to the setting of the bits[22:21] at register address 0x811C (see Tab 8.2).

REGISTER 0x811C Bits[22:21]	FUNCTIONAL DESCRIPTION	Reserved /TRG OPTIONS INFORMATION (16 bits in the 2 nd header word)
00 (default)	Reserved	Must be 0 .
01	Event Trigger Source	Indicates the trigger source causing the event acquisition: Bits[23:19] = 00000 Bit[18] = Software Trigger Bit[17] = External Trigger Bit[16:12] = 000000 Bits[11:8] = Channel self-trigger (refer to Sec. Self-Trigger).
10	Extended Trigger Time Tag (ETTT)	A 48-bit Trigger Time Tag (ETTT) information is configured, where Bits[23:8] contributes as the 16 most significant bits together to the 32-bit TTT field (4 th header word). Note: in the ETTT option, the overflow bit is not provided.
11	Not used	If configured, it acts like “00” setting.

Tab. 8.2: Reserved/Trg Options configuration table.

- **CHANNEL MASK** (bits[3:0] of 2nd header word) is the mask of the channels participating in the event (e.g. CH0 and CH2 participating → Channel Mask = 0x3). This information must be used by the software to acknowledge from which channel the samples are coming (the first event contains the samples from the channel with the lowest number).
- **EVENT COUNTER** (bits[23:0] of 3rd header word) is the trigger counter; it can count either accepted triggers only, or all triggers (bit[3] of register address 0x8100).
- **trigger TIME TAG** (bits[31:0] of 4th header word) is the 31-bit Trigger Time Tag (TTT) information (31 bit counter and 32nd bit as roll-over flag), which is the trigger time reference. If the ETTT option is enabled, then this field becomes the 32 less significant bits of the 48-bit Extended Trigger Time Tag

information in addition to the 16 bits (MSB) of the TRG OPTIONS field (2nd event word). Note that, in the ETTT case, the roll-over flag is no more provided. The trigger time tag is reset either at the start of acquisition, or via front panel signal on S-IN or LVDS I/O connectors, and increments with 250 MHz frequency (i.e. every 2 ADC clock cycles). The TTT value is read at half the frequency (i.e. 125 MHz) so that the specifications are 16 ns resolution and 17 s range ($8 \text{ ns} \times (2^{31}-1)$), which can be extended to 625 h ($8 \text{ ns} \times (2^{48}-1)$) if ETTT is enabled.

Data

Data are the stored samples. Data from masked channels are not read.

Event Format Examples

The event can be stored in the board memory in two ways by setting bit[11] of register 0x8000 [RD1]:

- Standard Mode: data format is 32 bit long word, and each long_word may contain 2 samples;
- Pack2.5 Mode: data format is 32 bit long word, and each long_word may contain “two and a half” samples.

Specific examples are reported in Fig. 8.4 and 8.5 respectively.

The data format modifies when the Zero Length Encoding is enabled. Refer to Figs. 8.6 and 8.7 for more details.

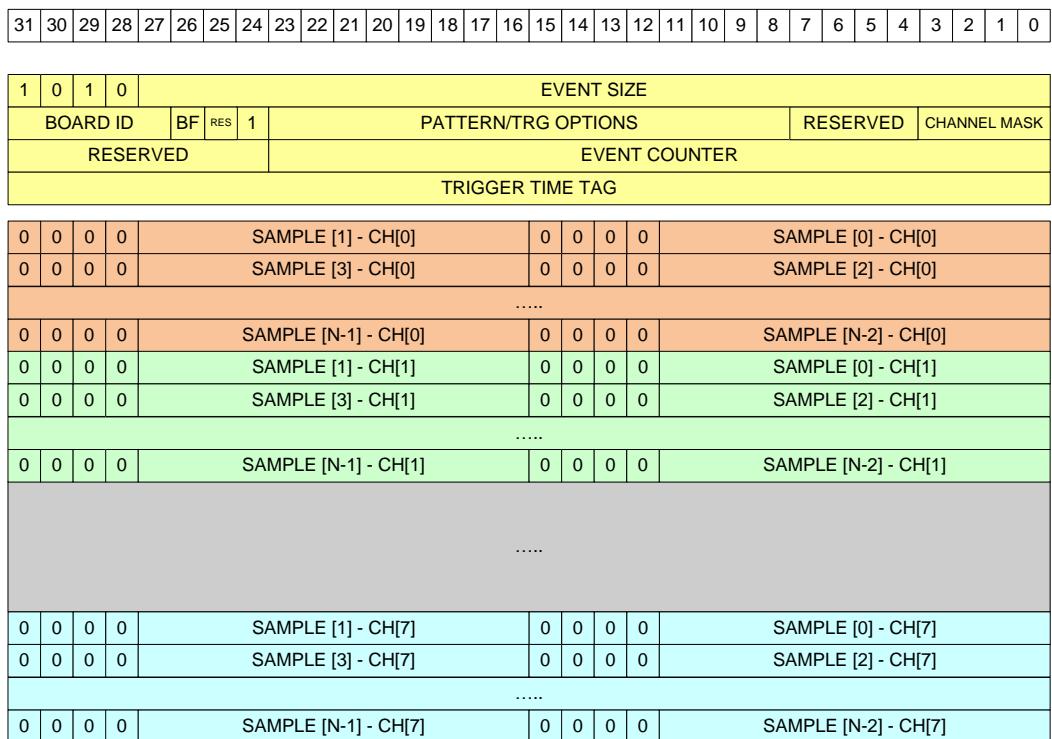


Fig. 8.4: Event Format in Standard Mode

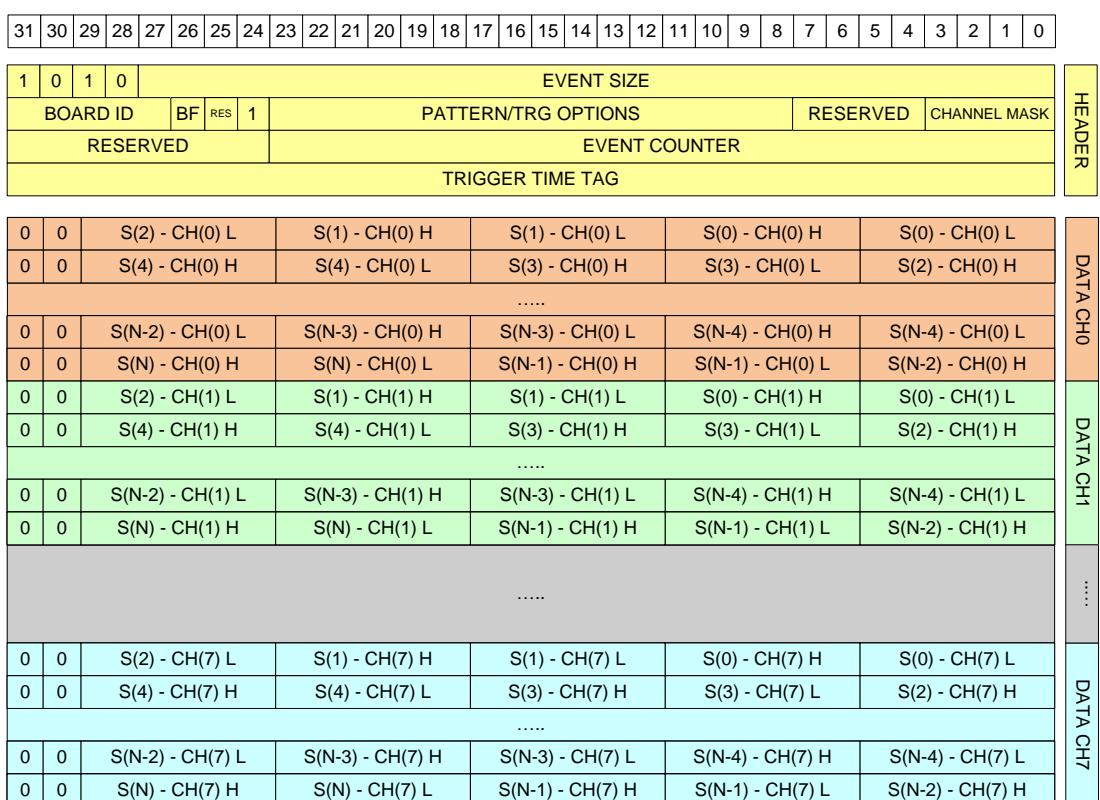


Fig. 8.5: Event Format in Pack2.5 Mode

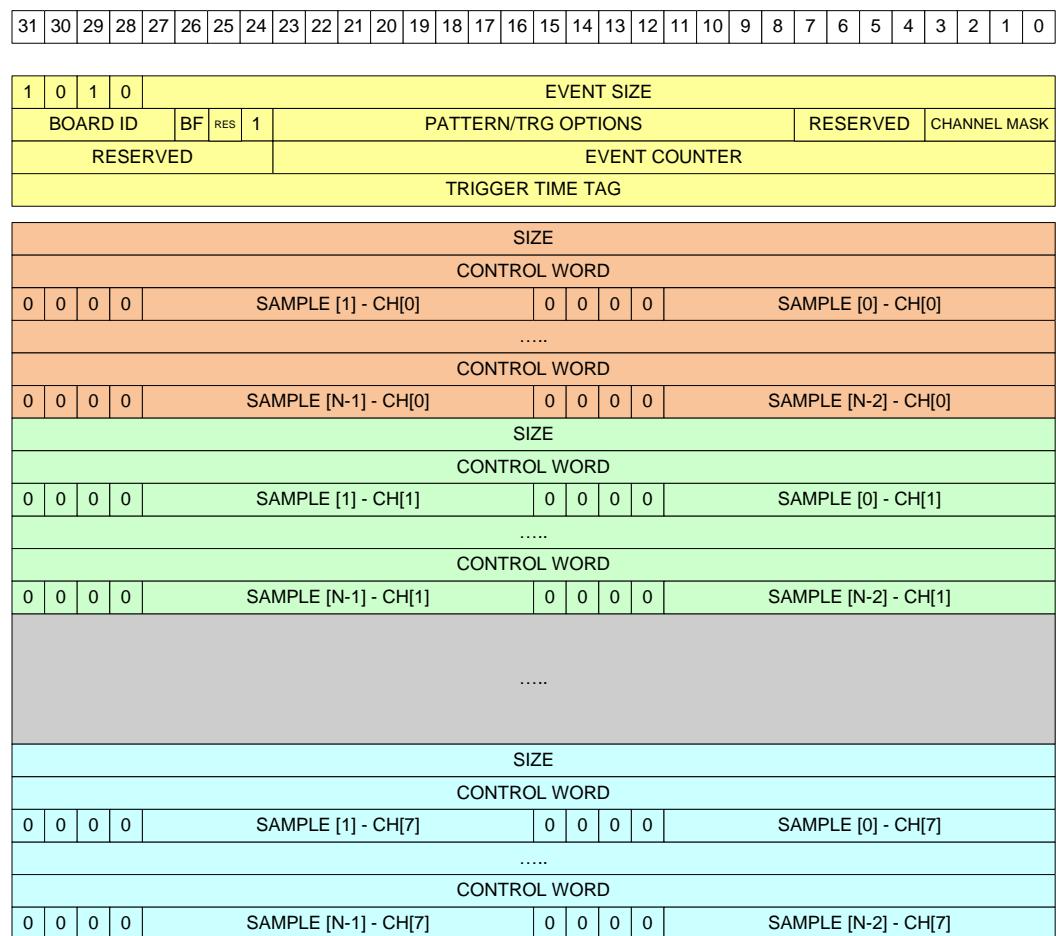


Fig. 8.6: Event Format in Standard Mode (Zero Length Encoding enabled)

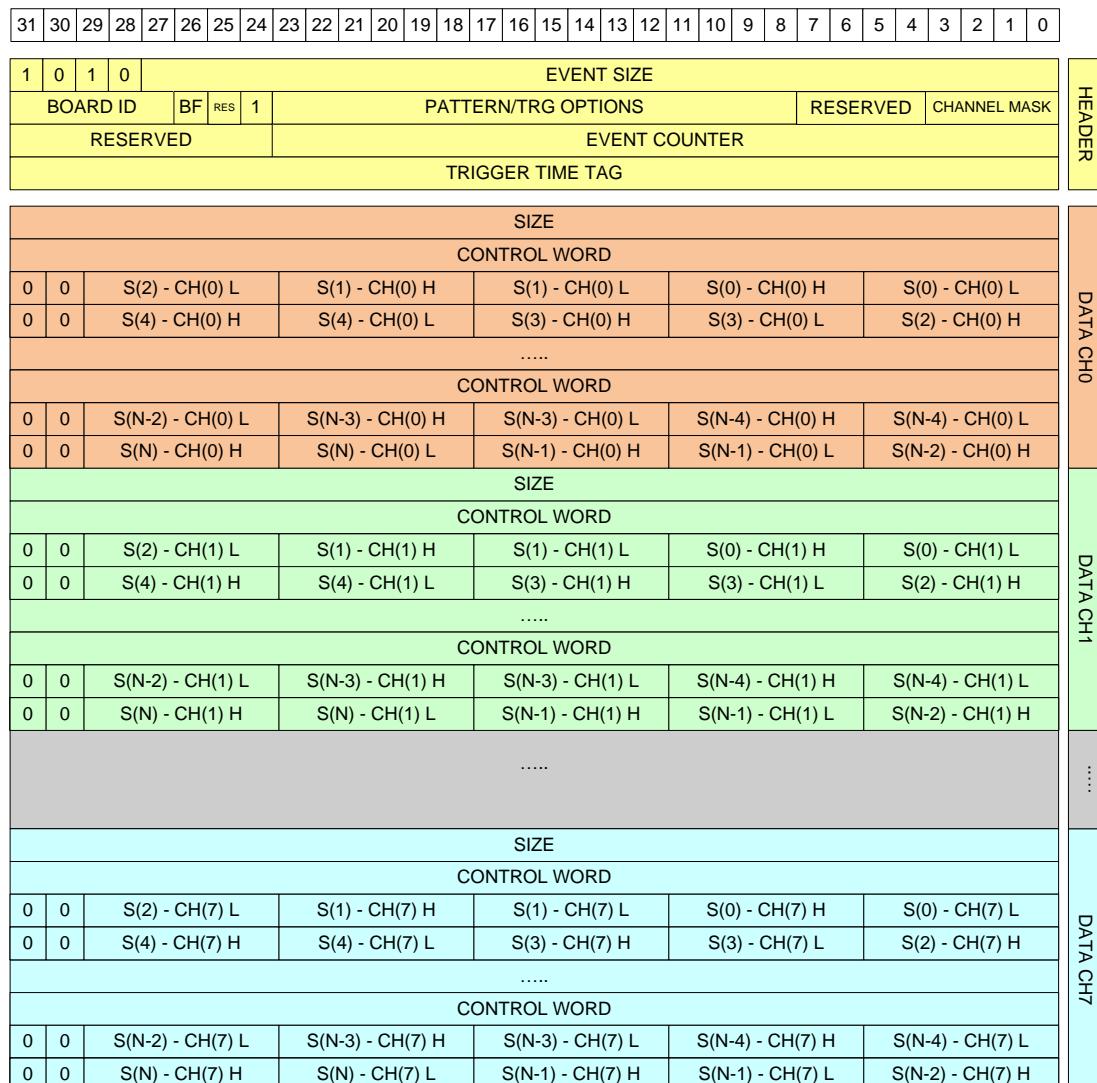


Fig. 8.7: Event Format in Pack2.5 Mode (Zero Length Encoding enabled)

Acquisition Synchronization

Each channel of the digitizer is provided with a SRAM memory that can be organized in a programmable number N_b of circular buffers ($N_b = [1 : 1024]$, see Tab. 8.1). When the trigger occurs, the FPGA writes further a programmable number of samples for the post-trigger and freezes the buffer, so that the stored data can be read via USB or Optical Link. The acquisition can continue in a new buffer.

When all buffers are filled, the board is considered FULL: no trigger is accepted and the acquisition stops (i.e. the samples coming from the ADC are not written into the memory, so they are lost). As soon as one buffer is read out and freed, the board exits the FULL condition and acquisition restarts.

IMPORTANT: When the acquisition restarts, no trigger is accepted until at least the entire buffer is written. This means that the dead time is extended for a certain time (depending on the size of the acquisition window) after the board exits the FULL condition.

A way to eliminate this extra dead time is by setting bit[5] = 1 at register address 0x8100 [**RD1**]. The board is so programmed to enter the FULL condition when $N_b - 1$ buffers are filled: no trigger is then accepted, but samples writing continues in the last available buffer. As soon as one buffer is read out and becomes free, the boards exits the FULL condition and can immediately accept a new trigger. This way, the FULL reflects the BUSY condition of the board (i.e. inability to accept triggers).



Note: when bit[5] = 1, the minimum number of circular buffers to be programmed is $N_b = 2$.

In some cases, the BUSY propagation from the digitizer to other parts of the system has some latency and it can happen that one or more triggers occur while the digitizer is already FULL and unable to accept those triggers. This condition causes event loss and it is particularly unsuitable when there are multiple digitizers running synchronously, because the triggers accepted by one board and not by other boards cause event misalignment.

In these cases, it is possible to program the BUSY signal to be asserted when the digitizer is close to FULL condition, but it has still some free buffers (Almost FULL condition). In this mode, the digitizer remains able to accept some more triggers even after the BUSY assertion and the system can tolerate a delay in the inhibit of the trigger generation. When the Almost FULL condition is enabled by setting the Almost FULL level to "X" (register address 0x816C [**RD1**]), the BUSY signal is asserted as soon as X buffers are filled, although the board still goes FULL (and rejects triggers) when the number of filled buffers is N_b or $N_b - 1$, depending on bit[5] at register address 0x8100 as above described.

It is possible to provide the BUSY signal on the digitizer front panel GPO output (bit[20], bits[19:18] and bits[17:16] of register address 0x811C are involved [**RD1**]).

Zero Suppression

In the x720 boards it is possible to select the events according to a "Zero Suppression" criterion. The zero suppression allows the user to reduce the amount of data transferred from the board by transferring only the useful information. Anyway, since the zero suppression condition is verified during the readout phase, this might imply a latency in the readout. All events are acquired with the common trigger and saved into the board memory. During the readout the FPGA analyses the event and transfers it when the zero suppression condition is verified.

Three types of zero suppression algorithms are implemented in the 720 digitizer series:

- Full Suppression based on the signal amplitude (ZS_AMP).
- Zero Length Encoding (ZLE).

The user can select the zero suppression algorithm by setting bits[19:16] of register 0x8000 **[RD1]**.

Full Suppression based on the Amplitude of the Signal

Full Suppression based on the signal amplitude (ZS_AMP) allows the user to discard data from one channel if the signal does not exceed the programmed threshold for at least Ns subsequent data. Threshold and Ns can be defined through registers 0x1n24 and 0x1n28 respectively [RD1], and Ns is programmable specifically by register address 0x1n28.

It is also possible to define a logic of acquisition according to bit[31] of register 0x1n24. In case of positive logic, the condition is met when the data is over threshold; in case of negative logic, the condition is met when the data is under threshold.

Fig. 8.8 shows an example of ZS_AMP in case of 4 channels. Channel 0 and channel 2 are over ZS_Threshold (T_{AMP}) for at least N_{s} samples (N_{OVT}) and the corresponding channels are written in the output data. Samples from channel 1 are not over-threshold, and samples from channel 3 are over-threshold for less than N_{s} samples. The latter two channels are not recorded.

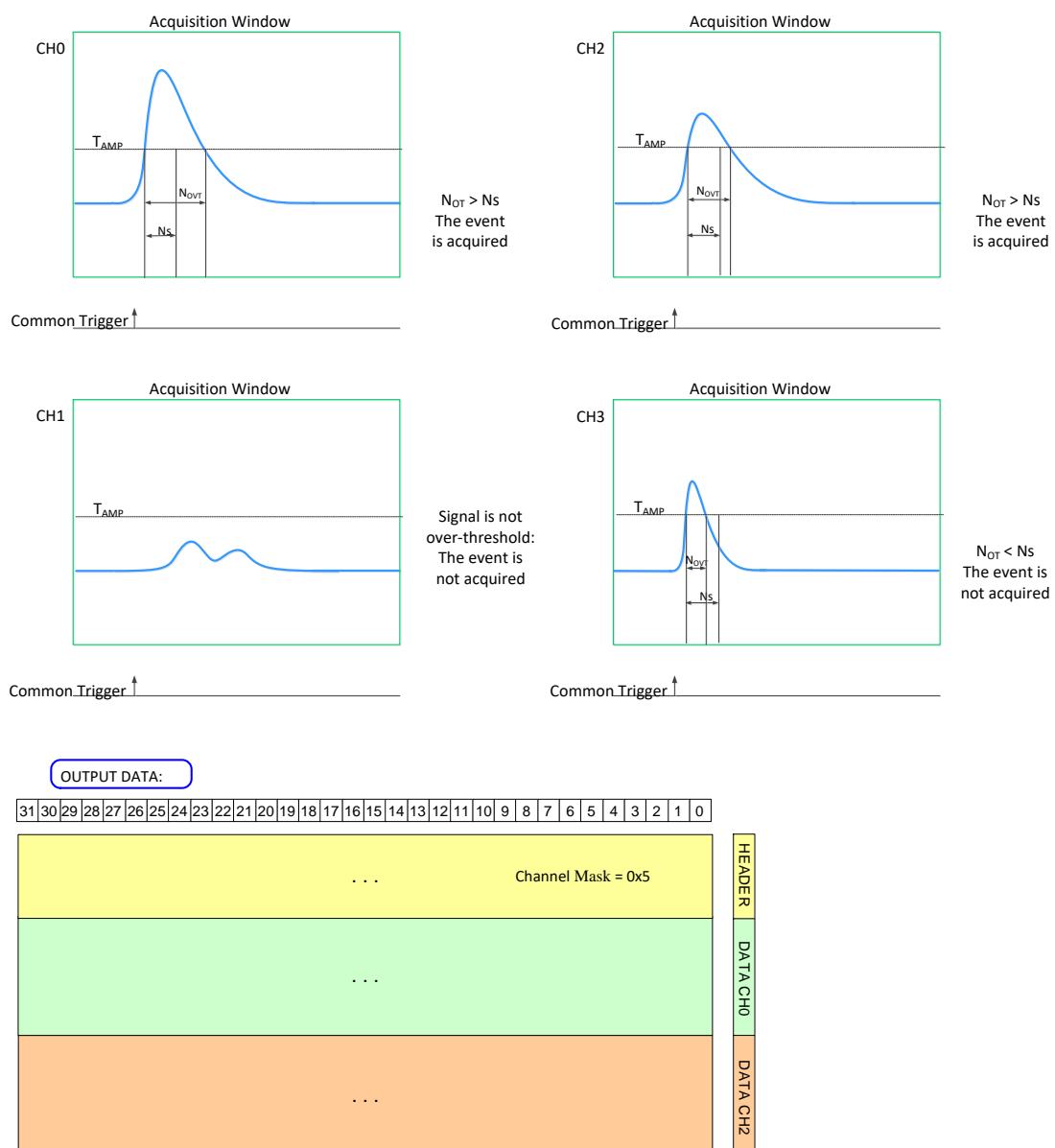


Fig. 8.8: Zero Suppression based on the amplitude.

Zero Length Encoding ZLE

Once the event is acquired, the Zero Length Encoding mode is able to tag the samples as "good" or "skipped". Samples are defined as "good" if they are over/under threshold according to the logic polarity (see bit[31] of register 0x1n24 [RD1]). "Skipped" events are those under/over the threshold and they are rejected. Only the number of skipped events is reported in the output data.

It is also possible to acquire data before the signal crosses the threshold (N_{LBK} , look back) and/or data after the over-threshold (N_{LFWD} , look forward). Those samples are tagged as good and reported in the output data. N_{LBK} and N_{LFWD} can be set through register 0x1n24 .

The channel event format in ZLE mode has the following structure:

- **Total size of the event (total number of transferred data per channel)**
- **Control word**
- [stored valid data if control word is "good"]
- ...

The total size is the number of 32-bit data that compose the event (including the size itself).

The control word has the following format:

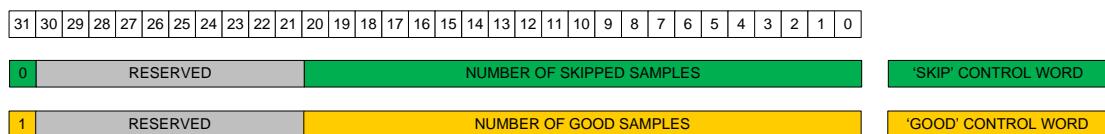


Fig. 8.9: Control Word format.

A "good" control word is followed by as many sample words as those indicated in the "number of good samples" field; if the control word type is "skip", then it is followed by a "good" control word, unless the end of event is reached.



Note: The maximum allowed number of control words is 62 (14 for mezzanine FPGA release 0.6 and earlier); therefore the ZLE is active until the 62th transition between a "good"/"skip" zone is reached. All the subsequent samples are considered "good" and stored.

Fig. 8.10 shows an example of Zero Length Encoding with positive logic. The top picture shows the skipped and good areas (N_{SKIP} and N_{GOOD}). Within the good area there are the samples back, the over-threshold and the samples forward (N_{LBK} , N_{OVTH} , and N_{LFWD} respectively). The bottom figure shows the corresponding event structure.

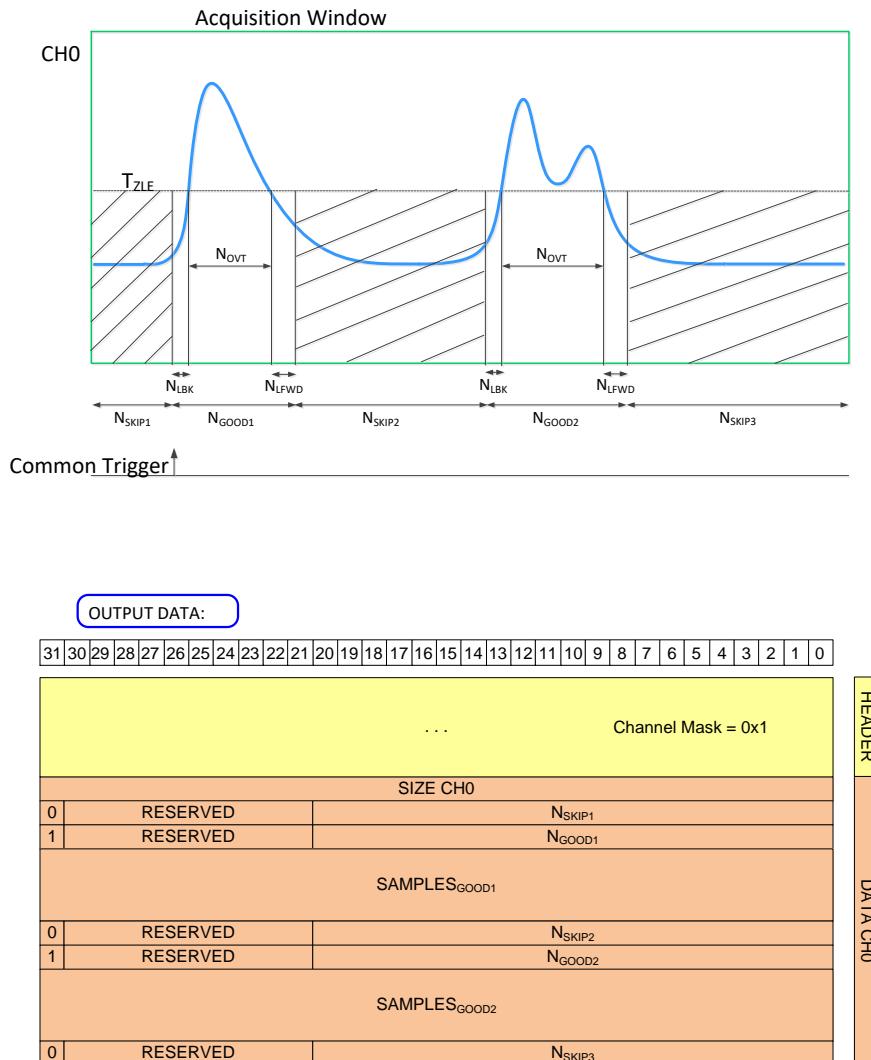


Fig. 8.10: Zero Suppression based on the Zero Length Encoding.

ZLE Examples

This section reports some examples of ZLE.

1. In the simplest case N_{LBK} and N_{LFWD} do not overlap. Fig. 8.11 reports the case of positive logic on the left, and negative logic on the right. The green areas correspond to the over threshold samples, while the yellow ones correspond to the under threshold samples:

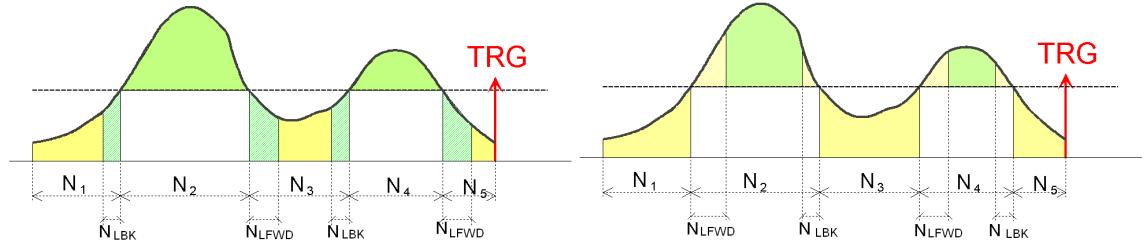


Fig. 8.11: Example of non-overlapping N_{LBK} and N_{LFWD} in case of positive logic (left) and negative logic (right).

The corresponding channel data is as follows.

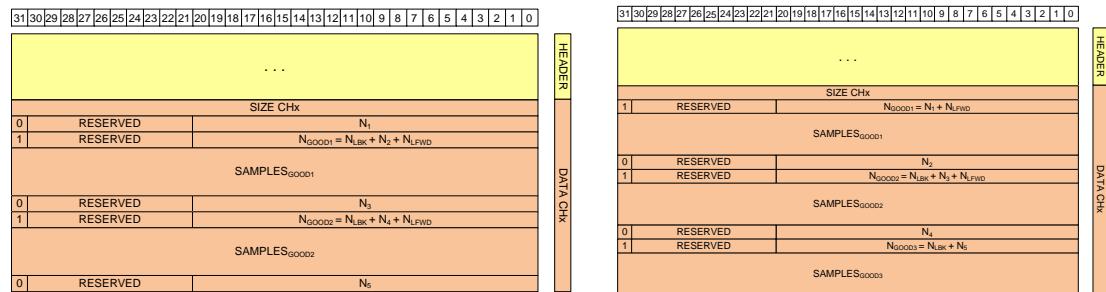


Fig. 8.12: Event format for non-overlapping N_{LBK} and N_{LFWD} .in case of positive logic (left) and negative logic (right).

2. In some cases the number of data to be discarded can be smaller than N_{LBK} and N_{LFWD} :
For example, consider the case where $N_1 \leq N_{LBK} < N_3$ and $N_{LFWD} = 0$ (positive logic) as reported in Fig. 8.13. The corresponding event format is reported on the right. All N_1 samples are tagged as good and acquired.



Note: The same example can be easily generalized for negative polarity.

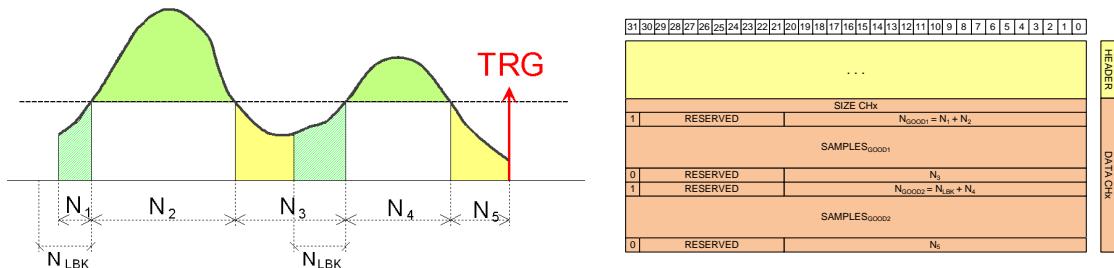


Fig. 8.13: Example with positive logic, N_{LBK} overlapping with N_1 , and $N_{LFWD} = 0$.

Analogously, in case $N_{LBK} = 0$ and N_{LFWD} overlaps with N_5 ($N_5 \leq N_{LFWD} < N_3$), all samples of N_5 are tagged as good and acquired ($N_{GOOD2} = N_4 + N_5$).

3. Consider the case where N_{LBK} overlaps with N_3 ($N_3 \leq N_{LBK} < N_1$) and $N_{LFWD} = 0$. In this case all samples of N_3 are tagged as good and acquired. See for example Fig. 8.14. The same happens in case $N_{LBK} = 0$ and $N_3 \leq N_{LFWD} < N_5$.



Note: In this case there are two subsequent “GOOD” intervals.

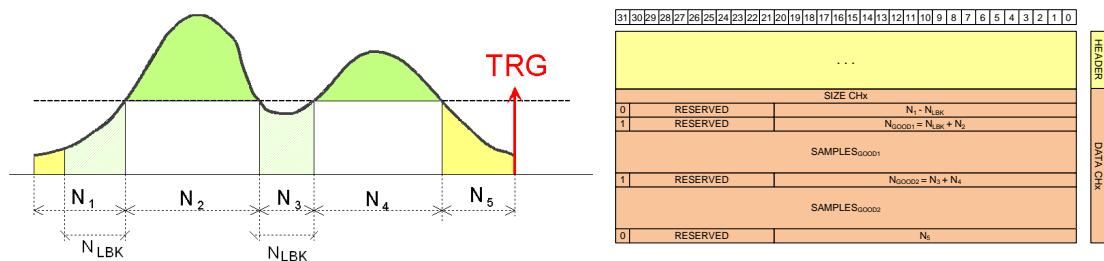


Fig. 8.14: Example with positive logic and N_{LBK} overlapping with N_3 .

Trigger Management

When operating the waveform recording firmware, all board channels share the same trigger (board common trigger), so they acquire an event simultaneously and in the same way (determined number of samples according to buffer organization and custom size settings, as well as position with respect to the trigger defined by the post-trigger).

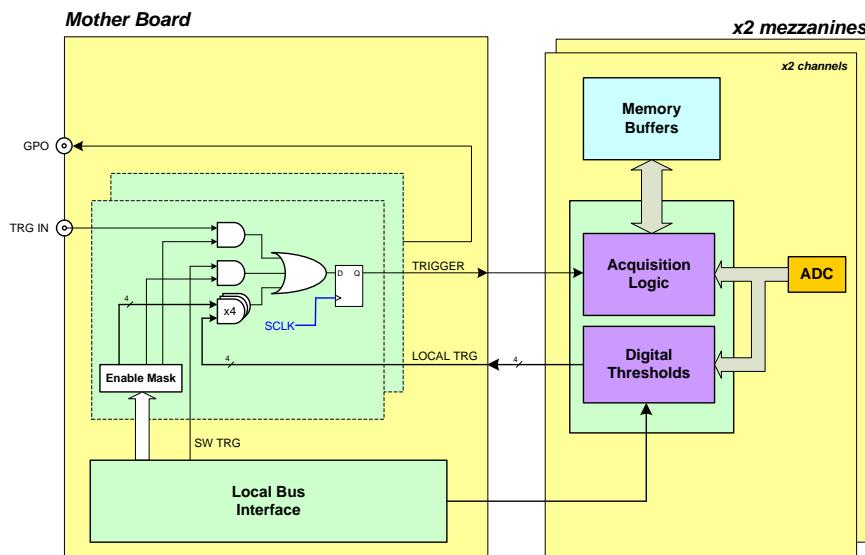


Fig. 8.15: Block diagram of Trigger management.

- **Software Trigger**
- **External Trigger**
- **Self-trigger**
- **Coincidences**
- **TRG-IN as Gate**

Software Trigger

Software triggers are internally produced via software command (write access at register address 0x8108) through USB or Optical Link.

External Trigger

A TTL or NIM external signal can be provided to the front panel TRG-IN connector (configurable at register address 0x811C). If the external trigger is not synchronized with the internal clock, a 1-clock period jitter occurs.

Self-Trigger

Each channel can generate a self-trigger signal (SELF-TRG) when the digitized input pulse exceeds a configurable threshold set through the register address 0x1n80 [RD1]. The condition for the self-trigger generation is that the pulse must stay under/over the threshold (according to the trigger polarity parameter, globally set through bit[6] of the register address 0x8000) for a number of $N^{\text{th}} \times 4(5)$ consecutive samples (N^{th} can be set through the register address 0x1n84 [RD1], 4 samples are in case of normal mode, 5 samples in case of Pack2.5 mode). The self-trigger is therefore delayed by N^{th} quartets/quintets of samples with respect to the input signal (see Fig. 8.16).

The individual self-triggers from all channels are propagated to the central trigger logic on the motherboard (see Fig. 8.15) where they participate in logic OR to produce the board common trigger, which is finally distributed back to all channels on the mezzanines causing the event acquisition (see Sec. **Trigger distribution**).

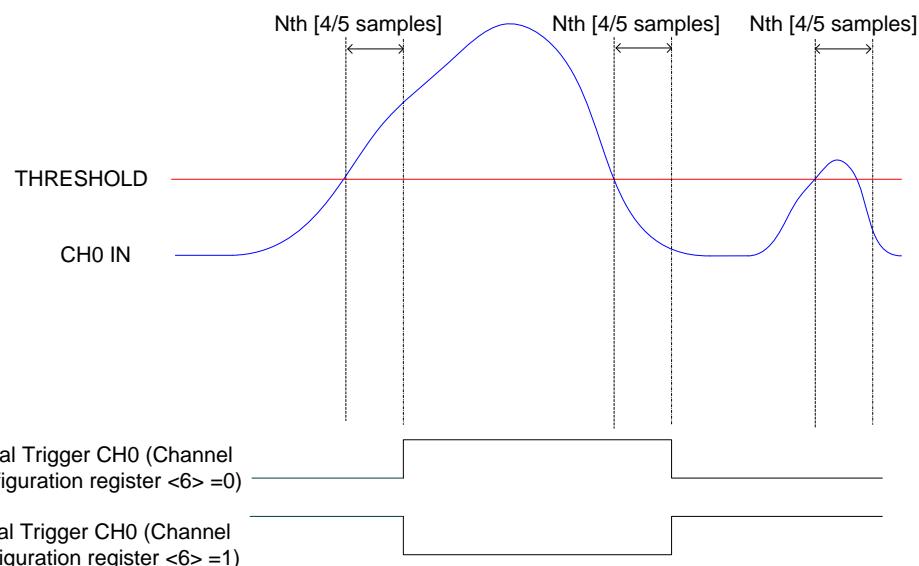


Fig. 8.16: Self-trigger generation.

Bits[3:0] of register 0x810C allows the user to program which channel participates to the global trigger generation.

Trigger coincidence level

Operating the waveform recording firmware, the acquisition trigger is common to the whole board. This common trigger allows the coincidence acquisition mode to be performed through the Majority operation.

Enabling the coincidences is possible by writing at register address 0x810C [**RD1**]:

- Bits[3:0] enable a specific channel self-trigger to participate in the coincidence;
- Bits[23:20] set the coincidence window (T_{TVAW}) linearly in steps of the Trigger clock (8 ns);
- Bits[26:24] set the Majority (i.e. Coincidence) level; the coincidence takes place when:

$$\text{Number of enabled channels} > \text{Majority level}$$

Supposing that bits[3:0] = F (i.e. all channels are enabled) and bits[26:24] = 01 (i.e. Majority level = 1), a common trigger is issued whenever at least two of the enabled self-triggers are in coincidence within the programmed T_{TVAW} .

The Majority level must be smaller than the number of channels enabled via bits[3:0] mask. By default, bits[26:24] = 00 (i.e. Majority level = 0), which means the coincidence acquisition mode is disabled and the T_{TVAW} is meaningless. In this case, the common trigger is simple OR of the enabled channel self-triggers.



Note: in order not to overload the plots but preserve the clearness of concept, only CH0 and CH1 are supposed to be fed with input pulses in the following figures.

Fig. 8.17 shows the trigger management in case the coincidences are disabled.

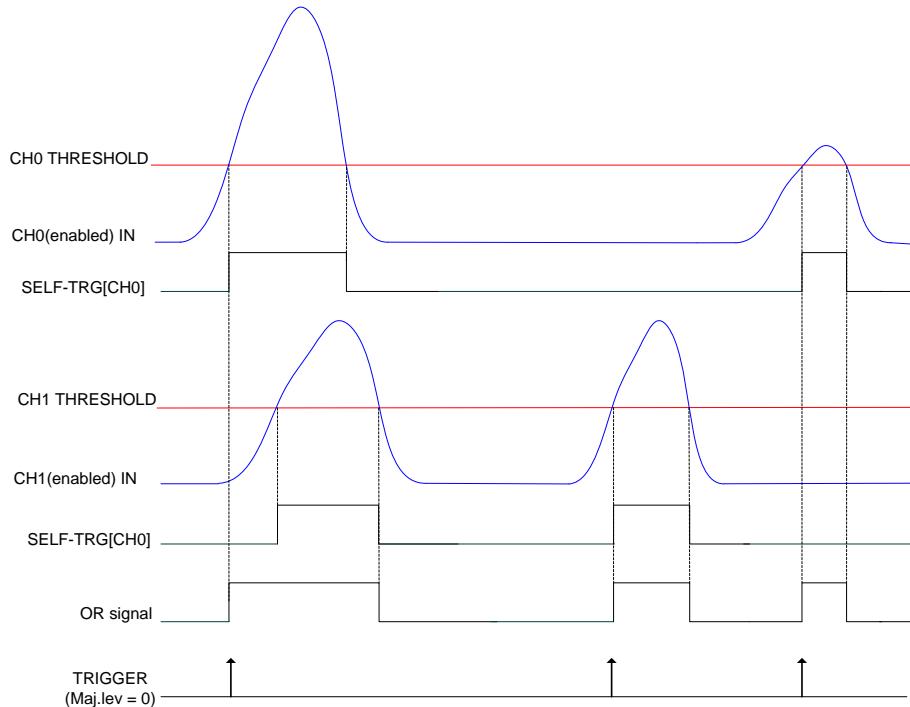


Fig. 8.17: Self-trigger relationship with Majority level = 0.

Fig. 8.18 shows the trigger management in case the coincidences are enabled with Majority level = 1 and T_{TVAW} is a value different from 0.



Note: with respect to the position where the common trigger is generated, the portion of input signal stored depends on the programmed length of the acquisition window and on the post trigger setting.

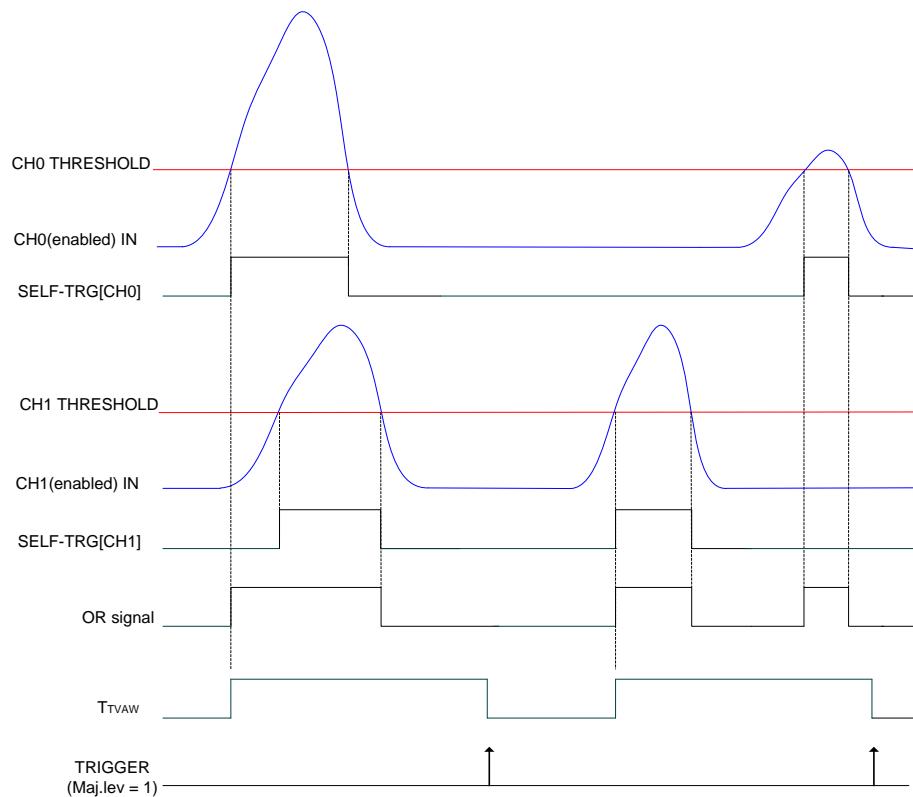


Fig. 8.18: Self-trigger relationship with Majority level = 1 and $T_{TVAW} \neq 0$.

Fig. 8.19 shows the trigger management in case the coincidences are enabled with Majority level = 1 and $T_{TVAW} = 0$ (i.e. 1 clock cycle).



Note: CAEN provides a guide to coincidences including a practical example of making coincidences with the waveform recording firmware [RD4].

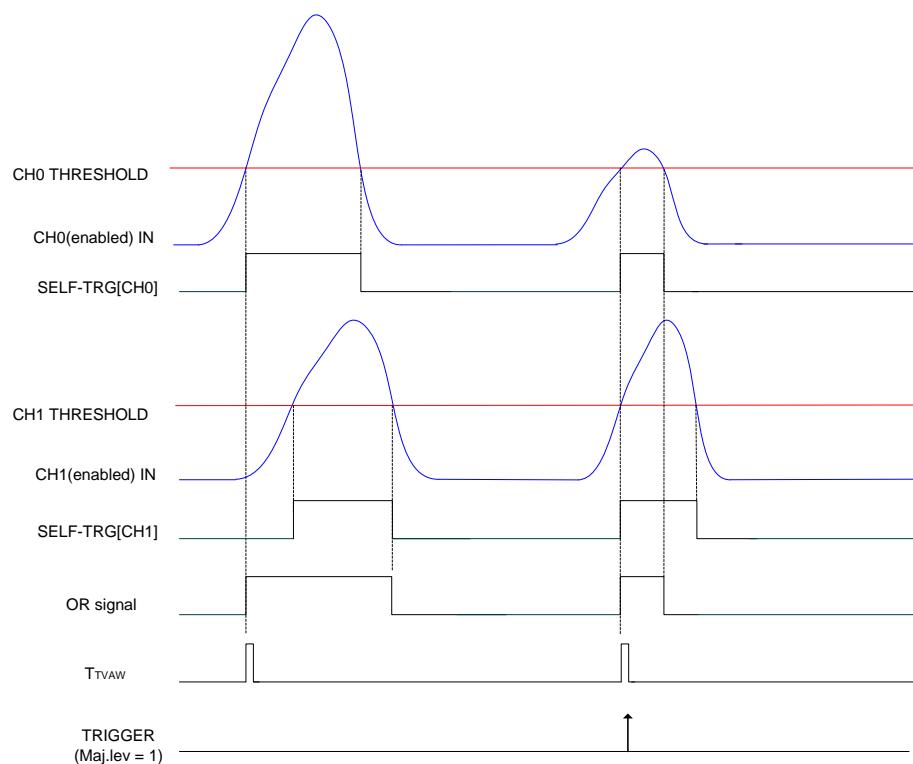


Fig. 8.19: Self-trigger relationship with Majority level = 1 and $T_{TVAW} = 0$.

TRG-IN as Gate

It is possible to configure TRG-IN as a gate for trigger anti-veto function. The common acquisition trigger is then issued upon the AND between the external signal on TRG-IN and the other trigger sources but the software trigger (i.e. the software trigger cannot participate in the Trigger as Gate mode).

This mode is enabled by setting bit[27] = 1 of register 0x810C and bit[10] = 1 of register 0x811C [RD1]. The trigger sources participating in AND with TRG-IN are configurable through register 0x810C as well.

Trigger distribution

As described in Sec. **Trigger Management**, the OR of all the enabled trigger sources, synchronized with the internal clock, becomes the common trigger of the board that is fed in parallel to all channels, consequently causing the capture of an event. By default, only the Software Trigger and the External Trigger participate in the common acquisition trigger (refer to the red path on top of Fig. 8.20).

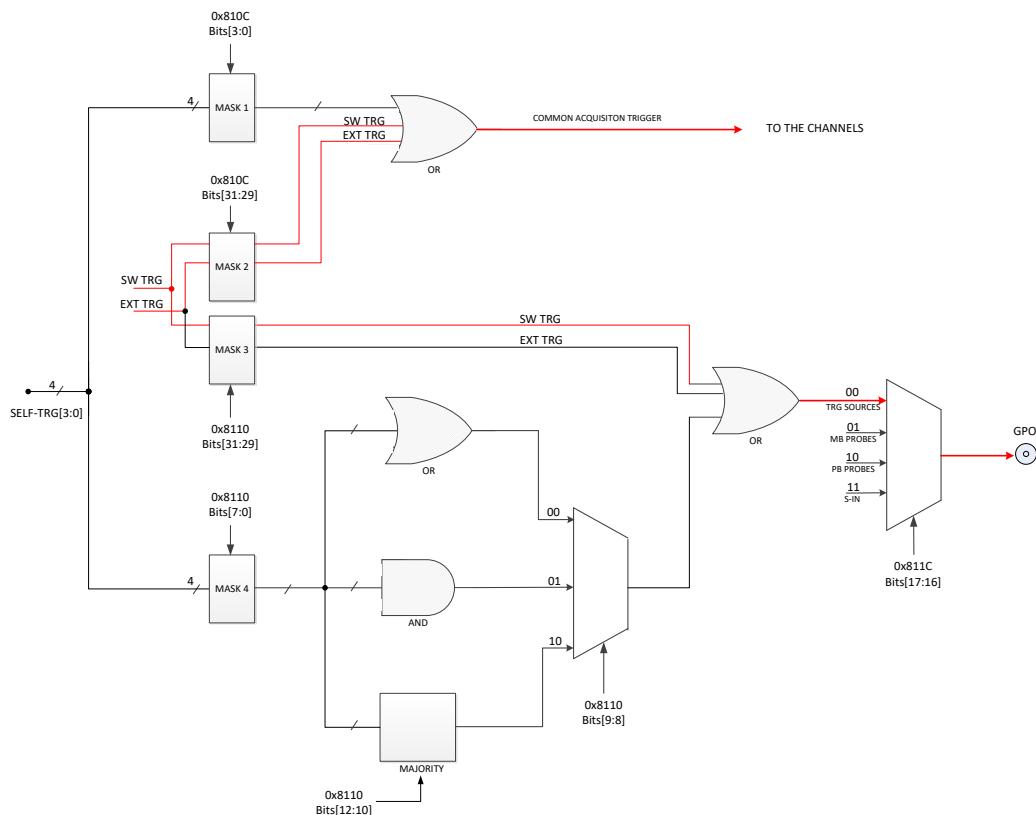


Fig. 8.20: Trigger configuration of TRG-OUT front panel connector.

A Trigger Out signal is also generated on the relevant front panel GPO connector (NIM or TTL), and allows to extend the trigger signal to other boards. Thanks to its configurability, GPO can propagate out:

- the OR of all the enabled trigger sources (only the Software Trigger is provided by default, as in the red path of Fig. 8.20);
- the OR, AND or MAJORITY exclusively of the channel self-triggers.

The registers involved in the GPO programming are:

- Register address 0x8110;
- Register address 0x811C.

Example

It could be required to start the acquisition on all the channels of a multi-board system as soon as one of the board channels (board “n”) crosses its threshold. Trigger Out signal is then fed to an external Fan Out logic unit (e.g. CAEN V2495 board); the obtained signal has then to be provided to the external trigger input TRG-IN of all the boards in the system (including the board which generated the Trigger Out signal). In this case, the programming steps to perform are thereafter described.

1. Register 0x8110 on board “n”:
 - Enable the desired self-trigger as Trigger Out signal on board “n” (by bits[3:0] mask).
 - Disable Software Trigger, External Trigger as Trigger Out signal on board “n” (bits[31:30] = 00).
 - Set Trigger Out signal as the OR of the enabled self-trigger on board “n” (bits[9:8] = 00).
2. Register 0x811C on board “n”:
 - Configure the digitizer to propagates on GPO the internal trigger sources according to the 0x8110 settings (i.e. the enabled self-trigger, in the specific case) on board “n” (bits[17:16] = 00).
3. Register 0x810C on all the boards in the system (including board “n”):
 - Enable External Trigger to participate in the board common acquisition trigger, disable Software Trigger and the channel self-triggers (bits[31:30] = 01; bits[3:0] = 0000).

Test Pattern Generator

The AMC FPGA can emulate the ADC and write into memory a triangular shape from 0 to 7FF and back from 7FF to 0 for test purposes. It can be enabled via register address 0x8000.

Reset, Clear and Default Configuration

Global Reset

Global Reset is performed at power-on of the module or via software by write access at register address 0xEF24 **[RD1]**. It allows to clear the data off the Output Buffer, the event counter and performs a FPGAs global reset, which restores the FPGAs to the default configuration. It initializes all counters to their initial state and clears all detected error conditions.

Memory Reset

The Memory Reset clears the data off the Output Buffer.

The Memory Reset can be forwarded via a write access at register address 0xEF28 **[RD1]**.

Timer Reset

The Timer Reset allows to initialize the timer which tags an event. The Timer Reset can be forwarded with a pulse sent either to the GPI input (leading edge sensitive).

Data Transfer Capabilities and Events Readout

The board features a Multi-Event digital memory per channel, configurable by the user to be divided into 1 up to 1024 buffers, as detailed in Sec. **Multi-Event Memory Organization**. Once they are written in the memory, the events become available for readout via USB or Optical Link. During the memory readout, the board can store other events (independently from the readout) on the available free buffers.

The events are read out sequentially and completely, starting from the Header of the first available event, followed by the samples of the enabled channels (from 0 to 3) as reported in Fig. 8.4. Once an event is completed, the relevant memory buffer becomes free and ready to be written again (old data are lost). After the last word in an event, the first word (Header) of the subsequent event is readout. It is not possible to read out an event partially.

The size of an event (EVENT SIZE) is configurable and depends on register addresses 0x8020 and 0x800C [**RD1**], as well as on the number of enabled channels.

Block Transfer

The Block Transfer readout mode allows to read N complete events sequentially, where N is set at register address 0xEF1C [**RD1**], or by using the *SetMaxNumEventsBLT* function of the CAENDigitizer library [**RD5**].

When developing programs, the readout process can be implemented on different basis:

- Using **Interrupts**: as soon as the programmed number of events is available for readout, the board sends an interrupt to the PC over the optical communication link (**not supported by USB**).
- Using **Polling** (interrupts disabled): by performing periodic read accesses to a specific register of the board it is possible to know the number of events present in the board and perform a BLT read of the specific size to read them out.
- Using **Continuous Read** (interrupts disabled): continuous data read of the maximum allowed size (e.g. total memory size) is performed by the software without polling the board. The actual size of the block read is determined by the board that terminates the BLT access at the end of the data, according to the configuration of register address 0xEF1C, or the library function *SetMaxNumEventsBLT* mentioned above. If the board is empty, the BLT access is immediately terminated and the “Read Block” function will return 0 bytes (it is the *ReadData* function in the CAENDigitizer Library [**RD5**]).

Independently from above method, it is suggested to ask the board for the maximum of events per block being set. Furthermore, the greater this maximum, the greater the readout efficiency, despite a larger memory allocation required on the host station this is not a real drawback considering nowadays personal computers.

Single Data Transfer

This mode allows the user to readout a word per time, from the header (actually 4 words) of the first available event, followed by all the words until the end of the event, then the second event is transferred. The exact sequence of the transferred words is shown in Sec. **Event structure**.

It is suggested, after the 1st word is transferred, to check the EVENT SIZE information and then do as many cycles as necessary (actually EVENT SIZE -1) in order to read completely the event.

Optical Link and USB Access

The board houses a USB2.0 compliant port, providing a transfer rate up to 30 MB/s, and a daisy chainable Optical Link (communication path which uses optical fiber cables as physical transmission line) able to transfer data at 80 MB/s, therefore it is possible to connect up to eight DT5720 to a single Optical Link Controller by using the A2818 PCI card or up to thirty-two DT5720 with the A3818 PCIe card.

Detailed information on CAEN PCI/PCIe Controllers can be find at www.caen.it:

Home / Products / Modular Pulse Processing Electronics / PCI/PCIe / Optical Controller

The parameters for read/write accesses via optical link are Address Modifier, Base Address, data Width, etc.; wrong parameter settings cause Bus Error.

Bit[3] at register address 0xEF00 [**RD1**] enables the module to broadcast an interrupt request on the Optical Link; the enabled Optical Link Controllers propagate the interrupt on the PCI bus when a request from the Optical Link is sensed. Interrupts can also be managed at the CAENDigitizer library level (see “Interrupt Configuration” [**RD5**]).

 **Note:** CONET2 is CAEN proprietary serial protocol developed to allow the optical link communication between the host PC, equipped with a A2818 or a A3818 Controller, and a CAEN CONET slave. CONET2 is 50% more efficient in the data rate transfer than the previous CONET1 version. The two protocol versions are not compliant to eachother and before to migrate from CONET1 to CONET2 it is recommended to read the instructions provided by CAEN in the dedicated Application Note [**RD6**].

9 Drivers & Libraries

Drivers

In order to interface with the board, CAEN provides the drivers for the supported physical communication channels and compliant with Windows® and Linux® OS:

- **CONET Optical Link**, managed by the A2818 PCI card or the A3818 PCIe card. The driver installation package is available on CAEN website in the “Software/Firmware” tab at the A2818 or A3818 page (**login required**).



Note: For the installation of the Optical Link driver, refer to the User Manual of the specific card.

- **USB 2.0** Drivers are downloadable on CAEN website (www.caen.it) in the “Software/Firmware” tab at the DT5720 page (**login required**).



Note: CAEN provides a guide on the installation instructions for USB drivers in Microsoft Windows OS [RD7].

Libraries

CAEN libraries are a set of middleware software required by CAEN software tools for a correct functioning. These libraries, including also demo and example programs, represent a powerful base for users who want to develop customized applications for the digitizer control (communication, configuration, readout, etc.):

- **CAENDigitizer** is a library of functions designed specifically for the Digitizer families supporting both waveform recording firmware and DPP firmware. The CAENDigitizer library is based on the CAENComm library. For this reason, the **CAENComm libraries must be already installed on the host PC before installing the CAENDigitizer**.

The CAENDigitizer installation package and relevant documentation [RD5] are available on CAEN website in the “Download” tab at the CAENDigitizer Library page.

- **CAENComm** library manages the communication at low level (read and write access). The purpose of the CAENComm is to implement a common interface to the higher software layers, masking the details of the physical channel and its protocol, thus making the libraries and applications that rely on the CAENComm independent from the physical layer. Moreover, the CAENComm requires the CAENVMElib library (access to the VME bus) even in the cases where the VME is not used. This is the reason why **CAENVMElib has to be already installed on your PC before installing the CAENComm**.

The CAENComm installation package, the relevant documentation and the link to the required CAENVMElib, are available on CAEN website in the “Download” tab at the CAENComm Library page.

CAENComm (and other libraries here described) supports the following communication channels (Fig. 9.1):

PC → USB → DT5720

PC → PCI (A2818) → CONET → DT5720

PC → PCIe (A3818) → CONET → DT5720

WHEN TO INSTALL CAEN LIBRARIES:

WINDOWS® compliant CAEN software = NOT. CAEN software for Windows® OS are stand-alone, which means the program locally installs the DLL files of the required libraries.

LINUX® compliant CAEN software = YES. CAEN software for Linux® OS is not stand-alone. The user must install the required libraries apart to run the software.

WINDOWS® and LINUX® compliant customized software = YES. The user must install the required libraries apart in case of custom software development.

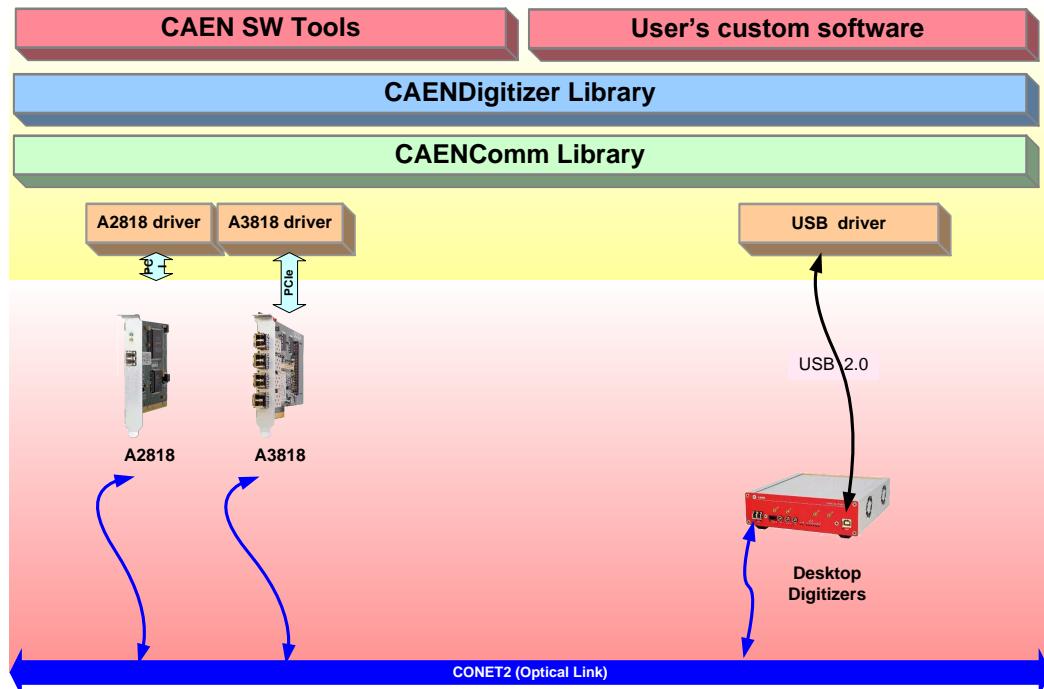


Fig. 9.1: Drivers and software layers.

10 Software Tools

CAEN provides software tools to interface the 720 digitizer family, which are available for [free download](#) at www.caen.it following the path:

Home / Products / Firmware/Software / Digitizer Software

CAENUpgrader

CAENUpgrader is free software composed of command line tools together with a Java Graphical User Interface.

CAENUpgrader, for the DT5720 , allows in few easy steps to:

- Upload different FPGA firmware versions on the digitizer
- Read the firmware release of the digitizer and the bridge (when included in the communication chain)
- Manage the firmware license, in case of DPP firmware
- Upgrade the internal PLL
- Get the Board Info file, useful in case of support

The software relies on the CAENComm and CAENVMELib libraries (see Chap. **Drivers & Libraries**) and requires third-party Java™ SE 8 update 40 (or later) to be installed.

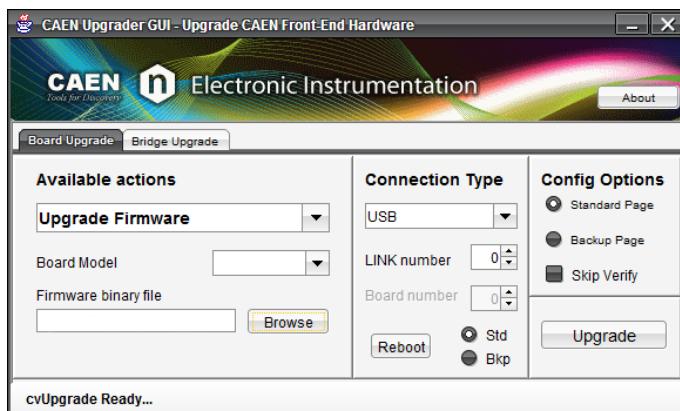


Fig. 10.1: CAENUpgrader Graphical User Interface

CAENUpgrader installation package can be downloaded on CAEN web site (**login required**) at:

Home / Products / Firmware/Software / Digitizer Software / Configuration Tools / CAENUpgrader

CAEN provides a guide to the software features and usage [**RD3**], free downloadable at the web page above.

 **Note:** CAENUpgrader is available for Windows® platforms (32 and 64-bit) as stand-alone version (all the required CAEN libraries are installed locally with the program). Only the drivers for the specific communication link must be installed apart by the user. The CAENUpgrader version for Linux® platform is not stand-alone, so it needs the required libraries to be installed apart by the user.

CAENComm Demo

CAENComm Demo is simple software developed in C/C++ source code and provided both with Java™ and LabVIEW™ GUI interface. The demo mainly allows for a full board configuration at low level by direct read/write access to the registers and may be used as a debug instrument.

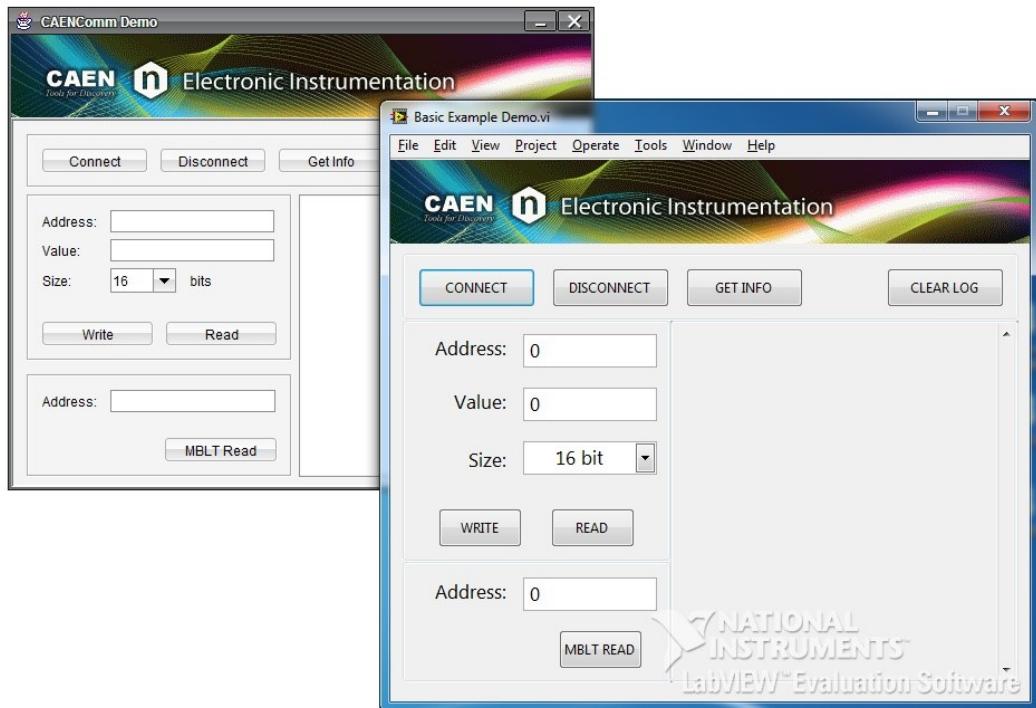


Fig. 10.2: CAENComm Demo Java and LabVIEW graphical interface

The Demo is included in the CAENComm library installation Windows package, which can be downloaded on CAEN web site (**login required**) at:

Home / Products / Firmware/Software / Digitizer Software / Software Libraries / CAENComm Library

CAEN provides the Demo description in the CAENComm library User Manual, free downloadable at the web page above.



Note: CAENComm Demo is available for Windows® platforms (32 and 64-bit) and requires CAENComm and CAENVMElib as additional software to be installed by the user (see Chap. **Drivers & Libraries**).

CAEN WaveDump

WaveDump is a basic console application, with no graphics, supporting only CAEN digitizers running the waveform recording firmware. It allows the user to program a single board (according to a text configuration file containing a list of parameters and instructions), to start/stop the acquisition, read the data, display the readout and trigger rate, apply some post-processing (e.g. FFT and amplitude histogram), save data to a file and also plot the waveforms using Gnuplot (third-party graphing utility: www.gnuplot.info).

WaveDump is a very helpful example of C code demonstrating the use of libraries and methods for an efficient readout and data analysis. Thanks to the included source files and the VS project, starting with this demo is strongly recommended to all those users willing to write the software on their own.

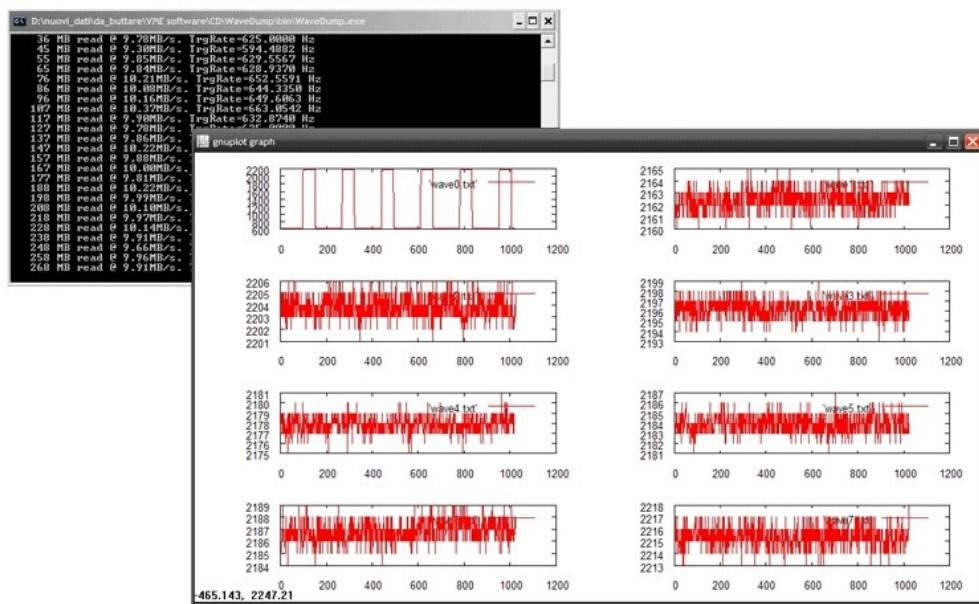


Fig. 10.3: CAEN WaveDump

The installation packages can be downloaded on CAEN web site (**login required**) at:

[Home / Products / Firmware/Software / Digitizer Software / Readout Software / CAEN WaveDump](http://www.caen.it/Products/Firmware/Software/Digitizer%20Software/Readout%20Software/CAEN%20WaveDump)

CAEN provides the software User Manual [**RD8**] and a guide for getting started with it, free downloadable at the web page above.

Note: CAEN WaveDump can operate with Windows® and Linux® platforms (32 and 64 bits); the software relies on the CAENDigitizer, CAENComm and CAENVMELib libraries (see Chap. **Drivers & Libraries**). Windows® versions of WaveDump are stand-alone (all required libraries are present within the software package), while the Linux® versions need the required libraries to be previously installed by the user. Moreover Linux® users are required to install the third-party Gnuplot.



CAEN WaveDump does not work with digitizers running DPP firmware.

CAEN Scope

In a brand new framework, CAENScope software allows to manage the CAEN digitizers running the waveform recording firmware.

CAENScope user friendly interface presents different sections to easily manage the digitizer configuration and plot the waveforms. Once connected, the program retrieves the digitizer information. Different parameters can be set for the channels, trigger and trace visualization (up to 12 traces) can be simultaneously plotted. Signals can be recorded to files in two different formats: Binary (SQLite db) and Text (XML). It is also possible to save and restore the program settings.

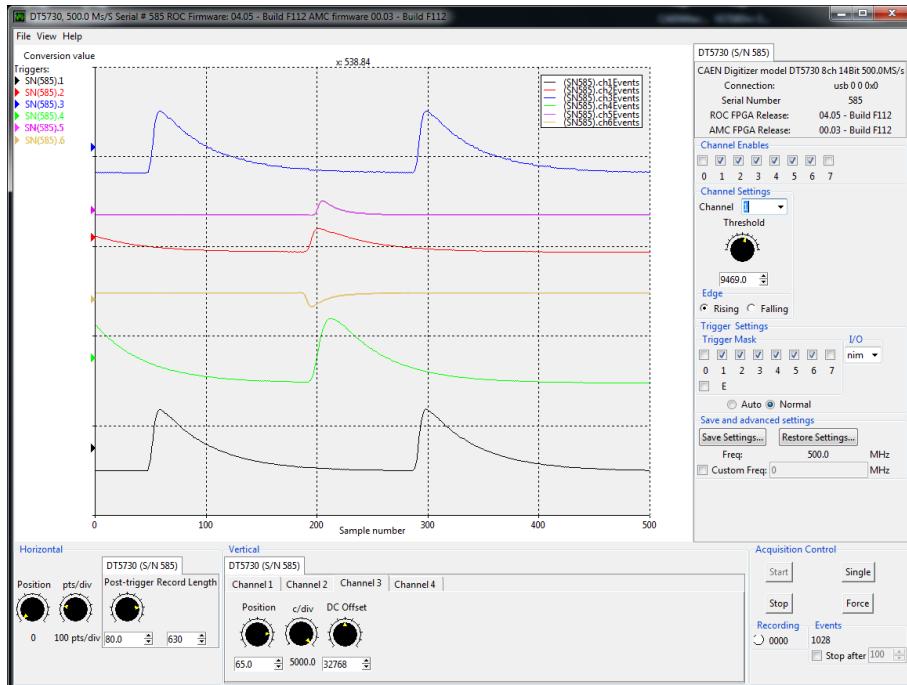


Fig. 10.4: CAENScope main frame.

CAENScope installation packages can be downloaded on CAEN web site (**login required**) at:
[Home](#) / [Products](#) / [Firmware/Software](#) / [Digitizer Software](#) / [Readout Software](#) / [CAENSCOPE](#)
 CAEN provides the software User Manual [**RD9**], free downloadable at the web page above.

Note: Windows® and Linux® versions are stand-alone. The software downloads the required CAENDigitizer, CAENComm and CAENVMElib libraries.

Linux users are required to install the following packages:

- sharutils;
- libXft;
- libXss (specifically for Debian derived distributions, e.g. Debian, Ubuntu, etc.);
- libXScrnSaver (specifically for RedHat derived distributions, e.g. RHEL, Fedora, Centos, etc.).

CAENScope does not work with digitizers running DPP firmware.

DPP-PSD Control Software

DPP-PSD Control Software is a demo application introducing the user to understand the principle of operation of the Digital Pulse Processing for the Pulse Shape Discrimination (DPP-PSD). It can manage single-board communication and acquisition of CAEN 720, 725, 730, and 751 Digitizer series running DPP-PSD firmware and the DT5790 Digital Pulse Analyzer.

DPP-PSD Control Software is based on a Java Graphical User Interface for the parameters setting (connection, DPP algorithm, acquisition, etc.), a C console application working as an acquisition engine (DPPRunner) and a third-party graphing utility (Gnuplot: www.gnuplot.info). The GUI directly handles the acquisition engine through run time commands and generates also a textual configuration file that contains all the selected parameters values. This file is read by DPPRunner, which programs the Digitizer according to the parameters, starts the acquisition and manages the data readout.

The software can operate in the Oscilloscope mode, where digitized input waveforms and digital signals from the internal filters are monitored in order to better tune the DPP parameters, and in the Histogram mode, where energy (i.e. charge) and time histograms (built by the software) can be monitored.

According to the operating mode, raw data like waveforms or charges, PSD and time stamp lists, as well as energy or time histograms can be saved to output files for off-line analysis.

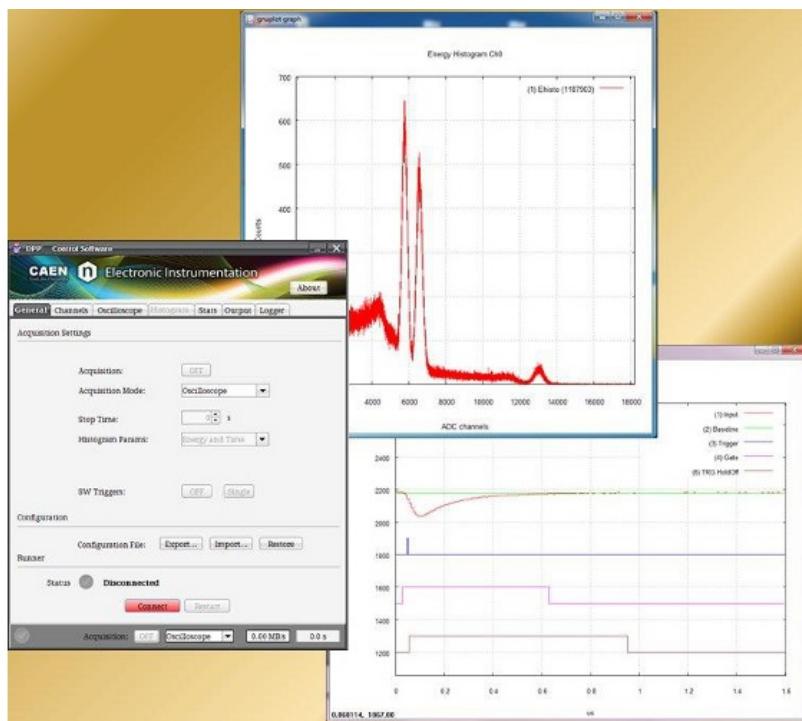


Fig. 10.5: CAEN DPP-PSD Control Software.

The installation package can be downloaded on CAEN web site (**login required**) at:

[Home / Products / Firmware/Software / Digitizer Software / Readout Software / DPP-PSD Control Software](#)

CAEN provides the software User Manual [**RD2**], free downloadable at the web page above.

CAEN DPP-PSD Control Software does not work with waveform recording firmware.

CoMPASS

CoMPASS (CAEN Multi-PArameter Spectroscopy Software) is the new software from CAEN able to implement a Multi-parametric DAQ for Physics Applications, where the detectors can be connected directly to the digitizers inputs and the software acquires energy, timing, and PSD spectra.

CoMPASS software has been designed as a user-friendly interface to manage the acquisition with all the CAEN DPP algorithm. CoMPASS can manage multiple boards, even in synchronized mode, and the event correlation between different channels (hardware and/or software), apply energy and PSD cuts, calculate and show the statistics (trigger rates, data throughput, etc...), save the output data files (raw data, lists, waveforms, spectra) and use the saved files to run off-line with different processing parameters.

CoMPASS Software supports CAEN x720, x724, x725, x730, x740D, x751 digitizer families running the DPP-PSD, DPP-PHA and DPP-QDC firmware, and the x781 MCA family.

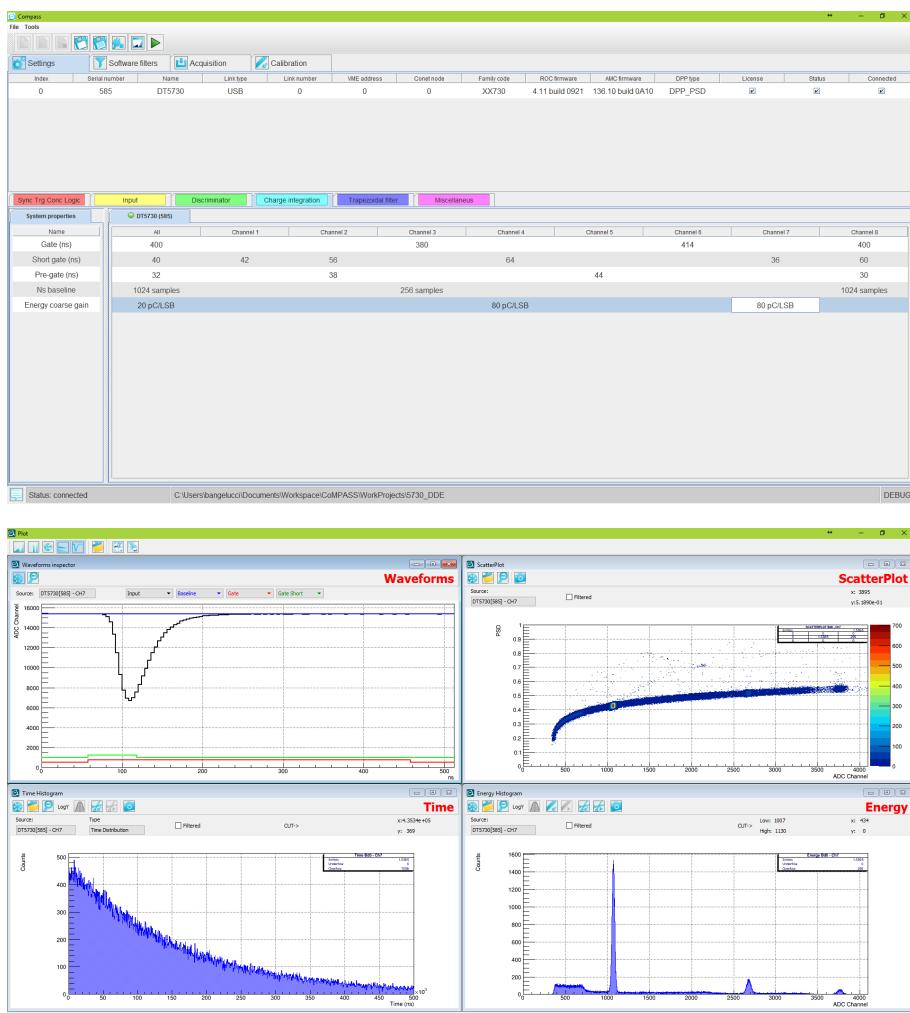


Fig. 10.6: CoMPASS software tool.

The installation package can be downloaded on CAEN web site (**login required**) at:

[Home / Products / Firmware/Software / Digitizer Software / Readout Software / CoMPASS](#)

CAEN provides the software User Manual [**RD10**], free downloadable at the web page above.

CoMPASS does not work with waveform recording firmware.

11 HW Installation

Power-on Sequence

To power on the board, perform the following steps:

1. connect the 12V DC power supply to the DT5720 through the DC input rear connector;
2. power up the DT5720 through the ON/OFF rear switch.

Power-on Status

At power-on, the module is in the following status:

- the Output Buffer is cleared;
- registers are set to their default configuration

After the power-on, only the NIM and PLL LOCK LEDs must stay ON (see Fig. 11.1).



Fig. 11.1: Front panel LEDs status at power-on.

12 Firmware and Upgrades

The board hosts one FPGA on the mainboard and two FPGAs per mezzanine (i.e. one FPGA per channel). The channel FPGAs firmware is identical. A unique file is provided that will update all the FPGAs at the same time.

ROC FPGA MAINBOARD FPGA (Readout Controller + VME interface):

FPGA Altera Cyclone EP1C20

AMC FPGA MEZZANINE FPGA (ADC readout/Memory Controller):

FPGA Altera Cyclone EP1C20

The firmware is stored onto the on-board FLASH memory. Two copies of the firmware are stored in two different pages of the FLASH, referred to as Standard (STD) and Backup (BKP). In case of waveform recording firmware, the board is delivered equipped with the same firmware version on both pages. At power-on, a micro-controller reads the FLASH memory and programs the module automatically loading the first working firmware copy, that is the STD one in normal operating.

It is possible to upgrade the board firmware via USB or Optical Link by writing the FLASH with the CAENUpgrader software (see Chap. **Software Tools**).

IT IS STRONGLY SUGGESTED TO OPERATE THE DIGITIZER UPON THE STD COPY OF THE FIRMWARE. UPGRADES ARE SO RECOMMENDED ONLY ON THE STD PAGE OF THE FLASH. THE BKP COPY IS TO BE INTENDED ONLY FOR RECOVERY USAGE. IF BOTH PAGES RESULT CORRUPTED, THE USER WILL NO LONGER BE ABLE TO UPLOAD THE FIRMWARE VIA USB OR OPTICAL LINK AGAIN AND THE BOARD NEEDS TO BE SENT TO CAEN FOR REPAIR!

Firmware Upgrade

All firmware updates are available for download on CAEN website www.caen.it (**login required**) at the following path:

Home / Products / Modular Pulse Processing Electronics / Desktop / Digitizers / DT5720

Different firmware are available for the 720 family:

- The waveform recording firmware;
- The special DPP firmware for Physics Applications:
 - DPP-PSD firmware to use the digitizer as a digital replacement Dual Gate QDC, Discriminator and Gate Generator.

DPP firmware updates can also be found at the relevant DPP firmware web page:

Home /Products / Firmware/Software / DPP Firmware/Software Tools (Digitizer) / DPP Firmware / <DPP-FIRMWARE>

Firmware File Description

The programming file has the extension .CFA (CAEN Firmware Archive). It is an archiving file format that aggregates all the programming files of the same firmware kind which are compatible with the same digitizer family.

The CFA naming convention follows this general scheme:

- x720_rev_X.Y_W.Z.CFA for the waveform recording firmware
- x720_DPP-PSD_rev_X.Y_131.Z.CFA for the DPP-PSD firmware for 720

where x720 are all the supported boards (the 720 family includes DT5720, N6720, V1720, VX1720), X.Y is the major/minor revision number of the mainboard FPGA, and W.Z is the major/minor revision number of the channel FPGA.

The major revision number of the channel FPGA is a fixed number specific for each DPP and digitizer family, and it can be equal or greater than 128 (for example, 720 series have 131 for PSD). The waveform recording firmware major revision number is not fixed and it is less than 128.



Note: DPP special firmware is a pay firmware requiring a license to be purchased. If not licensed, the firmware can be loaded but it will run fully functional with a time limitation per power cycle (30 minutes). Details on the license ordering procedure are included in the CAENUpgrader guide [\[RD3\]](#).

Troubleshooting

In case of upgrade failure (e.g. STD FLASH page is corrupted), the user can try to reboot the board: after a power cycle, the system programs the board automatically from the alternative FLASH page (e.g. BKP FLASH page), if this is not corrupted as well. The user can so perform a further upgrade attempt on the STD page to restore the firmware copy.

Note: old versions of the digitizer motherboard have a slightly different FLASH management. Use CAENUpgrader 1.6.0 or later to get the BoardInfoFile (using the "Get Information" function) and check that the FLASH_TYPE=0. Alternatively, use a software utility like CAENComm Demo to read at register address 0xF050 and check that bit[7]=0.

In this case, at power-on, the micro-controller loads exactly the firmware copy from the STD page of the FLASH .

When a failure occurs during the upgrade of the STD page of the FLASH, which compromises the communication with the DT5720 , the user can perform the following recovering procedure as first attempt:



- force the board to reboot loading the copy of the firmware stored on the BKP page of the FLASH. For this purpose, make sure to connect by USB link and use the Reboot function in CAENUpgrader software by checking "Bkp" option .
- use CAENUpgrader to read the firmware revision (in this case the one of the BKP copy). If this succeeds, it is so possible to communicate again with the board;
- use CAENUpgrader to load the proper firmware file on the STD page, then power-cycle in order the board to get operative again.

If neither of the procedures here described succeeds, it is recommended to send the board back to CAEN in repair (see Chap. **Technical Support**).

13 Technical Support

CAEN support services are available for the user by accessing the *Support & Services* area on CAEN website at <http://www.caen.it>.

Returns and Repairs

Users who need for product(s) return and repair have to fill and send the Product Return Form (PRF) in the *Returns and Repairs* area at *Home / Support & Services*, describing the specific failure. A printed copy of the PRF must also be included in the package to be shipped.

Contacts for shipping are reported on the website at *Home / Contacts*.

Technical Support Service

CAEN makes available the technical support of its specialists at the e-mail addresses below:

support.nuclear@caen.it
(for questions about the hardware)

support.computing@caen.it
(for questions about software and libraries)



CAEN SpA is acknowledged as the only company in the world providing a complete range of High/Low Voltage Power Supply systems and Front-End/Data Acquisition modules which meet IEEE Standards for Nuclear and Particle Physics. Extensive Research and Development capabilities have allowed CAEN SpA to play an important, long term role in this field. Our activities have always been at the forefront of technology, thanks to years of intensive collaborations with the most important Research Centres of the world. Our products appeal to a wide range of customers including engineers, scientists and technical professionals who all trust them to help achieve their goals faster and more effectively.



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