MC-ISAR_AS42x_AURIX2G_TC38xA_TC39xB_BASIC_1.0.0-rc

Release Notes
Product name: MC_AURIX2G_SW_MCAL
Release number: 1.0.0-rc
Type of release: RC*
Release method: via Release Area
AUTOSAR specification: 4.2.2
Compiler support: Tasking 6.2r2, HighTec GNU 4.9.2.0, WindRiver v5.9.6.4, Patch Diab5964_CSO-31481
Processor platform: TC38xAA, TC38xAB, TC38xAC, TC38xAD, TC39xBA, TC39xBB, TC39xBC
Date: 2018-10-08
Previous release number: 1.0.0-beta

About this document

Scope and purpose

This release notes, for the 1.0.0-rc delivery of TC3xx_SW_MCAL basic drivers, details the release contents, all known issues in the release and the changes from the last release. This document also provides information on tools, compiler options and support packages.

New issues identified since the last release of this document are detailed first, followed by all issues identified in previous versions of this release.

The following modules are supported in this release:

- Adc (2.1.0)
- Can_17_McmCan (4.0.0)
- Crc (4.1.0)
- Dio (3.0.0)
- Fee (3.0.0)
- Fls_17_Dmu (3.0.0)
- Gpt (3.0.0)
- Icu_17_TimerIp (3.0.0)
- McalLib (3.0.0)
- Mcu (4.0.0)
- Port (3.0.0)
- Pwm_17_GtmCcu6 (4.0.0)
- Spi (2.0.0)
- Wdg_17_Scu (2.1.0)

Further generic references to Modules are indicated as <Mod>, where <Mod> represents the above module short names.

Note: ** This release is not intended for production use.*

About this document

Attention**: **Refer to the Limitations and deviations section before using the software for integration.

Intended audience

This document is intended for anyone using the TC3xx_SW_MCAL software.

Reference documents

Not applicable.

Table of contents

1 Release contents

1.1 Release overview

This release is of RC quality. Section 1.4 provides module-wise quality information. This build is meant to start the integration and not for production usage, hence no legal liabilities.

1.2 Released items

The release is contained in the `MC-ISAR_AS42x_AURIX2G_TC38xA_TC39xB_BASIC_1.0.0-rc.zip` file. The contents of this file include the MCAL software, EB tresos plugin files (BMD included), and User Manual and Release Notes.

Note: The package also includes Build Environment and Demo Application, which are not attached with any quality but provided for demonstration purpose only.

Table 1 Release zip contents

Package content	Description
`MC-ISAR_AS42x_AURIX2G_TC38xA_TC39xB_BASIC_1.0.0-rc.exe`	Product installer to be used with AUTOSAR Version 4.2.2
User Manuals	Contains the User Manual
`MC-ISAR_AS42x_AURIX2G_TC3xx_BASIC_1.0.0-rc.pdf`	Contains the Release Notes
`TC3xx_SW_MCAL_HWErrataAnalysis.xlsx`	Contains analysis for the hardware errata sheet

1.2.1 Driver files

Table 2 Driver file description

File name	Description
`<Mod>_<Ie>.c`	Contains the <Mod>_<Ie> source files located in `\McIsar\Src\Mcal\Tricore\<Mod>\ssc\src`.
`<Mod>_<Ie>.h`	Contains the <Mod>_<Ie> header files located in `\McIsar\Src\Mcal\Tricore\<Mod>\ssc\inc`.

Note: In the above table, `Ie` stands for implementation specific.

1.2.2 Common files

Table 3 Common files

File / folder name	Description
McalLib.c	Contains MCAL function source file located in \McIsar\Src\Infra\McalLib\Tricore\ssc\src
McalLib.h	Contains MCAL/GTM library function header file located in \McIsar\Src\Infra\McalLib\Tricore\ssc\inc
\McIsar\Src\Infra\Platform\Tricore	Contains the compiler abstraction and standard type definitions
\McIsar\Src\Infra\Sfr\TC39A_Reg	Contains the Special Function Register (SFR) definitions for device(s)
\McIsar\Src\Mcal\Tricore\McalLib\ssc\inc\<compiler>	Contains the intrinsic definitions for different compilers supported
Mcal_Compiler.h	Contains MCAL-specific compiler abstractions file located in \McIsar\Src\Infra\McalLib\Tricore\ssc\inc

1.2.3 EB tresos plugin files

Note: Resource_Aurix2G contains the properties for the TC38xA and TC39xB devices.

Table 4 Plugin files

Folder name	Description
Autosar	Contains the BMD files for the module located in \McIsar\PluginsTresos\eclipse\Plugins\<Mod>_Aurix2G
Config	Contains the XDM tresos plugin files for the module located in \McIsar\PluginsTresos\eclipse\Plugins\<Mod>_Aurix2G
Generate	Contains the template for the generated files for the module located in \McIsar\PluginsTresos\eclipse\Plugins\<Mod>_Aurix2G
plugin.properties	Contains the plugin property for the module located in \McIsar\PluginsTresos\eclipse\Plugins\<Mod>_Aurix2G
plugin.xml	Contains the plug-in information, located in \McIsar\PluginsTresos\eclipse\Plugins\<Mod>_Aurix2G
anchors.xml	

1.3 Safety

This release has no safety claim.

1.4 Module-wise quality

Table 5 Module-wise quality

Module	Release quality
Adc	RC
Can_17_McmCan	RC
Crc	RC
Dio	RC
Fee	RC
Fls_17_Dmu	RC
Gpt	RC
Icu_17_TimerIp	RC
Mcu	RC
Port	RC
Pwm_17_GtmCcu6	RC
Spi	RC
McalLib	RC
Wdg_17_Scu	RC

1.5 Compatibility

This release is tested with the following SFR packages:

- TC38x - REG_TC38X_UM_V1.0.0.R0
- TC39xB - REG_TC39XB_UM_V1.0.0.R0

2 Tool information

Table 6 Tool information

Tool description	Version details
Compiler	TASKING TriCore 6.2r2 HighTec TriCore 4.9.2.0 WindRiver v5.9.6.4, Patch Diab5964_CSO-31481
Processor platform	TC38xAA, TC38xAB, TC38xAC, TC38xAD TC39xBA, TC39xBB, TC39xBC
Evaluation hardware	TriBoard TC3x9 TriBoard TC3x7
Code configuration and generation tool	EB tresos Studio 23.0.0 Build Nr. b170330-0431

2.1 Compiler options

Table 7 TASKING compiler options used

Options	Description
Compiler options	`--core=tc1.6.2 --iso=99 -O2 --eabi-compliant -AGKpvX --switch=auto --integer-enumeration --default-near-size=0 --fp-model=1`
Assembler options	`--core=tc1.6.2 --list-format=1 --optimize=gs`
Linker options	`--map-file -OcLtXY --core=mpe:vtc`

Table 8 HighTec compiler options used

Options	Description
Compiler options	`-DGNU -Wall -std=c99 -c -O2 -mtc162 -meabi -fno-short-enums -ffunction-sections -fdata-sections -fstrict-volatile-bitfields`
Assembler options	`-DGNU -Wall -std=c99 -c -O2 -mtc162 -meabi -fno-short-enums -ffunction-sections -fdata-sections -fstrict-volatile-bitfields`
Linker options	`-Wl,--mcpu=tc162 -Wl,--gc-sections -nostartfiles -n`

Table 9 WindRiver Diab compiler options used

Options	Description
Compiler options	`-tTC162NF:simple -O -XO -Xsection-split=1 -Xkeep-assembly-file=2 -g3 -Xinline=0 -Xdialect-c99 -ei5388,2273,5387 -ei1824 -Xsmall-data=0 -Xsmall-const=0`
Assembler options	`-tTC162NF:simple -O -XO -Xsection-split=1 -Xkeep-assembly-file=2 -g3 -Xinline=0 -Xdialect-c99 -ei5388,2273,5387 -ei1824 -Xsmall-data=0 -Xsmall-const=0`

Tool information

Table 9 WindRiver Diab compiler options used (continued)

Options	Description
Linker options	`-tTC162NF:simple -m6 -Xremove-unused-sections`

Note: Compiler options which influence code generation and are not listed, should be left to the default compiler settings. All the above-listed compiler options are mandatory.

***Attention*: If the compiler options are changed by the user, and if the generated binary output is different than the one generated by the usage of the mandatory compiler options, the functionality and reliability of the drivers cannot be ensured.**

3 Summary of changes

This chapter describes the fixes for issues from previous version(s).

Configuration changes

Compatibility check	Result
Are there any change in parameters supplied from previous version?	Yes
Added parameters	**Icu_17_TimerIp**: OverflowISRThreshold, Note: • Enable/Disable condition is removed from EruInputPin parameter • Editable true/false condition is added for IcuDefaultStartEdge parameter **Fls_17_Dmu**: FlsProgVerifyErrNotif
Deleted parameters	**Mcu**: McuEthRamFrequency
Modified parameters	The following modules parameter range values are modified. User shall choose the modified range value from the EB tresos GUI. **Fls_17_Dmu:** Note: • FlsWaitStateRead parameter range value is modified as mentioned below From: FLS_WAIT_STATE_READACCESSx To: FLS_17_DMU_WAIT_STATE_READACCESSx (x: 0 to 255) • FlsWaitStateErrorCorrection parameter range value is changed - From FLS_WAIT_STATE_ERRORCORRECTIONx - To FLS_17_DMU_WAIT_STATE_ERRORCORRECTIONx (x:0 to 7) - FlsInitApiMode and FlsRuntimeApiMode range values are modified From FLS_MCAL_SUPERVISOR To: FLS_17_DMU_MCAL_SUPERVISOR From: FLS_MCAL_USER1 To: FLS_17_DMU_MCAL_USER1 **Mcu:** Note: • McuGetRamStateApi parameter is enabled for configuration • Added additional literals for McuExtClockOutSel0 and McuExtClockOutSel1 parameters • McuAscLinChannelAllocationConf parameter is made editable true

Summary of changes

Compatibility check	Result
Modified parameters	**Can_17_McmCan:** Note: • For CanHwFilterMask Parameter editable true/ false condition check is added. • CanInitDeInitApiMode parameter range values are modified as mentioned below From: CAN_MCAL_USER1 To: CAN_17_MCMCAN_MCAL_USER1 From: CAN_MCAL_SUPERVISOR To: CAN_17_MCMCAN_MCAL_SUPERVISOR
Can the previously saved configuration be reused?	Yes

3.1 Issues fixed in release 1.0.0-rc

This chapter describes the fixes for issues from previous version(s).

Table 10 Summary of changes from 1.0.0-beta to 1.0.0-rc

Module	Issue number	Description
General	0000053912-2896 0000053912-2897	Various BSWMD files contain implementation data types (empty structures), which may cause errors during "Build of internal data structures" due to empty structures.
	0000053912-3770	ARXML descriptions updated for SchM function.
	0000053912-1782	Inclusion order corrected to work with ACCESS keyword as this is defined in both IfxGtm_Reg.h and OS files, which otherwise would lead to a compilation issue.
	0000053912-2519	Vendor API infix and Vendor ID to be used for all C literals / interfaces.
	0000053912-3219	Removed inclusion of Mod.h in Mod_PBCfg.h and added the inclusion of Mod_PBcfg.h at the end of in Mod.h.

Summary of changes

Table 10 Summary of changes from 1.0.0-beta to 1.0.0-rc (continued)

Module	Issue number	Description
Adc	0000053912-2381	GxALIAS and GxBOUND registers are updated without checking if they are being used.
	0000053912-2467	No Tresos error is reported if the AdcSyncConvChannelEnable parameter for the Slave core is set to True.
	0000053912-2654	Unintended safety error, ADC_SE_INT_PLAUSIBILITY, is reported when configured as follows: - Safety is ON - Queuing is enabled - Group used is software triggered, continuous, circular streaming
	0000053912-2379	The Adc_SetPowerState API checks for all groups to be in the Idle state and then puts all the kernels in low power mode. There is no lock between checking the group status and placing the kernel to low power mode. If in between these steps, groups are started they may not convert.
	0000053912-3154	Pre-compile macros are generated as Supervisor instead of User1 mode even though mode configured is User1.
	0000053912-3212	A trap is raised due to null pointer access when the Adc_TriggerStartupCal API is called without the Adc_Init API.
	0000053912-3409	Software queue feature does not work as expected in the HW_SW priority as per the User Manual.
	0000053912-3551	Warning reported for TASKING compiler when configured with AdcSafetyEnable as OFF and low power mode support enabled.
	0000053912-3558	Compilation error is reported for SIDs when DET is OFF and SAFETY is OFF.
	0000053912-3574	Warning reported when ADC_STARTUP_CALIB_API is OFF and ADC_ENABLE_START_STOP_GROUP_API is OFF.
	0000053912-3781	Local functions are placed in pre-compile switches since they may not be used in all configurations.
	0000053912-3783	Code Generator error message added: - if synchronous group does not have a master - if synchronous group does not have even one slave
	0000053912-3789	Channel reservation error added if GTM/ERU channels are reserved in MCU for ADC but not used by ADC gating configurations (EruGatingConfig/ GtmGatingTimerConfig).

Summary of changes

Table 10 Summary of changes from 1.0.0-beta to 1.0.0-rc (continued)

Module	Issue number	Description
Can_17_McmCan	0000053912-1538	PN mode Rx indication is wrongly getting generated on payload length error detection when CanIcomPayloadLengthError is configured.
	0000053912-1555	PN mode busoff Indication is not getting generated when CAN busoff event occurs though CanIcomWakeOnBusOff is configured as True.
	0000053912-1935	CAN messages are getting dropped by the CAN driver. This is only seen in the TASKING compiler.
	0000053912-2639	Transmission order of CAN messages queued for transmission in Tx queue differs across compilers.
	0000053912-2877	CanIf_TriggerTransmit call should be protected by the pre-compile switch.
	0000053912-3074	Zero generated as HRH mask for RxHW object index greater than 32 in case of multiple Rx periods.
	0000053912-3279	Re-entrant multiple call to Can_17_McmCan_Write () to transmit CAN messages leads to the CAN messages being transmitted with correct Id but wrong data length and values after few hundreds of correct transmissions.
	0000053912-3362	Transmit notifications are not generated correctly for TxQueue in the Polling mode.
	0000053912-3550	Error checks added for invalid configuration having CanControllerId added in order other than ascending order.
	0000053912-3566	Error in Config generation observed when multiple Rx periods are configured for multiple receive objects and Tx periods are not configured in multiples.
	0000053912-3751	CAN message reception is missed out in some cases.
	0000053912-3784	HRH filter accepting range of IDs not compatible with ICOM setup.
	0000053912-3959	BMD corrections for the CanRxInputSelection parameter includes whole list of options.
	0000053912-3973	Hardware filter does not work for a single buffer setup.
	0000053912-759	FIFO reception stops indefinitely after message lost error is encountered.
	0000053912-3345	Wrong address at the beginning of Node RAM area due to wrong number of messages considered for internal algorithm.
	0000053912-3747 0000053912-4057	Transmission controller confirmation event not received for all the frames.
Dio	0000053912-3211	BSWMD schema updated for the BSW-MODULE-DEPENDENCY element.
	0000053912-3560	Driver code warning removed due to dead assignment to RetVal in the Dio_FlipChannel() API.

Summary of changes

Table 10 Summary of changes from 1.0.0-beta to 1.0.0-rc (continued)

Module	Issue number	Description
Fee	0000053912-1336	GC is triggered before reaching threshold.
	0000053912-1337	Few pages are skipped between two block writes.
	0000053912-2328	Driver status not returning to IDLE, if job is requested after canceled GC erase.
	0000053912-2343	Second NVM read not working after QS erase suspend.
	0000053912-2417	Fee_GetPrevData() is reading DFlash contents beyond the old size when NVM block size is increased.
	0000053912-2501	Illegal state handling is different for NVM and QS blocks.
	0000053912-2598	Variation point build with two different configs in single build is failing.
	0000053912-2641	A trap is raised when passing invalid block number to Fee_17_GetPrevData().
	0000053912-2788	Suspended QS erase operation is not resuming immediately, but resumes in the next main function cycle.
	0000053912-2789	NVM Write/GetPrevData/InvalidateBlock requests rejected during QS erase, even though the Suspend feature is enabled.
	0000053912-2792	Invalid block number DET/Safety Error not reported for few APIs (when NVM APIs are called with QS blocks and QS API called with NVM block).
	0000053912-2809	Driver is stuck in an infinite loop during init, if failed Word Line address is at the beginning of DFlash0.
	0000053912-2810	Word Line is not skipped if state page writing encounters PVER error.
	0000053912-2817	Word Line issue during GC erase leads to illegal state only in TC39x device.
	0000053912-2835	Hardening rate is slower than expected.

Summary of changes

Table 10 Summary of changes from 1.0.0-beta to 1.0.0-rc (continued)

Module	Issue number	Description
Fee	0000053912-3305	Function Fee_17_GetPrevData() is hitting trap for the following: - Erase DFlash0, call FLS and FEE Init functions - Wait until driver status is MEMIF_IDLE - Call Fee_Write() on a NVM block of data and wait until driver status is idle to read the job result - Call Fee_Write() on the same block of data and wait until driver status is idle - Invalidate the same block with Fee_InvalidateBlock() - Read the previous data of the block with Fee_17_GetPrevData() and wait until driver status becomes idle and read the job result
	0000053912-3398	In the virgin Flash, Fee_Init() is not setting the erase complete marker to configured QS block instances.
	0000053912-3399	The QsM_Cbk.h file is included unconditionally in the Fee_Cfg.h file.
	0000053912-3501	Re-programming, due to ECC error, introduces memory leaks.
	0000053912-3555	Unconfigured blocks are overwritten if two Word Line issues are found during GC copy.
	0000053912-3596	Pending read request is not executed immediately after erase during GC.
	0000053912-3623	QS Erase suspend/resume gives both Job End and Job Error in a specific case when Fee_Read() is invoked on the common block, Block1, with offset greater than boot configuration size (> 100) and valid size .
	0000053912-3706	Driver not returning to IDLE if hardening error is encountered.
	0000053912-3713	Hitting trap during GC if ECC error found in block to be copied.
	0000053912-3725	When GC on GC gets triggered, the driver does not return to the IDLE or illegal states.
	0000053912-3738	Big block not copied completely during GC.
	0000053912-3888	For variation point, the file name generated for PBCfg.c is not consistent.
	0000053912-3944	GetPrevData is reading wrong data if immediate block is written during GC.

Summary of changes

Table 10 Summary of changes from 1.0.0-beta to 1.0.0-rc (continued)

Module	Issue number	Description
Fee	0000053912-3946	QS Erase getting suspended when suspend feature is disabled in FEE and enabled in FLS.
	0000053912-3947	NVM Write accepted (but not completed) after canceling Read, Read is issued during QS Erase (EraseSupend=ON).
	0000053912-3982	QS hardening offset resetting to 0 during first GC after the power cycle.
	0000053912-4031	Warning observed in the driver code when NVM sector size is set to minimum size (4 Kb).
	0000053912-507	Fee blocks with ECC errors are stored in the cache table and this will lead to illegal state while copying FEE blocks with ECC during GC.
	0000053912-598	High variation in the Fee_MainFunction for the Fee_Write operation.
	0000053912-4006	A trap is raised during initialization if data block marker is corrupted such that the calculated block header address lies beyond DFash0.
	0000053912-3525	For every GC erase caused by normal Write, suspend-resume kicks in.
	0000053912-2792	Invalid block number DET/Safety Error not reported for few APIs (when NVM APIs are called with QS blocks and QS API is called with NVM block).
	0000053912-2787	Invalidate block request does not finish if called during suspend GC Erase.

Summary of changes

Table 10 Summary of changes from 1.0.0-beta to 1.0.0-rc (continued)

Module	Issue number	Description
Fls_17_Dmu	0000053912-3378	Range check is implemented for sector parameter of Fls_17_Dmu_VerifySectorErase().
	0000053912-2419	Fls_17_Dmu_SuspendErase returns E_OK when Erase operation is not on-going.
	0000053912-3222	Fls_17_Dmu_CompareWordsSync() should return E_NOT_OK when ECC error is set and safety is OFF
	0000053912-3236	Fls_17_Dmu_GetNotifCaller() does not return proper value when notification is raised by CANCEL job.
	0000053912-2426	Runtime error not reported when operation error occurs by Write and Erase APIs.
	0000053912-3377	Definition of FLS_17_DMU_CMDCYCLE_TIMEOUT is moved out from (Fls_17_Dmu_Cfg.h) file.
	0000053912-3109	Calculated values for few config items are not correct in the EB tresos.
	0000053912-3166	Safety Error protection is not required for few registers.
	0000053912-3686	Software is hitting a trap when ClearStatus command is executed when PROG bit is HIGH.
	0000053912-3295	Word line failures reported by FLS erase may not be correct.
	0000053912-2633	Fls_17_Dmu_MainFunction() does not set module status to MEMIF_JOB_FAILED when Write Job fails due to PVER error.
	0000053912-3339	Safety error not reported by non-AUTOSAR APIs when non-word-aligned address is passed.
	0000053912-3376	Range check was not implemented for input parameter of Fls_17_Dmu_SetMode().
	0000053912-3412	AERM bit is not cleared before read from DFlash in Fls_17_Dmu_VerifyErase, Fls_17_Dmu_VerifySectorErase and in readback of Fls_17_Dmu_Write APIs.
	0000053912-3494	Hardening check-related issues. - Fail criteria is wrongly implemented in Fls_17_Dmu_IsHardeningRequired() - Hardening check command execution has delay of 21 µs always - Sequence and operation error checks are not present in Fls_17_Dmu_IsHardeningRequired - FSI_COMM_1 and FSI_COMM_2 are not cleared in Fls_17_Dmu_IsHardeningRequired - Clear status command is not called in the Fls_17_Dmu_IsHardeningRequired() API
	0000053912-3502	Compilation error when DET is disabled and RTE is enabled.
	0000053912-3656	The Fls_17_Dmu_ControlTimeoutDet() API continues execution even after DET is raised.

Summary of changes

Table 10 Summary of changes from 1.0.0-beta to 1.0.0-rc (continued)

Module	Issue number	Description
Fls_17_Dmu	0000053912-3657	Compilation error in Fls_17_Dmu_SuspendErase when FLS_17_DMU_IFX_FEE_USED is OFF.
	0000053912-3664	The Fls_17_Dmu_InitCheck() API return E_NOT_OK when FLS_17_DMU_USE_INTERRUPTS is ON.
	0000053912-3797	EVER error is not raised for the previous suspend erase.
	0000053912-3818	Writejob not processed when called immediately after SuspendErase.
	0000053912-3820	Compilation warnings in the Fls_lMainErase() API of Fls_17_Dmu.c.
	0000053912-3858	Variation point support was not working for few configurable items.
	0000053912-3928	Fls_17_Dmu_Isr() takes 12.5 ms to execute when safety is ON.
	0000053912-3953	Fls_WriteCmdCycles() API is proceeding if any of the SQER and PROER are set.
	0000053912-3954	Fls_lMainErase() is checking EVER error even when OPER error is set.
	0000053912-3815	Safety error not reported for invalid sector(e.g: 128) passed to the Fls_17_Dmu_VerifySectorErase() API.
	0000053912-3702	Removed the critical sections in FLS command sequence.
	0000053912-3532	Setting of read hard margin value and setting of tight marginvalue can be done together.
Gpt	0000053912-3304	Pulse notify mode feature is supported.
	0000053912-3545	The Gpt_EnableWakeup API generates Class 1 trap when DET and Safety Enable are OFF.
	0000053912-3575	Compilation warning observed with GNU/TASKING compiler.
	0000053912-3769	Compilation error for GPT_ENABLE_IRQ.
	0000053912-3152	The wake up interrupt should be enabled in the Gpt_SetMode API when called with parameter GPT_MODE_SLEEP, but it was wrongly enabled in the Gpt_EnableWakeup API.

Summary of changes

Table 10 Summary of changes from 1.0.0-beta to 1.0.0-rc (continued)

Module	Issue number	Description
Icu_17_TimerIp	0000053912-2700	GetInputState is not working for ERU in the Sleep mode with notifications disabled.
	0000053912-2855	With multicore and DET ON, a trap is raised if ICU channel is not allocated to master core and tries to call from Master core.
	0000053912-2857	TASKING compilation error if no channel allocated to the Master core.
	0000053912-3011	GetDutyCycleValues() returns improper values first time after init for GTM channels.
	0000053912-3081	Configuration issue (with IcuDefaultStartEdge) for a channel used to measure high time.
	0000053912-3084	Conflicting result when duty-cycle is measured after a stop/start of channel.
	0000053912-3112	Overflow of HIGH TIME and LOW TIME incorrectly detected.
	0000053912-3131	DutyCycle requirement update changes.
	0000053912-3150	Non-coherent values returned for DUTY, HIGH TIME, LOW TIME.
	0000053912-3524	ICU Max channel configured with wrong value is not throwing EB tresos generation error.
	0000053912-3580	Warnings are observed as wrong configuration is not giving a generation error.
	0000053912-3644	Icu_17_TimerIp_GetInputState returns wrong value after a particular sequence. P5: Call Icu_17_TimerIp_CheckWakeup function with wakeup source P6: Call Icu_17_TimerIp_SetMode to NORMAL MODE P7: Call Test_Icu_17_TimerIp_DisableWakeup function for the same channel
	0000053912-3785	Icu_17_TimerIp_GetTimeElapsed API gives compilation warnings.
	0000053912-3801	Icu_lTim_Isr gives compilation warnings.
	0000053912-3957	BSWMD GtmGetDutyCycle Exclusive area to be added.
	0000053912-3101	Configuration issue (with McuGtmSleepModeEnabled) when a wake-up enabled channel is configured.
	0000053912-4074	GPT12 clock initialization not done properly.
McalLib	0000053912-3552	The module Id and software version are missing in the McalLib_Bswmd.arxml file.

Summary of changes

Table 10 Summary of changes from 1.0.0-beta to 1.0.0-rc (continued)

Module	Issue number	Description
Mcu	0000053912-3941	Trap during clock initialization as wrong configuration allowed to generate during code generation.
	0000053912-3753	Compilation/linking errors in the Supervisor_User(SV_U) mode.
	0000053912-3666	Trap during initialization of Cluster configuration module.
	0000053912-3659	Trap during initialization of Clock management unit.
	0000053912-3651	The Mcu_InitCheck API fails to return E_OK with different clock settings.
	0000053912-3563	Incomplete code generation for GtmClusterConf if name is modified.
	0000053912-3536	Trap occurred in the Mcu_InitCheck API.
	0000053912-3535	Hanging issues while initializing clock without reset.
	0000053912-3533	CCUCON5 divider values are wrongly generated for ADAS, GEth and McanH peripherals.
	0000053912-3527	Mcu_17_Eru_GatingIsr is causing infinite loop for Icu_17_TimerIp_EnableEdgeDetection.
	0000053912-3508	Safety error needed for the Mcu_17_Gtm_TimChannelIsr API.
	0000053912-3444	Mcu_InitCheck unsuccessful with backup clock.
	0000053912-3347	Compilation issues due to undeclared identifier MCU_CLOCK_SETTING_DEFUALT_INDEX.
	0000053912-3342	Trap while de-initialization as GTM de-initialization attempted when GTM frequency is set to zero in configuration.
	0000053912-3306	Trap occurs while clock initialization when McuGTMFrequency is set to 0.
	0000053912-3296 0000053912-3200 0000053912-3199 0000053912-3202	BMD corrections as per the updated XDM files.
	0000053912-3132	New feature Mcu_GetRamState added.
	0000053912-3009	CCUCON LCK bit check added in Mcu.c as per Hardware document recommendations.
	0000053912-3088	The McuAscLinChannelAllocationConf parameter is changed to editable.
	0000053912-2887	When configuring VCO to 600 MHz and PLL frequency to 300 MHz, the allowed fGTM in MCU is only 100 MHz instead of 200 MHz.
	0000053912-2811	Mcu_17_Gtm_TomChannelIsr is not able to route to Wdg_17_Scu_Isr.
	0000053912-3350	Trap while initializing clock without reset.
	0000053912-3292	ERU interrupts not routed properly.

Summary of changes

Table 10 Summary of changes from 1.0.0-beta to 1.0.0-rc (continued)

Module	Issue number	Description
Mcu	0000053912-2803	Clock configuration generation error when setting McuClockReferencePointFrequency2 to 2e8 and setting the McuI2CFrequency to 6.6e7.
	0000053912-2503	The Mcu_17_Eru_GatingIsr API is giving additional safety error.
	0000053912-3340	Configuration plug-in names updated to match the AUTOSAR naming convention.
	0000053912-3344	Unused timer module initializations removed during MCU initialization.
Port	0000053912-4016	Port PDISC value getting generated for all pins instead of the Port PDIC available Ports only.
	0000053912-3799	Property file has Reserve keyword instead of Reserved.
	0000053912-3478	BMD file correction for PortPinId max value.
	0000053912-2898 0000053912-2631	BSWMD file corrections.
	0000053912-2871	Configuration issue for P10.7 as ALT2 is not selectable.
	0000053912-2448	Slow pads drive strength configuration added for PortPinOutputPadDriveStrength configuration parameter.
Pwm_17_GtmCcu6	0000053912-4028	InitCheck returns E_OK even when register is corrupted.
	0000053912-3963	Precompile guard missing in driver code leading to compiler warning.
	0000053912-3896	Glitch observed when duty is 100% in CCU6.
	0000053912-3528	Wrong Toutsel mapping when PwmHandleShiftByOffset is ON.
	0000053912-3341	Clock/prescaler generated for T12 comparators not unique.
	0000053912-3268	Compilation error is observed in the PWM_UnInitChIdCheck API with undeclared PWM_DEINITIALIZE_REQ error message.
	0000053912-3115	Init status variables are not split core-wise for CCU6 units.
	0000053912-3080	Missing CCU6 period match notification callback with two T12 comparators.
	0000053912-3002	Wrong compilation error message when PwmNotificationSupported is OFF.
	0000053912-2903	SetPeriodAndDuty new period value not updated when duty is 0%.
	0000053912-2488	Pwm_ISR is raising unexpected safety error by considering that the module is already de-initialized even when it is not initialized.
	0000053912-918	CCU6 configuration not throwing error if shifted period channel (CCU61 and T13) is referring to fixed period channel.

Summary of changes

Table 10 Summary of changes from 1.0.0-beta to 1.0.0-rc (continued)

Module	Issue number	Description
Spi	0000053912-3735	Separated the CommonPublishedInfomation and SpiPublishedInformation containers.
	0000053912-3564	Trap is observed in Spi_GetSequenceResult during hardware failure.
	0000053912-3544	Compilation issue as MCAL_NO_OF_CORES macro not available.
	0000053912-3482	Max core number is hardcoded in the template Spi_Cfg.h file.
	0000053912-3443	Async IB buffer size more than 256 bytes is not working.
	0000053912-3286	Maximum value for the SpiSyncTransmitTimeoutDuration parameter is corrected.
	0000053912-3283	In configuration when interruptible sequence feature is disabled when a high-priority sequence is requested for transmission sequence, high priority should be transmitted first though low-priority sequence in queue.
	0000053912-3281	Critical section is updated in the Spi_Synctransmit API.
	0000053912-3118	Check for error on Tx channel is missing.
	0000053912-3013	Data transfer not working in the IB mode for different data widths.
	0000053912-3001	Non-interruptible sequence is interrupted.
	0000053912-2968	Interruptible sequence not functional.
	0000053912-2793	Compiler warnings.
	0000053912-2486	DET is not reported for invalid channel type.
	0000053912-2304	Memmap section for BACON array changed to where kernel variables are defined from current 256-bit aligned section.
Wdg_17_Scu	0000053912-3298	Pre-compile macro WDG_17_SCU_INIT_CHECK_API is generated wrongly in the Wdg_17_Scu_Cfg.h file.
	0000053912-3198	Code generation error is generated if STM is set as Watchdog trigger and any other module is configured after STM in ResourceM.
	0000053912-2886	The configuration parameter Wdg/WdgSettingsConfig/ WdgSystemClockRef contains a wrong reference value.

3.2 Issues fixed in release 1.0.0-beta

This chapter describes the fixes for issues from previous version(s).

Table 11 Summary of changes from 1.0.0-alpha.1 to 1.0.0-beta

Module	Issue number	Description
Generic	0000053912-1926	An error is generated when a module is added in the EB tresos with default values.
	0000053912-1381	AMDC violation A207 is observed in the Port, Smu and McalLib modules.
	0000053912-1696	Ambiguous MemMap section names in Can, Smu and Crc.

Summary of changes

Table 11 Summary of changes from 1.0.0-alpha.1 to 1.0.0-beta (continued)

Module	Issue number	Description
Adc	0000053912-2246	Set power state issue for master and stand-alone kernels.
	0000053912-2341	Incorrect DET implementation for the ADC_E_CORE_GROUP_MISMATCH DET.
	0000053912-2285	No EB tresos error is reported, if AdcHwTrigTimer is set for software-triggered groups.
	0000053912-2028	When the slave core is initialized before the master core, the DET ADC_E_PARAM_CONFIG DET is reported instead of ADC_E_MASTER_CORE_UNINIT DET.
	0000053912-2014	Compilation fails when AdcDevErrorDetect and AdcSafetyEnable are OFF and AdcInitCheckApi is ON.
	0000053912-1848	Triggering ADC conversion based on gate signal through ERU leads to unexpected conversion at start-up if we are controlling the EVADC registers (ENGT of GxQMRi) by keeping fixed configuration to ERU registers (EICR) based on Gate signal (High/Low).
	0000053912-2341	Incorrect DET implementation for ADC_E_CORE_GROUP_MISMATCH.
	0000053912-2378	Running channels and result registers not cleared under critical section.
	0000053912-2701	Overflow occurs for the following local functions: Adc_lUpdateSlaveResult and Adc_lReadSlaveResult.
	0000053912-2468	The Adc_InitCheck API returns E_NOT_OK if AdcSyncConvEnable is True.
	0000053912-2465	A trap is observed if Adc_GetStreamLastPointer is passed with NULL_PTR as input parameter.

Summary of changes

Table 11 Summary of changes from 1.0.0-alpha.1 to 1.0.0-beta (continued)

Module	Issue number	Description
Can_17_McmCan	0000053912-2220	Re-entrant functions are implemented wrongly as non-re-entrant local functions are used.
	0000053912-2118	Compilation error occurs when only one hardware object of Receive type is configured.
	0000053912-2032	Compilation fails for TC39xB variant.
	0000053912-2009	Can_17_McmCan_MainFunction_Write_x() raises a trap when called to poll for the transmitted CAN messages.
	0000053912-2008	Can_17_McmCan_MainFunction_Read_x() raises a trap when called to poll for the received CAN messages.
	0000053912-2003	Can_17_McmCan_Init() does not report CAN_E_CONFIG_INVALID development error when called from master and slave cores with config pointers to different variants.
	0000053912-1985	Development error check for CAN_E_NOT_CONFIGURED is wrongly provided for CAN main function and DeInit API.
	0000053912-1958	Compilation error occurs when CanMultiCoreErrorDetect is OFF and CanDevErrorDetection is ON.
	0000053912-1941	The CanIf_Cbk.h file is wrongly included in the Can_17_McmCan.h file.
	0000053912-1887	Compilation error occurs when CanDevErrorDetection is OFF.
	0000053912-1879	A value of zero is returned as SwPduHandle for any CAN message transmitted from Can Controller0.
	0000053912-1875	CAN_INITIALIZED state is used instead of CAN _READY.
	0000053912-1724	Wrong check is used to determine invalid ControllerId input argument in multiple APIs.
	0000053912-1620	Node3 of CAN Kernel 0 does not transmit and receive CAN messages.
	0000053912-1544	Can_17_McmCan_SetIcomConfiguration () raises a trap when called with invalid controller Id.
	0000053912-1464	Multiple APIs raise a trap instead of reporting development error to DET when called prior to Can_17_McmCan_Init ().
	0000053912-1463	Can_17_McmCan_Init() raises a trap when called with NULL_PTR.
	0000053912-1462	Can_17_McmCan_SetControllerMode() does not return CAN_NOT_OK whenever it reports any development error.
	0000053912-955	Configurations for transmit/receive hardware objects having multiple period is not generated.
	0000053912-928	Wrong value generated for controller handle Id and hardware object handle Id.
	0000053912-1936	Can_17_McmCan_DeInit() and Can_17_McmCan_GetVersionInfo() only reports compilation error when CanDevErrorDetection is ON if called when CanDeInitApi and CanVersionInfoApi Configuration parameter are OFF, respectively.

Summary of changes

Table 11 Summary of changes from 1.0.0-alpha.1 to 1.0.0-beta (continued)

Module	Issue number	Description
Can_17_McmCan	0000053912-1842	Multicore support does not work.
	0000053912-2414	A trap is raised when Can_17_McmCan_MainFunction_Read_x() is called in the multicore environment.
	0000053912-2408	Array of size zero is generated in the generated configuration code.
	0000053912-2118	Compilation error occurs when only one hardware object of Receive type is configured.
	0000053912-1988	Can_17_McmCan_Write () does not report CAN_E_NOT_CONFIGURED development error when called with Hth configured for a controller, which is not mapped to the core from which API is called.
	0000053912-1804	Can_17_McmCan_Init() does not set the default baud rate correctly if any baud rate other than the first one is selected.
	0000053912-2407	Compilation warning is observed in the Can driver code and generated configuration file.
Crc	0000053912-2331	CRC_MCAL_USER1 mode is not available if CRC_SAFETYENABLE is OFF.
	0000053912-2244	Bswmd file correction is done for the re-entrant APIs.
Fee	0000053912-2347	Data in Flash is getting cleared after calling Fee init.
	0000053912-2335	QS erase not working; driver is not returning to the IDLE state.
	0000053912-2333	QS write for the third instance is not working.
	0000053912-2310	A trap is generated during every garbage collection.
	0000053912-2290	Initialized variable definition added under cleared variable section.
	0000053912-2286	Fee reaching illegal state during init.
	0000053912-2040	Calling Fee_17_GetQuasiStaticBlockInfo() corrupts the stack area.
	0000053912-2473	Data block is lost during GC.
	0000053912-2459	FEE_E_BUSY DET/SE is not raised for QS read/write operations.
	0000053912-2458	FEE_E_INVALID_BLOCK_LEN safety error is not raised for QS Read API.
	0000053912-2457	FEE_E_INVALID_BLOCK_LEN DET/SE is raised instead of FEE_E_INVALID_BLOCK_OFS.
	0000053912-2428	Calling Read/Write/Invalidate/Cancel APIs before calling Fee_Init() leads to a trap.
	0000053912-2418	QS erase request rejected if second block instance is passed.
	0000053912-2370	Driver is stuck in an infinite loop, if failed WL address is beginning of Dflash0.
	0000053912-2620	In the Fee_lQsBlockErase() API, while calculating the Blocksize there is a possibility of overflow based on the QS block configurations as blocksize is declared as uint16 whereas it needs to declared as uint32.
	0000053912-666	The driver stays in the MEMIF_BUSY state if written beyond threshold while GC is disabled.

Summary of changes

Table 11 Summary of changes from 1.0.0-alpha.1 to 1.0.0-beta (continued)

Module	Issue number	Description
Fee	0000053912-2368	Second failed WL address getting stored wrongly.
	0000053912-2349	Gaps in the data copied to the new sector, when data contains unconfigured blocks.
	0000053912-2044	Warning during build.
	0000053912-2037	FEE_E_UNINIT DET is not expected from Fee_GetStatus() API.
	0000053912-2287	QS block initialization (to erased state) is not done during virgin Flash init.
	0000053912-2243	QsM_Cbk.h header file inclusion missing in Fee_Cfg.h file.
	0000053912-2041	Incorrect service IDs are reported during DET/SE.
	0000053912-1456	Tresos generation fails on enabling variation post build.
	0000053912-1373	Job error notification is not raised when just registered write/ invalidate request is canceled.
	0000053912-1271	Two job error notifications coming for single QS job during fault injection test.
	0000053912-1264	Fee_17_EraseQuasiStaticData() returns E_OK even if configured NVM block number is passed as input.
	0000053912-1221	A trap is observed if APIs are called before calling the Fee_Init() function.
	0000053912-772	Fee_17_GetQuasiStaticBlockInfo() returns E_OK even if configured NVM block number is passed as input.
	0000053912-764	Fee_InvalidateBlock() is accepting job request even when driver is MEMIF_BUSY_INTERNAL.
	0000053912-628	QS block write is rejected if driver state is MEMIF_BUSY_INTERNAL.
	0000053912-610	Calling Fee_CancelAll() while GC erase is ongoing leads the driver to be stuck in BUSY_INTERNAL state.
	0000053912-555	The Fee_17_CancelAll() API is not working for Fee_Read(), which is just registered.
	0000053912-2313	Fee_17_GetCycleCount() giving wrong sector count after GC is interrupted and then GC is retriggered.
	0000053912-1334	Fee_17_GetPrevData() API immediately after GC reads the latest data.
	0000053912-1096	Config test failures.

Summary of changes

Table 11 Summary of changes from 1.0.0-alpha.1 to 1.0.0-beta (continued)

Module	Issue number	Description
Fls_17_Dmu	0000053912-2237	Fls_MainFunction raises runtime error 0x05 if Flash blank check job fails due to hardware error.
	0000053912-2208	Generated code in Fls_config structure has structure elements for RAM access code (legacy feature).
	0000053912-2128	FLS_E_UNINIT DET is not reported for the Fls_17_Dmu_IsHardeningRequired, Fls_17_Dmu_ControlTimeoutDet, Fls_17_Dmu_CancelNonEraseJobs, Fls_17_Dmu_CompareWordsSync APIs.
	0000053912-2127	Fls_17_Dmu_SuspendErase is not suspending ongoing erase operation.
	0000053912-2126	The Fls_17_Dmu_IsHardeningRequired API returns TRUE (hardening required) on the successful erased/written portion of the memory.
	0000053912-2125	Fls_17_Dmu_Erase not reporting DET (FLS_E_PARAM_LENGTH) when erase end address is not aligned to a Flash sector boundary.
	0000053912-1694	DET FLS_E_UNINIT is not reported for some of the APIs.
	0000053912-1692	Variation-specific PBCfg.c files are not created.
	0000053912-1483	Max line for FlsMaxReadFastMode and FlsMaxReadNormalMode is not limited to MAX Fls size configured in EB tresos.
	0000053912-1482	Interrupt mode should not be supported if Infineon Fee is used.
	0000053912-1480	DFlash wait cycles for Flash supported from 0 to 63 instead of 0x00 to 0xFF.
	0000053912-1469	The Fls_17_Dmu_Erase() API sets trap when misaligned sector address is passed.
	0000053912-2426	Runtime error is not reported when operation error occurs by Write and Erase APIs.
	0000053912-2342	Fls_17_Dmu_IsHardeningRequired not returning TRUE in presence of multi-bit error and dual-bit error.
	0000053912-2315	FLS_E_VERIFY_ERASE_FAILED DET is not reported by Fls_MainFunction for Erase Job.
	0000053912-2476	Sequence error during Fee_Write() is observed sporadically.
	0000053912-577	Fee driver is not coming to the normal state after reaching the illegal state due to FLS timeout DET.
	0000053912-2180	Wait time (tFL_MarginDel) after margin change not met.
	0000053912-1476	The Fls driver status should be set in the Fls_17_Dmu_Init() API.
	0000053912-2740	Compilation error in Fls_17_Dmu_CompareWordsSync() When RTE is ON.
	0000053912-2661	Sequence error reported for Fls Erase job due to compiler optimization.
	0000053912-2616	Warning in Fls driver code with Windriver compiler.

Summary of changes

Table 11 Summary of changes from 1.0.0-alpha.1 to 1.0.0-beta (continued)

Module	Issue number	Description
Gpt	0000053912-2387 0000053912-1622	Compilation warnings/errors.
	0000053912-2346	Compilation error occurs when GptDevErrorDetect and GptSafetyEnable is ON while GptMultiCoreErrorDetect is OFF.
	0000053912-2170	Slave core reports GPT_E_MASTER_UNINIT even though master core is initialized.
	0000053912-2114	Gpt_InitCheck does not return E_OK.
	0000053912-2004	Wrong inclusion of Gpt.h file in the Mcu_Cfg.h file.
	0000053912-1932	Wrong multicore DET values are reported.
	0000053912-1931	Compilation error occurs when GptDevErrorDetect, GptMultiCoreErrorDetect and GptSafetyEnable are OFF and GptPredefTimer100us32bitEnable is ON.
	0000053912-1701	Compilation error occurs while configuring GPT with 100 µs Predef timer only.
	0000053912-2613	Bswmd file wrongly points to Mcu_PBcfg.c instead of Gpt_PBcfg.c.
	0000053912-1774	Removed unnecessary GPT_STOP_SEC_CONST_ASIL_B_CORE0_8 section in Gpt_PbCfg.c as there was no corresponding START section.
Icu_17_TimerIp	0000053912-2396	Channel status is incorrect between mode switch.
	0000053912-2388	Get input state is not working when safety ON.
	0000053912-2366	IcuMeasurementMode post-build variant is not True.
	0000053912-2357	Warnings removed from the driver code in Tasking compiler.
	0000053912-2326	Notifications are not reported in the Sleep mode, if IcuReportWakeupSource= OFF.
	0000053912-2325	Overflow interrupt safety check condition is incorrect for GTM TIM ISR.

Summary of changes

Table 11 Summary of changes from 1.0.0-alpha.1 to 1.0.0-beta (continued)

Module	Issue number	Description
Icu_17_TimerIp	0000053912-2235 0000053912-1851 0000053912-2667	Compilation issue/errors.
	0000053912-2163	A trap is observed if ISR is invoked before ICU_init even if safety is enabled.
	0000053912-2072	Get Dutycycle API returns incorrect values with CCU6 if Activation Edge is FALLING edge.
	0000053912-2043	EDGE DETECTION is not working for TIM if configured in the Pulse Interrupt mode.
	0000053912-2024	Enable and disable notification APIs are not raising ICU_E_INVALID_MODE safety DET.
	0000053912-1996	Gpt12 edge count is inconsistent when ICU channel is configured in the Edge count mode using GPT12 Timer 5.
	0000053912-1986	A trap is observed if Icu_17_TimerIp_StopTimestamp is called on the Edge Counter channel.
	0000053912-1960	ICU_E_INVALID_NOTIF DET is reported for all input edges when notification is enabled in the master core.
	0000053912-1955	Get duty cycle returns active time > 24-bit value even safety enable.
	0000053912-1900	Duty cycle functionality is not working with CCU6.
	0000053912-1861	Derived config parameter names violate AUTOSAR standard.
	0000053912-2089	Init check API returns E_NOT_OK even if called immediately after the ICU init API.
McalLib	0000053912-2078	OS functions to support the User mode is wrongly defined.
	0000053912-1950	Mcal_GetGlobalPsprAddress (const uint32 CpuId, const uint32 LocalPsprAddress) is not implemented properly.
	0000053912-2103	Incorrect OS function syntax is used for the User mode implementation.
	0000053912-2002	The McalLib_Cfg.h file should not be included in the McalLib.c file.
	0000053912-1742	In the McalLib.c file, Schm_McalLib.h is included. This will lead to an error because Rte will generate Sch*M*_McalLib.
	0000053912-1618	The Os_Stub.h file is included in the McalLib_OsStub.h file.

Summary of changes

Table 11 Summary of changes from 1.0.0-alpha.1 to 1.0.0-beta (continued)

Module	Issue number	Description
Mcu	0000053912-2405	Mcu_Init and Mcu_InitCheck are not working correctly for SCU_PMSWCR1, SCU_PMSWCR4 and SCU_PMSWCR5.
	0000053912-2327	Mcu_Bswmd.arxml file has double entry <BSW-CALLED-ENTITY> without closing entry </BSW-CALLED-ENTITY> in between, therefore, the XML file is invalid.
	0000053912-2011	The Mcu_17_Gtm_TomChUpdateEnDis API is not setting the UPEN bit properly for the TOM channels belonging to TGC_1.
	0000053912-1954	PLLs are not locked when MCU_InitClock is called for a second time for a different configuration.
	0000053912-1949	MCU_InitClock does not function when backup clock is selected as an input to the clock distribution unit.
	0000053912-1944	Wrong options in McuPllInputSrcSelection as SYS_CLOCK_PIN_CLOCK_SRC_SELECT_SEL2 is not supported in the device.
	0000053912-1898	Plugin generates wrong Mcu_17_TimerIp_Cfg.h file for the Wdg user.
	0000053912-1772	Missing ApiInfix in the McupPlugin and bmd file.
	0000053912-1556	Missing error check in Xpath for ERU channel resource allocation.
	0000053912-2446	Mcu_17_Ccu6_TimerInitCheck is not working correctly for Timer T13.
	0000053912-1871	Incorrect DET reported for multicore-related DET.
	0000053912-1880	McuMCanClockSourceSelection and McuMCanFrequency configured parameter values are not getting generated in the configuration code.
	0000053912-2340	Mcu_17_Gpt12_TimerInitCheck will fail for MCU_GPT12_TIMER3.
	0000053912-1945	Missing error check for the McuClockSourceFailureNotification API added in EB tresos configurations.
	0000053912-2464	Mcu_17_Gpt12_TimerInitCheck is not reporting correct status for the GPT registers.
	0000053912-2698	McuRamSectorSettingId issue.
	0000053912-2692	CCUCON2 values are wrongly generated in TC38x.
	0000053912-2759	The Mcu_InitCheck API fails in the WindRiver compiler.
Port	0000053912-1965	EB tresos does not throw error for the following conditions when: • SetPinDirectionApi is made ON and in any PortContainer ->PortPinDirectionChangeable is made ON, then no error is generated. • If PortPinDirectionChangeable=ON and SetPinDirectionApi=OFF no error is thrown when Configuration is generated.
	0000053912-1964	Compilation issue for TC397_ADAS device.
	0000053912-2047	InitCheck API not returning ReturnValue E_OK.

Summary of changes

Table 11 Summary of changes from 1.0.0-alpha.1 to 1.0.0-beta (continued)

Module	Issue number	Description
Pwm_17_GtmCcu6	0000053912-2394	Const keyword missing in init prototype.
	0000053912-2245	Error checking is not performed for incorrect hardware resource allocation.
	0000053912-2079	PWM_INIT goes into a trap when NULL_PTR is passed (DET ON).
	0000053912-1979	PWM_CCU6_NOTIFI_STATUS_POS macro, when PwmNotificationSupport is OFF. Compilation error is observed for PWM_CONST_4 Macro, when PwmDevErrorDetect is OFF.
	0000053912-1971	Program flow is getting into a trap during API execution when the Pwm_17_GtmCcu6_Deinit() API is called in more than one core (for example, core 0, core 1 and core 2).
	0000053912-1872	PwmPeriodDefault incorrect data type in the EB tresos config.
	0000053912-1857	Rising edge notification is not coming for CCU6.
	0000053912-1801	The Pwm_17_GtmCcu6_SetPeriodAndDuty API raises unintended DET.
	0000053912-1799	GetOutput state API hits trap.
	0000053912-2478	The Det.h file is included even if DET is disabled.
	0000053912-2477	CCU6 notification callback is not aligned to respective edges.
	0000053912-2717	Compilation (or linking) issue.
Spi	0000053912-2400 0000053912-2389	Incorrect section name for core-specific variable in productive files.
	0000053912-2055	Spi_InitCheck API returns a DET instead of E_NOT_OK if any failure occurs.
	0000053912-1961 0000053912-2018 0000053912-1938 0000053912-1783 0000053912-1484	Compiler errors in the following conditions: • Spi driver configured in the User mode • Spi driver configured with Core 2 and Core 3 as master • Non-zero Kernel is configured • Synchronous mode GNU compilation warning • Variation Point
	0000053912-1947	Error check is missing for non-inclusion of Max Seq, job, channels and, hence, no values are filled in the Max Seq, Max job, Max channel containers.
	0000053912-1933	Jobs are not canceled after Spi cancel invocation.
	0000053912-1929	CS_VIA_GPIO chip-select polarity is inverted.
	0000053912-1897	Error is not reported during code generation in case data buffers size is more than 8191.

Summary of changes

Table 11 Summary of changes from 1.0.0-alpha.1 to 1.0.0-beta (continued)

Module	Issue number	Description
Spi	0000053912-1865	In multicore environment, if a sequence is being canceled, the status of sequence is updated in the logical index instead of the physical index due to which Spi_GetSequenceResult is not returning the expected result.
	0000053912-1822	MRST pins configuration in BMD are incomplete.
	0000053912-1795	Spi APIs are called without init results in trap instead of SPI_E_UNINIT DET being raised.
	0000053912-1739	Multiple extern declaration are generated in case same function is configured under multiple SpiJobEndNotification or SpiSeqEndNotification.
	0000053912-1738	Macro SPI_[core]_ENABLE is generated for core 6, which is not available in the TC3xx devices.
	0000053912-1727	Software-driven CS mode in synchronous communication does not function as intended.
	0000053912-1628	Wrong IB buffer size and total channels count per core.
	0000053912-1526	Continuous looping in synchronous transmission due to hardware failure.
	0000053912-1517	Spi_GetSequenceResult is called after init returns SPI_SEQ_FAILED instead of SPI_SEQ_OK when DEM is enabled.
	0000053912-1279	Autocalc delay limitation for SpiTimeClk2Cs.
	0000053912-2056	Incorrect boundary value for asynchronous SPI transfer.
	0000053912-2626	Multicore multi-Kernel compiler error.
	0000053912-2618	Spi_init check returns E_NOK.
	0000053912-2485	Compiler warning is observed in the multicore environment when SPI is configured for asynchronous Level 01 EB and Core 1 is configured as master core.
	0000053912-2734	Core5 IB count is not generated as expected.
	0000053912-2704	Incorrect range is generated for SpiInitDeInitApiMode and SpiRuntimeApiMode.
	0000053912-2702	User mode incorrect data access for CLC registers.
	0000053912-2619	Multicore asynchronous transmit with setup EB failure.
	0000053912-2758	Init de-init supervisor runtime user mode limitation.

Summary of changes

Table 11 Summary of changes from 1.0.0-alpha.1 to 1.0.0-beta (continued)

Module	Issue number	Description
Wdg_17_Scu	0000053912-2124	Class 1 TRAP is observed when we try to service the Wdg without Wdg initialization.
	0000053912-2384	Servicing of Wdg does not happen for STM trigger as CMP enable is not set by MCU.
	0000053912-2123	Class 4 trap is observed when we initialize the Wdg for core0 and then call the Setmode API with FAST_MODE from Core3.
	0000053912-2121	Memmap section is used for config root Wdg_17_Scu_Config_0 is different in PBCfg.c and PBCfg.h files.
	0000053912-1927	Timeout parameter passed to the Wdg_17_Scu_SetTriggerCondition API does not update the reload value accordingly.
	0000053912-1901	While setting STM interrupt during WDG operation, STM CMPVAL is written with wrong value in the Mcu_17_Stm_SetupCompareOperation().
	0000053912-1850	Does not compile because of undeclared identifier, Wdg_17_Scu_Config.

3.3 Issues fixed in release 1.0.0-alpha.1

This chapter describes the fixes for issues from previous version(s).

Table 12 Summary

Module	Issue number	Description
Can_17_McmCan	0000053912-1488	Compilation issue observed when working with 6 cores.
	0000053912-1481	Compilation error is observed when only CAN hardware objects of CanIdType EXTENDED are configured.
Gpt	0000053912-1752	Compilation error occurs while configuring GPT with 100 µs predef timer only.
	0000053912-1622	Compilation issue observed when core 4 or 5 is configured as master core.
Icu_17_TimerIp	0000053912-1621	Compilation issue observed when core 3 is configured as master core.
	0000053912-1475	Compilation warning is seen when configured with only CCU6 channels in signal measurement mode, and no GTM TIM Configured for signal measurement mode.
	0000053912-1471	ICU provides incorrect values in duty cycle measurement with CCU6.
	0000053912-1704	Compilation issues observed when core 4 or core 5 is configured as master core.
	0000053912-1465	Compilation issues when variation point is enabled due to incorrect config structure declaration in Pbcfg.h.

Summary of changes

Table 12 Summary (continued)

Module	Issue number	Description
Mcu	0000053912-1514	When McuPll2DivSelect is selected as MCU_K3_DIV_FACTOR_NOT_BYPASSED_SEL0, the code generation fails due to syntax error.
Port	0000053912-1470	Port 15 pins 0 and 1 are incorrectly configured for the Fast mode instead of the Slow mode.
Spi	0000053912-1450	SPI_NUM_SYNC_IB_CHANNELS_QSPIx for kernels 3 and 4 are generated with the incorrect values affecting the IB channels count (EB channel count not affected) for level delivered 0.
	0000053912-1202	Spi_GetStatus() function if called before Spi_Init() generates a trap.
	0000053912-1628	Wrong generated code for IB Buffer size and total count per core in case if the number of channels configured is beyond 10.
	0000053912-1509	In the Resource Manager module, the Spi module is missing for the multicore configuration.
	0000053912-1736	QSPI kernel 5 missed in SpiHWConfiguraion.
	0000053912-791	SPI driver accesses array with out-of-bound index.
	0000053912-1822	The SpiHWPinMRSTQspix parameter does not have the same range of configuration options in the bmd file as compared to the ranges given in the property file.

3.4 Issues fixed in release 1.0.0-alpha

This is the first Alpha delivery for the product.

4 Known issues

This chapter describes the prescribed workarounds for all the open issues identified.

Table 13 Known issues

Module	Issue number	Description
Can_17_McmCan	0000053912-2874	Impact: MCAN Erratum 20: Message transmitted with wrong arbitration and control fields no workaround implemented. Workaround: None
Fee	0000053912-4051	Impact: Warning in the driver file when block configuration has 256 QS blocks of 4 Kb each. Workaround: The total number of Quasi Static data blocks shall not exceed 255 blocks.
	0000053912-4049 0000053912-4050	Impact: When a sector used by the double-sector algorithm contains two un-erasable word lines, detected during GC, then the usable memory in this sector depends on the location of the second un-erasable word line. Memory space located before the second un-erasable word line remains unused. Workaround: None
	0000053912-4052	Impact: BCC value for QS block is incremented beyond the upper limit. Workaround: The total number of Quasi Static block erase/write cycles in the Quasi Static area of the DFlash0 memory should not exceed 500 and the number of erase/write cycles should be limited to 50 per Quasi Static block.
General	0000053912-3945	Impact: Potential issue due to TASKING compiler errata T TCVX-43309 and TCVX-43620. Workaround: The initial review has been done and no issues seen.

5 Limitations and deviations

This chapter describes the limitations and deviations due to software/hardware design constraints.

5.1 Limitations

Refer to the *Deviation and limitations* section in the respective MCAL User Manual.

5.2 Deviations

Table 14 Known limitations

Module name	Description	Impact on module
Tresos Tool/BMD	The BMD files provided in the package are not 100% compliant to AS4.2.2.	Following warnings are observed in the plug-in files: • Software version check: No corresponding BSW-IMPLEMENTATION node for component 'MOD' found. • Vendor ID check: No corresponding BSW-IMPLEMENTATION node for component 'MOD' found. • BSW-IMPLEMENTATION node should exist but was not found. ArMajorVersion/ArMinorVersion/ArPatchVersion/ SwMajorVersion/SwMinorVersion/SwPatchVersion/ VendorId/VendorApiInfix should not be set in the CommonPublishedInformation container in AUTOSAR Version 3.x or higher. Parameter maximum value should not be set with the value 'INF' in VSMD
	Limited variation point support.	Configuration testing with Variation Point Support is limited due to EB tresos tool issue. The tool hangs randomly with the variation points added.
	Multiplicity of the `Wdg/WdgSettingsConfig` container is not valid according to AUTOSAR standard parameter definition.	Since the container multiplicity is dependent on the number of watchdog timers/number of cores for a device. The multiplicity will be from 0 to 5. (According to AUTOSAR it is 1)
	Minimum value of the `Port/PortConfigSet/PortContainer/PortPin/PortPinId` parameter in VSMD (0) may not be smaller than minimum value defined in StMD(1).	As per the AURIX2G hardware, port number starts from 0 to max port. Therefore, the portpinId minimum value is given as 0 in VSMD
	DestinationRef of AUTOSAR reference `Gpt/GptDriverConfiguration/GptClockReferencePoint/GptClockReference` should be `/AUTOSAR/EcucDefs/Mcu/McuModuleConfiguration/McuClockSettingConfig/McuClockReferencePoint`.	The `McuClockReferencePointConfig` container contains the configuration (parameters) for the Clock settings of the MCU. Therefore, the reference is modified as per vendor-specific module definition.

Limitations and deviations

Table 14 Known limitations (continued)

Module name	Description	Impact on module
Tresos Tool/BMD	DefinitionRef of reference `Gpt/GptDriverConfiguration/GptClockReferencePoint/GptClockReference` with origin AUTOSAR_ECUC must start with `/AUTOSAR/EcucDefs/`.	McuClockReferencePointConfig is a non-AUTOSAR param. Therefore, the path should be AURIX2G only.
	Maximum value of the `Pwm/PwmChannelConfigSet/PwmChannel/PwmDutycycleDefault` parameter in VSMD (16777215) may not be larger than maximum value defined in StMD (32768).	To support non-AUTOSAR requirement, that is, PwmDutyShiftInTicks is ON range of Duty parameter should be 24 bit. Therefore, for this parameter max value for range attribute is deviated from AUTOSAR. Refer to the following for additional details: When PwmDutyShiftInTicks is OFF, the value is relative to period. (AUTOSAR range 16 bit) 0- 0x8000 When PwmDutyShiftInTicks is ON, the value is in absolute ticks. (Non-AUTOSAR range 24 bit) 0 to 0x8000, if PwmDutyShiftInTicks is STD_OFF for TOM/ATOM/CCU6 0 to 0xFFFF, if PwmDutyShiftInTicks is STD_ON and the module is TOM, CCU6 0 to 0xFFFFFF, if PwmDutyShiftInTicks is STD_ON and the module is ATOM
	Maximum value of the `Pwm/PwmChannelConfigSet/PwmChannel/PwmPeriodDefault` parameter in VSMD (16777215) may not be larger than maximum value defined in StMD (Inf).	Period input is taken in ticks instead of seconds. Range of Period parameter should be 24 bit. Therefore, for this parameter max value for range attribute is deviated from AUTOSAR. Refer to the following additional details: 0 to 0xFFFF, if module is TOM, CCU6 0 to 0xFFFFFF, if module is ATOM
	According to AUTOSAR standard parameter definition `Pwm/PwmChannelConfigSet/PwmChannel/PwmPeriodDefault` should be ECUC-FLOAT-PARAM-DEF	AUTOSAR insists period value to be given in terms of seconds. But in current PWM implementation period value is given in terms of ticks. Therefore, PwmPeriodDefault type is changed to integer.
	Multiplicity of the `Pwm/PwmGeneral/PwmDutycycleUpdatedEndperiod` parameter is not valid according to AUTOSAR standard parameter definition.	This parameter decides duty cycle update is coherent (end of cycle)/ non-coherent (immediate) for all PWM channels. This is a non-AUTOSAR requirement to select coherency channel wise. Hence, when channel wise selection is enabled this parameter should be disabled. Therefore, the multiplicity is zero.

Table 14 Known limitations (continued)

Module name	Description	Impact on module
Tresos Tool/BMD	Multiplicity of `Pwm/PwmGeneral/PwmPeriodUpdatedEndperiod` parameter is not valid according to AUTOSAR standard parameter definition.	This parameter decides period update is coherent (end of cycle)/ non-coherent (immediate) for all PWM channels. To support non-AUTOSAR requirement to select coherency channel wise. When channel wise selection is enabled this parameter this parameter should be disabled. Therefore, the multiplicity is zero.

5.2.1 HIS-MISRA violations

Table 15 MISRA violations due to SFR access / compiler intrinsic functions and AUTOSAR

MISRA_2012_Rule	Rule description	Justification for deviation	Modules applicable
1.3	There shall be no occurrence of undefined or critical unspecified behavior	This rule violation is agreed as we need to store the address passed is in the called function in many scenarios.	Adc, Can_17_McmCan, Fee, Fls_17_Dmu, Icu_17_TimerIp, Pwm_17_GtmCcu6, Spi, Wdg_17_Scu
2.5	A project should not contain unused macro declarations	Allowed violations as macros used in different configuration.	Fls_17_Dmu, Icu_17_TimerIp, Pwm_17_GtmCcu6, Spi
4.6	Typedefs that indicate size and signedness should be used in place of the basic numerical types	Basic numerical type - int/ unsigned int * is used while invoking compiler intrinsic functions. These compiler * intrinsic functions are implemented specific to TriCore™. Hence to align * with compiler declaration, use of unsigned int is mandatory.	Fee, Icu_17_TimerIp, McalLib
4.9	A function should be used in preference to a function-like macro where they are interchangeable	Allowed violations in cases where function like macro, '*_GetVersionInfo', and intrinsic macros.	Adc, Can_17_McmCan, Crc, Fee, Fls_17_Dmu, Gpt, Icu_17_TimerIp, McalLib, Mcu, Pwm_17_GtmCcu6, Port, Spi, Wdg_17_Scu
4.10	Precautions shall be taken in order to prevent the contents of a header file being included more than once	Allowed violations in case where Mod_Memmap.h is repeatedly included without include guard. This is as per AUTOSAR.	Adc, Can_17_McmCan, Crc, Dio, Fee, Fls_17_Dmu, Gpt, Icu_17_TimerIp, McalLib, Mcu, Pwm_17_GtmCcu6, Port, Spi, Wdg_17_Scu

Limitations and deviations

Table 15 MISRA violations due to SFR access / compiler intrinsic functions and AUTOSAR (continued)

MISRA_2012_Rule	Rule description	Justification for deviation	Modules applicable
5.1	External identifiers shall be distinct	Allowed violations in cases where external identifiers are going beyond 32 chars (some due to AS naming conventions, some due to module design, but mostly in generated code.)	Adc, Can_17_McmCan, Crc, Dio, Fee, Fls_17_Dmu, Gpt, Icu_17_TimerIp, Mcu, Pwm_17_GtmCcu6, Port, Spi, Wdg_17_Scu
5.2	Identifiers declared in the same scope and name space shall be distinct	Allowed violations in cases where external identifiers are going beyond 32 chars (some due to AS naming conventions, some due to module design, but mostly in generated code.)	Adc, Can_17_McmCan, Crc, Dio, Fee, Fls_17_Dmu, Gpt, Icu_17_TimerIp, Mcu, Pwm_17_GtmCcu6, Port, Spi, Wdg_17_Scu
5.4	Macro identifiers shall be distinct	Allowed violations in cases where external identifiers are going beyond 32 chars (some due to AS naming conventions, some due to module design, but mostly in generated code.)	Adc, Can_17_McmCan, Crc, Dio, Fee, Fls_17_Dmu, Gpt, Icu_17_TimerIp, Mcu, Pwm_17_GtmCcu6, Port, Spi, Wdg_17_Scu
5.5	Identifiers shall be distinct from macro names	Allowed violations in cases where Macro names are going beyond 32 chars (some due to AS naming conventions, some due to module design, but mostly in generated code.)	Adc, Can_17_McmCan, Crc, Dio, Fee, Fls_17_Dmu, Gpt, Icu_17_TimerIp, Mcu, Pwm_17_GtmCcu6, Port, Spi, Wdg_17_Scu
8.4	A compatible declaration shall be visible when an object or function with external linkage is defined	Allowed violations for following intrinsic functions: IMASKLDMST, EXTRACT.	Fee, Fls_17_Dmu, Mcu, Spi
8.9	An object should be defined at block scope if its identifier only appears in a single function	Global constants not declared within block scope, but used only in one function. Declaring const in a API scope may lead to confusion.	Adc, Crc, Icu_17_TimerIp, Mcu, Spi
8.13	A pointer should point to a const-qualified type whenever possible	Use of assembly instruction on some address pointers, hence cannot pass them as const.	Adc, Icu_17_TimerIp, Mcu, Pwm_17_GtmCcu6, Port

Limitations and deviations

Table 15 MISRA violations due to SFR access / compiler intrinsic functions and AUTOSAR (continued)

MISRA_2012_Rule	Rule description	Justification for deviation	Modules applicable
11.4	A conversion should not be performed between a pointer to object and an integer type	Allowed violations in cases where rule is violated for SFR access only.	Adc, Can_17_McmCan, Fls_17_Dmu, Icu_17_TimerIp, Mcu, Spi
11.5	A conversion should not be performed from pointer to void into pointer to object	Allowed violations as internal function performs initialization 1 byte at a time, for such operations pointer type conversion is required.	Dio, Gpt, Icu_17_TimerIp, McalLib, Mcu, Pwm_17_GtmCcu6, Port, Spi
11.6	A cast shall not be performed between pointer to void and an arithmetic type	Allowed violations for SFR access only.	Adc, Can_17_McmCan, Fls_17_Dmu, Icu_17_TimerIp, Mcu, Spi
11.8	A cast shall not remove any const or volatile qualification from the type pointed to by a pointer	Allowed violation for SFR access only and the solution gives compile time warning with different compilers.	Adc, Crc, Fee, Fls_17_Dmu, Icu_17_TimerIp, McalLib, Mcu, Pwm_17_GtmCcu6, Port, Spi
18.4	The +, -, += and -= operators should not be applied to an expression of pointer type	Allowed violation in cases where pointer arithmetic other than array indexing is used.	Adc, Dio, Fee, Fls_17_Dmu, Gpt, Icu_17_TimerIp, Mcu, Pwm_17_GtmCcu6, Port
19.2	The union keyword should not be used	Allowed violation in cases where pointer arithmetic other than array indexing is used for SFR access.	Adc, Can_17_McmCan, Icu_17_TimerIp, Mcu, Spi, Wdg_17_Scu
20.1	#include directives should only be preceded by pre-processor directives or comments	Allowed violations in cases where declaration before #include memap.h as per the AUTOSAR.	Adc, Can_17_McmCan, Crc, Dio, Fee, Fls_17_Dmu, Gpt, Icu_17_TimerIp, McalLib, Mcu, Pwm_17_GtmCcu6, Port, Spi, Wdg_17_Scu

Table 16 MISRA violations in drivers

MISRA_2012_Rule	Rule description	Justification for deviation	Modules applicable
2.2	There shall be no dead code	Values are assigned in assembly instructions, so they are actually used and not dead code.	Adc, Dio, Gpt, Icu_17_TimerIp, Mcu, Pwm_17_GtmCcu6, Port
2.7	There should be no unused parameters in functions	Parameters are used in assembly instructions, so they are actually used.	Adc, Dio, Icu_17_TimerIp, Mcu, Pwm_17_GtmCcu6

Table 16 MISRA violations in drivers (continued)

MISRA_2012_Rule	Rule description	Justification for deviation	Modules applicable
8.7	Functions and objects should not be defined with external linkage if they are referenced in only one translation unit	The extern declaration should be done by application. Hence, the structure is not made static.	Fee, Spi
10.1	Operands shall not be of an inappropriate essential-type	The code is reviewed to ensure there are no side effects foreseen by violating this.	Icu_17_TimerIp
10.3	The value of an expression shall not be assigned to an object with a narrower essential type or of a different essential type category	DataType is defined as enum to differentiate between type of data NORMAL DATA and IMMEDIATE DATA. It is defined as enum to increase the readability of the code such that the values being used could be identified. Changing this will cause the code maintainability and readability to be compromised.	Adc, Fee, Mcu, Port, Spi
10.4	Both operands of an operator in which the usual arithmetic conversions are performed shall have the same essential type category	Typecasting is done. Types are same and hence no issue is seen.	Fee, Fls_17_Dmu, Icu_17_TimerIp, Spi
10.5	Impermissible cast; cannot cast from 'essentially unsigned' to 'essentially enum'.	DataType is defined as enum to differentiate between type of data NORMAL DATA and IMMEDIATE DATA. It is defined as enum to increase the readability of the code such that the values being used could be identified. Changing this will cause the code maintainability and readability to be compromised.	Mcu

Limitations and deviations

Table 16 MISRA violations in drivers (continued)

MISRA_2012_Rule	Rule description	Justification for deviation	Modules applicable
10.8	The value of a composite expression shall not be cast to a different essential type category or a wider essential type	Impermissible cast of composite expression used for hardware descriptor access. Hence no issues are seen.	Fls_17_Dmu
11.3	A cast shall not be performed between a pointer to object type and a pointer to a different object type	Cast performed between a pointer to object type and a pointer to a different object type due to SFR access.	Can_17_McmCan, Crc, Dio, Fee, Fls_17_Dmu, Gpt, Icu_17_TimerIp, McalLib, Mcu, Pwm_17_GtmCcu6, Port, Spi, Wdg_17_Scu
13.2	The value of an expression and its persistent side effects shall be the same under all permitted evaluation orders	No side effects foreseen. This rule violation is agreed as we need to store the address passed in the called function in many scenarios.	Fls_17_Dmu, Wdg_17_Scu
13.5	The right hand operand of a logical && or || operator shall not contain persistent side effects	SFR register which is volatile is used to check for condition directly. It is checked in the timeout count while loop. The checked value does not keep changing. It is checked only for transition from 0 to 1. Hence, it is not an issue.	Crc, Fls_17_Dmu
15.4	More than one 'break' terminates loop [MISRA 2012 Rule 15.4, advisory]	Terminating the loop is required, since every element needs to be checked before inserting in Queue.	Spi
18.1	A pointer resulting from arithmetic on a pointer operand shall address an element of the same array as that pointer operand	The timer values are read from status register and therefore value of timer is within range.	Adc, Crc, Fee
20.10	The # and ## pre-processor operators should not be used	Function like macro used to call the TriCore™ intrinsic function, and reviewed to confirm no side effects.	McalLib

6 Support packages

Attention: ***The following information is given for evaluation purposes only. Modifications to these packages are made at your own risk.***

6.1 Build environment

Table 17 Build environment

Folder name	Description
Tools\ Bifaces	Contains tools for the Build environment

6.1.1 Open source software

The `Tools\Bifaces` folder contains items that are governed by Open Source Software.

The following table lists details related to copyright information, licensing terms and additional information (for example, how to obtain the source code of such Open Source Software).

Table 18 Bifaces and tools

Folder name	Copyright and licensing details
`bin`	Contains GNU tools. GNU General Public License, version 2 (GPLv2): ***https://www.gnu.org/licenses/old-licenses/gpl-2.0.en.html*** GNU General Public License, version 3 (GPLv3): ***https://www.gnu.org/licenses/gpl.html***
`DocTools\doxygen`	Contains Doxygen tool. GNU General Public License, version 2 (GPLv2): ***https://www.gnu.org/licenses/old-licenses/gpl-2.0.en.html***
`DocTools\Graphviz`	Contains Graph tool. Common Public License, version 1.0 (CPL-1.0) ***https://opensource.org/licenses/cpl1.0.php***

`Php\license.txt`
`Php\php.exe`
`Php\php5.dll`
	Contains PHP script interpreter.
	PHP License, version 3.01
	http://php.net/license/3_01.txt

6.2 Example demo application

These files contain the TC38xA demo routines. The following table describes different folders/files.

Table 19 Demo workspace

Folder / file name	Description
`\DemoWorkspace\McalDemo\0_Src`	Contains the source files needed to run the Demo application

Support packages

Table 19 Demo workspace (continued)

Folder / file name	Description
\DemoWorkspace\McalDemo\1_ToolEnv	Contains the tools necessary to build the Demo application
DemoAppBuild.bat	Batch file that can be used to build the Demo application

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