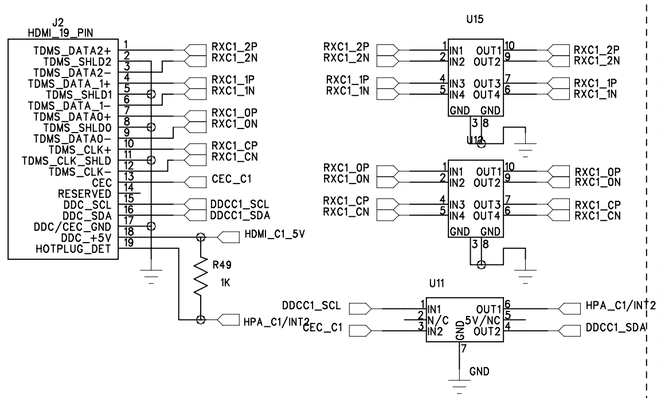
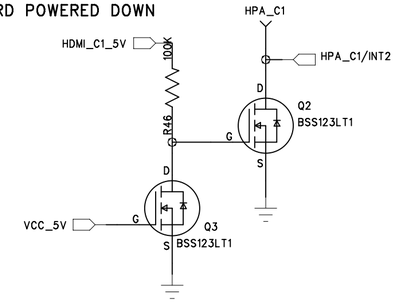
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

HDMI Port A – Connector and ESD Suppression

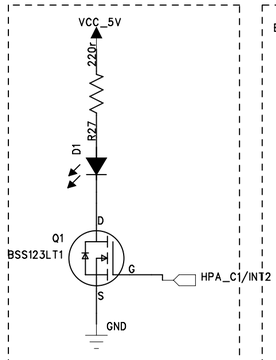


HPD A

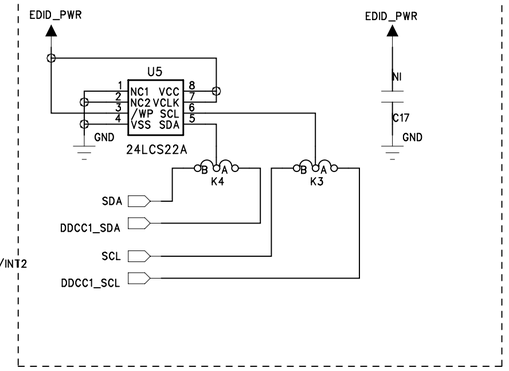


INSERT THIS ONLY WHEN NO EXT. EDID

HPD A LED

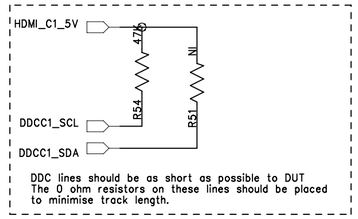


EXT EDID1



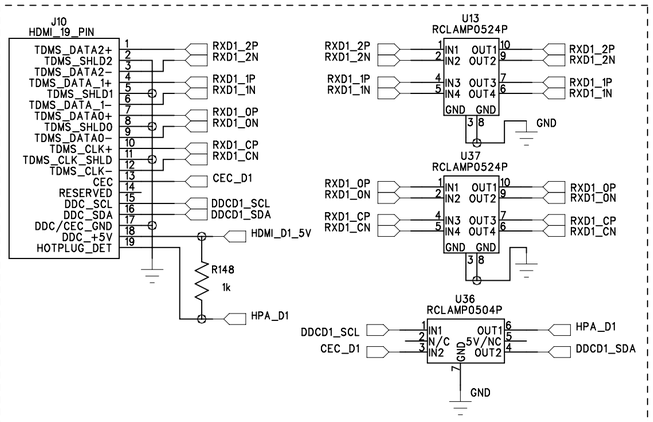
INSERT ONLY ONE: U5 OR Q3+Q2+R46

DDC A Circuitry

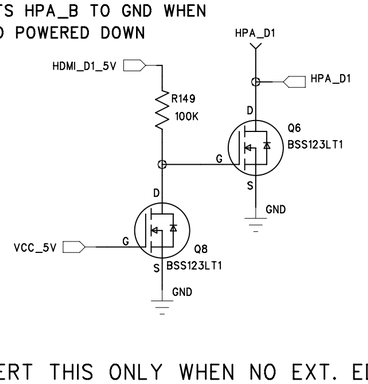


DDC lines should be as short as possible to DUT
The 0 ohm resistors on these lines should be placed to minimise track length.

HDMI Port B – Connector and ESD Suppression

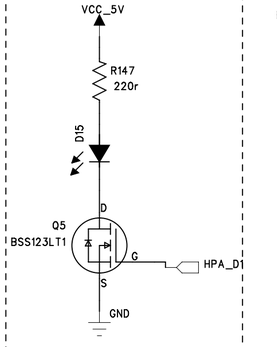


HPD B

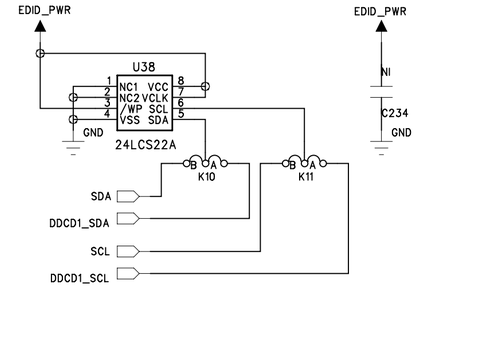


INSERT THIS ONLY WHEN NO EXT. EDID

HPD B LED

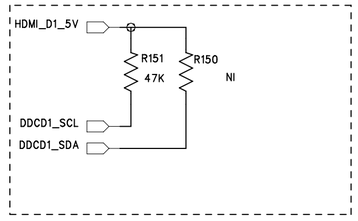


EXT EDID2

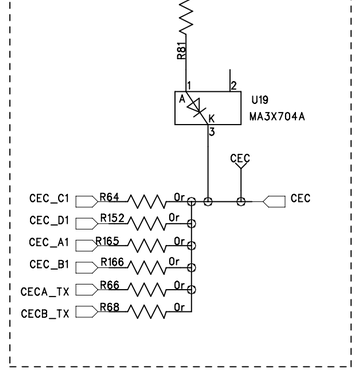


INSERT ONLY ONE: U38 OR Q8+Q6+R149

DDC B Circuitry



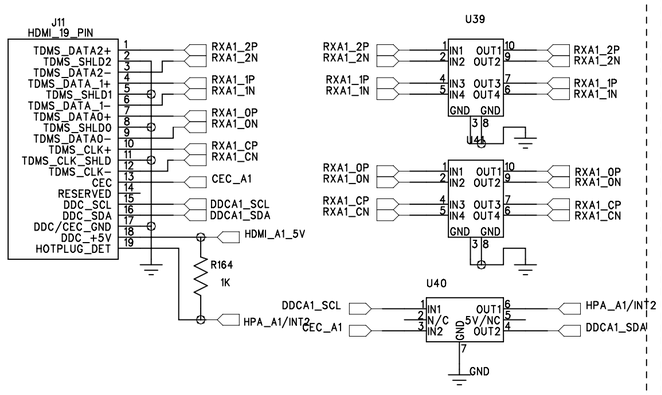
CEC To 168-Pin Connector



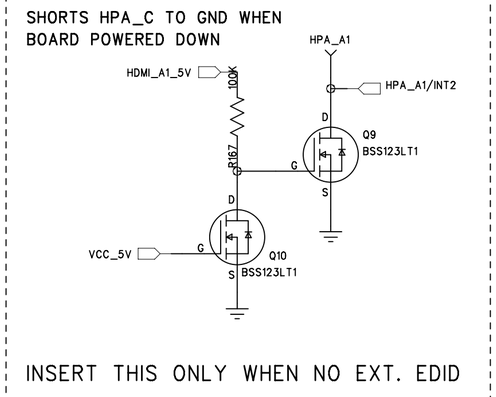
DRAWN:	DATED: 10/07/10	COMPANY: Analog Devices			
CHECKED:	DATED:	TITLE: ATV Group Dual ADV7612 Eval Board: HDMI Connector Sheet 1			
QUALITY CONTROL:	DATED:	CODE:	SIZE:	DRAWING NO:	REV: 0
RELEASED:	DATED:	SCALE:		SHEET: 1 OF 10	

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

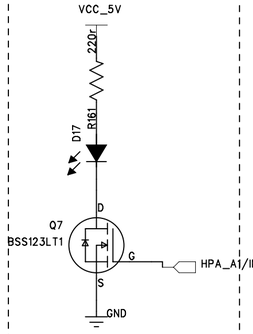
HDMI Port A – Connector and ESD Suppression



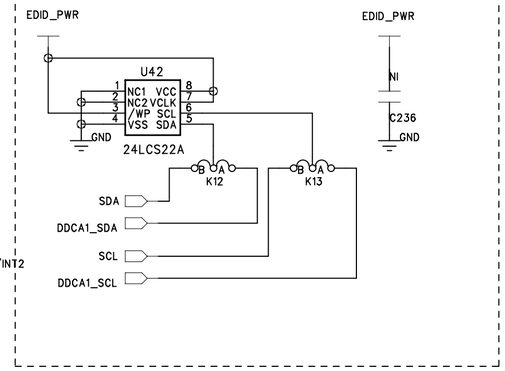
HPD A



HPD A LED

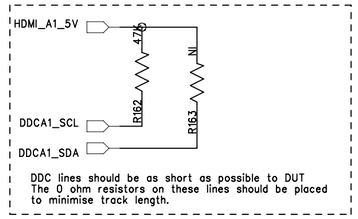


EXT EDID1



INSERT ONLY ONE: U42 OR Q10+Q9+R167

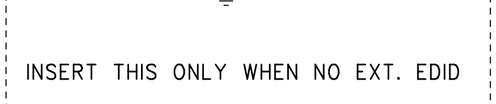
DDC A Circuitry



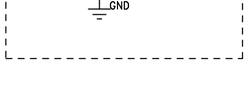
DDC lines should be as short as possible to DUT
The 0 ohm resistors on these lines should be placed to minimise track length.

HDMI Port B – Connector and ESD Suppression

HPD B



HPD B LED



EXT EDID2

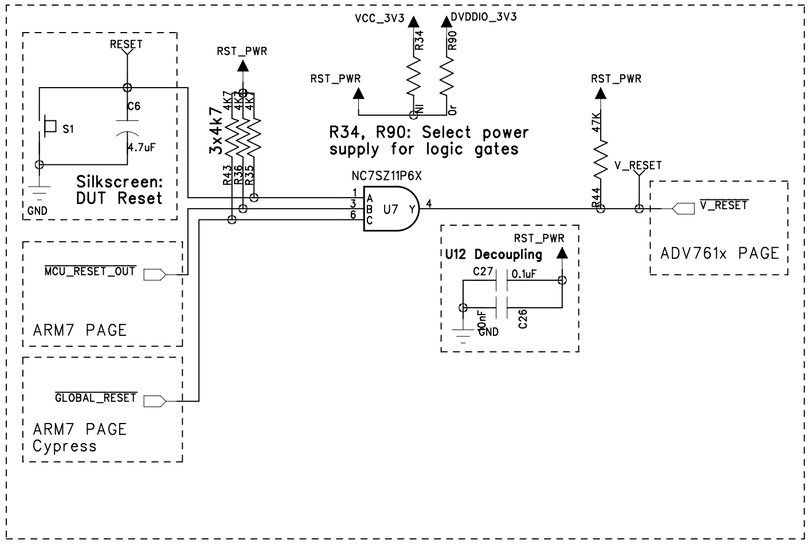
INSERT ONLY ONE: U47 OR Q13+Q12+R171

DDC B Circuitry

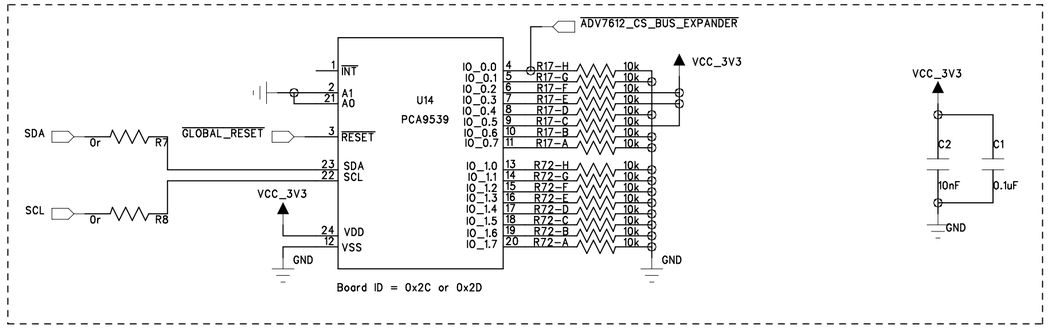
DRAWN:	DATED: 10/07/10	COMPANY: Analog Devices			
CHECKED:	DATED:	TITLE: ATV Group Dual ADV7612 Eval Board: HDMI Connector Sheet 2			
QUALITY CONTROL:	DATED:	CODE:	SIZE:	DRAWING NO:	REV: 0
RELEASED:	DATED:	SCALE:		SHEET: 2 OF 10	

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

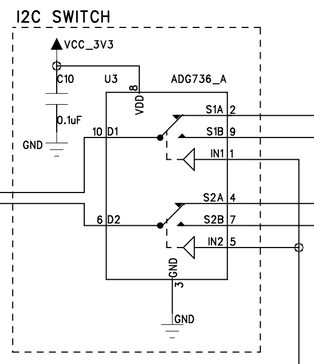
Reset Circuitry



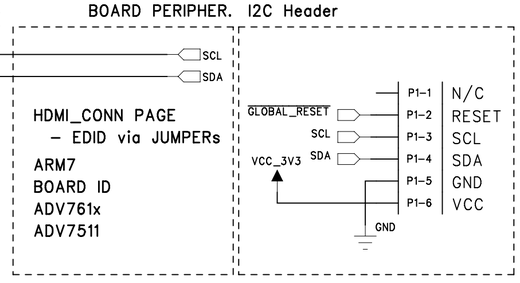
Board Identification Bus Expander



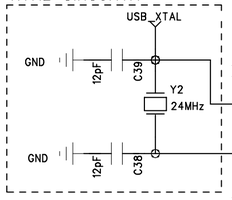
I2C SWITCH



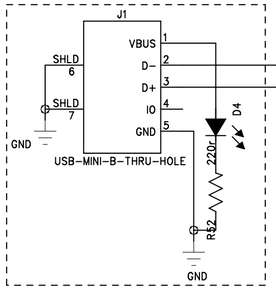
BOARD PERIPHER. I2C Header



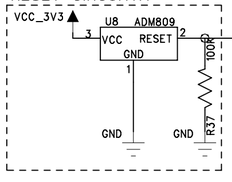
XTAL CIRCUITRY



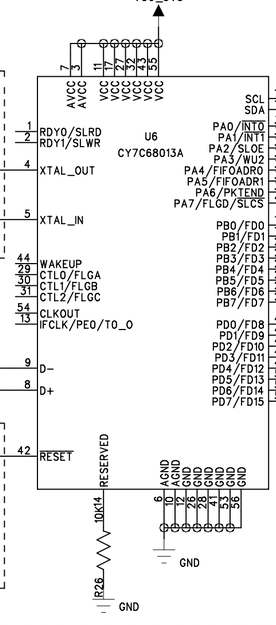
USB CONNECTOR



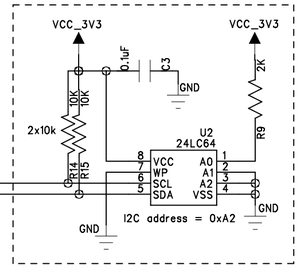
RESET CIRCUITRY



U6 CY7C68013A



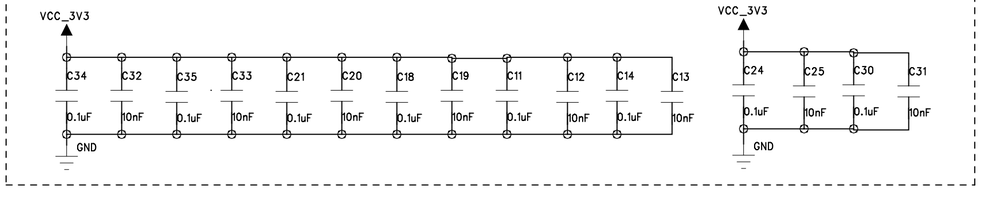
USB PROM



RESET1
0r
R42
GLOBAL_RESET
VCC_3V3
K5
1K
R41
GND

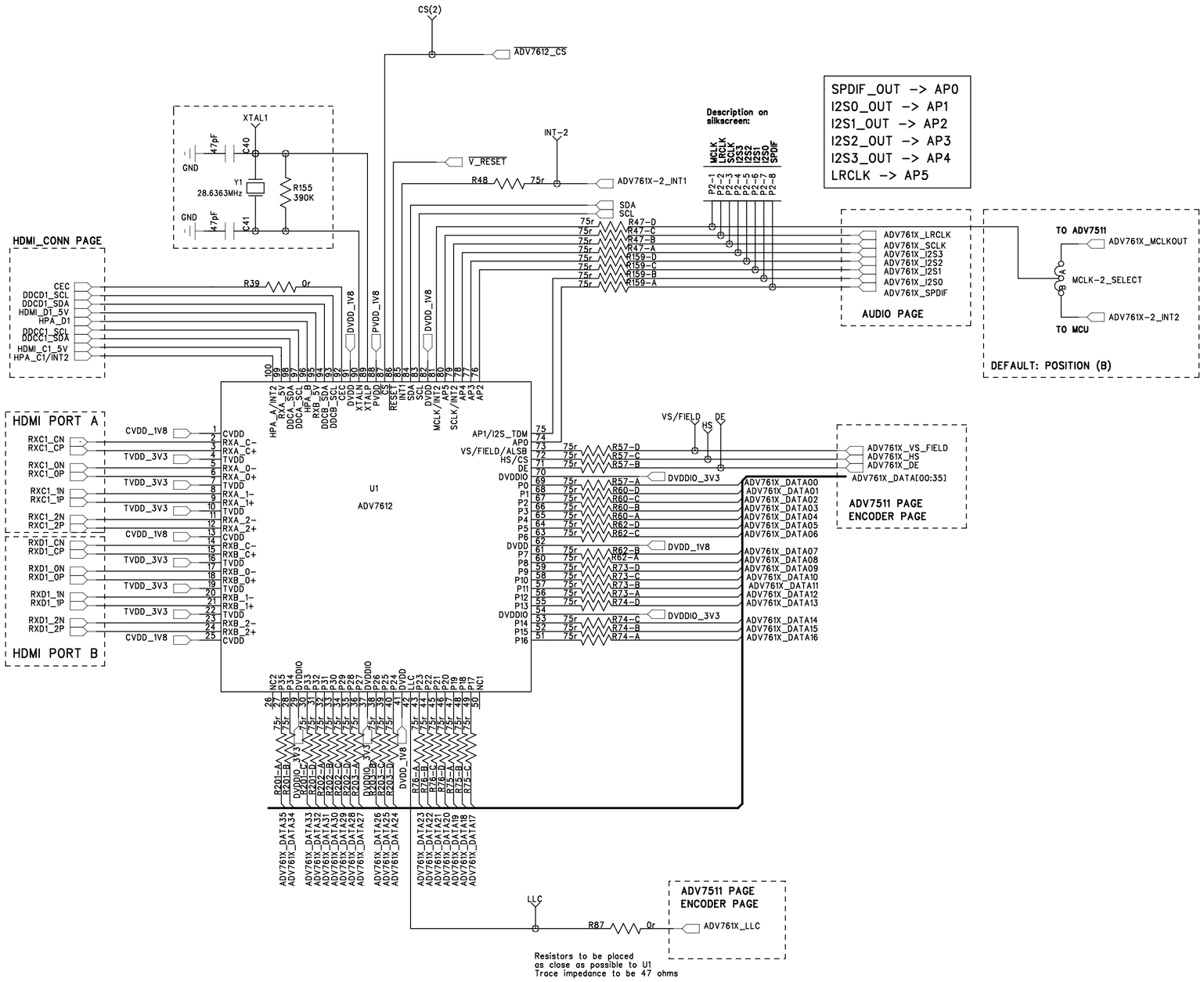
Line controlls I2C switch:
0 = PROM
1 = BOARD
After loading the PROM into Cypress – line is programmed HI

U19 Decoupling

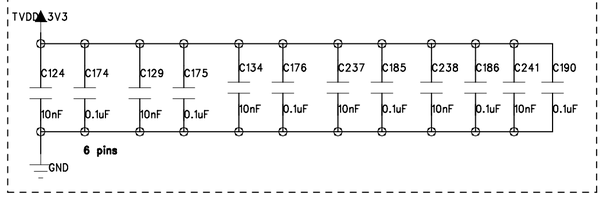


COMPANY:	Analog Devices		
TITLE:	ATV Group Dual ADV7612 Eval Board: USB+RESET		
DRAWN:	DATED: 10/07/10	CODE:	SIZE:
CHECKED:	DATED:	DRAWING NO:	REV: 0
QUALITY CONTROL:	DATED:		
RELEASED:	DATED:	SCALE:	SHEET: 3 OF 10

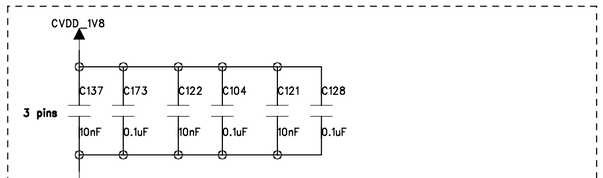
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



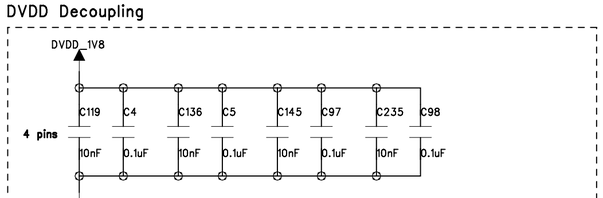
TVDD Decoupling



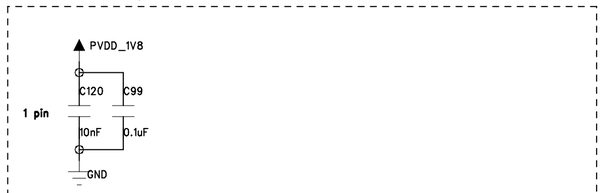
CVDD Decoupling



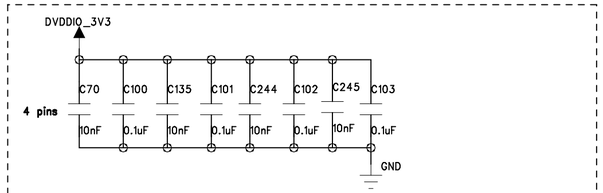
DVDD Decoupling



PVDD Decoupling

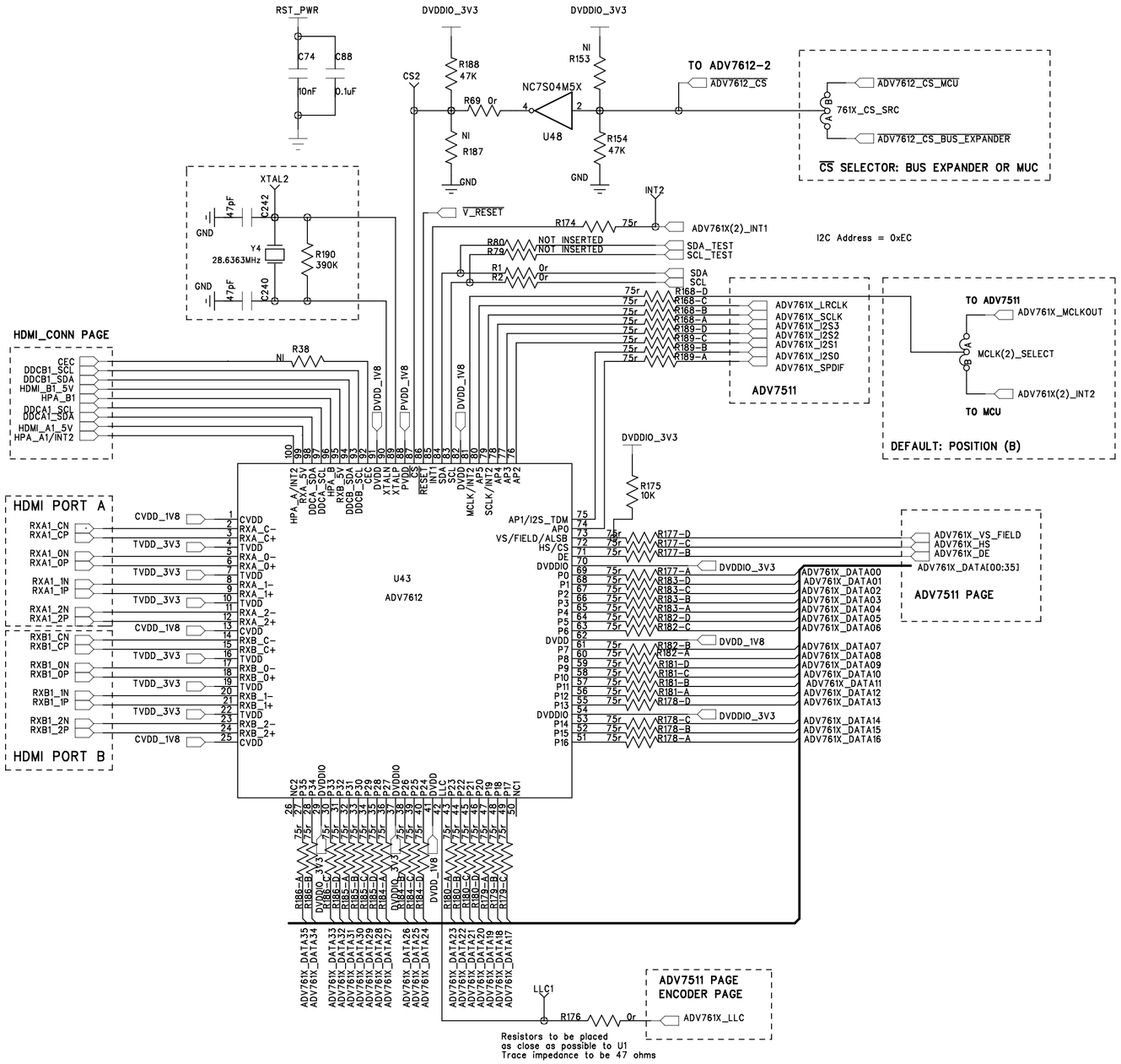


DVDDIO Decoupling

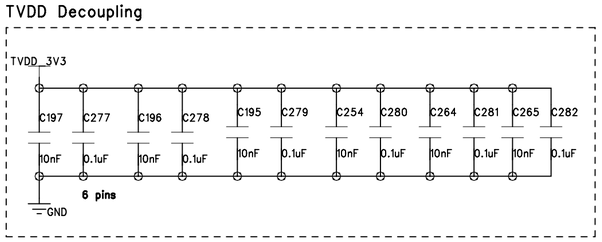


DRAWN:	DATED: 10/07/10	COMPANY: Analog Devices	
CHECKED:	DATED:	TITLE: ATV Group Dual ADV7612 Eval Board: ADV761X(1) Sheet	
QUALITY CONTROL:	DATED:	CODE:	SIZE: DRAWING NO: REV:
RELEASED:	DATED:	SCALE:	SHEET: 4 OF 10

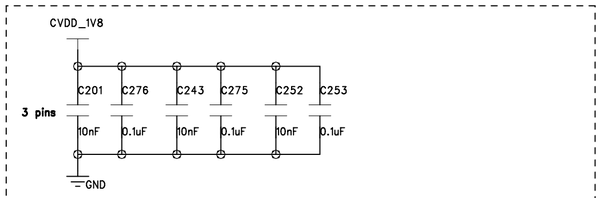
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



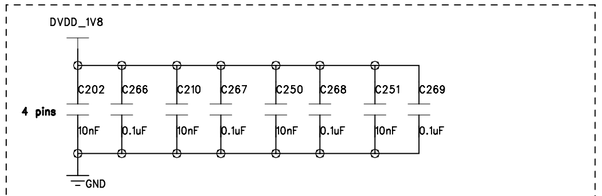
TVDD Decoupling



CVDD Decoupling

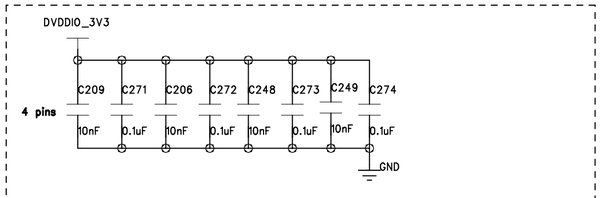


DVDD Decoupling

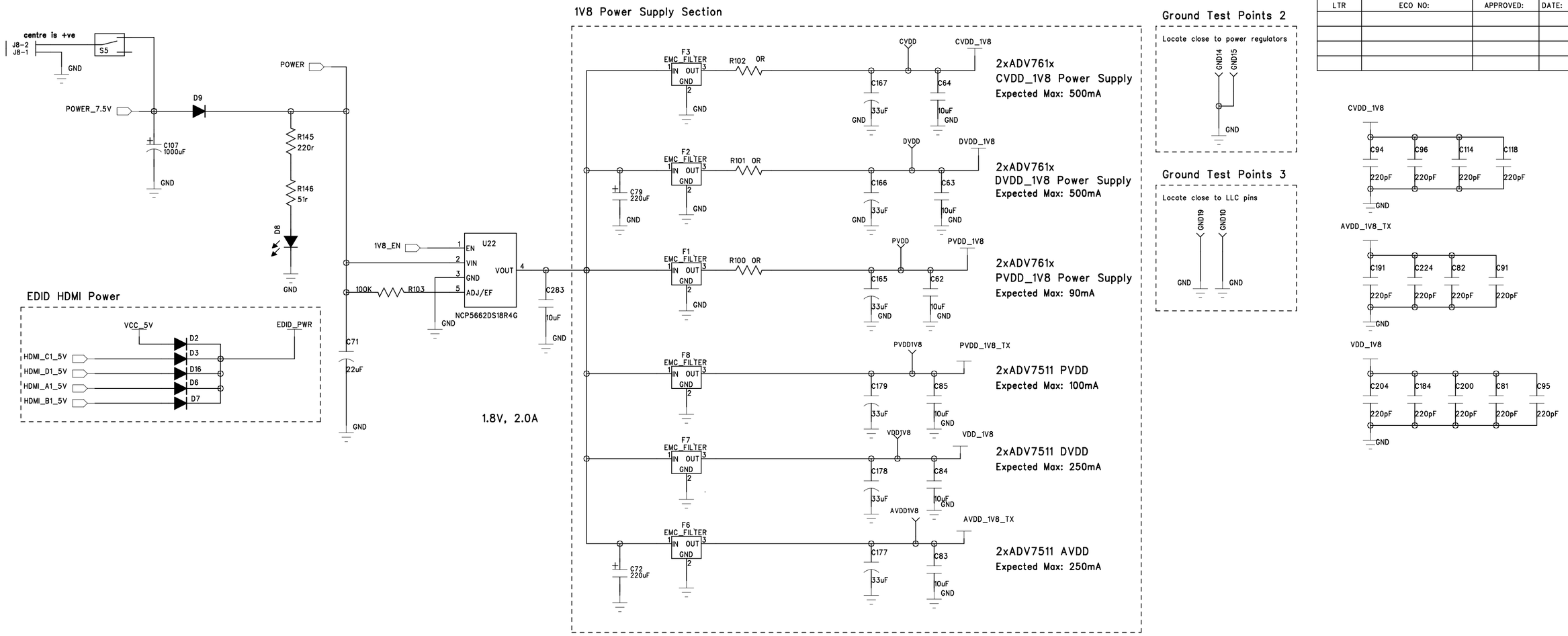


PVDD Decoupling

DVDDIO Decoupling



DRAWN:	DATED: 10/07/10	COMPANY: Analog Devices	
CHECKED:	DATED:	TITLE: ATV Group Dual ADV7612 Eval Board: ADV761X(2) Sheet	
QUALITY CONTROL:	DATED:	CODE:	SIZE: DRAWING NO: REV:
RELEASED:	DATED:	SCALE:	SHEET: 5 OF 10



REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

DRAWN:	DATED: 10/07/10		
CHECKED:	DATED:		
QUALITY CONTROL:	DATED:		
RELEASED:	DATED:		

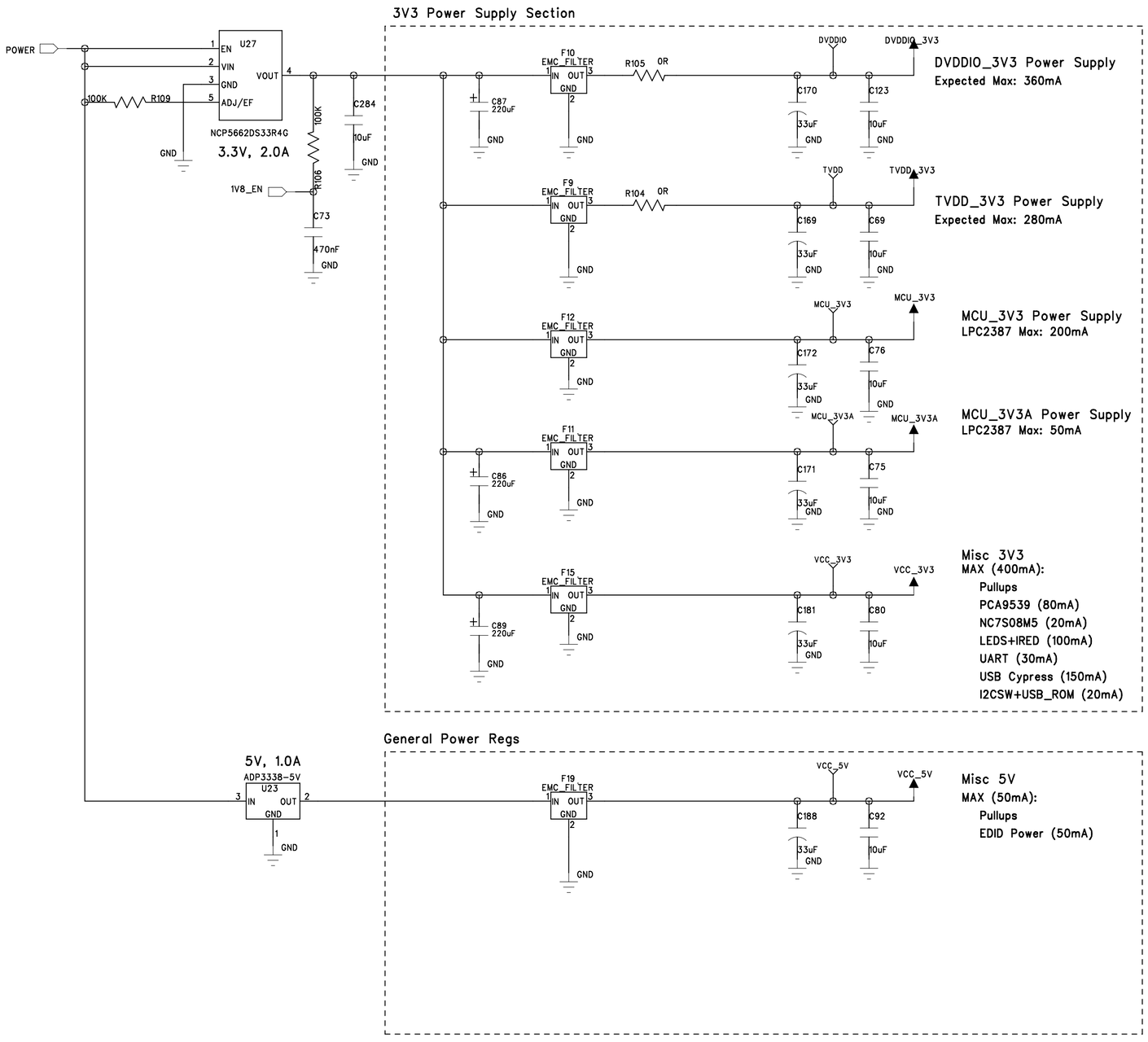
COMPANY: Analog Devices

TITLE: ATV Group
Dual ADV7612 Eval Board:
Board Power Supply Sheet

CODE:	SIZE:	DRAWING NO:	REV:
			0

SCALE:

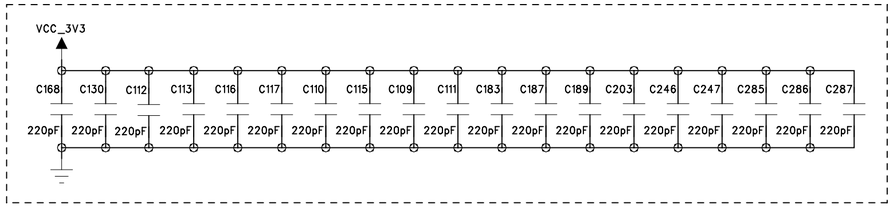
SHEET: 6 OF 10



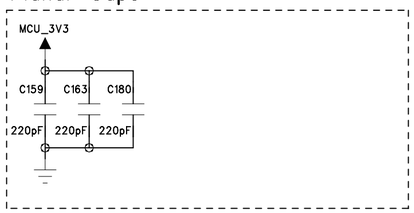
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

DRAWN:	DATED: 10/07/10	COMPANY: Analog Devices	
CHECKED:	DATED:	TITLE: ATV Group Dual ADV7612 Eval Board: Board Power Supply Sheet	
QUALITY CONTROL:	DATED:	CODE:	SIZE: DRAWING NO: REV:
RELEASED:	DATED:	SCALE:	SHEET: 7 OF 10

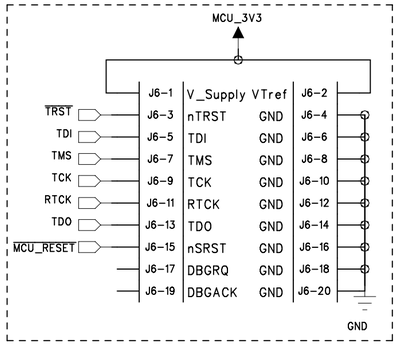
Planar Caps



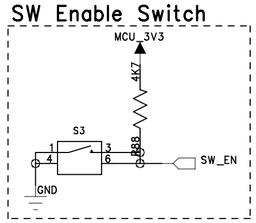
Planar Caps



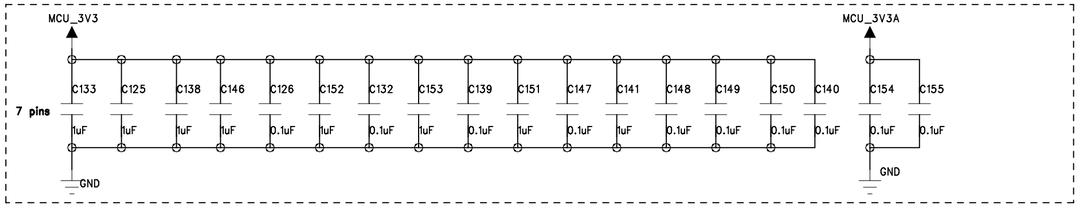
JTAG Interface – 20 Pin Interface



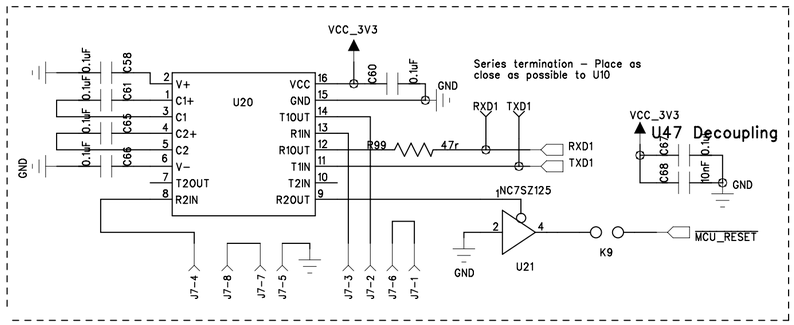
SW Enable Switch



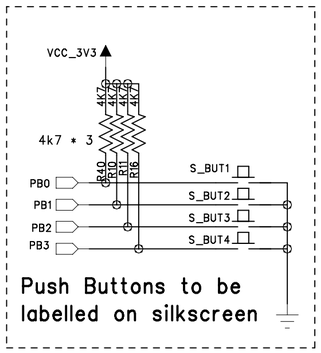
MCU Decoupling



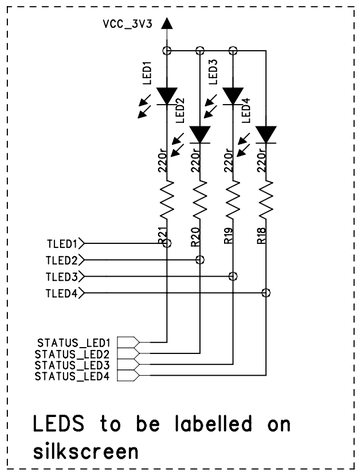
UART Interface



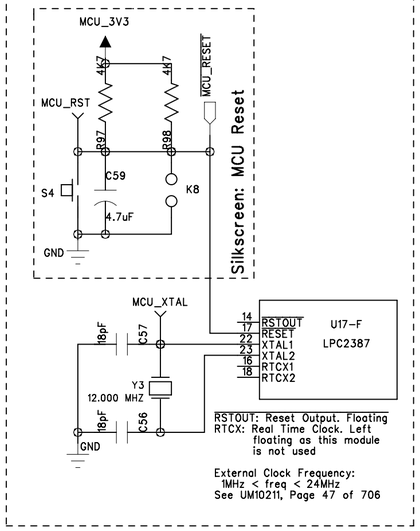
Push Buttons



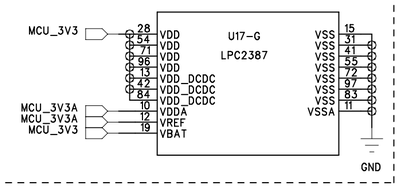
LEDs



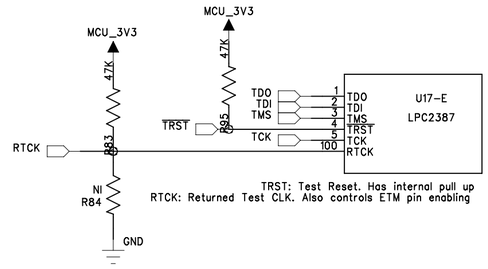
MCU – XTAL + RESET



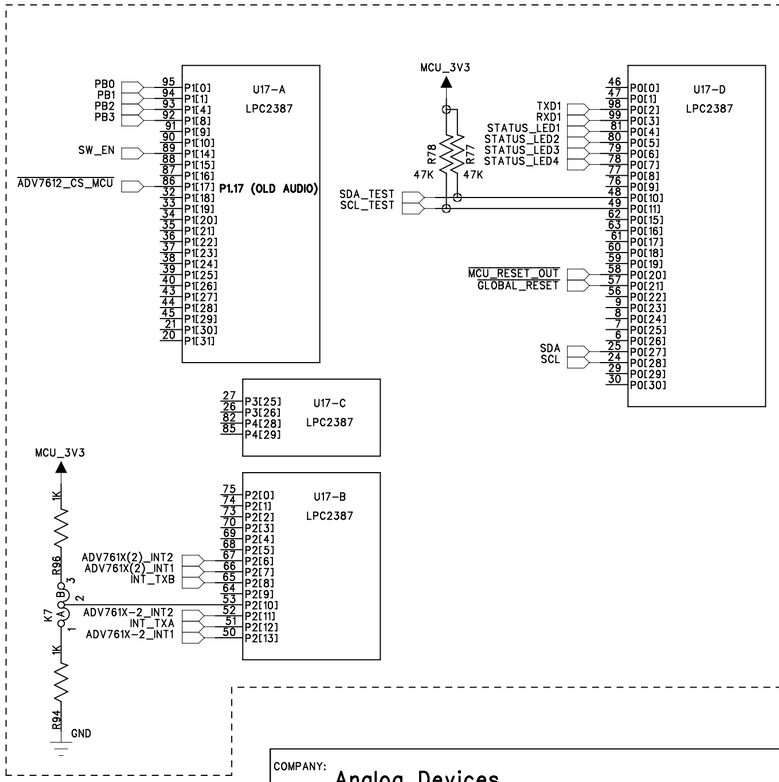
MCU – Power



MCU – JTAG



MCU – GPIOs + TRACE



REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

DRAWN:	DATED: 10/07/10	COMPANY: Analog Devices	
CHECKED:	DATED:	TITLE: ATV Group Dual ADV7612 Eval Board: ARM7 Sheet	
QUALITY CONTROL:	DATED:	CODE:	SIZE: DRAWING NO: REV:
RELEASED:	DATED:	SCALE:	SHEET: 8 OF 10

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

ADV761x PAGE

ADV761X_DATA35 ADV761X_DATA34 ADV761X_DATA33 ADV761X_DATA32 ADV761X_DATA31 ADV761X_DATA30 ADV761X_DATA29 ADV761X_DATA28 ADV761X_DATA27 ADV761X_DATA26 ADV761X_DATA25 ADV761X_DATA24 ADV761X_DATA23 ADV761X_DATA22 ADV761X_DATA21 ADV761X_DATA20 ADV761X_DATA19 ADV761X_DATA18

SDA SCL DDCTXA_SDA DDCTXA_SCL

At the end of the track

VCC_3V3 R115 150r VDD_1V8 R114 150r C93 NI

ADV761X_DATA17 ADV761X_LLC ADV761X_DATA16 ADV761X_DATA15 ADV761X_DATA14 ADV761X_DATA13 ADV761X_DATA12 ADV761X_DATA11 ADV761X_DATA10 ADV761X_DATA09 ADV761X_DATA08 ADV761X_DATA07 ADV761X_DATA06 ADV761X_DATA05 ADV761X_DATA04 ADV761X_DATA03 ADV761X_DATA02 ADV761X_DATA01 ADV761X_DATA00 ADV761X_DE ADV761X_HS ADV761X_VS_FIELD

GND DDCSCL DDCSDA HEAC+ HEAC−

R119 1K R123 1K GND

CEC_CLK AVDD_1V8_TX VDD_1V8 CEC DVDDIO_3V3 DVDDIO_3V3

R55 NI R130 4K7 R131 33r INT_TXA

U25 ADV7511

DVDD DVDD D17 CLK D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 DE HSYNC GND GND

CEC_CLK DVDD CEC_IN DVDD_3V SPDIF_OUT INT GND TX2+ TX2− AVDD TX1+ TX1− PD GND TX0+ TX0− AVDD TXC+ TXC− GND HPD AVDD R_EXT GND BGV_DD

TXA2+ TXA2− TXA1+ TXA1− TXA0+ TXA0− TXAC+ TXAC− HPD_TXA

DVDD VSYNC DSD0 DSD1 DSD2 DSD3 DSD4 DSD5 DSD_CLK SPDIF MCLK I2S0 I2S1 I2S2 I2S3 SCLK LRCLK GND DVDD GND PVDD GND PVDD GND PVDD

VDD_1V8 PVDD_1V8_TX

R144 887R C229 NI

Place R42 and C71 as close as possible to Pin 28 on the underside of PCB

Keep this away from any switching signals.

R160 0r R161 0r R162 0r R163 0r R164 0r R165 0r R166 0r R167 0r R168 0r R117 0r R116 0r

ADV761X_SPDIF ADV761X_MCLKOUT ADV761X_I2S0 ADV761X_I2S1 ADV761X_I2S2 ADV761X_I2S3 ADV761X_SCLK ADV761X_LRCLK

ADV761x PAGE

R70 47K

Power−Down and I2C Address Set−Up

VCC_3V3 NI R28 R25 2K

ESD Supression

U32

TXA2+ TXA2− TXA1+ TXA1− GND GND

U33

TXA0+ TXA0− TXAC+ TXAC− GND GND

U34

CECA_TX DDCTXA_SCL DDCTXA_SDA HPD_TXA GND GND

TXC, TX0, TX1 and TX2 pairs should be routed as 100 Ohms differential pairs (50 Ohms to GND)

J9 HDMI_19_PIN

TXA2+ TXA2− TXA1+ TXA1− TXA0+ TXA0− TXAC+ TXAC− CECA_TX DDCTXA_SCL DDCTXA_SDA HPD_TXA

TDMS_DATA2+ TDMS_SHLD2 TDMS_DATA2− TDMS_DATA_1+ TDMS_SHLD1 TDMS_DATA_1− TDMS_DATA0+ TDMS_SHLD0 TDMS_DATA0− TDMS_CLK+ TDMS_CLK_SHLD TDMS_CLK− CEC UTILITY/HEAC+ DDC_SCL DDC_SDA DDC/CEC_GND DDC_+5V HPD/HEAC−

VCC_5V R143 2K2 R142 2K2

C108 NI

U35 NC7SZ125 R132 220r D11 LED

U31 Decoupling

VCC_3V3 C105 10nF C106 0.1uF

CEC 12MHz Clock

AVDD_1V8 FB1 FERRITE C42 R56 4K7 Y5 GXO−3301G VCC OP EN GND CEC_CLK

U30 Decoupling

PVDD_1V8_TX C216 0.1uF C215 10nF C223 0.1uF C222 10nF C230 0.1uF C226 10nF

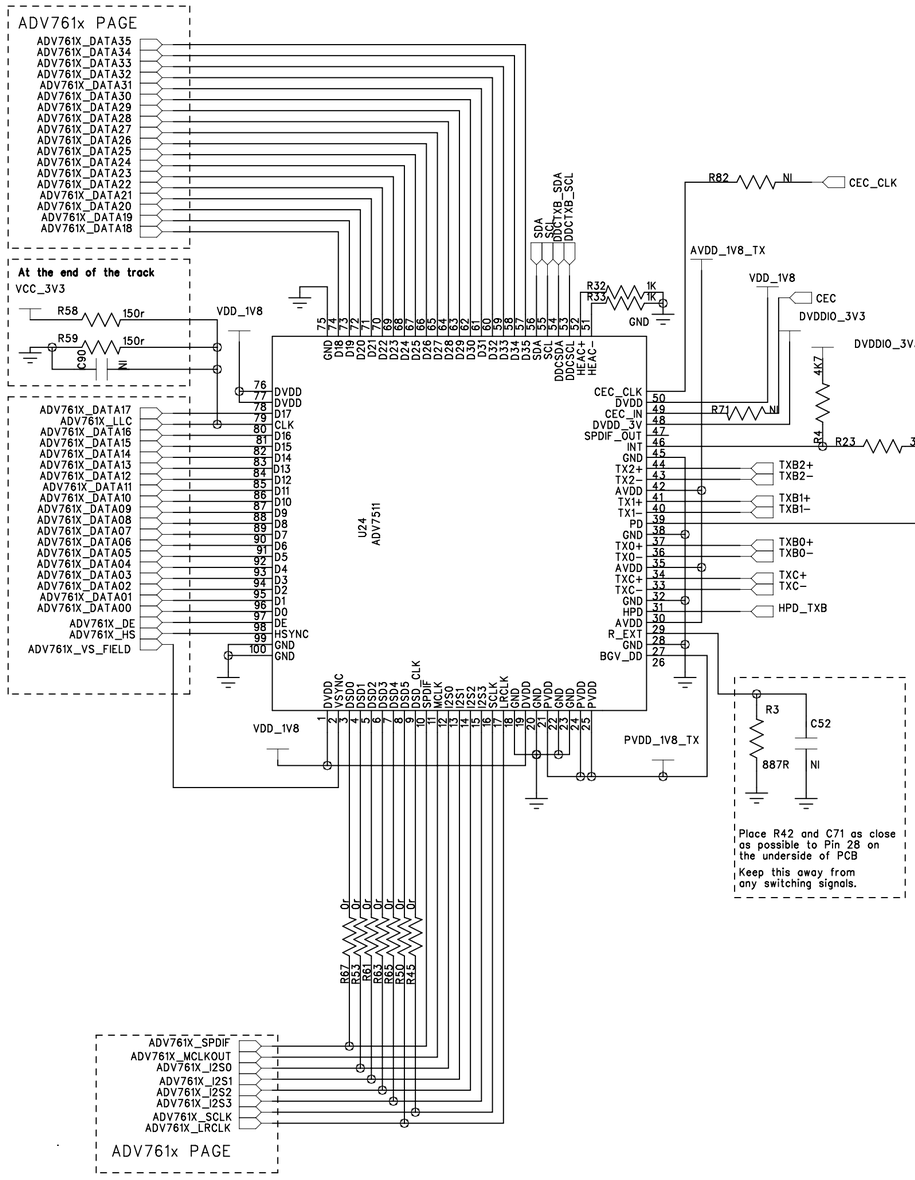
DVDDIO_3V3 C228 0.1uF C225 10nF

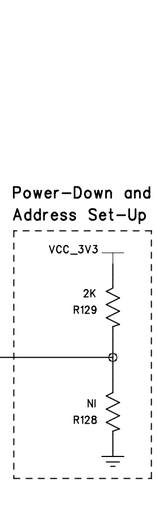
VDD_1V8 C211 0.1uF C218 10nF C198 0.1uF C192 10nF C193 0.1uF C194 10nF C207 0.1uF C208 10nF

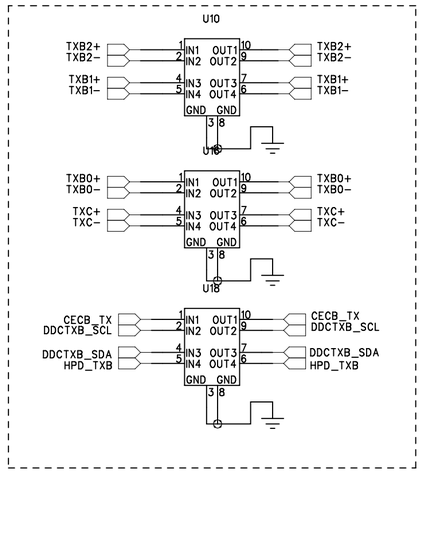
AVDD_1V8_TX C214 0.1uF C221 10nF C213 0.1uF C220 10nF C212 0.1uF C219 10nF

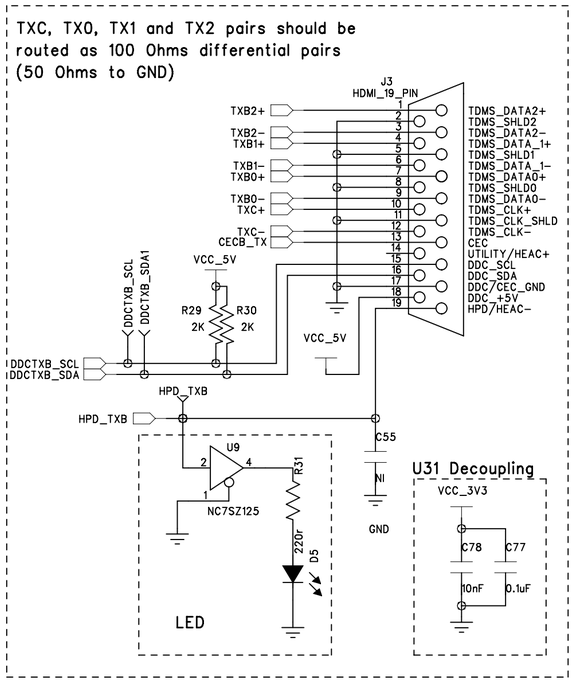
DRAWN:	DATED: 10/07/10	COMPANY: Analog Devices	
CHECKED:	DATED:	TITLE: ATV Group Dual ADV7612 Eval Board: ADV7511 Sheet	
QUALITY CONTROL:	DATED:	CODE:	SIZE: DRAWING NO: REV: 0
RELEASED:	DATED:	SCALE:	SHEET: 9 OF 10

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

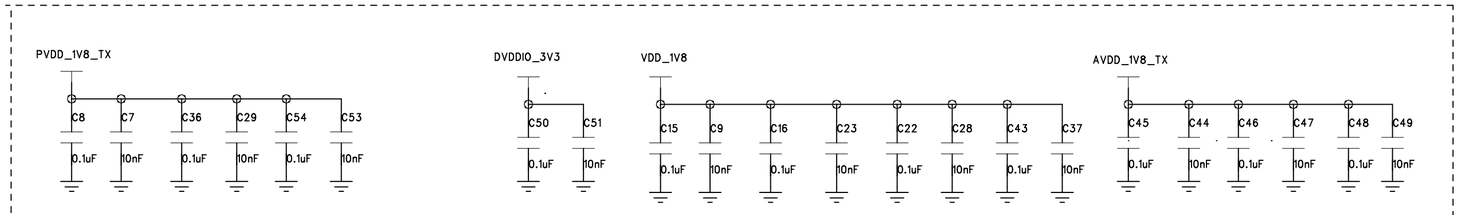








U30 Decoupling



DRAWN:	DATED: 10/07/10	COMPANY: Analog Devices			
CHECKED:	DATED:	TITLE: ATV Group Dual ADV7612 Eval Board: ADV7511 Sheet			
QUALITY CONTROL:	DATED:	CODE:	SIZE:	DRAWING NO:	REV: 0
RELEASED:	DATED:	SCALE:		SHEET: 10 OF 10	