具有自动方向感应和 ±15kV ESD 保护功能的 TXB0108 8 位双向电压电平转换器

1 特性

- A 端口电压范围为 1.2V 至 3.6V 且 B 端口电压范围为 1.65V 至 5.5V ($V_{CCA} \leq V_{CCB}$)
- V_{CC} 隔离特性—如果任何一个 V_{CC} 输入在接地 (GND) 上，所有输出在高阻抗状态
- 以 V_{CCA}为基准的输出使能 (OE) 输入电路
- 低功耗，最大 I_{CC} 为 4μA
- I_{off} 支持局部关断模式运行
- 闩锁性能超出 JESD 78 II 类规范要求的 100mA
- 静电放电 (ESD) 保护性能超过 JESD 22 规范的要求
  - A 端口
    - 2000V 人体放电模型 (A114-B)
    - 1000V 充电器件模型 (C101)
  - B 端口
    - ±15kV 人体放电模型 (A114-B)
    - ±8kV 人体放电模型 (A114-B)（仅限 YZP 封装）
    - 1000V 充电器件模型 (C101)

2 应用

- 手持终端
- 智能手机
- 平板电脑
- 台式计算机

3 说明

这个 8 位同相转换器使用两个独立的可配置电源轨。A 端口设计用于跟踪 V_{CCA}。V_{CCA} 支持从 1.2V 到 3.6V 范围内的任一电源电压。B 端口设计用于跟踪 V_{CCB}。V_{CCB} 支持从 1.65V 到 5.5V 范围内的任意电源电压。这使得该器件可在 1.2V、1.5V、1.8V、2.5V、3.3V 和 5V 电压节点之间任意进行通用低压双向转换。V_{CCA} 不应超过 V_{CCB}。

当输出使能端 (OE) 输入为低电平时，所有输出都被置于高阻抗状态。

TXB0108 旨在实现通过 V_{CCA} 对 OE 输入电路供电。

该器件完全 适用于 使用 I_{off} 的不完全断电应用。I_{off} 电路会禁用输出，从而在器件掉电时防止电流回流损坏器件。

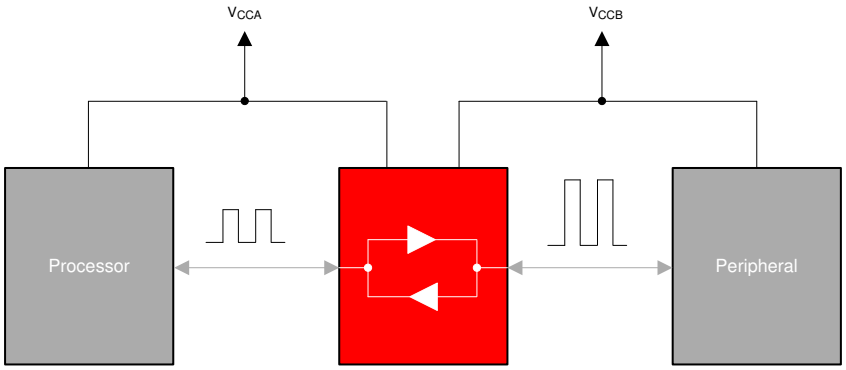
为确保在加电或断电期间处于高阻抗状态，应将 OE 通过下拉电阻器接至 GND；该电阻器的最小值取决于驱动器的拉电流能力。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TXB0108	TVSOP (20)	5.00mm x 4.40mm
	SON (20)	2.00mm x 4.00mm
	BGA MICROSTAR JUNIOR (20)	2.50mm x 3.00mm
	TSSOP (20)	6.50mm x 4.40mm
	VQFN (20)	4.50mm x 3.50mm
	DSGBA (20)	1.90mm x 2.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

TXB010X 典型应用方框图



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision F (November 2014) to Revision G — **Page**

- Added pinout image for the ZYPR2 package option ... 3
- Added text string 'GRID LOCATOR' to Pin Functions table YZP column to clarify pin location from 'Signal Name' ... 4

Changes from Revision E (April 2012) to Revision F — **Page**

- 已添加 *引脚配置和功能*部分，*处理额定值*表，*特性 说明* 部分、*器件功能模式*、*应用和实施*部分、*电源建议*部分、*布局*部分、*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1
- Changed V_{OLA} value 0.9 to 0.3 ... 6

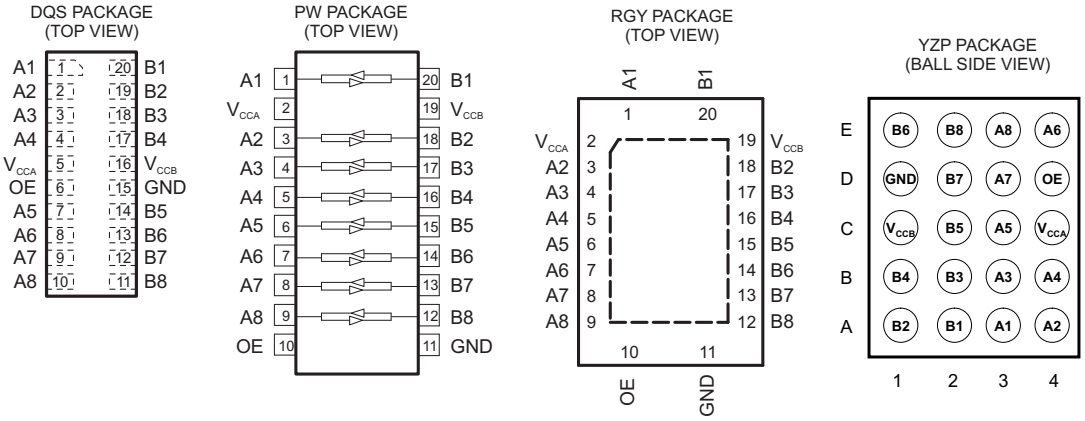
Changes from Revision D (September 2011) to Revision E — **Page**

- Added notes to pin out graphics. ... 3

Changes from Revision C (August 2011) to Revision D — **Page**

- 已添加 ±8kV 人体放电模型 (A114-B) (仅限 YZP 封装) 改为 特性 ... 1

5 Pin Configuration and Functions



Note: For the RGY package, the exposed center thermal pad must be connected to ground.

A. Pullup resistors are not required on both sides for Logic I/O.

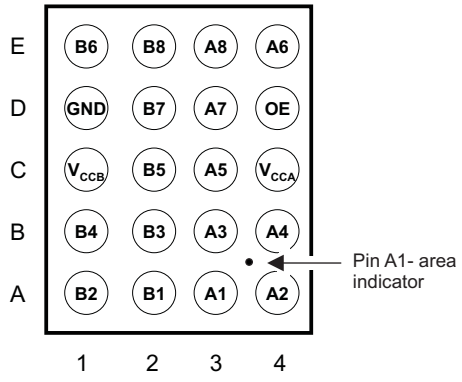
B. If pullup or pulldown resistors are needed, the resistor value must be over 50 kΩ.

C. 50 kΩ is a safe recommended value, if the customer can accept higher V_{OL} or lower V_{OH}, smaller pullup or pulldown resistor is allowed, the draft estimation is $V_{OL} = V_{CCOUT} \times 4.5\ k/(4.5\ k + R_{PU})$ and $V_{OH} = V_{CCOUT} \times R_{DW}/(4.5\ k + R_{DW})$.

D. If pullup resistors are needed, please refer to the TXS0108 or contact TI.

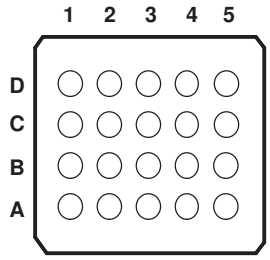
E. For detailed information, please refer to application note SCEA043.

YZPR2 PACKAGE[1]
(BALL SIDE VIEW)



[1] See orderable addendum at the end of the data sheet

GXY OR ZXY PACKAGE
(BOTTOM VIEW)



Pin Functions

PIN				I/O(1)	FUNCTION
SIGNAL NAME	PW, RGY NO.	DQS NO.	YZP GRID LOCATOR		
A1	1	1	A3	I/O	Input/output 1. Referenced to V_{CCA}.
V_{CCA}	2	5	C4	S	A-port supply voltage. 1.1 V ≤ V_{CCA} ≤ 3.6 V, V_{CCA} ≤ V_{CCB}.
A2	3	2	A4	I/O	Input/output 2. Referenced to V_{CCA}.
A3	4	3	B3	I/O	Input/output 3. Referenced to V_{CCA}.
A4	5	4	B4	I/O	Input/output 4. Referenced to V_{CCA}.
A5	6	7	C3	I/O	Input/output 5. Referenced to V_{CCA}.
A6	7	8	E4	I/O	Input/output 6. Referenced to V_{CCA}.
A7	8	9	D3	I/O	Input/output 7. Referenced to V_{CCA}.
A8	9	10	E3	I/O	Input/output 8. Referenced to V_{CCA}.
OE	10	6	D4	I	Output enable. Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}.
GND	11	15	D1	S	Ground
B8	12	11	E2	I/O	Input/output 8. Referenced to V_{CCB}.
B7	13	12	D2	I/O	Input/output 7. Referenced to V_{CCB}.
B6	14	13	E1	I/O	Input/output 6. Referenced to V_{CCB}.
B5	15	14	C2	I/O	Input/output 5. Referenced to V_{CCB}.
B4	16	17	B1	I/O	Input/output 4. Referenced to V_{CCB}.
B3	17	18	B2	I/O	Input/output 3. Referenced to V_{CCB}.
B2	18	19	A1	I/O	Input/output 2. Referenced to V_{CCB}.
V_{CCB}	19	16	C1	S	B-port supply voltage. 1.65 V ≤ V_{CCB} ≤ 5.5 V.
B1	20	20	A2	I/O	Input/output 1. Referenced to V_{CCB}.
Thermal Pad	—			—	For the RGY package, the exposed center thermal pad must be connected to ground.

(1) I = input, O = output, I/O = input and output, S = power supply

Pin Assignments (20-Ball GXY/ZXY Package)

	1	2	3	4	5
D	V_{CCB}	B2	B4	B6	B8
C	B1	B3	B5	B7	GND
B	A1	A3	A5	A7	OE
A	V_{CCA}	A2	A4	A6	A8

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage range		–0.5	4.6	V
V_{CCB}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range(2)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state(2) (3)	A inputs	–0.5	V_{CCA} + 0.5	V
		B inputs	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
T_{stg}	Storage temperature range		–65	150	°C
T_J	Junction temperature			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

6.2 Handling Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1), A Port		2	kV
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1), B Port	–15	15	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2), A Port		1	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2), A Port (YZP Package only)	–8	8	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2), B Port		1	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1) (2)

			V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.2	3.6	V
V_{CCB}					1.65	5.5	
V_{IH}	High-level input voltage	Data inputs	1.2 V to 3.6 V	1.65 V to 5.5 V	V_{CCI} x 0.65(3)	V_{CCI}	V
		OE			V_{CCA} x 0.65	5.5	
V_{IL}	Low-level input voltage	Data inputs	1.2 V to 5.5 V	1.65 V to 5.5 V	0	V_{CCI} x 0.35(3)	V
		OE	1.2 V to 3.6 V		0	V_{CCA} x 0.35	
Δt/Δv	Input transition rise or fall rate	A-port inputs	1.2 V to 3.6 V	1.65 V to 5.5 V		40	ns/V
		B-port inputs	1.2 V to 3.6 V	1.65 V to 3.6 V		40	
				4.5 V to 5.5 V		30	

(1) The A and B sides of an unused data I/O pair must be held in the same state, i.e., both at V_{CCI} or both at GND.
(2) V_{CCA} must be less than or equal to V_{CCB} and must not exceed 3.6 V.
(3) V_{CCI} is the supply voltage associated with the input port.

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)(1) (2)

		V_{CCA}	V_{CCB}	MIN	MAX	UNIT
T_A	Operating free-air temperature			–40	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TXB0108						UNIT
		PW	RGY	DQS	YZP	GXY	ZXY	
		20 PINS						
$R_{\theta JA}$	Junction-to-ambient thermal resistance	101.8	35.3	108.5	66.2	156.7	156.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.5	42.1	32.3	0.4	39.9	39.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.8	11.1	42.4	52.0	85.9	85.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.2	0.7	0.7	1.5	1.1	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	52.2	11.2	42	51.9	85.4	85.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	3.8	–	–	–	–	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)(1)(2)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	T_A = 25°C			–40°C to 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
V_{OHA}		I_{OH} = –20 μA	1.2 V			1.1				V
			1.4 V to 3.6 V					V_{CCA} – 0.4		
V_{OLA}		I_{OL} = 20 μA	1.2 V			0.3				V
			1.4 V to 3.6 V						0.4	
V_{OHB}		I_{OH} = –20 μA		1.65 V to 5.5 V				V_{CCB} – 0.4		V
V_{OLB}		I_{OL} = 20 μA		1.65 V to 5.5 V					0.4	V
I_I	OE		1.2 V to 3.6 V	1.65 V to 5.5 V			±1		±2	μA
I_{off}	A port		0 V	0 V to 5.5 V			±1		±2	μA
	B port		0 V to 3.6 V	0 V			±1		±2	
I_{OZ}	A or B port	OE = GND	1.2 V to 3.6 V	1.65 V to 5.5 V			±1		±2	μA
I_{CCA}		V_I = V_{CCI} or GND, I_O = 0	1.2 V	1.65 V to 5.5 V		0.06				μA
			1.4 V to 3.6 V						5	
			3.6 V	0 V					2	
			0 V	5.5 V					–2	
I_{CCB}		V_I = V_{CCI} or GND, I_O = 0	1.2 V	1.65 V to 5.5 V		3.4				μA
			1.4 V to 3.6 V						5	
			3.6 V	0 V					–2	
			0 V	5.5 V					2	
I_{CCA} + I_{CCB}		V_I = V_{CCI} or GND, I_O = 0	1.2 V	1.65 V to 5.5 V		3.5				μA
			1.4 V to 3.6 V						10	
I_{CCZA}		V_I = V_{CCI} or GND, I_O = 0, OE = GND	1.2 V	1.65 V to 5.5 V		0.05				μA
			1.4 V to 3.6 V						5	
I_{CCZB}		V_I = V_{CCI} or GND, I_O = 0, OE = GND	1.2 V	1.65 V to 5.5 V		3.3				μA
			1.4 V to 3.6 V						5	

(1) V_{CCI} is the supply voltage associated with the input port.
(2) V_{CCO} is the supply voltage associated with the output port.

Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)(1)(2)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	T_A = 25°C			–40°C to 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
C_I	OE		1.2 V to 3.6 V	1.65 V to 5.5 V		5			5.5	pF
C_{io}	A port		1.2 V to 3.6 V	1.65 V to 5.5 V		5			6.5	pF
	B port					8			10	

6.6 Timing Requirements: V_{CCA} = 1.2 V

T_A = 25°C, V_{CCA} = 1.2 V

			V_{CCB} = 1.8 V	V_{CCB} = 2.5 V	V_{CCB} = 3.3 V	V_{CCB} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
	Data rate		20	20	20	20	Mbps
t_w	Pulse duration	Data inputs	50	50	50	50	ns

6.7 Timing Requirements: V_{CCA} = 1.5 V ± 0.1 V

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (unless otherwise noted)

			V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate			50		50		50		50	Mbps
t_w	Pulse duration	Data inputs	20		20		20		20		ns

6.8 Timing Requirements: V_{CCA} = 1.8 V ± 0.15 V

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (unless otherwise noted)

			V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate			52		60		60		60	Mbps
t_w	Pulse duration	Data inputs	19		17		17		17		ns

6.9 Timing Requirements: V_{CCA} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted)

			V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate			70		100		100	Mbps
t_w	Pulse duration	Data inputs	14		10		10		ns

6.10 Timing Requirements: V_{CCA} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (unless otherwise noted)

			V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
	Data rate			100		100	Mbps
t_w	Pulse duration	Data inputs	10		10		ns

6.11 Switching Characteristics: V_{CCA} = 1.2 V

T_A = 25°C, V_{CCA} = 1.2 V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V	V_{CCB} = 2.5 V	V_{CCB} = 3.3 V	V_{CCB} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
t_{pd}	A	B	9.5	7.9	7.6	8.5	ns
	B	A	9.2	8.8	8.4	8	
t_{en}	OE	A	1	1	1	1	µs
		B	1	1	1	1	
t_{dis}	OE	A	20	17	17	18	ns
		B	20	16	15	15	
t_{rA}, t_{fA}	A-port rise and fall times		4.1	4.4	4.1	3.9	ns
t_{rB}, t_{fB}	B-port rise and fall times		5	5	5.1	5.1	ns
$t_{SK(O)}$	Channel-to-channel skew		2.4	1.7	1.9	7	ns
Max data rate			20	20	20	20	Mbps

6.12 Switching Characteristics: V_{CCA} = 1.5 V ± 0.1 V

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.4	12.9	1.2	10.1	1.1	10	0.8	9.9	ns
	B	A	0.9	14.2	0.7	12	0.4	11.7	0.3	13.7	
t_{en}	OE	A		1		1		1		1	µs
		B		1		1		1		1	
t_{dis}	OE	A	6.6	33	6.4	25.3	6.1	23.1	5.9	24.6	ns
		B	6.6	35.6	5.8	25.6	5.5	22.1	5.6	20.6	
t_{rA}, t_{fA}	A-port rise and fall times		0.8	6.5	0.8	6.3	0.8	6.3	0.8	6.3	ns
t_{rB}, t_{fB}	B-port rise and fall times		1	7.3	0.7	4.9	0.7	4.6	0.6	4.6	ns
$t_{SK(O)}$	Channel-to-channel skew			2.6		1.9		1.6		1.3	ns
Max data rate			50		50		50		50		Mbps

6.13 Switching Characteristics: V_{CCA} = 1.8 V ± 0.15 V

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.6	11	1.4	7.7	1.3	6.8	1.2	6.5	ns
	B	A	1.5	12	1.2	8.4	0.8	7.6	0.5	7.1	
t_{en}	OE	A		1		1		1		1	µs
		B		1		1		1		1	
t_{dis}	OE	A	5.9	26.7	5.6	21.6	5.4	18.9	4.8	18.7	ns
		B	6.1	33.9	5.2	23.7	5	19.9	5	17.6	
t_{rA}, t_{fA}	A-port rise and fall times		0.7	5.1	0.7	5	1	5	0.7	5	ns
t_{rB}, t_{fB}	B-port rise and fall times		1	7.3	0.7	5	0.7	3.9	0.6	3.8	ns
$t_{SK(O)}$	Channel-to-channel skew			0.8		0.7		0.6		0.6	ns
Max data rate			52		60		60		60		Mbps

6.14 Switching Characteristics: V_{CCA} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.1	6.4	1	5.3	0.9	4.7	ns
	B	A	1	7	0.6	5.6	0.3	4.4	
t_{en}	OE	A		1		1		1	µs
		B		1		1		1	
t_{dis}	OE	A	5	16.9	4.9	15	4.5	13.8	ns
		B	4.8	21.8	4.5	17.9	4.4	15.2	
t_{rA}, t_{fA}	A-port rise and fall times		0.8	3.6	0.6	3.6	0.5	3.5	ns
t_{rB}, t_{fB}	B-port rise and fall times		0.6	4.9	0.7	3.9	0.6	3.2	ns
$t_{SK(O)}$	Channel-to-channel skew			0.4		0.3		0.3	ns
Max data rate			70		100		100		Mbps

6.15 Switching Characteristics: V_{CCA} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (unless otherwise noted)

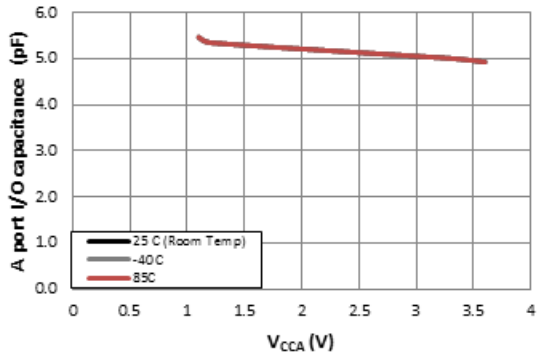
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	A	B	0.9	4.9	0.8	4	ns
	B	A	0.5	5.4	0.2	4	
t_{en}	OE	A		1		1	µs
		B		1		1	
t_{dis}	OE	A	4.5	13.9	4.1	12.4	ns
		B	4.1	17.3	4	14.4	
t_{rA}, t_{fA}	A-port rise and fall times		0.5	3	0.5	3	ns
t_{rB}, t_{fB}	B-port rise and fall times		0.7	3.9	0.6	3.2	ns
$t_{SK(O)}$	Channel-to-channel skew			0.4		0.3	ns
Max data rate			100		100		Mbps

6.16 Operating Characteristics

T_A = 25°C

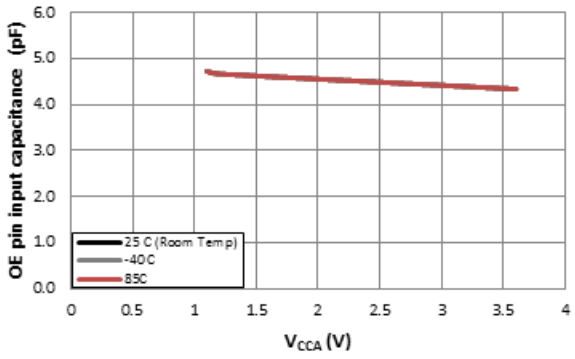
PARAMETER		TEST CONDITIONS	V_{CCA}							UNIT
			1.2 V	1.2 V	1.5 V	1.8 V	2.5 V	2.5 V	3.3 V	
			V_{CCB}							
			5 V	1.8 V	1.8 V	1.8 V	2.5 V	5 V	3.3 V to 5 V	
			TYP	TYP	TYP	TYP	TYP	TYP	TYP	
C_{pdA}	A-port input, B-port output	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns, OE = V_{CCA} (outputs enabled)	9	8	7	7	7	7	8	pF
	B-port input, A-port output		12	11	11	11	11	11	11	
C_{pdB}	A-port input, B-port output		35	26	27	27	27	27	28	
	B-port input, A-port output		26	19	18	18	18	20	21	
C_{pdA}	A-port input, B-port output	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns, OE = GND (outputs disabled)	0.01	0.01	0.01	0.01	0.01	0.01	0.01	pF
	B-port input, A-port output		0.01	0.01	0.01	0.01	0.01	0.01	0.01	
C_{pdB}	A-port input, B-port output		0.01	0.01	0.01	0.01	0.01	0.01	0.03	
	B-port input, A-port output		0.01	0.01	0.01	0.01	0.01	0.01	0.03	

6.17 Typical Characteristics



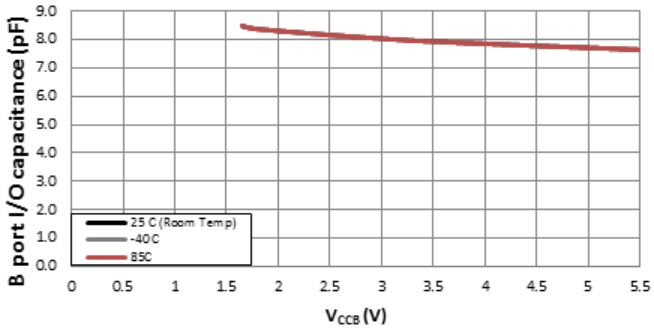
V_{CCB} = 3.3 V

Figure 1. Input Capacitance for OE Pin (C_I) vs Power Supply (V_{CCA})



V_{CCB} = 3.3 V

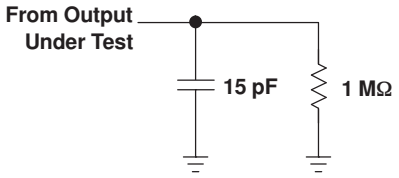
Figure 2. Capacitance for A Port I/O Pins (C_{IO}) vs Power Supply (V_{CCA})



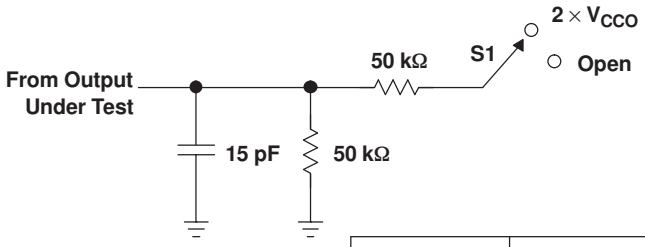
V_{CCA} = 1.8 V

Figure 3. Capacitance fpr B Port I/O Pins (C_{IO}) vs Power Supply (V_{CCB})

7 Parameter Measurement Information

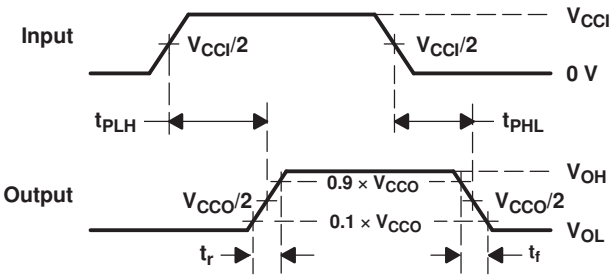


LOAD CIRCUIT FOR MAX DATA RATE, PULSE DURATION PROPAGATION DELAY OUTPUT RISE AND FALL TIME MEASUREMENT

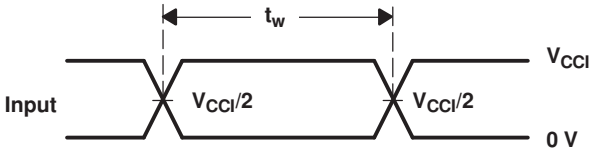


LOAD CIRCUIT FOR ENABLE/DISABLE TIME MEASUREMENT

TEST	S1
t_{PZL}/t_{PLZ} t_{PHZ}/t_{PZH}	$2 \times V_{CCO}$ Open



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS PULSE DURATION

A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.
E. V_{CCI} is the V_{CC} associated with the input port.
F. V_{CCO} is the V_{CC} associated with the output port.
G. All parameters and waveforms are not applicable to all devices.

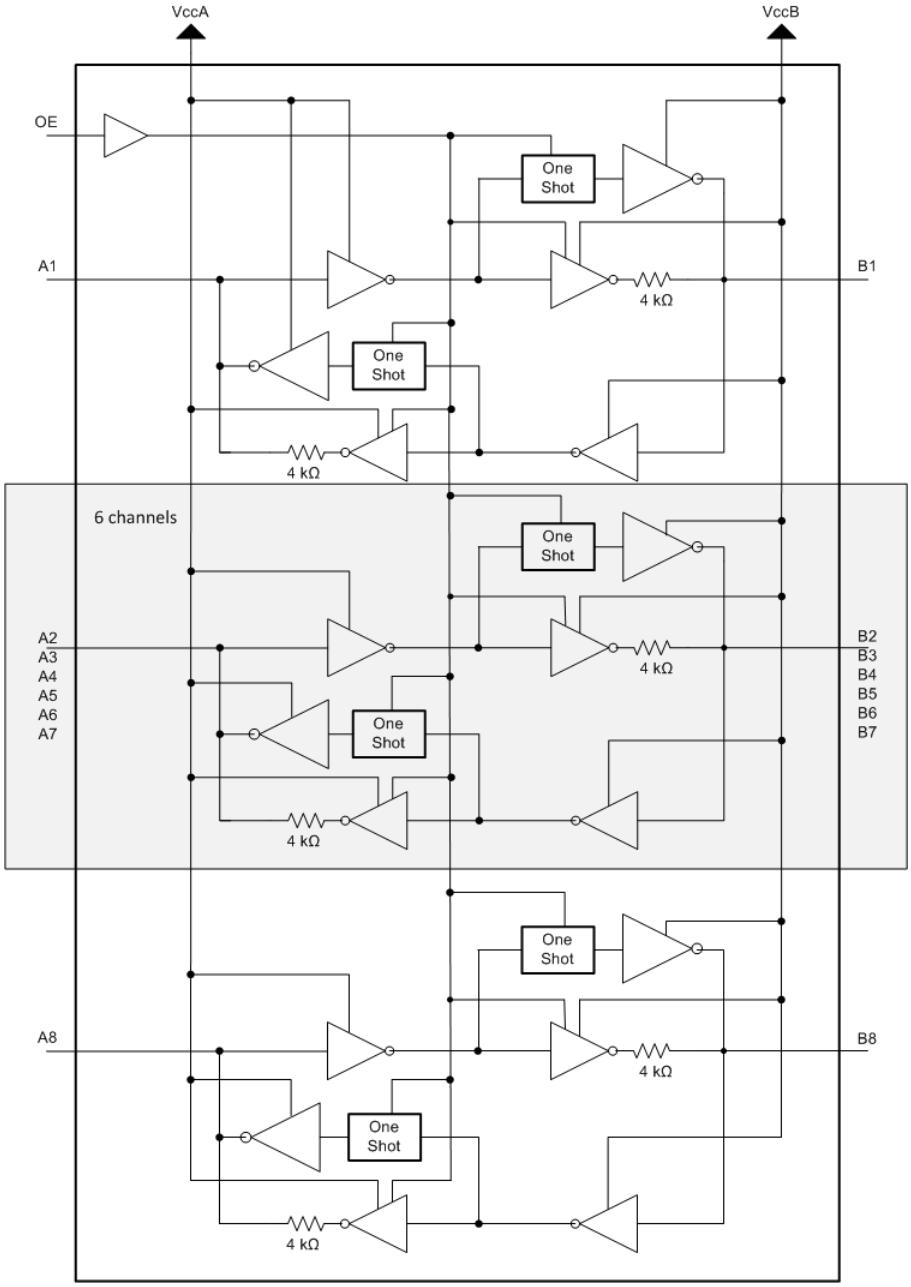
Figure 4. Load Circuits and Voltage Waveforms

8 Detailed Description

8.1 Overview

The TXB0108 device is an 8-bit, directionless voltage-level translator specifically designed for translating logic voltage levels. The A port is able to accept I/O voltages ranging from 1.2 V to 3.6 V, while the B port can accept I/O voltages from 1.65 V to 5.5 V. The device is a buffered architecture with edge-rate accelerators (one-shots) to improve the overall data rate. This device can only translate push-pull CMOS logic outputs. If for open-drain signal translation, please refer to TI TXS products.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Architecture

The TXB0108 architecture (see Figure 5) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a dc state, the output drivers of the TXB0108 can maintain a high or low, but are designed to be weak so that they can be overdriven by an external driver when data on the bus starts flowing the opposite direction. The output one-shots detect rising or falling edges on the A or B ports. During a rising edge, the one-shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one-shot turns on the NMOS transistors (T2, T4) for a short duration, which speeds up the high-to-low transition. The typical output impedance during output transition is 70 Ω at VCCO = 1.2 V to 1.8 V, 50 Ω at VCCO = 1.8 V to 3.3 V and 40 Ω at VCCO = 3.3 V to 5 V.

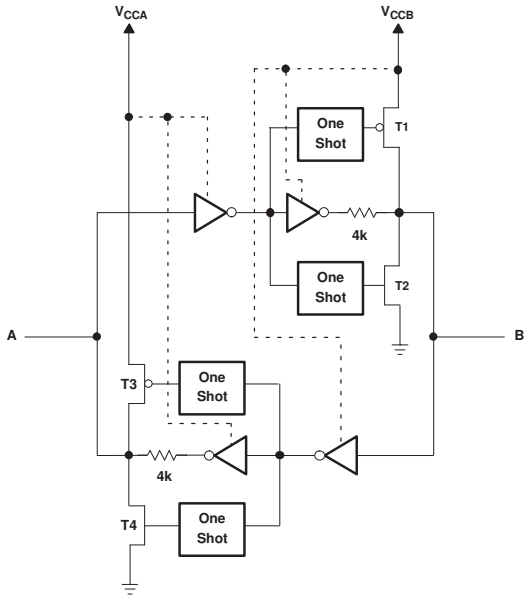
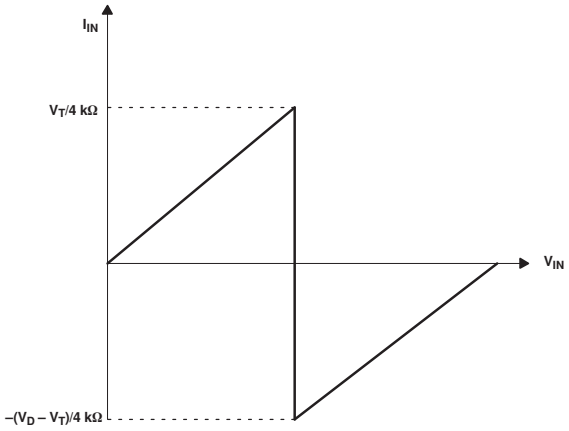


Figure 5. Architecture of TXB0108 I/O Cell

8.3.2 Input Driver Requirements

Typical I_{IN} vs V_{IN} characteristics of the TXB0108 are shown in Figure 6. For proper operation, the device driving the data I/Os of the TXB0108 must have drive strength of at least ±2 mA.



A. V_T is the input threshold voltage of the TXB0108 (typically $V_{CCI}/2$).
B. V_D is the supply voltage of the external driver.

Figure 6. Typical I_{IN} vs V_{IN} Curve

Feature Description (continued)

8.3.3 Output Load Considerations

TI recommends careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and to ensure that proper O.S. triggering takes place. PCB signal trace-lengths should be kept short enough such that the round-trip delay of any reflection is less than the one-shot duration. This improves signal integrity by ensuring that any reflection sees a low impedance at the driver. The O.S. circuits have been designed to stay on for approximately 10 ns. The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration. With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The O.S. duration has been set to best optimize trade-offs between dynamic ICC, load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance that the TXB0108 output sees, so it is recommended that this lumped-load capacitance be considered to avoid O.S. re-triggering, bus contention, output signal oscillations, or other adverse system-level affects.

8.3.4 Enable and Disable

The TXB0108 has an OE input that is used to disable the device by setting OE = low, which places all I/Os in the high-impedance (Hi-Z) state. The disable time (tdis) indicates the delay between when OE goes low and when the outputs actually get disabled (Hi-Z). The enable time (ten) indicates the amount of time the user must allow for the one-shot circuitry to become operational after the OE is high.

8.3.5 Pullup or Pulldown Resistors on I/O Lines

The TXB0108 is designed to drive capacitive loads of up to 70 pF. The output drivers of the TXB0108 have low dc drive strength. If pullup or pulldown resistors are connected externally to the data I/Os, their values must be kept higher than 50 kΩ to ensure that they do not contend with the output drivers of the TXB0108. For the same reason, the TXB0108 should not be used in applications such as I2C or 1-Wire where an open-drain driver is connected on the bidirectional data I/O. For these applications, use a device from the TI TXS01xx series of level translators.

8.4 Device Functional Modes

The TXB0108 device has two functional modes, enabled and disabled. To disable the device, set the OE input low, which places all I/Os in a high impedance state. Setting the OE input high will enable the device.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TXB0108 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. It can only translate push-pull CMOS logic outputs. If for open-drain signal translation, please refer to TI TXS010X products. Any external pulldown or pullup resistors are recommended to be larger than 50kΩ.

9.2 Typical Application

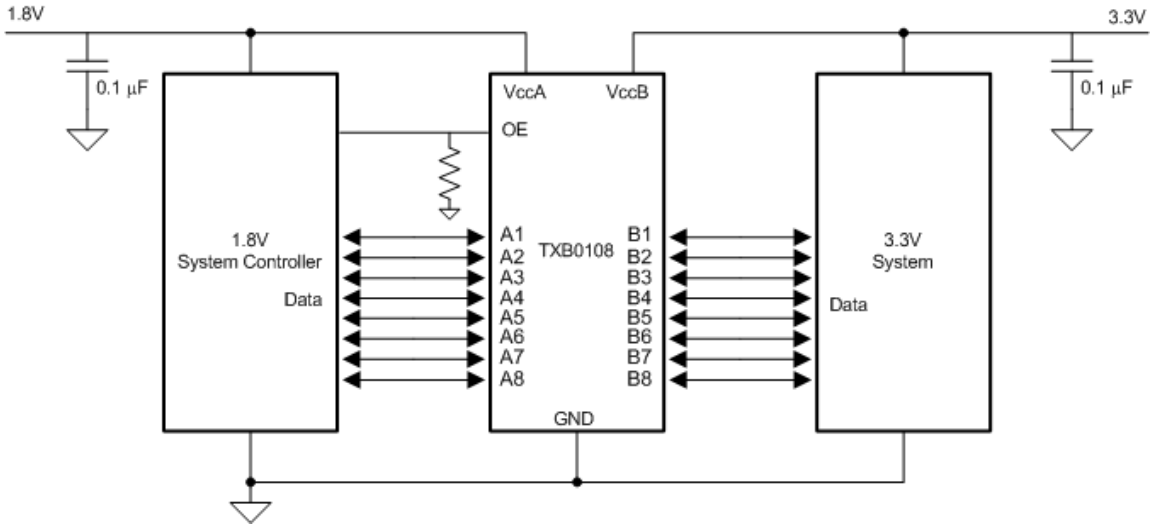


Figure 7. Typical Operating Circuit

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 1. Make sure the VCCA ≤VCCB.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.2 V to 3.6 V
Output voltage range	1.65 V to 5.5 V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the TXB0108 device to determine the input voltage range. For a valid logic high the value must exceed the VIH of the input port. For a valid logic low, the value must be less than the VIL of the input port.
- Output voltage range
  - Use the supply voltage of the device that the TXB0108 device is driving to determine the output voltage range.

- Do not recommend having the external pullup or pulldown resistors. If mandatory, it is recommended the value should be larger than 50 kΩ.

• An external pulldown or pullup resistor decreases the output V_{OH} and V_{OL}. Use the below equations to draft estimate the V_{OH} and V_{OL} as a result of an external pulldown and pullup resistor.

$V_{OH} = V_{CCx} \times R_{PD} / (R_{PD} + 4.5\ k\Omega)$

$V_{OL} = V_{CCx} \times 4.5k\Omega / (R_{PU} + 4.5\ k\Omega)$

Where:

- V_{CCx} is the output port supply voltage on either VCCA or VCCB
- R_{PD} is the value of the external pull down resistor
- R_{PU} is the value of the external pull up resistor
- 4.5 kΩ is the counting the variation of the serial resistor 4 kΩ in the I/O line. Refer to the Effects of external pullup and pulldown resistors on TXB application note

9.2.3 Application Curves

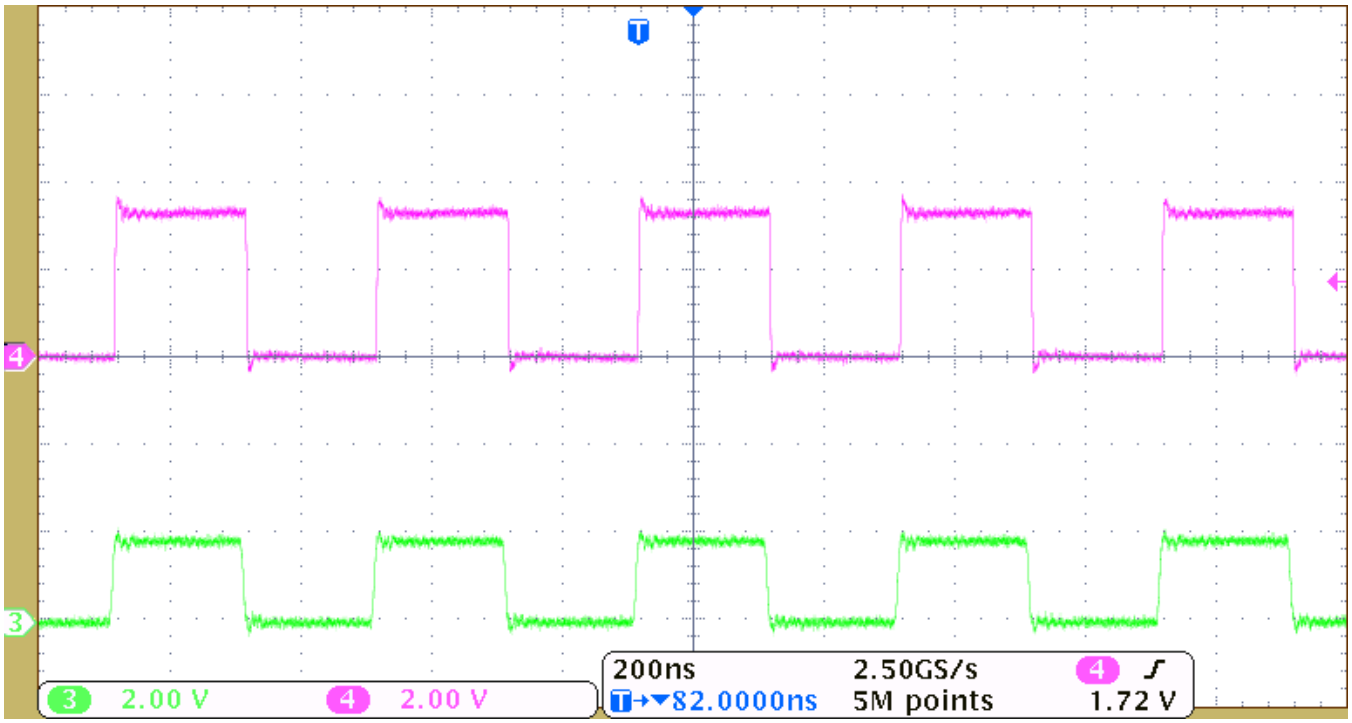


Figure 8. Level-Translation of a 2.5-MHz Signal

10 Power Supply Recommendations

During operation, ensure that $V_{CCA} \leq V_{CCB}$ at all times. During power-up sequencing, $V_{CCA} \geq V_{CCB}$ does not damage the device, so any power supply can be ramped up first. The TXB0108 has circuitry that disables all output ports when either VCC is switched off ($V_{CCA/B}$ = 0 V).

The output-enable (OE) input circuit is designed so that it is supplied by V_{CCA} and when the (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power-up or power-down, the OE input pin must be tied to GND through a pulldown resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pulldown resistor to ground is determined by the current-sourcing capability of the driver.

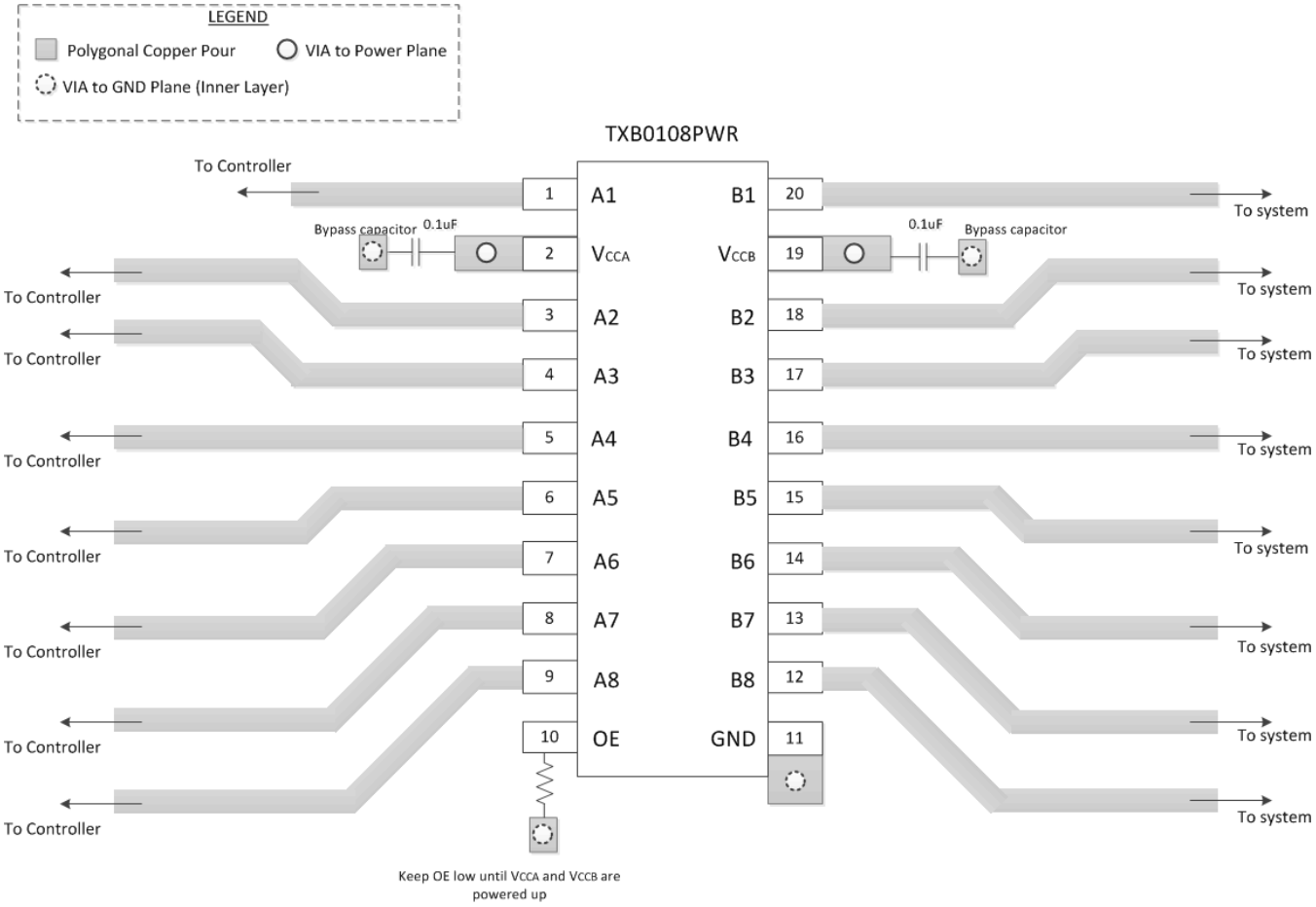
11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, the following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies and should be placed as close as possible to the V_{CCA}, V_{CCB} pin and GND pin.
- Short trace lengths should be used to avoid excessive loading.
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one-shot duration, approximately 10 ns, ensuring that any reflection encounters low impedance at the source driver.

11.2 Layout Example



12 器件和文档支持

12.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** 此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 术语表

SLYZ022 — *TI 术语表*。

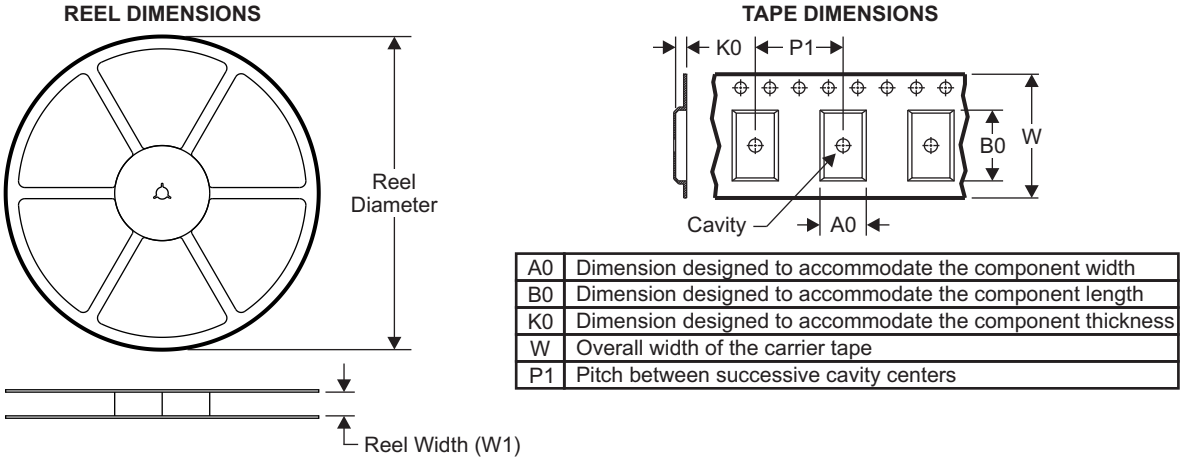
这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

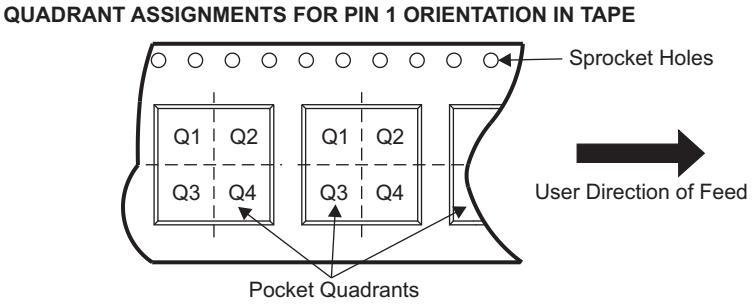
以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

13.1 Package Addendum

13.1.1 Tape and Reel Information



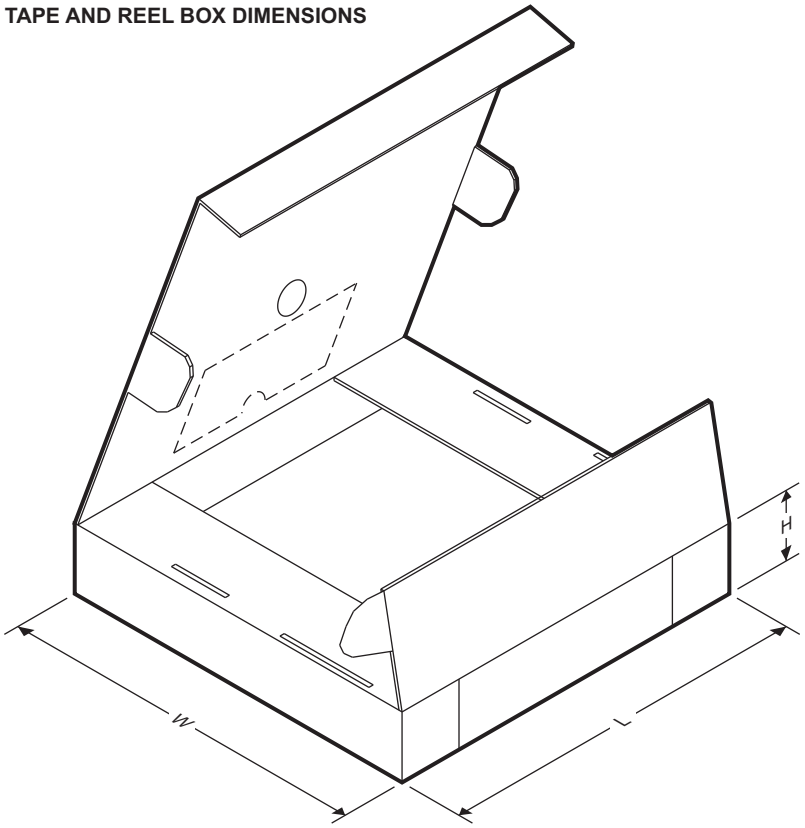
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXB0108DQSR	USON	DQS	20	3000	177.8	12.4	2.21	4.22	0.81	4.0	12.0	Q1
TXB0108RGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
TXB0108YZPR	DSBGA	YZP	20	3000	180.0	8.4	1.99	2.49	0.56	4.0	8.0	Q1
TXB0108YZPR2	DSBGA	YZP	20	3000	180.0	8.4	1.99	2.49	0.56	4.0	8.0	Q2
TXB0108ZXYR	BGA MICROSTAR JUNIOR	ZXY	20	2500	330.0	12.4	2.8	4.22	3.3	1.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXB0108DQSR	USON	DQS	20	3000	202.0	201.0	28.0
TXB0108RGYR	VQFN	RGY	20	3000	355.0	350.0	50.0
TXB0108YZPR	DSBGA	YZP	20	3000	182.0	182.0	20.0
TXB0108YZPR2	DSBGA	YZP	20	3000	182.0	182.0	20.0
TXB0108ZXYR	BGA MICROSTAR JUNIOR	ZXY	20	2500	336.6	336.6	28.6

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TXB0108DQSR	ACTIVE	USON	DQS	20	3000	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	5MR 5MH	Samples
TXB0108NMER	ACTIVE	NFBGA	NME	20	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	29WW	Samples
TXB0108PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YE08	Samples
TXB0108PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YE08	Samples
TXB0108RGYR	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YE08	Samples
TXB0108YZPR	ACTIVE	DSBGA	YZP	20	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	5M	Samples
TXB0108YZPR2	ACTIVE	DSBGA	YZP	20	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	EK	Samples
TXB0108ZXYR	ACTIVE	BGA MICROSTAR JUNIOR	ZXY	20	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	YE08	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

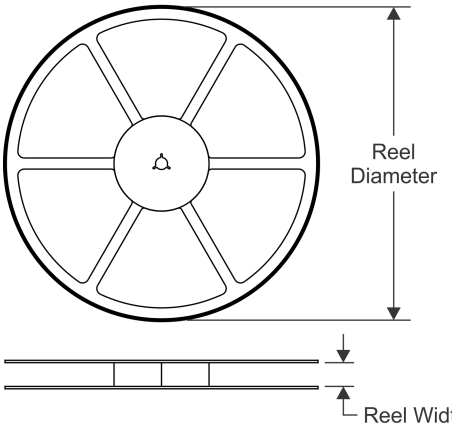
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

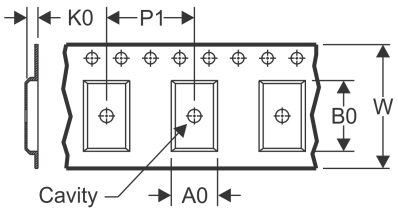
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

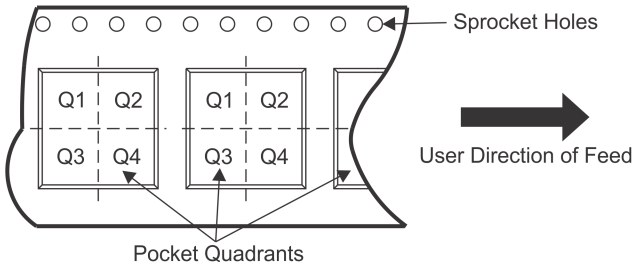


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

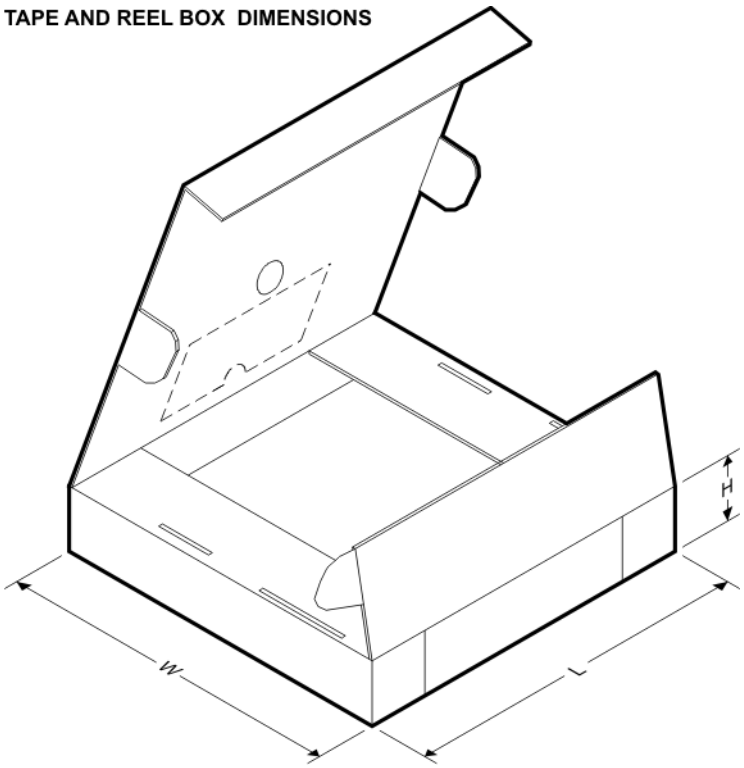
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXB0108DQSR	USON	DQS	20	3000	177.8	12.4	2.21	4.22	0.81	4.0	12.0	Q1
TXB0108PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
TXB0108RGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
TXB0108YZPR	DSBGA	YZP	20	3000	180.0	8.4	1.99	2.49	0.56	4.0	8.0	Q1
TXB0108YZPR2	DSBGA	YZP	20	3000	180.0	8.4	1.99	2.49	0.56	4.0	8.0	Q2
TXB0108ZXYR	BGA MICROSTAR JUNIOR	ZXY	20	2500	330.0	12.4	2.75	3.45	1.05	4.0	12.0	Q2

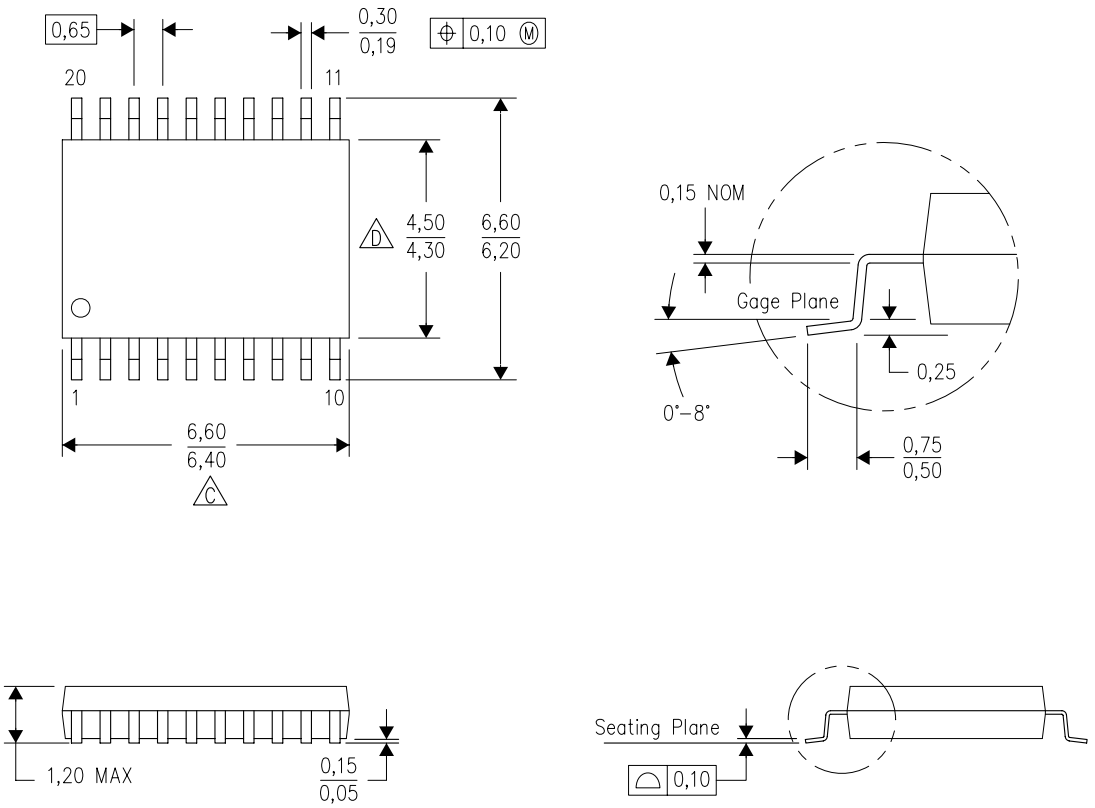
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXB0108DQSR	USON	DQS	20	3000	202.0	201.0	28.0
TXB0108PWR	TSSOP	PW	20	2000	367.0	367.0	38.0
TXB0108RGYR	VQFN	RGY	20	3000	853.0	449.0	35.0
TXB0108YZPR	DSBGA	YZP	20	3000	182.0	182.0	20.0
TXB0108YZPR2	DSBGA	YZP	20	3000	182.0	182.0	20.0
TXB0108ZXYR	BGA MICROSTAR JUNIOR	ZXY	20	2500	350.0	350.0	43.0

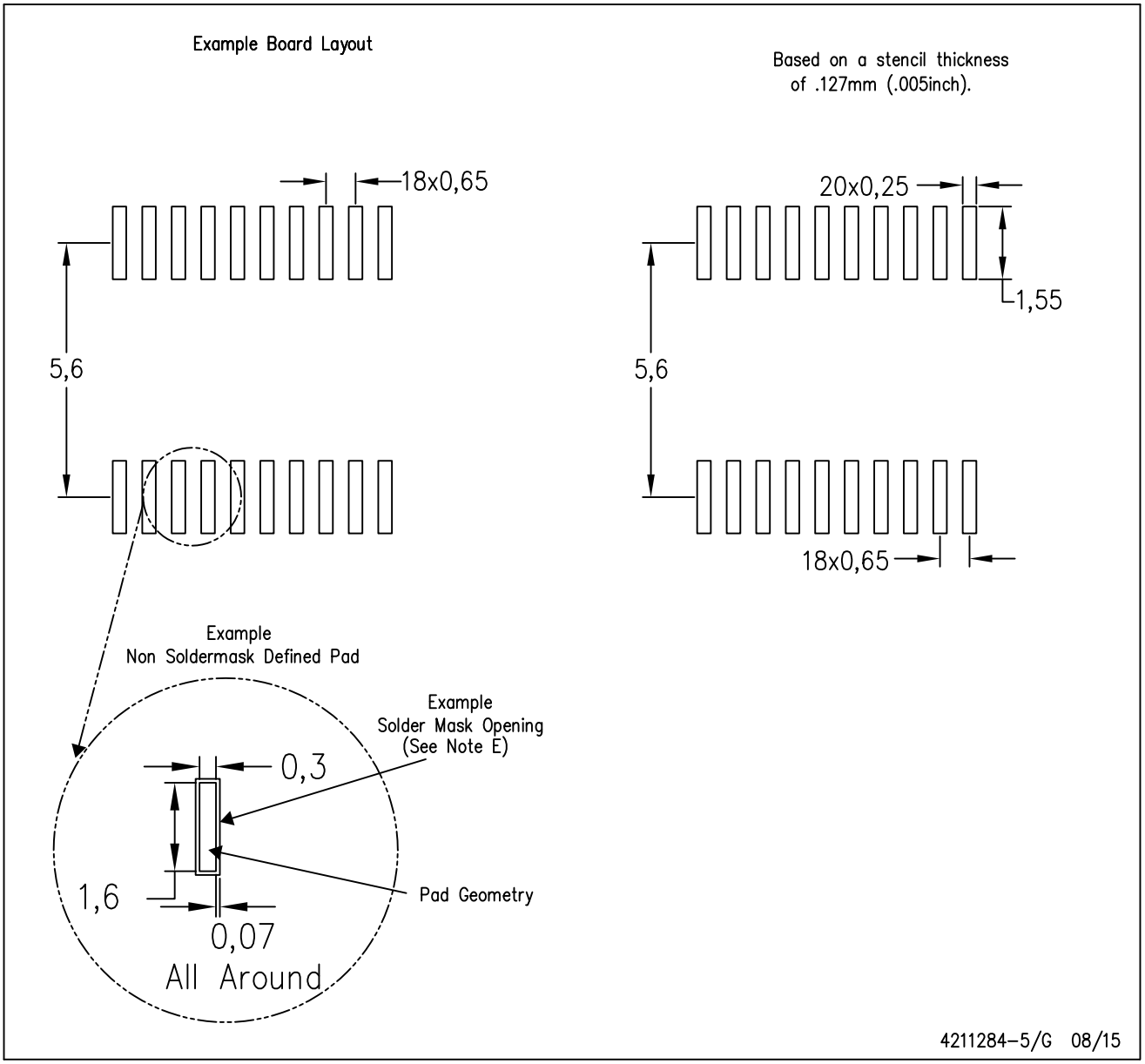
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



4040064–5/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

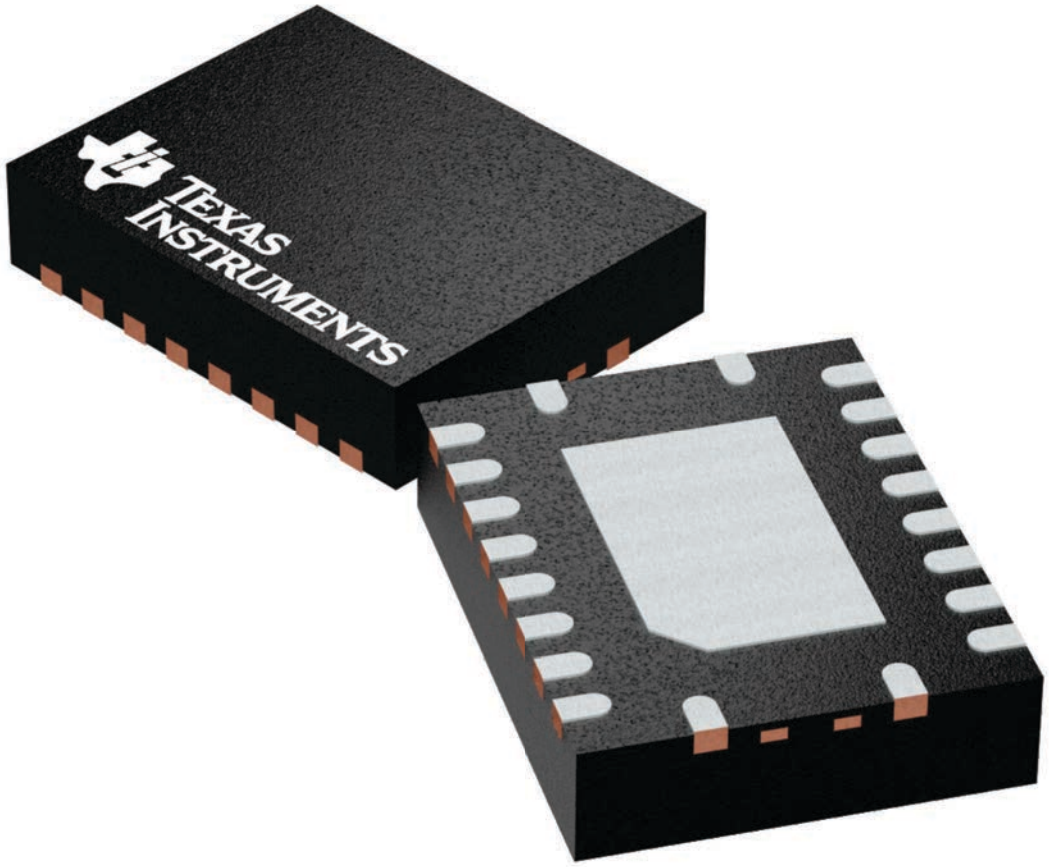
RGY 20

VQFN - 1 mm max height

3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



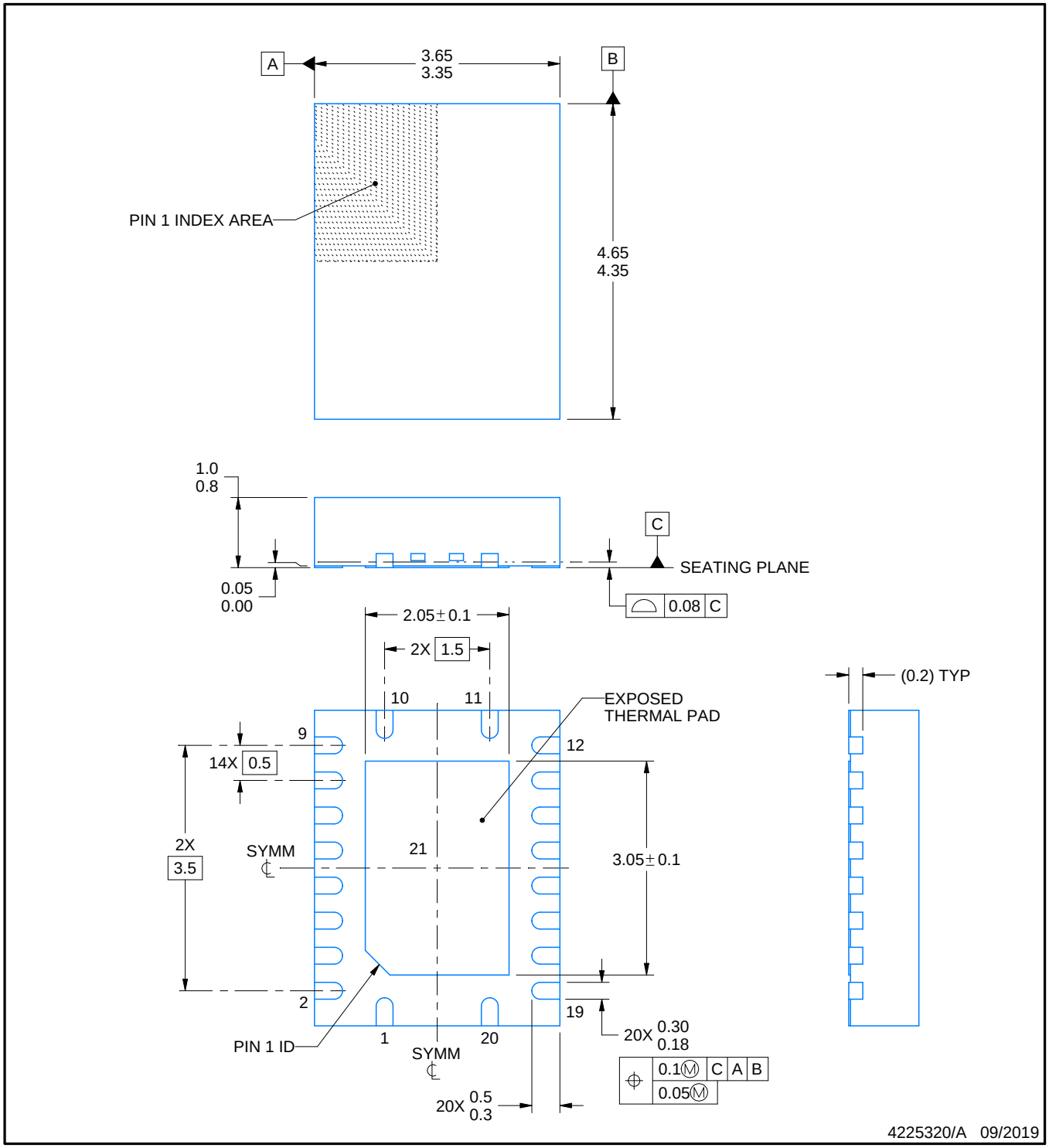
4225264/A

PACKAGE OUTLINE

RGY0020A

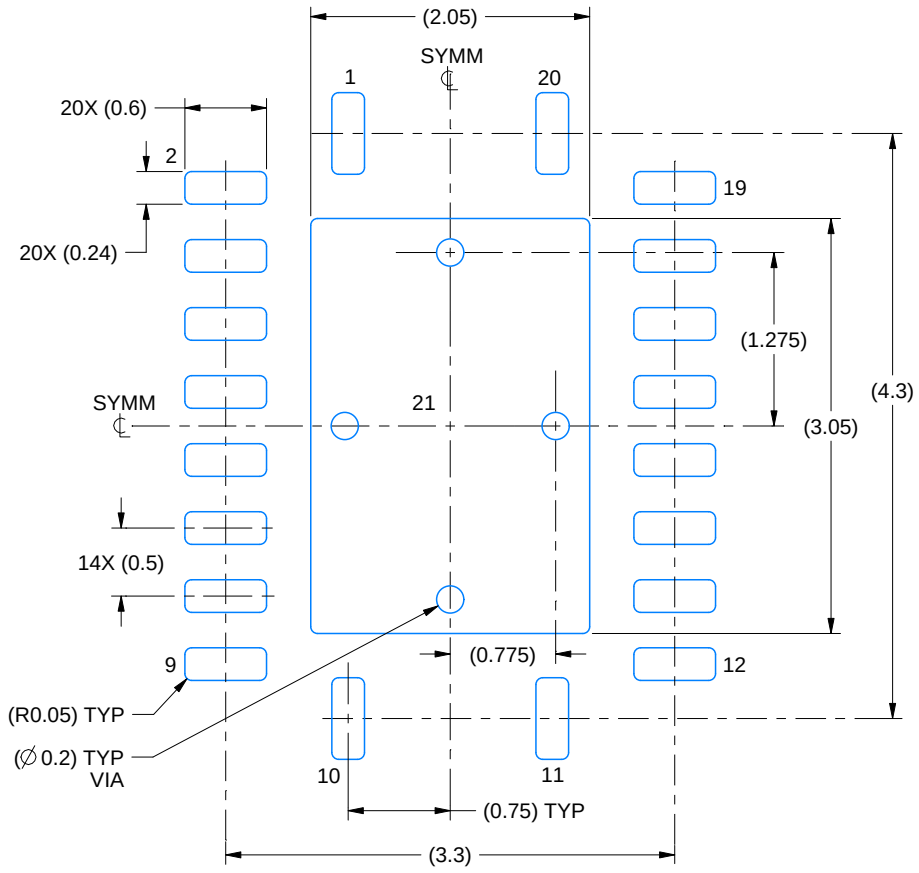
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

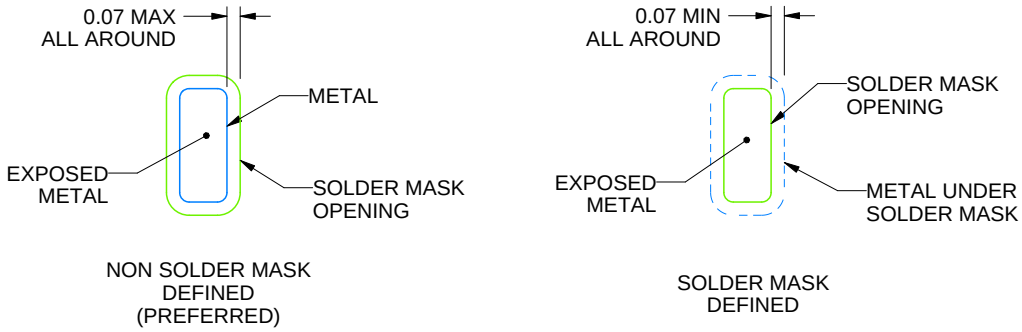


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

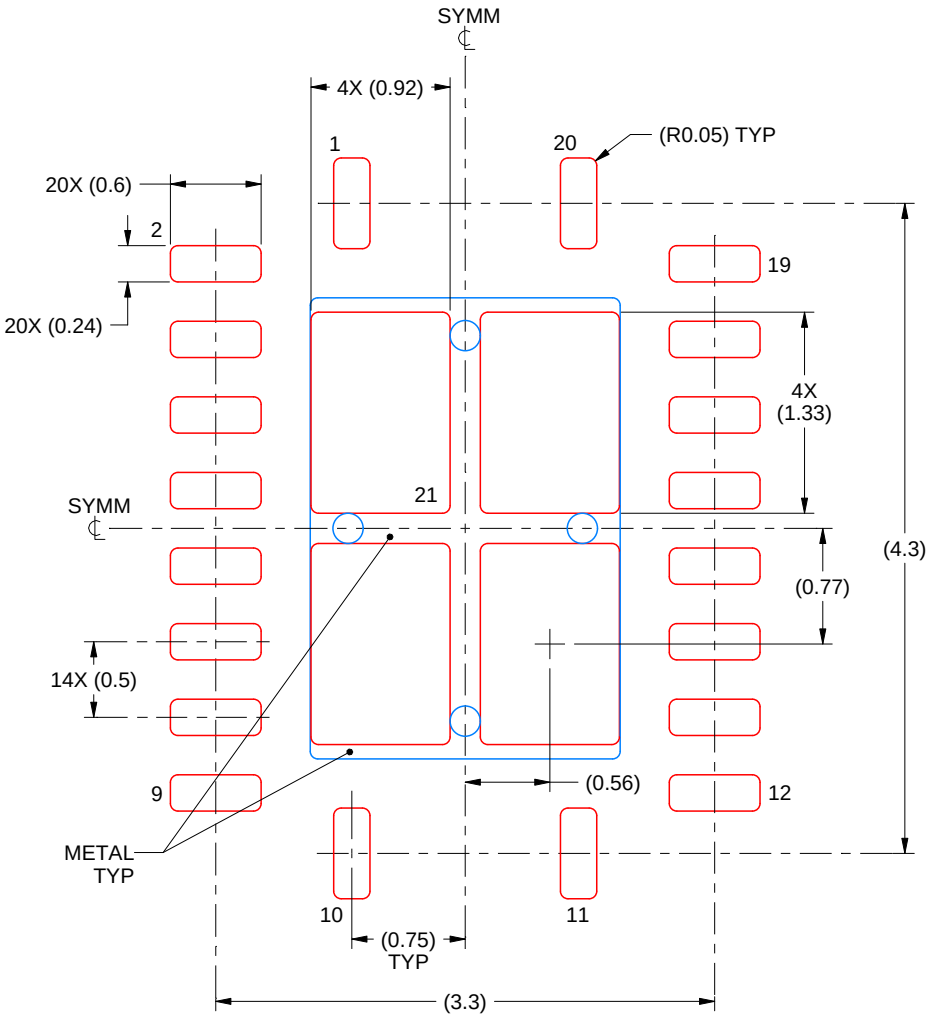


SOLDER MASK DETAILS

4225320/A 09/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4225320/A 09/2019

NOTES: (continued)

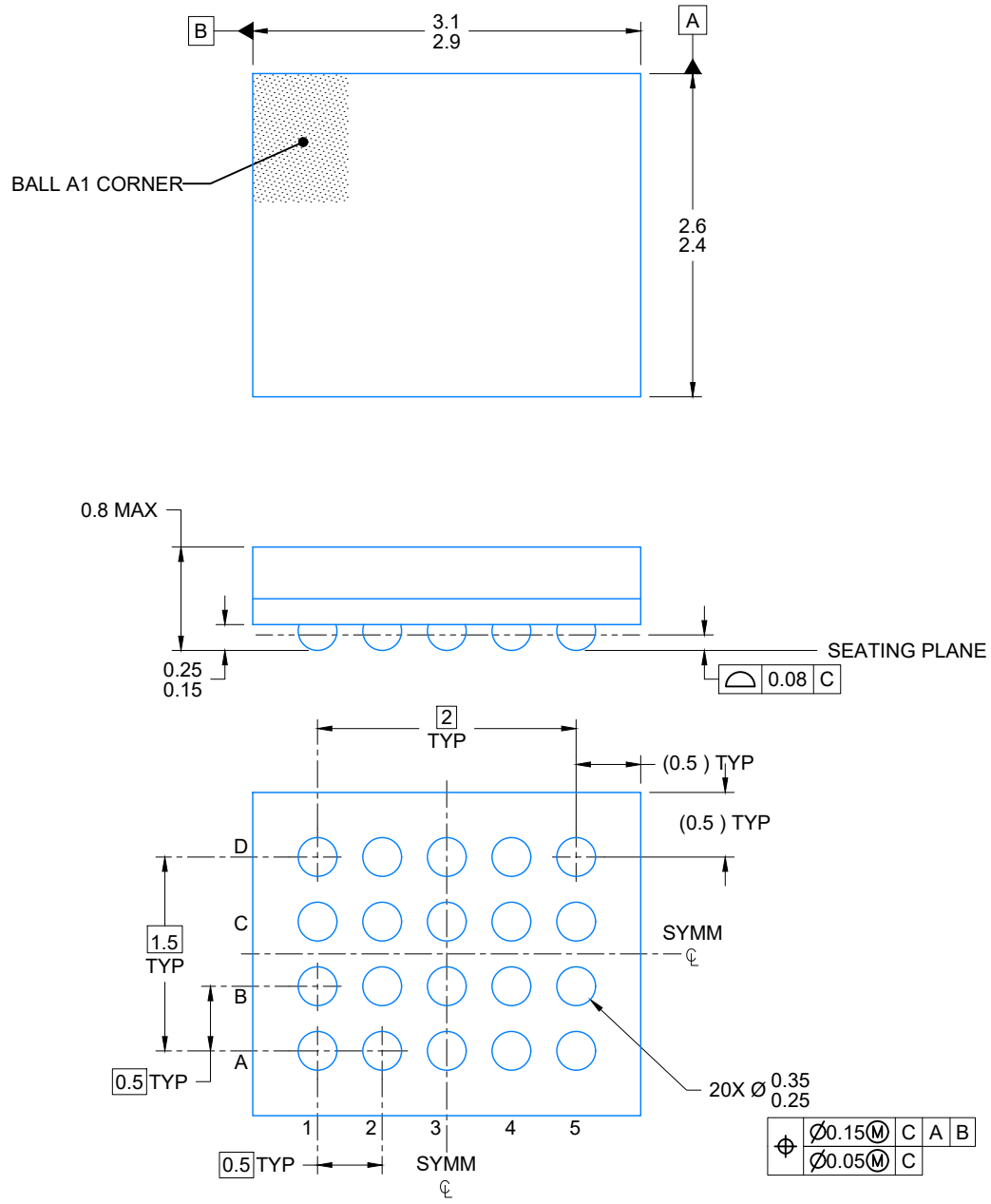
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

NME0020A

NFBGA - 0.8 mm max height

PLASTIC BALL GRID ARRAY

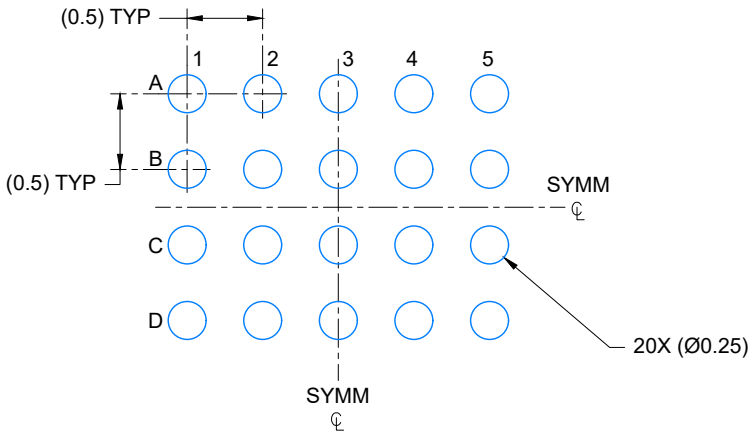


4224888/B 08/2019

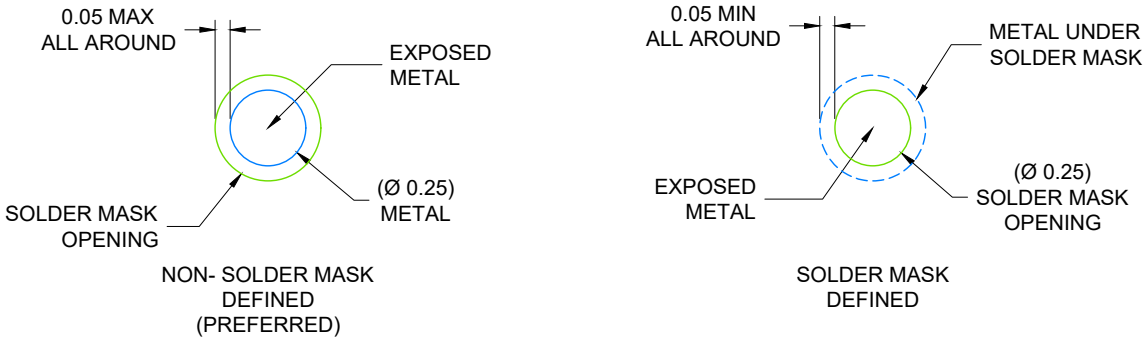
NOTES:

NanoFree is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE: 20X

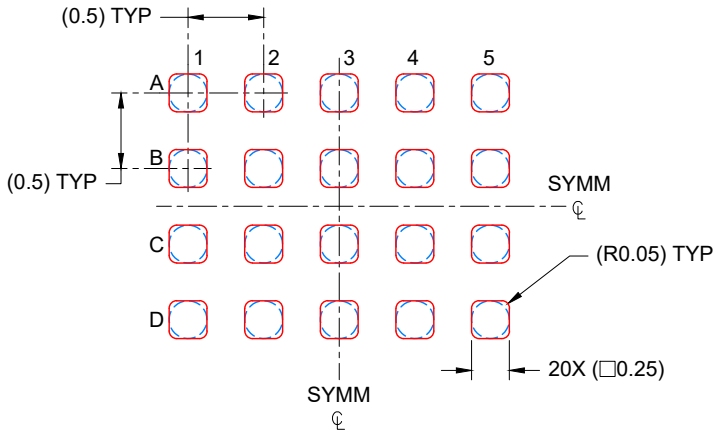


SOLDER MASK DETAILS
NOT TO SCALE

4224888/B 08/2019

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL
SCALE: 20X

4224888/B 08/2019

NOTES: (continued)

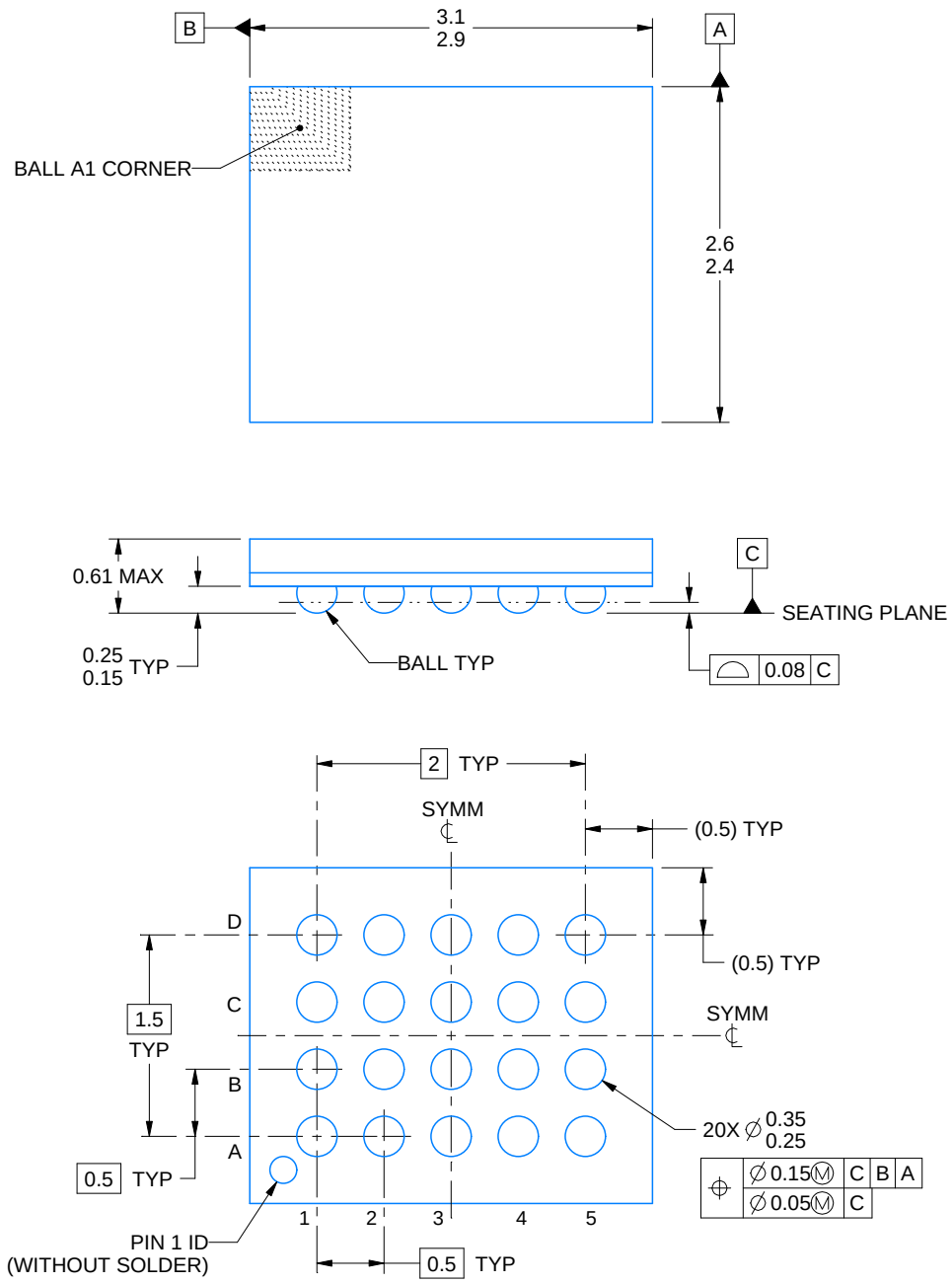
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

ZXY0020A

VFBGA - 0.61 mm max height

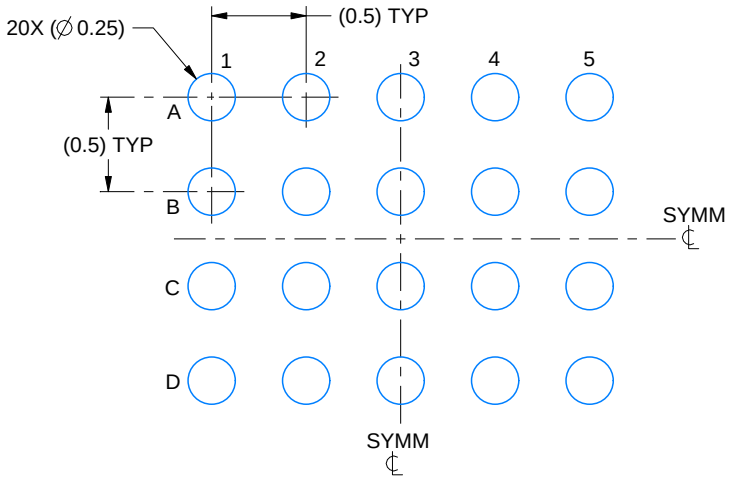
PLASTIC BALL GRID ARRAY



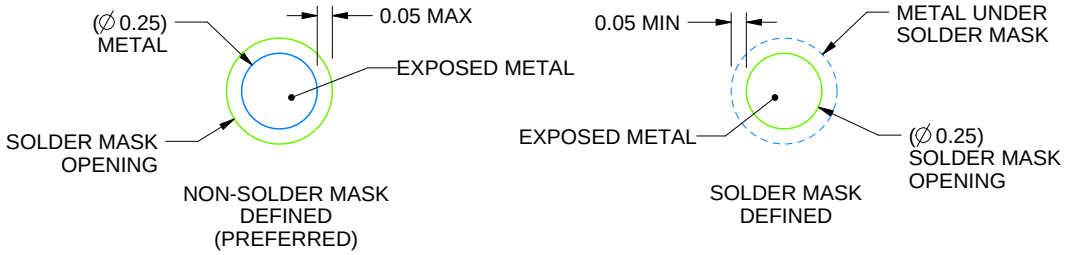
4222996/A 12/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

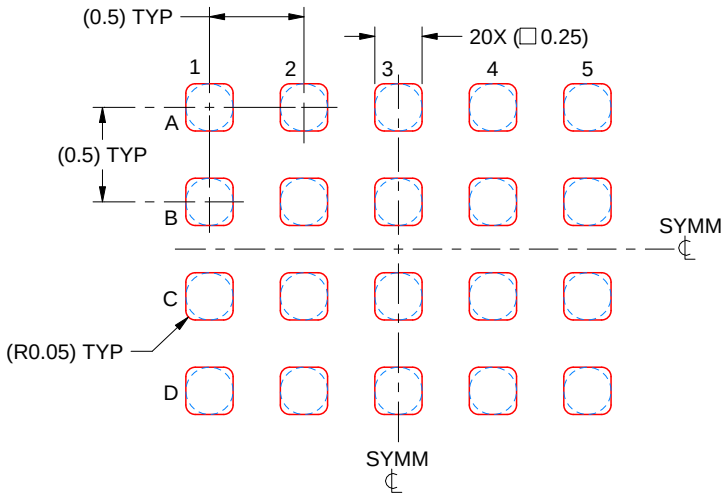


SOLDER MASK DETAILS
NOT TO SCALE

4222996/A 12/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).



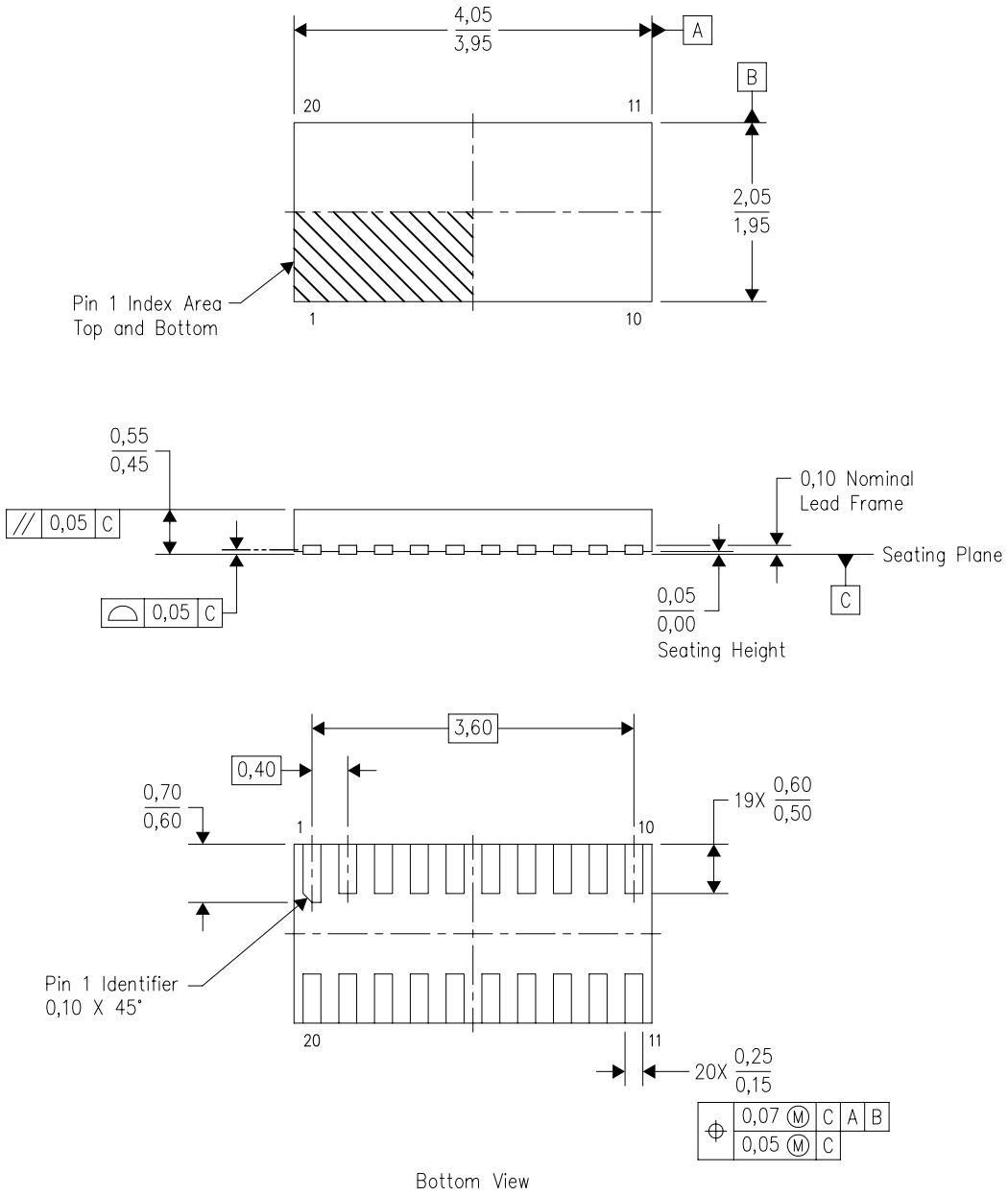
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 25X

4222996/A 12/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

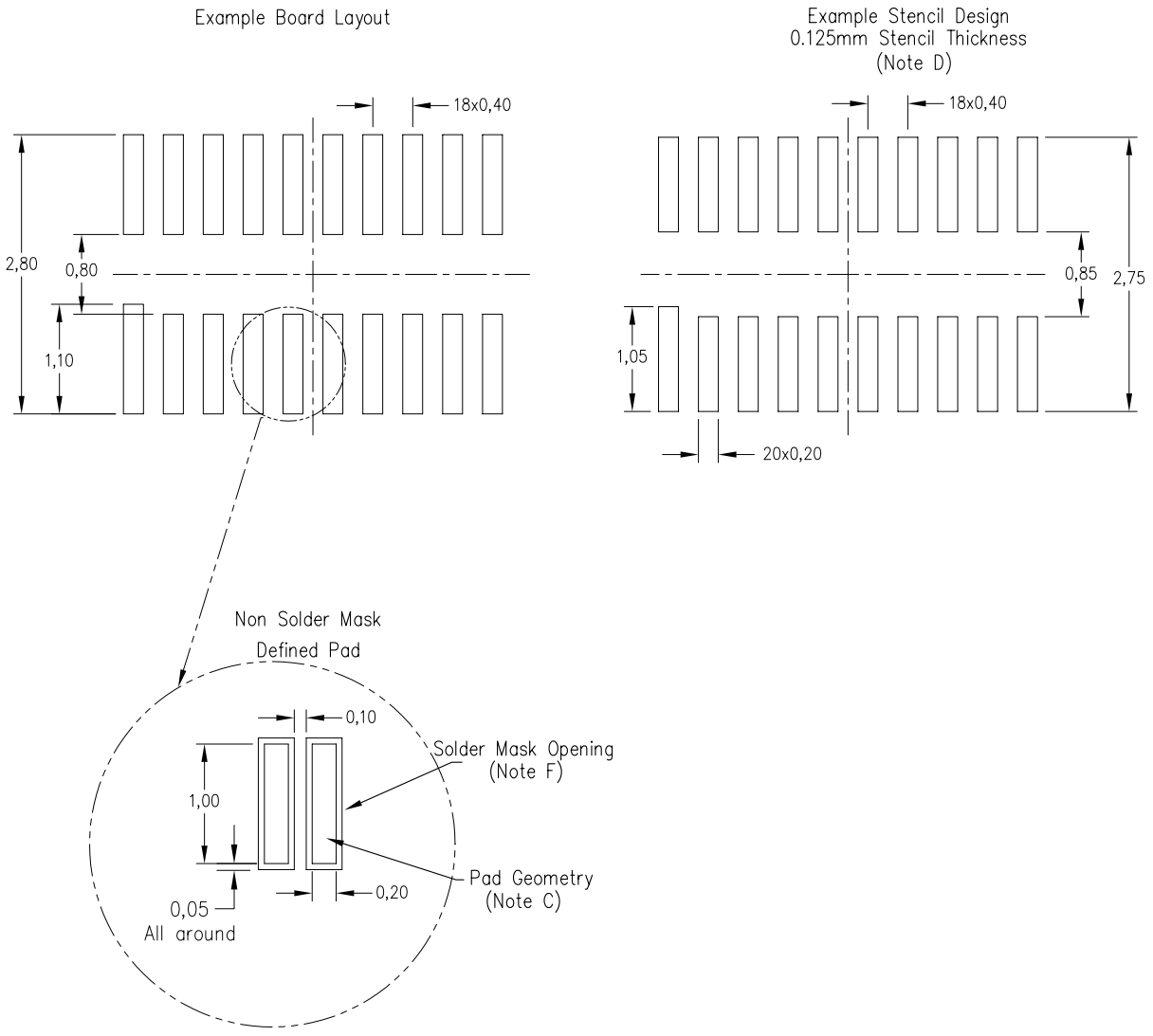
DQS (R–PUSON–N20) PLASTIC SMALL OUTLINE NO–LEAD



4210558/B 03/11

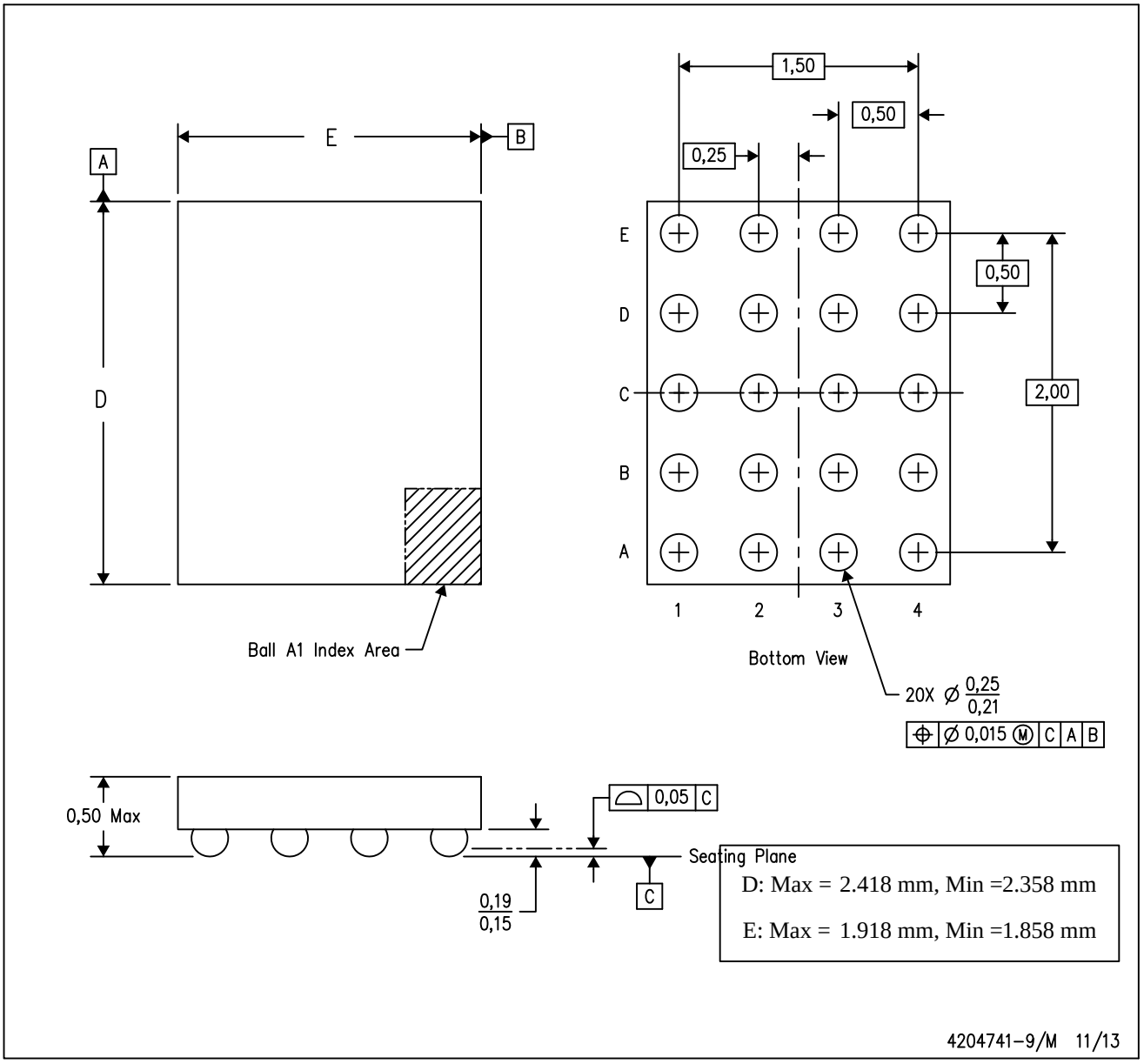
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.

DQS (R–PUSON–N20) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

YZP (R–XBGA–N20) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

重要声明和免责声明

TI 均以“原样”提供技术性及可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (http://www.ti.com.cn/zh-cn/legal/termsofsale.html) 以及ti.com.cn上或随附TI产品提供的其他可适用条款的约束。TI提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122