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| **Section:** | *AL2* |

**ECE 408/CS483 Milestone 3 Report**

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| 1. List Op Times, whole program execution time, and accuracy for batch size of 100, 1k, and 10k images from your basic forward convolution kernel in milestone 2. This will act as your baseline this milestone. |
| |  |  |  |  |  | | --- | --- | --- | --- | --- | | Batch Size | Op Time 1 | Op Time 2 | Total Execution Time | Accuracy | | 100 | *2.07946 ms* | *31.8139 ms* | *1.117 s* | *0.86* | | 1000 | *20.7417 ms* | *322.405 ms* | *9.517 s* | *0.886* | | 10000 | *207.877 ms* | *3242.94 ms* | *1 m 33.543 s* | *0.8714* |   *(build-fbba3)* |
| 1. **Optimization 1: *Weight matrix (kernel values) in constant memory*** |
| * 1. Which optimization did you choose to implement and why did you choose that optimization technique. |
| *Calculation for all outputs require kernel, and it does not change during grid execution. These characteristics make kernel array a nice candidate to move into constant memory with minimal code change.* |
| * 1. How does the optimization work? Did you think the optimization would increase performance of the forward convolution? Why? Does the optimization synergize with any of your previous optimizations? |
| *Constant memory resides in device memory and caches in the constant cache. In case of cache hit, the resulting memory requests are served at the throughput of the constant cache. Since kernel weight will not change throughout the inference, I believe constant memory can provide some improvements, and can work well with other optimization (this is my first optimization).* |
| * 1. List the Op Times, whole program execution time, and accuracy for batch size of 100, 1k, and 10k images using this optimization (including any previous optimizations also used). |
| |  |  |  |  |  | | --- | --- | --- | --- | --- | | Batch Size | Op Time 1 | Op Time 2 | Total  Execution  Time | Accuracy | | 100 | *1.86608 ms* | *30.5911 ms* | *1.093 s* | *0.86* | | 1000 | *18.702 ms* | *314.776 ms* | *9.420 s* | *0.886* | | 10000 | *186.951 ms* | *3183.48 ms* | *1 m 32.670 s* | *0.8714* | |
| * 1. Was implementing this optimization successful in improving performance? Why or why not? Include profiling results from *nsys* and *Nsight-Compute* to justify your answer, directly comparing to your baseline (or the previous optimization this one is built off of). |
| ***Op 1***    ***Op 2***    *In all following sections, I will use numbers directly instead of screenshot SOL.*   |  |  |  |  |  | | --- | --- | --- | --- | --- | |  | ***SM [%]*** | ***Memory [%]*** | ***L1 Cache [%]*** | ***Duration [%]*** | | *Op 1* | *+10.4%* | *-36.58%* | *-37.8%* | *-10.36%* | | *Op 2* | *+0.81%* | *-43.65%* | *-45.45%* | *-3.11%* |   *The statistics shows marginal improvement when we move the kernel to constant memory. Memory bandwidth drastically decreases as expected, but L1 cache utilization also decreases for some reason.*  *(build-08beb)* |
| * 1. What references did you use when implementing this technique? |
| *CUDA Toolkit v11.5.0 Programming Guide* |
| 1. **Optimization 2: *Sweeping various parameters to find best values (block sizes, amount of thread coarsening)*** |
| 1. Which optimization did you choose to implement and why did you choose that optimization technique. |
| *Nsight Compute shows my kernel launch only execute 4 blocks, which is less than the GPU’s 80 MPs. It also shows on average, each warp spends 3.3 cycles stalled on a fixed latency execution dependency. This calls for adjust block size.*  *Originally, I go for block size (32, 32), since maximum per thread block is 1024. However, dumping out the data dimension shows*  ***Op 1*** *(B=100, M=4, C=1, H=86, W=86, K=7)*  ***Op 2*** *(B=100, M=16, C=4, H=40, W=40, K=7)*  *Plug these numbers into kernel size calculation W-K+1 shows 80 and 34 respectively.*  *Therefore, I decided to do the following tests*   * *(4, 4), since GCD(80, 36)=4.* * *(8, 8), which leaves some warps unused for Op2.* * *(17, 17), perfect match for Op2, but not so much for Op1.* * *(20, 20), similar to (8, 8) with some idle warps for Op2, but larger block.*   *This implementation stacks on top of the constant memory one, but asides from comparing with previous optimization, we will compare with respect to (4, 4).*   * *(4, 4) vs (8, 8), (20, 20), to figure out if increase block size works.* * *(4, 4) vs (17, 17), (20, 20), whether we should optimize for individual ops.* |
| 1. How does the optimization work? Did you think the optimization would increase performance of the forward convolution? Why? Does the optimization synergize with any of your previous optimizations? |
| *<answer here>* |
| 1. List the Op Times, whole program execution time, and accuracy for batch size of 100, 1k, and 10k images using this optimization (including any previous optimizations also used). |
| ***Block size (4, 4)***   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Batch Size | Op Time 1 | Op Time 2 | Total  Execution  Time | Accuracy | | 100 | *1.19454 ms* | *16.3916 ms* | *1.084 s* | *0.86* | | 1000 | *11.8864 ms* | *163.821 ms* | *9.314 s* | *0.886* | | 10000 | *119.357 ms* | *1695.41 ms* | *1 m 31.348 s* | *0.8714* |   ***Block size (8, 8)***   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Batch Size | Op Time 1 | Op Time 2 | Total  Execution  Time | Accuracy | | 100 | *1.15893 ms* | *15.9704 ms* | *1.131 s* | *0.86* | | 1000 | *11.5606 ms* | *160.342 ms* | *9.702 s* | *0.886* | | 10000 | *114.973 ms* | *1603.01 ms* | *1 m 34.981 s* | *0.8714* |   ***Block size (17, 17)***   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Batch Size | Op Time 1 | Op Time 2 | Total  Execution  Time | Accuracy | | 100 | *1.20952 ms* | *18.0999 ms* | *1.165 s* | *0.86* | | 1000 | *11.8804 ms* | *187.275 ms* | *10.205 s* | *0.886* | | 10000 | *120.622 ms* | *1909.28 ms* | *1 m 40.053 s* | *0.8714* |   ***Block size (20, 20)***   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Batch Size | Op Time 1 | Op Time 2 | Total  Execution  Time | Accuracy | | 100 | *1.26736 ms* | *19.9817 ms* | *1.097 s* | *0.86* | | 1000 | *12.6605 ms* | *204.028 ms* | *9.310 s* | *0.886* | | 10000 | *125.81 ms* | *2071.2 ms* | *1 m 31.560 s* | *0.8714* | |
| 1. Was implementing this optimization successful in improving performance? Why or why not? Include profiling results from *nsys* and *Nsight-Compute* to justify your answer, directly comparing to your baseline (or the previous optimization this one is built off of). |
| *In this section, we will first compare performance with respect to block (4, 4), which can accommodate both ops without idle warps, but has utilize computation resource much worse.*  ***Increase block size***  *Block size (8, 8), optimize for op 1, op 2 has half warps left over.*   |  |  |  |  |  | | --- | --- | --- | --- | --- | |  | ***SM [%]*** | ***Memory [%]*** | ***L1 Cache [%]*** | ***Duration [%]*** | | *Op 1* | *-48.61%* | *-46.94%* | *-46.9%* | *-2.65%* | | *Op 2* | *-43.22%* | *-40.48%* | *+86.15%* | *-2.01%* |   *Block size (20, 20), similar to previous block condition.*   |  |  |  |  |  | | --- | --- | --- | --- | --- | |  | ***SM [%]*** | ***Memory [%]*** | ***L1 Cache [%]*** | ***Duration [%]*** | | *Op 1* | *-51.2%* | *-60.03%* | *+100.11%* | *+6.69%* | | *Op 2* | *-56.36%* | *-46.17%* | *+993.35%* | *+24.64%* |   ***Optimize for different ops***  *Block (20, 20), optimize for op 1*   |  |  |  |  |  | | --- | --- | --- | --- | --- | |  | ***SM [%]*** | ***Memory [%]*** | ***L1 Cache [%]*** | ***Duration [%]*** | | *Op 1* | *-51.2%* | *-60.03%* | *+100.11%* | *+6.69%* | | *Op 2* | *-56.36%* | *-46.17%* | *+993.35%* | *+24.64%* |   *Block (17, 17), optimize for op 2*   |  |  |  |  |  | | --- | --- | --- | --- | --- | |  | ***SM [%]*** | ***Memory [%]*** | ***L1 Cache [%]*** | ***Duration [%]*** | | *Op 1* | *-42.09%* | *-50.17%* | *+59.72%* | *-0.20%* | | *Op 2* | *-56.83%* | *-35.56%* | *+1181.68%* | *+13.44%* |   *Analysis shows that optimizing for op 2 (17, 17) indeed increases occupancy,*   |  |  |  |  |  | | --- | --- | --- | --- | --- | |  | ***(4, 4)*** | ***(8, 8)*** | ***(17, 17)*** | ***(20, 20)*** | | *Op 1* | *7.62%* | *3.9%* | *14.44%* | *20.3%* | | *Op 2* | *1.58%* | *2.81%* | *15.02%* | *16.11%* |   *and average active threads per warp indicates resources are utilized*   |  |  |  |  |  | | --- | --- | --- | --- | --- | |  | ***(4, 4)*** | ***(8, 8)*** | ***(17, 17)*** | ***(20, 20)*** | | *Op 1* | *16* | *32* | *27.71* | *30.77* | | *Op 2* | *14.29* | *25.69* | *28.9* | *26.27* |   *From these results, we can see that while larger block size can hide latency effect and better utilize our cache, they are not particularly beneficial at current stage, since large amount of uncoalesced global will only hinder the performance.*  *To improve this, we can batch across the B (batch) or M (output channel) dimension, however, this will need shared memory in the kernel in order to hold the calculation results before writing it back.*  *In next stage, we should start looking into tweaking the kernel itself, instead of lingering with the naïve implementation.*  *(build-7649f; build-9c79b; build-df87b; build-aa107)* |
| 1. What references did you use when implementing this technique? |
| [*How do I choose grid and block dimensions for CUDA kernels?*](https://stackoverflow.com/questions/9985912/how-do-i-choose-grid-and-block-dimensions-for-cuda-kernels) |

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| 1. **Optimization 3: *Tiled shared memory convolution*** |
| * 1. Which optimization did you choose to implement and why did you choose that optimization technique. |
| *From previous optimization, we already know naïve implementation will cause lots of uncoalesced global memory access. A straightforward way to solve this is to use shared memory, similar to what we have done in MP4.*  *This also has an added benefit of batch process across other independent dimensions (B and M) mentioned in previous optimization.* |
| * 1. How does the optimization work? Did you think the optimization would increase performance of the forward convolution? Why? Does the optimization synergize with any of your previous optimizations? |
| *Since shared memory is on-chip, it has a much higher bandwidth and lower latency than global memory. From previous optimization, we know that the device is heavily under utilized due to inefficient memory access pattern, and lack of complete utilization of CUDA cores.*  *We should be able to build on-top of constant memory improvements. In this optimization, we will also slightly go over parameter sweep again.* |
| * 1. List the Op Times, whole program execution time, and accuracy for batch size of 100, 1k, and 10k images using this optimization (including any previous optimizations also used). |
| *Basic implementation of tiled convolution kernel.*   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Batch Size | Op Time 1 | Op Time 2 | Total  Execution  Time | Accuracy | | 100 | *0.185767 ms* | *1.01014 ms* | *1.06 s* | *0.86* | | 1000 | *1.57127 ms* | *10.2723 ms* | *9.11 s* | *0.886* | | 10000 | *15.5011 ms* | *111.34 ms* | *1 m 30.141 s* | *0.8714* |   *With block (8, 8, 4), where z implies batched across the B dimension.*   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Batch Size | Op Time 1 | Op Time 2 | Total  Execution  Time | Accuracy | | 100 | *0.189615 ms* | *0.814923 ms* | *1.117 s* | *0.86* | | 1000 | *1.58099 ms* | *6.20755 ms* | *9.123 s* | *0.886* | | 10000 | *15.4214 ms* | *60.4442 ms* | *1 m 29.363 s* | *0.8714* |   *With block (8, 8, 8)*   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Batch Size | Op Time 1 | Op Time 2 | Total  Execution  Time | Accuracy | | 100 | *0.197114 ms* | *0.851227 ms* | *1.113 s* | *0.86* | | 1000 | *1.60071 ms* | *6.38676 ms* | *9.544 s* | *0.886* | | 10000 | *15.682 ms* | *61.8753 ms* | *1 m 33.212 s* | *0.8714* | |
| * 1. Was implementing this optimization successful in improving performance? Why or why not? Include profiling results from *nsys* and *Nsight-Compute* to justify your answer, directly comparing to your baseline (or the previous optimization this one is built off of). |
| *Yes, very successful.*  ***Increase B block size***  *Op 1, block size (8, 8, \*), compare with constant memory implementation*   |  |  |  |  |  | | --- | --- | --- | --- | --- | |  | ***SM [%]*** | ***Memory [%]*** | ***L1 Cache [%]*** | ***Duration [%]*** | | *1* | *+1155.91%* | *+1949.8%* | *+110.5%* | *-91.65%* | | *4* | *+1154.11%* | *+1920.96%* | *+107.84%* | *-91.64%* | | *8* | *+1137.85%* | *+1889%* | *+105.33%* | *-91.52%* |   *Op 2*   |  |  |  |  |  | | --- | --- | --- | --- | --- | |  | ***SM [%]*** | ***Memory [%]*** | ***L1 Cache [%]*** | ***Duration [%]*** | | *1* | *+4086.97%* | *+4369.92%* | *+72.17%* | *-96.56%* | | *4* | *+4549.94%* | *+7602.29%* | *+195.45%* | *-98.01%* | | *8* | *+4422.48%* | *+7385.23%* | *+189.69%* | *-97.96%* |   *Re-using the conclusion from previous optimization, with (8, 8) seems to be the balancing point, we can see that to full utilize all SMs, increase B block size to 4 is the sweet spot.*  *(build-e1787; build-4bde7)* |
| * 1. What references did you use when implementing this technique? |
| *My “MP4: 3D Convolution” on WebGPU.* |
| 1. **Optimization 4: *Tuning with restrict and loop unrolling (considered as one optimization only if you do both)*** |
| * 1. Which optimization did you choose to implement and why did you choose that optimization technique. |
| *After finish tuning the tiled shared memory convolution, we can see the actual convolution is performed on a fixed size kernel (after all, we already stores the kernel in constant memory).*  *We can do the low hanging fruit by adding* #pragma unroll *to the nested loop that performs kernel multiplication. We also know we are not working with in-place convolution, so we can simply drop in the* \_\_restrict\_\_ *keyword.* |
| * 1. How does the optimization work? Did you think the optimization would increase performance of the forward convolution? Why? Does the optimization synergize with any of your previous optimizations? |
| *<answer here>* |
| * 1. List the Op Times, whole program execution time, and accuracy for batch size of 100, 1k, and 10k images using this optimization (including any previous optimizations also used). |
| ***Restrict***   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Batch Size | Op Time 1 | Op Time 2 | Total  Execution  Time | Accuracy | | 100 | *0.139424 ms* | *0.530685 ms* | *1.169 s* | *0.86* | | 1000 | *1.13016 ms* | *4.16747 ms* | *9.991 s* | *0.886* | | 10000 | *10.9497 ms* | *40.5972 ms* | *1 m 38.343 s* | *0.8714* |   ***Unroll***   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Batch Size | Op Time 1 | Op Time 2 | Total  Execution  Time | Accuracy | | 100 | *0.138641 ms* | *0.521346 ms* | *1.08 s* | *0.86* | | 1000 | *1.12127 ms* | *4.15797 ms* | *9.127 s* | *0.886* | | 10000 | *10.9651 ms* | *40.5293 ms* | *1 m 37.837 s* | *0.8714* |   ***Restrict + unroll***   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Batch Size | Op Time 1 | Op Time 2 | Total  Execution  Time | Accuracy | | 100 | *0.137104 ms* | *0.556045 ms* | *1.088 s* | *0.86* | | 1000 | *1.1236 ms* | *4.17904 ms* | *9.113 s* | *0.886* | | 10000 | *10.9645 ms* | *40.5441 ms* | *1 m 29.418 s* | *0.8714* | |
| * 1. Was implementing this optimization successful in improving performance? Why or why not? Include profiling results from *nsys* and *Nsight-Compute* to justify your answer, directly comparing to your baseline (or the previous optimization this one is built off of). |
| *Compare with the tiled convolution in previous optimization, using block size (8, 8, 4) as baseline.*  ***Op 1***   |  |  |  |  |  | | --- | --- | --- | --- | --- | |  | ***SM [%]*** | ***Memory [%]*** | ***L1 Cache [%]*** | ***Duration [%]*** | | *Restrict* | *-18.35%* | *+32.37%* | *+32.48%* | *-28.89%* | | *Unroll* | *-17.93%* | *+33.04%* | *+33.01%* | *-29.32%* | | *Restrict*  *Unroll* | *-17.88%* | *+33.1%* | *+32.97%* | *-29.25%* |   ***Op 2***   |  |  |  |  |  | | --- | --- | --- | --- | --- | |  | ***SM [%]*** | ***Memory [%]*** | ***L1 Cache [%]*** | ***Duration [%]*** | | *Restrict* | *-9.52%* | *+38.42%* | *+39.95%* | *-33.07%* | | *Unroll* | *-8.13%* | *+40.13%* | *+40.35%* | *-33.09%* | | *Restrict*  *Unroll* | *-8.4%* | *+39.72%* | *+40.22%* | *-33.3%* |   *When adding the* \_\_restrict\_\_ *keyword, we can find the compiler unroll the inner most loop by examining the PTX.*   |  |  | | --- | --- | | ***Baseline*** | ***Restrict*** | | **mul.wide.s32 %rd10, %r32, 4;**  mov.u64 %rd11, kernel;  **add.s64 %rd12, %rd11, %rd10;**  ld.const.f32 %f21, [%rd12];  ld.shared.f32 %f22, [%r96];  fma.rn.f32 %f46, %f22, %f21, %f46; | mov.u64 %rd8, kernel;  add.s64 %rd9, %rd8, %rd7;  ld.const.f32 %f10, [%rd9];  ld.shared.f32 %f11, [%r78];  fma.rn.f32 %f12, %f11, %f10, %f32;  ld.const.f32 %f10, **[%rd9+4]**;  ld.shared.f32 %f11, **[%r78+4]**;  fma.rn.f32 %f15, %f14, %f13, %f12;  … |   *However, with #pragma unroll, we can force the compiler to further unroll the nested loop entirely*  for (int p = 0; p < K; p++) {  for (int q = 0; q < K; q++) {  }  }  *(build-f2beb; build-5c5e7; build-3361b)* |
| * 1. What references did you use when implementing this technique? |
| *<answer here>* |
| 1. **Optimization 5: *<optimization name>***   ***(Delete this section if you did not implement this many optimizations.)*** |
| * 1. Which optimization did you choose to implement and why did you choose that optimization technique. |
| *<answer here>* |
| * 1. How does the optimization work? Did you think the optimization would increase performance of the forward convolution? Why? Does the optimization synergize with any of your previous optimizations? |
| *<answer here>* |
| * 1. List the Op Times, whole program execution time, and accuracy for batch size of 100, 1k, and 10k images using this optimization (including any previous optimizations also used). |
| |  |  |  |  |  | | --- | --- | --- | --- | --- | | Batch Size | Op Time 1 | Op Time 2 | Total Execution Time | Accuracy | | 100 | *<op\_time>* | *<op\_time>* | *<exec\_time>* | *<accuracy>* | | 1000 | *<op\_time>* | *<op\_time>* | *<exec\_time>* | *<accuracy>* | | 10000 | *<op\_time>* | *<op\_time>* | *<exec\_time>* | *<accuracy>* | |
| * 1. Was implementing this optimization successful in improving performance? Why or why not? Include profiling results from *nsys* and *Nsight-Compute* to justify your answer, directly comparing to your baseline (or the previous optimization this one is built off of). |
| *<answer here>* |
| * 1. What references did you use when implementing this technique? |
| *<answer here>* |
| 1. **Optimization 6: *<optimization name>***   ***(Delete this section if you did not implement this many optimizations.)*** |
| * 1. Which optimization did you choose to implement and why did you choose that optimization technique. |
| *<answer here>* |
| * 1. How does the optimization work? Did you think the optimization would increase performance of the forward convolution? Why? Does the optimization synergize with any of your previous optimizations? |
| *<answer here>* |
| * 1. List the Op Times, whole program execution time, and accuracy for batch size of 100, 1k, and 10k images using this optimization (including any previous optimizations also used). |
| |  |  |  |  |  | | --- | --- | --- | --- | --- | | Batch Size | Op Time 1 | Op Time 2 | Total Execution Time | Accuracy | | 100 | *<op\_time>* | *<op\_time>* | *<exec\_time>* | *<accuracy>* | | 1000 | *<op\_time>* | *<op\_time>* | *<exec\_time>* | *<accuracy>* | | 10000 | *<op\_time>* | *<op\_time>* | *<exec\_time>* | *<accuracy>* | |
| * 1. Was implementing this optimization successful in improving performance? Why or why not? Include profiling results from *nsys* and *Nsight-Compute* to justify your answer, directly comparing to your baseline (or the previous optimization this one is built off of). |
| *<answer here>* |
| * 1. What references did you use when implementing this technique? |
| *<answer here>* |