On the Development of a Compact Sub-Nanosecond Tunable Monocycle Pulse Transmitter for UWB Applications

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***Abstract*—Development of a new sub-nanosecond monocycle pulse transmitter with tunable pulse duration for short-range low-power ultra-wideband radar and communication systems is presented along with detailed design and analysis. The developed pulse transmitter is simple, compact, and can be realized using planar or uniplanar integrated circuits. A novel *RC* coupling circuit along with a high driving current, provided by a high-speed amplifier and buffers, are used to obtain an increase in the output power. A decoupling circuit is implemented to reduce ringing on the monocycle pulse and provide necessary pulse clamping. Tuning of the output monocycle-pulse duration is achieved by using two distributed delay lines, coupled together by the decoupling network, each spatially loaded with antiparallel p-i-n diodes that are alternately switched on and off. Measurement results show tunable monocycle pulse durations in range of 0.4–1.2 ns, approximately corresponding to the operating frequency range of 0.15–3.7 GHz, and 200–400 mW of pulse peak power. The calculated and measured pulse durations also agree reasonably well.**

***Index Terms*—Pulse generator, pulse transmitter, ultra-wideband (UWB) radar and communication, UWB systems, UWB transmitter.**

I. Introduction

SUB-NANOSECOND baseband (or video) pulse waveforms are used in various types of ultra-wideband (UWB) impulse radar and communication systems for different applications such as pavement assessment, bridge-deck inspection, geophysical explorations, collision avoidance, fluid level sensing, detection and classification of unexploded ordnance (UXO) and land mines [1]–[8], and short-range in-building communications [9].

Baseband pulse generators are main components in the transmitter of an UWB impulse radar or communication system. Different types of pulse generators may be used, depending on requirements for output peak-power, bandwidth (BW), and system's components (e.g., antenna) through which the pulse is transmitted. Step-function, Gaussian impulse, and monocycle pulse are typical waveforms used in UWB systems. Step-function and impulse contain dc and a large portion of low-frequency spectral components, which cannot be transmitted through practical antennas. A monocycle pulse, on the other hand, has no dc component and band-limited characteristic, facilitating its transmission using a practical antenna. Furthermore, using a monocycle pulse facilitates the design of other components including an antenna in the system.

For high-power applications such as deep-penetration ground penetrating radar (GPR), pulse generators using avalanche transistors with or without a series stack of step-recovery diodes (SRDs) have been commonly used [4]–[6]. The opto-electronic design using a GaAs photoconductive semiconductor switch and the electronic design using a drift step-recovery diode (DSRD) and silicon avalanche shaper are also well-known methods for high-power pulse applications [10], [11]. These high-power pulse generators, however, have bulky complicated structures and are expensive. Devices such as DSRD are also difficult to find in the commercial market. Currently available high-power pulse generators have limited performance. Their achievable minimum pulsewidth is only approximately 1 ns and the maximum output pulse repetition frequency (PRF) is usually approximately 1 MHz.

Research in efficient pulse-generator design for low-power short-range UWB impulse radar and communication systems has not attracted much attention, partly because of the availability of commercial products with good performance [12]–[14]. However, with the increasing demand of low-power and compact UWB systems, it is naturally desirable to have compact low-cost pulse generators. Most of the sub-nanosecond pulse generators with low output power use only one or two SRDs [6], [15]–[25] for generation of step-function, impulse, or monocycle pulse. A desirable property for pulse generators is the tuning capability of the pulse duration. A pulse of wide duration contains large low-frequency components, enabling the pulse signal to propagate deeply into a medium because of the relatively low propagation loss of its low-frequency components. A pulse of shorter duration, on the other hand, has a wider frequency BW, making feasible a higher range resolution. The pulse that can change its duration, especially by an electronic means, would, therefore, have both advantages of increased penetration (or range) and fine-range resolution, and is attractive for UWB systems. Electronically tunable pulse generators are also desired for a measurement equipment. The polarimetric video impulse radar described in [7] and [8] is a good example showing the usefulness of the pulse's tuning capability. The pulse generators proposed in [25] and [26]

Manuscript received February 28, 2005; revised July 23, 2005. This work was supported in part by the National Science Foundation, by the Texas Transportation Institute, by the Southwest Region University Transportation Center, by the Texas Advanced Research Program, and by Dell.

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Digital Object Identifier 10.1109/TMTT.2005.860299

provide relatively high output pulse power and handy tuning capability, but the output waveform is an impulse or a step function. The tunable pulse generators reported in [20] also produce impulses only. The monocycle pulse generators shown in [17]–[19] provide relatively low output power (210 mW of peak power) without tuning capability.

In this paper, we present the development of a novel sub-nanosecond tunable monocycle pulse transmitter for short-range low-power UWB applications. The developed monocycle pulse transmitter produces monocycle pulses with 10 MHz of PRF, a tuning range of 0.4–1.2 ns for the pulse duration, corresponding approximately to 0.15–3.7-GHz operating frequency range. The output pulse amplitude is from 6 to 9 V_{pp} (peak-to-peak voltage), corresponding to 200–400 mW of peak power, which is comparable to the output power of commercial products.

The developed tunable monocycle pulse transmitter makes use of a single SRD to form a fast transient rise time. Relatively high output pulse power is obtained by using high driving power for the SRD, provided by a driving circuit consisting of high-speed amplifier and buffer integrated circuits (ICs). This design approach greatly simplifies the circuit design as compared to that using discrete components proposed in [24] and [25] and avoids using an expensive high-power wide-band monolithic microwave integrated circuit (MMIC) at the output stage of the pulse generator, as proposed in [18] and [19]. In addition to using high driving power, high output power can also be obtained by increasing the output power efficiency of the SRD pulse generator using a proper dc biasing scheme for the SRD, as described in [23]–[25]. In our transmitter, a novel coupling circuit for the SRD is designed to increase the output power efficiency. This circuit has the form of a first-order high-pass *RC* filter and does not require any external dc bias for normal operation. A decoupling circuit is also employed to reduce the ringing level of the output pulse.

The basic idea for realizing the monocycle pulse tuning ability relies on using p-i-n-diode switches proposed for tunable impulses [20]. The same tuning principle is extended to make a tunable monocycle rather than an impulse. In comparison with the tuning method using dc-bias control for the SRD [25], the p-i-n diode switching method is simpler, facilitates the design of tunable monocycle pulse waveforms, and provides a convenient tuning operation. In the developed monocycle pulse transmitter, an impulse is generated first and a pulse-shaping circuit is used to convert the impulse to a monocycle.

This paper is organized as follows. Section II discusses the design technique for the SRD impulse generator to obtain fast transient and improved output pulse power. Section III covers details of the design for the tunable monocycle pulse transmitter, including the tuning technique for the pulse duration and the design of the decoupling circuit required for the monocycle pulse shaping. Section IV describes the fabrication and performance of the tunable monocycle pulse transmitter. Finally, a conclusion is presented in Section V.

II. Design of Delay-Line SRD Impulse Generator

The basic element in the developed tunable monocycle pulse transmitter is the delay-line impulse generator. Formation of an impulse using the delay lines is a classical technique used

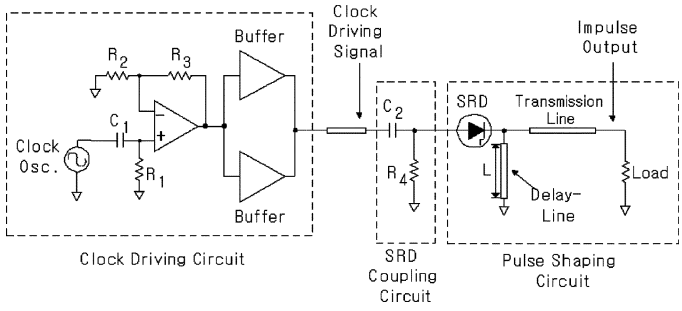


Fig. 1. Circuit diagram for the designed SRD delay-line impulse generator.

in the digital and/or pulse circuit areas. Some SRD impulse or monocycle-pulse generators have been designed using the same delay-line principle and implemented on microstrip or coplanar waveguide (CPW) structures [15]–[19]. Another type of SRD impulse generator, extensively used for sub-nanosecond pulse generation and the microwave multiplier, is the shunt-mode SRD impulse generator [21], [22].

Before beginning the circuit design, important SRD characteristics affecting the circuit performance of the impulse generator need to be identified. One of the important characteristics is the transition time of the SRD that determines the minimum achievable pulse's transition time. The other is the minority carrier lifetime (MCLT) of the SRD, which affects the storage time under reverse-bias conditions. If a clock signal is applied to the SRD pulse-shaping circuit, the rise time of the clock should be less than the MCLT of the SRD in order to obtain maximum achievable pulse amplitude [23]. In our design, the SRD is selected for 70-ps transition time and 10-ns MCLT, assuming that the output pulse duration to be generated is 200 ps and the rise time of the clock is 10 ns.

Fig. 1 shows the overall circuit diagram of the designed impulse generator. It can be subdivided into the clock driving, the SRD coupling, and the pulse shaping circuits according to their functions. The clock-driving circuit consists of a clock oscillator, a noninverted opamp voltage amplifier, and two current boosting buffers. The clock oscillator generates a transistor–transistor logic (TTL) compatible clock signal with 5 ns of rise time and 10 MHz of PRF. This fast rise-time clock signal is required according to the MCLT of the selected SRD. High voltages of the clock driving signal for the SRD, indicated in Fig. 1, produces large amplitudes for the output impulse. To increase the driving signal voltage level, the input clock signal is amplified by amplifier and buffers. The desired voltage level of the driving signal is set as 20 V_{pp}, taking into account the selected SRD having 15 V of breakdown voltage. The amplifier is designed to have a voltage gain of 4 in order to obtain 20 V_{pp} from a 5-V_{pp} TTL input signal and a BW of 100 MHz using a wide-band opamp with 400-MHz unity-gain BW in order to prevent the input rise time from slowing down. The buffer is used to supply the SRD, representing a low-impedance load, with enough current to obtain a high output voltage swing of 20 V_{pp} and to reduce the large loading effect on the amplifier. Two buffers are used to enhance the reduction of loading effects and to have some margins for its supplied current capacity. The loading circuit analysis, which will be shown below, determines the required current capacity for the buffers.

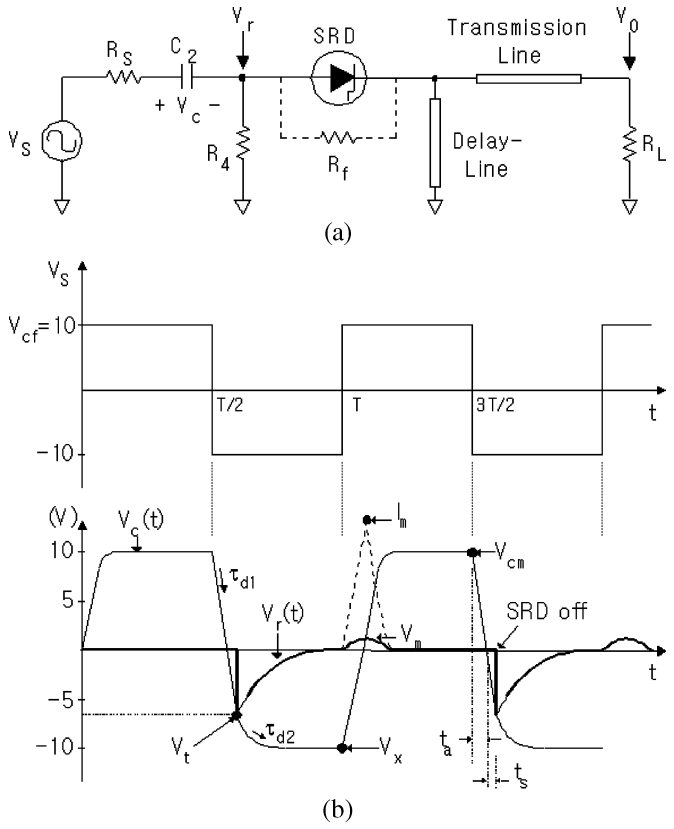


Fig. 2. (a) Equivalent circuit of the SRD delay-line impulse generator. (b) Voltage and current waveforms that occurred in the circuit.

To produce an impulse having high amplitudes and a transition as fast as possible, a proper dc bias can be applied to the SRD [23]–[25]. The dc bias controls the quantity of the stored charge in the SRD through the forward-bias current, which determines the storage time, thus affecting the turn-off transition time when the SRD is reverse biased. The stored charge should be large enough to have a sufficient storage time so that a fast transition may occur at the maximum voltage level of the input clock signal. On the other hand, it should also be minimized to obtain as fast a transition time as possible. In our design, we employ an SRD coupling circuit, as shown in Fig. 1, to avoid the use of an external bias network. The coupling circuit works effectively to control the quantity of the stored charge in the SRD. Detailed analysis of this circuit, included in the following, will explain this controlling effect and determine its optimal component values (R_4 and C_2 in Fig. 1).

An equivalent circuit for the delay-line impulse generator is shown in Fig. 2(a), in which the driving circuit in Fig. 1 is replaced by a voltage source with a source resistance. R_f represents the forward-biased resistance of the SRD. Fig. 2(b) displays the voltages and currents in Fig. 2(a). The source signal V_s is assumed as an ideal clock with instant transitions to simplify the analysis. The waveforms for V_c and V_r, defined in Fig. 2(a), are drawn by means of a basic transient analysis. In the waveform of $V_r(t)$ (input to the pulse shaping circuit), the fast transition that occurred due to the SRD's turn off of the SRD is illustrated. This transient is transformed to an impulse at the output in combination with the reflected one from the short-circuited transmission line representing the delay line. The waveform of the forward-biased current flowing through the SRD, which determines the stored charge quantity, is also shown with a peak value of I_m.

Our design goal is to determine optimum values for the resistors (R_4) and capacitors (C_2) in the equivalent circuit to produce a maximum transient amplitude of V_t for $V_r(t)$, described in Fig. 2(b). The values for R_4 is first determined qualitatively as follows. To obtain a sufficient storage time, the peak amplitude of the forward current I_m should be as large as possible. Since the forward current is proportional to the diode voltage,

$$I_m \propto V_m \propto -V_c(T^-) + V_s(T^+) = -V_x + V_{cf} \tag{1}$$

where V_{cf} is the peak voltage of the clock source that, in our case, is equal to 10 V. From the relationship given in (1), in order to increase I_m, $|V_x|$ should be equal to V_{cf}. To increase $|V_x|$ and V_t, $\tau_{d2} = (R_4 + R_s)C$ and $\tau_{d1} = (R_f + R_s)C$ should be decreased. Therefore, R_4, R_s, and R_f should be as small as possible. However, R_4 needs to be much greater than R_f to achieve a smooth transition after the fast diode turn-off transition in V_r. In general, a value greater than ten times of R_f should be used for R_4. As a result, assuming R_f is equal to the series resistance of the SRD, which, in our case, is 0.22 Ω, $R_4 = 10\,\Omega$ can then be selected as a reasonable value.

An optimal value for C_2 can be found by deriving equations for the waveforms shown in Fig. 2(b) and solving them using an iterative optimization method. First, a small negative value for V_x is assumed as an initial value. From the rising and falling edges of the waveform $V_c(t)$, the following equations can be derived:

$$V_{cm} = V_{cf} + (V_x - V_{cf})e^{-\frac{T}{2R_fC_2}} \tag{2}$$

$$V_t = -V_{cf} + (V_{cm} + V_{cf})e^{-\frac{t_t}{R_fC_2}} \tag{3}$$

where $t_t = t_s + t_a$ with t_s and t_a defined in Fig. 2(b), where T represents the clock period. The storage time t_s can be calculated from the fact that the stored charge in the SRD resulted from the forward current flowing is the same as the removed charge caused by the reverse current. Assuming the forward current is proportional to the applied diode voltage, it is straightforward to derive the following equation for the stored charge Q_f:

$$Q_f \cong \frac{V_a(t_k)}{R_f}\left[\frac{t_k}{2} + R_fC_2\left[e^{-\frac{t_k}{R_fC_2}} - e^{-\frac{t_L}{R_fC_2}}\right]\right] \tag{4}$$

where $V_a(t)$ is the response of a ramp signal with a slew rate of m,

$$V_a(t) = mR_fC_2\left(1 - e^{-\frac{t}{R_fC_2}}\right) \tag{5}$$

where

$$m = \frac{|V_x|}{t_k}$$

t_k is a half of the rise time t_r of the clock source and t_L is the MCLT of the SRD. Similarly, the removed charge quantity Q_r can be derived for two distinct cases. For $t_s \le t_r$,

$$Q_r \cong \frac{V_a(t_s)}{2R_f}t_s \tag{6}$$

where

$$m = \frac{V_{cm}}{t_k}$$

For $t_s > t_r$,

$$Q_r \cong \frac{V_a(t_k)}{R_f}\left[\frac{t_k}{2} + R_f C_2\left[e^{-\frac{t_k}{R_f C_2}} - e^{-\frac{t_s}{R_f C_2}}\right]\right]. \quad (7)$$

The estimate of t_s can now be obtained by an iterative optimization method using the following criterion:

$$\widehat{t_s} = \arg\left(\min_{t_o \le t \le t_L} |Q_f - Q_r|\right) \quad (8)$$

where t_o is a small time step used in the iteration process. Equation (8) defines a minimization problem in which the estimate of t_s is chosen to minimize the difference between Q_f and Q_r for the time interval from t_o to t_L. From (3), with the condition of $V_t = 0$,

$$\widehat{t_a} = -R_f C_2\left[\ln\left(\frac{V_{cf}}{V_{cm} + V_{cf}}\right)\right]. \quad (9)$$

Using a negative part of the waveform $V_c(t)$ corresponding to the portion after the SRD turn-off transition, the updated estimate value of V_x can be calculated as

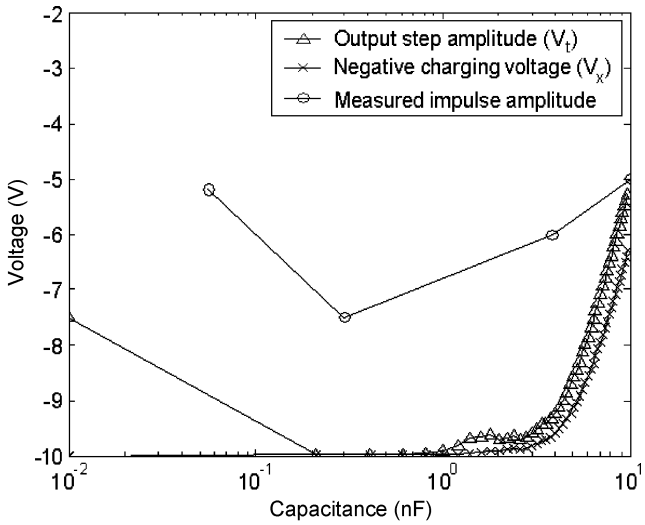
$$\widehat{V_x} = -V_{cf} + (V_t + V_{cf})e^{-\frac{\left(\frac{T}{2} - t_t\right)}{R_4 C_2}}. \quad (10)$$

Finally, the estimate of V_t can be obtained using the following criterion:

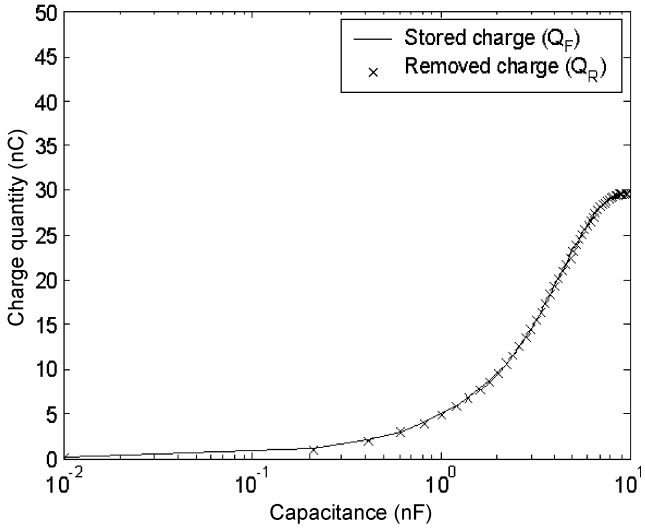
$$\widehat{V_t} = \arg\left(\min_{n \to \infty}\left|\widehat{V_x}(n) - \widehat{V_x}(n-1)\right|\right) \quad (11)$$

where n represents the number of iterations in the optimization procedure. Results from the simulation and measurement are given in Fig. 3. Fig. 3(a) shows calculated values for the negative charging voltage V_x and the transient step voltage V_t along with the measured impulse amplitude as a function of the capacitance values of the *RC* coupling circuit. The simulation result for the step amplitude V_t shows a consistent trend with the measured impulse amplitude, thus validating the simulation. The discrepancy between the calculated and measured voltages is due largely to the facts that the actual transition time of the SRD is not considered and the rise time of the employed clock driving signal is not sufficiently fast. From this result, an optimal value for C_2 can be chosen within the range of $0.2 \sim 1$ nF. The simulation results for the stored and removed charge quantities, shown in Fig. 3(b), confirms the fact that $Q_F \approx Q_R$ and, hence, verifies the convergence of the simulation. $C_2 = 200$ pF is chosen as an optimal initial value based on the result in Fig. 3(b), considering the fact that smaller stored charge makes faster transition.

The required current capacity for the current boosting buffer can be approximately calculated based on the previous analysis. The loading circuit for the buffer is the same as that shown in Fig. 2(a) and the voltage waveform applied to the load is the same as $V_r(t)$ in Fig. 2(b). Assuming $R_4 = 12\ \Omega$, $C_2 = 1$ nF, and $R_s + R_f = 1\ \Omega$, the peak voltage amplitude with respect to the forward current is calculated as 2.77 V using (5).



(a)



(b)

Fig. 3. (a) Calculated and measured voltages for the designed delay-line impulse generator. (b) Calculated results for the stored and removed charge quantities in the SRD.

The required positive average current can then be calculated as 173 mA. Similarly, the negative average current required is determined as 210 mA. This result shows that the two parallel-connected current buffers, each with ± 250 mA of output current capacity, can satisfy the driving current requirements with some design margin.

III. Design of Tunable Monocycle Pulse Transmitter

The tuning method used in our design is based upon the p-i-n diode switching method described in [20] for impulse generation. Here it is extended to generate various monocycle pulse durations. The underlying principle of the tuning method using p-i-n diode switching is relatively simple. Fig. 4(a) shows an instance of the distributed delay line for tuning of the impulse duration. The original delay line, seen in Figs. 1 and 2(a), is subdivided into several transmission-line sections, separated by dc blocking capacitors, to form a distributed delay line with each

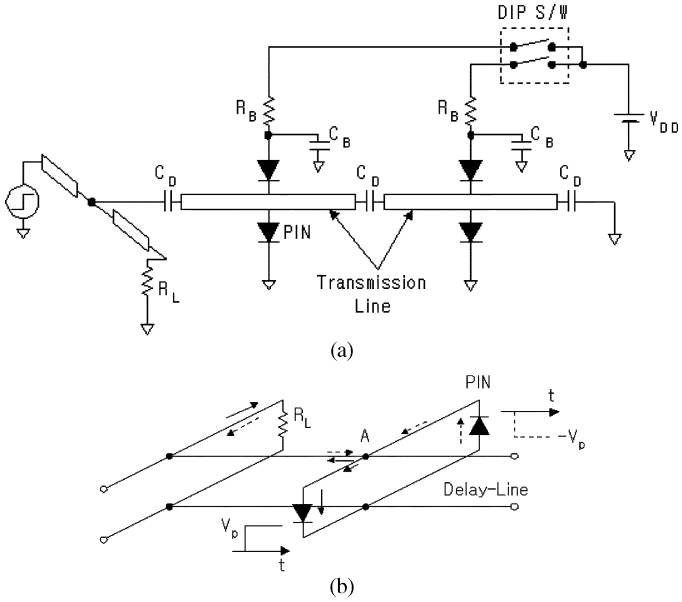


Fig. 4. (a) Circuit diagram for a distributed delay-line using antiparallel p-i-n–diode pairs. (b) Illustration showing the principle of using a p-i-n–diode pair to obtain a synthetic short circuit. The solid and dashed line arrows represent current flows corresponding to the positive and negative step voltage transients, respectively.

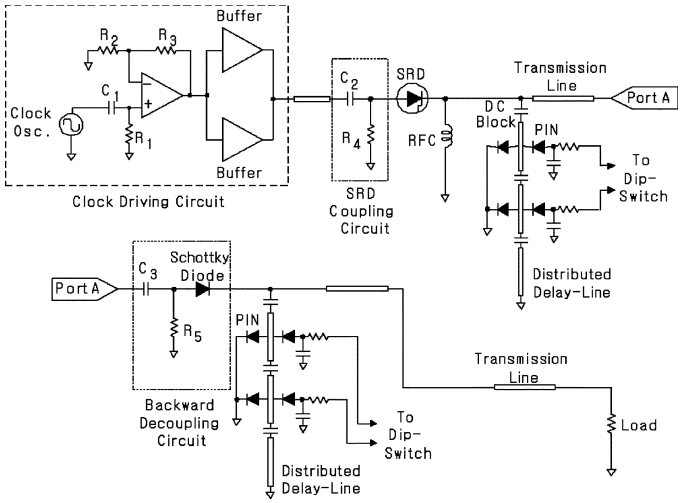


Fig. 5. Circuit diagram of the designed tunable monocycle pulse transmitter.

section containing an antiparallel p-i-n–diode pair and a biasing circuitry. A synthetic short circuit can be created at each diode-pair connection point by turning on the p-i-n diodes through a dual in-line package (DIP) switch. By changing the DIP switch connections alternately, various delay lines of different lengths can be effectively made, hence, generating different impulse durations corresponding to different roundtrip times of the step signal propagating on the delay line. Use of a pair of antiparallel p-i-n diodes instead of a single diode at each junction along the delay line is explained in Fig. 4(b). Let us assume a positive step pulse arrives at junction A on a delay-line section and both the p-i-n diodes are turned on. Assuming further that the step pulse is a large signal, then only two antiparallel connected p-i-n-diodes can support opposite current directions required by the incident and reflected step pulses. An antiparallel p-i-n diode-pair configuration, therefore, creates a synthetic short circuit closer to the ideal one than a single-diode configuration for a large-signal input. The other advantage of using a pair of p-i-n diodes is that one of the diodes can be placed on the side of the bias circuit to reduce the coupling of the incident pulse to the bias circuitry, resulting in better isolation than using a large resistance for biasing and isolation purposes. Moreover, using two diodes supports the balance of the circuit configuration.

Fig. 5 shows a simplified overall circuit diagram for the designed tunable monocycle pulse transmitter. The clock-driving and SRD coupling circuits have the same configurations as those for the impulse generator described in Section II. A broad-band RF choke (RFC) is used to provide a return for the low-frequency clock driving signal to the ground. This is necessary in order to create a similar loading circuit as in the impulse generator design so that the previous driving and coupling circuit designs result for the driving and coupling circuits of the impulse generator may be applied directly to the monocycle pulse transmitter. The RFC used in our design is ADCH-80A manufactured by the Mini-Circuits Company, Brooklyn, NY. Two distributed delay lines with identical configuration are used for tuning of the monocycle pulse duration. The first one is used for formation of various impulse durations. The other is used for controlling the roundtrip time of the generated impulse, which results in monocycle pulses with different durations at the output load.

A direct coupling of the two distributed delay lines may cause problem of backward transmission of the reflected impulse from the second to the first delay line, making large multiple reflections and eventually causing large ringing on the output signal. A backward decoupling circuit is, therefore, needed between the two delay lines to reduce the backward coupling effect. This decoupling circuit, consisting of a capacitor, resistor, and Schottky diode, as seen in Fig. 5, facilitates a direct coupling of the incident pulse from the first delay line into the second one. It also functions as a pulse-clamping circuit. Fig. 6(a) shows a simplified circuit diagram used for the design of the decoupling circuit, which includes the decoupling circuit, a source for the incident pulse, a delay line, an output transmission line, and a load. The impulse is clamped to a certain dc level, as shown in Fig. 6(b), and then combined with the reflected impulse from the delay line to make a composite signal of monocycle waveform. Part of the reflected signal, represented by region A in Fig. 6(b), propagates to the input port of the decoupling circuit in the backward direction. In order to reduce the ringing on the composite monocycle pulse, region A should be reduced. However, excessive reduction of this region may sacrifice the pulse-amplitude. enhancement. Compromise between the ringing level and pulse amplitude is, therefore, needed in the design.

The design of the backward decoupling circuit can be performed based on the well-known pulse-clamping circuit theory [27]. Assuming the input pulse is rectangular with 200-ps pulse duration and 12.5-MHz PRF, it is straightforward to draw the clamped output pulse, as shown in Fig. 7. In Fig. 7, A_f and A_r represent the areas under the positive and negative voltages, respectively, and are related by the following relationship:

$$\frac{A_f}{A_r} = \frac{R_f}{R_5} \tag{12}$$

where R_f is the forward-diode resistance, which can be approximated by the series resistance of the Schottky diode, and R_5 is

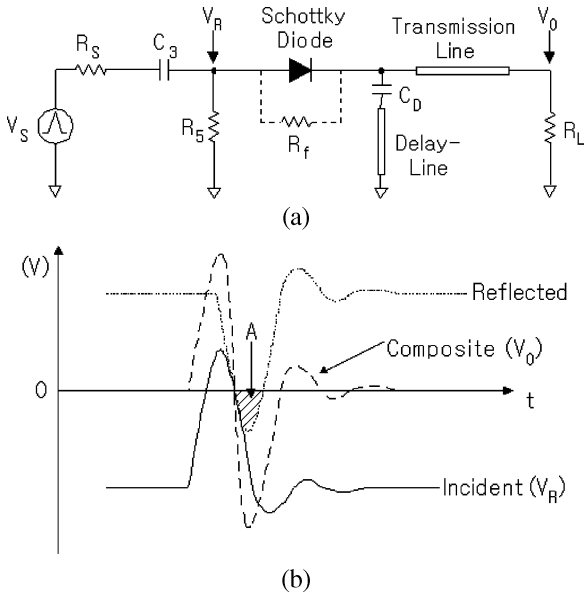


Fig. 6. (a) Circuit diagram used for the decoupling-circuit design. (b) Portions of the voltage waveforms involved in the composition of the monocycle.

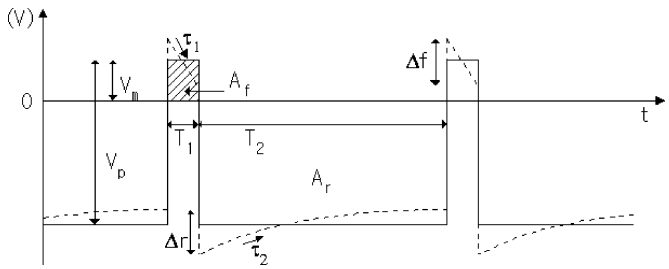


Fig. 7. Clamped impulse signal by the decoupling circuit with the circuit design parameters. The solid- and dashed-line waveforms represent ideal rectangular and actual distorted pulses, respectively.

the clamping resistance shown in Fig. 6(a). In our design, the pulse duration is relatively small compared to the period, resulting in a low duty cycle for the pulse generator. As implied in (12), for a low duty-cycle pulse signal, it is not practical to clamp the peak of the pulse to a small positive level close to zero. Therefore, assuming that $R_f = 10\ \Omega$ and the clamping level V_m is just a quarter of the pulse amplitude V_p, as shown in the ideal pulse waveform in Fig. 7, the required $R_5 = 10\ \mathrm{K}\Omega$ can be calculated using (12). The actual steady-state output pulse waveform of the clamping circuit has some distortion, as shown in Fig. 7. The distortion parameter Δf has the following relationship with Δr [27]:

$$\Delta f = \frac{R_f}{R_f + R_s} \frac{R_5 + R_s}{R_5} \Delta r \tag{13}$$

where R_s is the source resistance. In our case, $R_s \simeq 0$, resulting in $\Delta f \simeq \Delta r$. Therefore, as shown in Fig. 7, in order to increase Δf, $\tau_2 = R_5 C_3$ and, hence, C_3, should be decreased. Larger Δf produces a larger amplitude for the monocycle pulse, but also generates a higher ringing signal because of the increased portion of the backward coupling. As a compromise to achieving this contradictory objective, it is deemed reasonable to choose T_2, defined in Fig. 7, as $R_5 C_3$ or $R_5 C_3/2$ from which

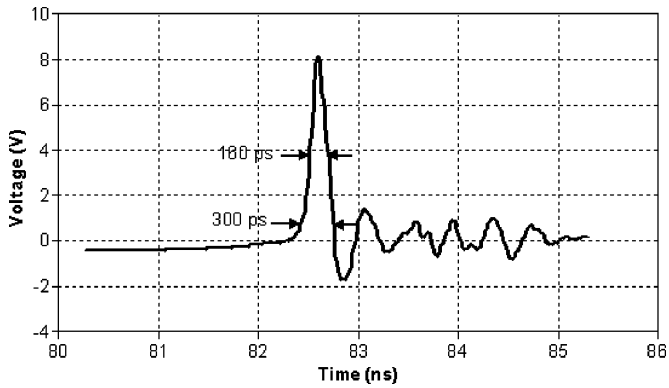


Fig. 8. Measured impulse output of the fabricated impulse generator.

TABLE I
DC-BIAS VOLTAGES (IN VOLTS) FOR THE DESIGNED IMPULSE GENERATOR AND TUNABLE MONOCYCLE PULSE TRANSMITTER

	Clock Osc. V_{DD}	Opamp		Buffer		PIN Diode
		V_{cc}^+	V_{cc}^-	V_{cc}^+	V_{cc}^-	
Impulse Generator	5	16	-5	18	-18	N/A
Monocycle Generator	5.2	14	-5	16	-18	5

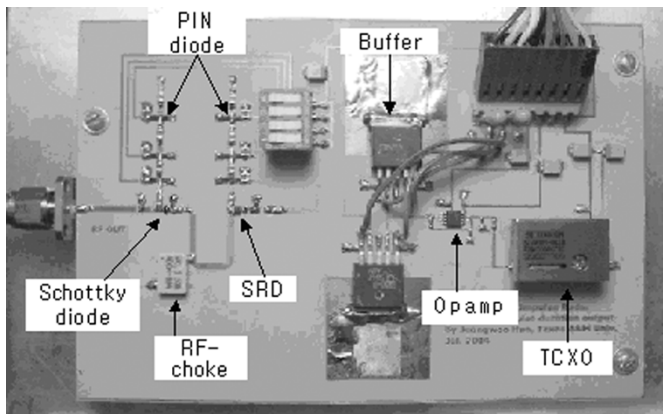


Fig. 9. Fabricated tunable monocycle pulse transmitter integrated with the clock driving circuit.

$C_3 = 8 \sim 16$ pF can be obtained as design values. To achieve a small-ringing signal, $C_3 = 15$ pF is finally used in our design.

IV. FABRICATION AND MEASUREMENT

The delay-line SRD impulse generator was designed based on the circuit diagram of Fig. 1, and fabricated first in order to verify the design concept. Note that this designed impulse generator can also be used for other applications such as time-domain reflectometry (TDR) as well. The circuit was fabricated using microstrip lines on an RT/Duriod 6010 substrate having a relative dielectric constant of 10.2 and a thickness of 0.127 cm. The clock oscillator used is the low-cost voltage-controlled crystal oscillator CSX-750VC manufactured by Citizen, Torrance, CA, which has 12-MHz PRF, 5-V CMOS logic output, and 5-ns rise and fall times. The opamp used in the clock driving circuit is THS3001 manufactured by Texas

TABLE II
SUMMARY OF THE DESIGN PARAMETERS FOR THE DISTRIBUTED DELAY LINES AND THE MEASURED PERFORMANCE OF THE TUNABLE MONOCYCLE PULSE TRANSMITTER

DIP S/W Setting	Delay-Line Length (mil)	Designed Round-Trip Time (ps)	Designed Pulse Width (ps)	Measured Pulse Width@10% (ps)	Operating Frequency Band (GHz)	Pulse Amplitude (V_{pp})
001	220	120	410	450	0.40-3.70	5.8
010	400	200	570	600	0.30-2.60	8.8
100	700	350	870	880	0.20-1.80	9.8
000	1000	500	1170	1170	0.15-1.30	9.4

Instruments Incorporated, Dallas, TX, which has 420-MHz unity-gain BW and 100-mA output driving capacity. The buffer is BUF634 manufactured by the Burr-Brown Company, Tucson, AZ, which has 180-MHz BW and ±250-mA output current capacity. In the SRD coupling circuit, $R_4 = 12\ \Omega$, which is the same as the design value, and $C_2 = 300$ pF, which is chosen as an the optimal value to achieve optimized power and overall waveform shape, through some experiments, rather than using the 200-pF initial design value. For the impulse shaping circuit, the SRD is SMMD-840 manufactured by the Metelics Company, Sunnyvale, CA, which has 70-ps minimum transition time, 10-ns MCLT, and 15 V of breakdown voltage. It should be noted that the actual transition time of an SRD depends on its storage time, which is determined by the rising and falling edge of the driving signal. The delay line is designed to have 100-ps roundtrip time. The output pulse from the fabricated circuit is measured by HP54750A digitizing oscilloscope with 12.4-GHz BW and the waveform is shown in Fig. 8. The measured impulse has 8-V peak amplitude, 160-ps full width at half maximum (FWHM), and 300-ps pulsewidth (defined at 10% of the peak amplitude). The bias voltages used for the designed impulse and tunable monocycle pulse generators are summarized in Table I.

The tunable monocycle pulse transmitter is also fabricated using a microstrip structure on the same substrate as that used for the impulse generator. Its photograph is shown in Fig. 9. The clock oscillator used in this circuit is the low-cost voltage-controlled–temperature-controlled crystal oscillator (VC–TCXO) GTXO-536V manufactured by Golledge Electronics, Somerset, U.K., which has 10-MHz PRF, 5-V HCMOS logic output, and frequency (or PRF) adjustment through the voltage control and a mechanical trimmer.

For the SRD coupling circuit, $C_2 = 1$ nF is chosen as an the optimal value through some experiments to obtain optimized results for the power and waveform, which is different rather than from 300 pF as used in the impulse generator. This change may be considered as a result of a slight difference in the circuit structure in the pulse shaping circuitry as compared with the impulse generator. The same SRD for the impulse generator is also used here. The switching p-i-n diodes used for this design are SMP1320-079 manufactured by Alpha Industries, Boston, MA. The dc block capacitors for decoupling of the p-i-n diode bias are a C08 series 20-GHz dc block manufactured by Dielectric Laboratories Inc., Cazenovia, NY. The Schottky diode used for the backward decoupling circuit is MSS50048-E25 manufactured by the Metelics Company. The required dc-bias voltage settings for the designed transmitter is shown in Table I.

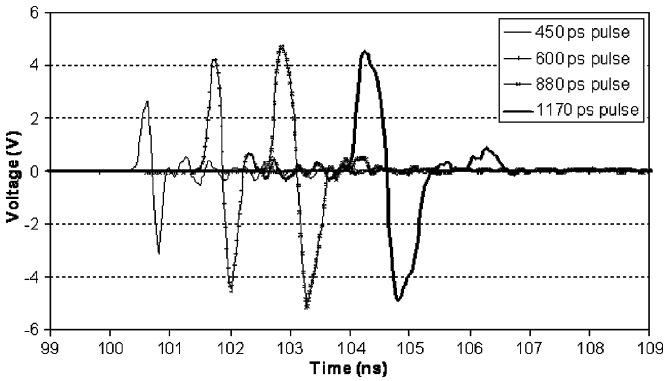
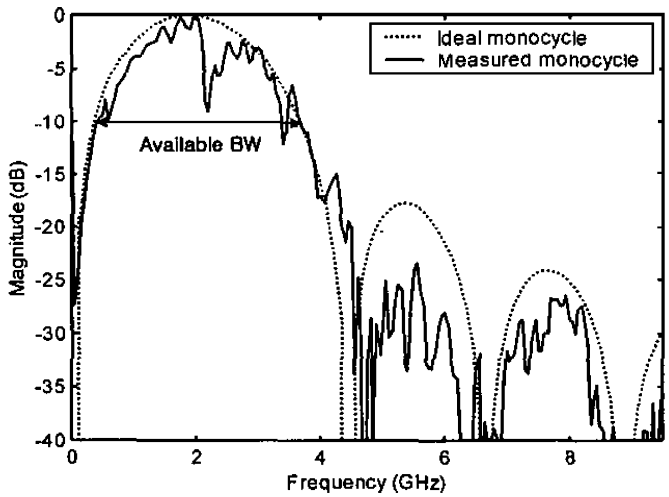


Fig. 10. Measured output monocycle pulses with four different pulse durations controlled by p-i-n diode switching.

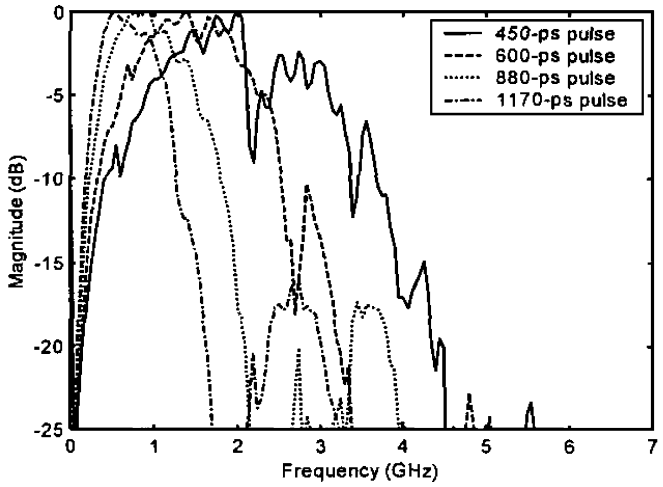
The designed tunable monocycle pulse transmitter employs two identical distributed delay lines, each divided into four sections to generate four different monocycle pulse durations. By turning on a branch of the DIP switches, the two corresponding p-i-n–diode pairs located on the two distributed delay lines are turned on simultaneously, generating an output monocycle pulse with a particular duration. The pulse duration, corresponding to the delay-line length, can be varied according to the selected turn-on position of the p-i-n–diode pairs. Table II shows the design parameters and results obtained for the tunable monocycle pulse generator. In the DIP switch setting, "1" represents connection of the corresponding branch of the switch and "0" represents disconnection. The designed pulsewidth T_p in Table II represents the desired pulsewidth of the output monocycle, which can be calculated approximately as $T_p = 2T_{rt} + t_r$, where T_{rt} is the designed roundtrip time and T_r is the rise time of the leading edge of the monocycle pulse, which is estimated as 170 ps through the impulse output waveform in Fig. 8.

Fig. 10 shows the measured output monocycle pulses with four different pulse durations. The characteristics of each generated pulse are summarized in Table II along with the designed values for comparison. The measured pulsewidth at 10% in Table II is the pulsewidth measured at an approximately 10% level of the peak amplitude. As can be seen, the measured pulses show practically good waveforms with acceptable ringing levels, and their measured and calculated pulsewidths agree reasonably well.

Spectrum analysis using a fast Fourier transform (FFT) has also been done for the generated measured monocycle pulse signals to find their frequency BWs. Fig. 11(a) compares the frequency-spectrum data between the ideal and measured 450-ps



(a)



(b)

Fig. 11. (a) Spectrums of the ideal monocycle with 450-ps duration and the measured monocycle with 450-ps duration. (b) Spectrums of all the monocycle pulses generated by the designed tunable pulse transmitter.

duration monocycle pulses. The ideal monocycle is represented as a perfect single cycle of sinusoid. In this figure, it is found that both of the main lobes and sidelobes of the ideal monocycle pulse are higher than those of the measured pulse. The reason is that the ideal pulse has abrupt transitions at the beginning and ending parts of the single-cycle duration. Nevertheless, the spectrum of the measured pulse follows that of the ideal monocycle pulse reasonably well for most engineering purposes. The available BW is defined in Fig. 11(a) as the instantaneous BW at the 10-dB level, which is known as a useful measurement to characterize the range resolution of the impulse radar [7], [8]. For instance, the 400-ps-duration monocycle pulse has approximately 4-GHz available BW, which corresponds to a range resolution of 1 in for typical pavements. Note that an UWB impulse GPR having more than 3-GHz available BW for the transmitting pulse signal is usually known as a high-resolution GPR, which can be used for high-resolution applications such as land-mine or UXO detection. Available BW data are also needed for the design of the system's components. Both the transmit and receive antennas and the receiver need to be designed to cover the entire available BW. Spectrum analysis results for all four of the generated monocycle pulses are shown in Fig. 11(b) and the measured operating frequency bands at the 10-dB level are specified in Table II. The operating frequency bands of these generated pulses are from 0.15 to 3.7 GHz. Measured pulse amplitudes are in the range of $6 \sim 9\ V_{pp}$ as seen in Fig. 10, which correspond to $200 \sim 400$ mW of pulse peak power. The smaller amplitude obtained for the 450-ps pulse is due to the fact that the designed roundtrip time of 120 ps along the delay line is smaller than the actual transition time of 170 ps, therefore, the incident step pulse could not reach the peak value before the arrival of the reflected one, resulting in reduction of the impulse amplitude. The only way to improve the amplitude for the 450-ps pulse is using a new SRD with faster transition time, acceptable MCLT, and breakdown voltage. Such a device, however, is not currently commercially available.

V. Conclusion

A new tunable monocycle pulse transmitter has been developed for low-power short-range UWB applications. It is made up of a clock driving circuit, an SRD coupling circuit, a backward decoupling circuit, and two distributed delay lines. The clock driving and SRD coupling circuits improve the output power and transition speed. Using opamp and buffer ICs for the clock driving circuit has greatly simplified the circuit design. In the SRD coupling circuit, a simple *RC* filter structure is used to achieve a near-optimal bias condition for the SRD without an external complicated bias control circuit. A new backward decoupling circuit was designed to reduce ringing in the output monocycle pulse. Tuning of the output monocycle pulse duration is achieved by alternately switching on and off the p-i-n–diode pairs spatially located along the delay lines. The employed tuning method is easy to implement and results in a compact circuit structure. The developed tunable transmitter achieves varying pulse duration from 0.4 to 1.2 ns, corresponding approximately to the operating frequency range of 0.15-3.7 GHz, and 200–400 mW of peak power. These results show that the designed monocycle pulse transmitter with advanced tuning capability can be used for most short-range UWB applications even for high-resolution radar applications such as UXO and land-mine detection. The impulse generator, developed along with the tunable monocycle pulse transmitter, exhibits a performance of 160-ps FWHM and 8-V peak amplitude, and can also be used for UWB systems, as well as for other applications such as TDR.

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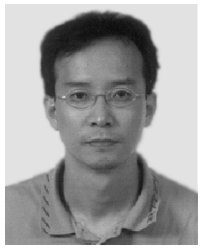

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