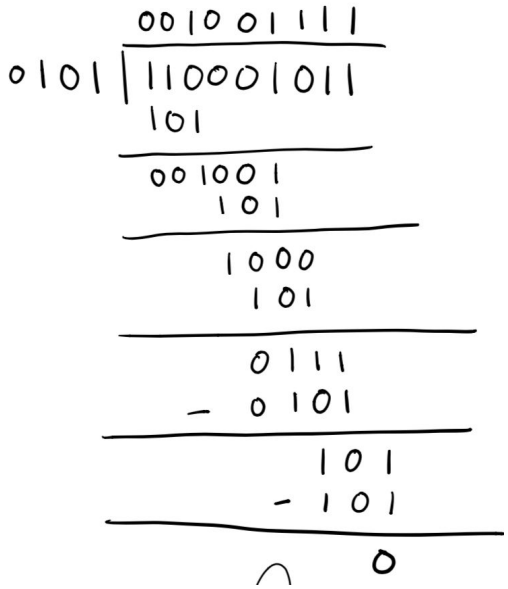
LAB 2 REPORT

Yang Liu and Shiyi Pang

- Description

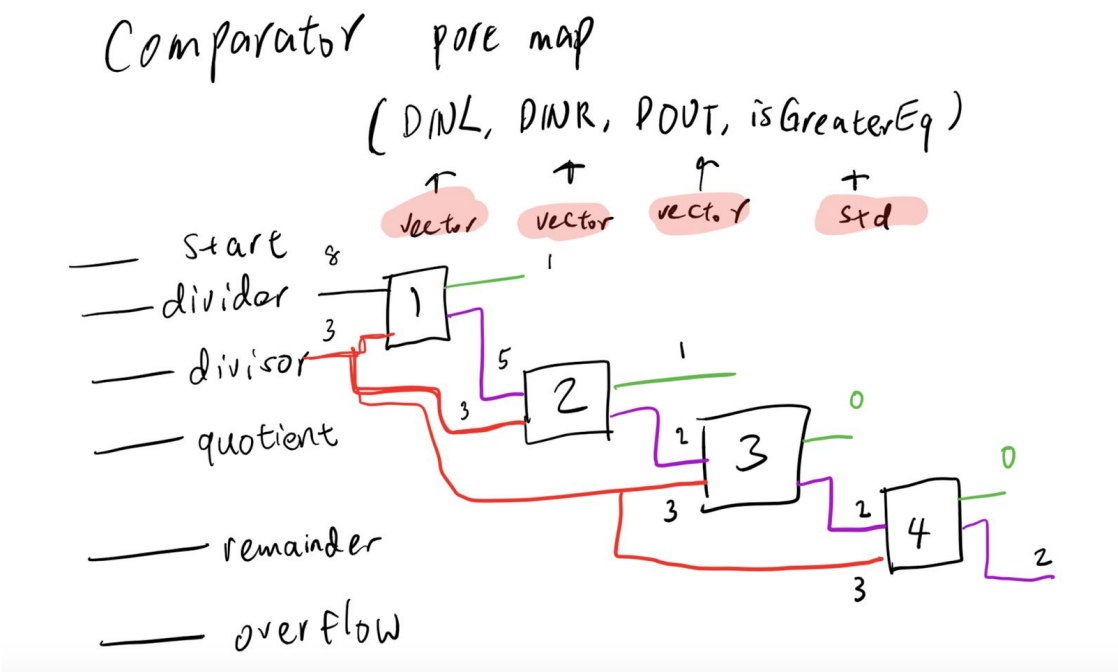
In lab 2, a combinational divider operating on unsigned numbers was designed and simulated. The divider was designed based on the long division theory.

- Long division calculation:
- Here is we perform the binary long division of 110001011 and 0101.



- Design

Here is what we go through the design when we trying to make it works using comparator units for making this divider using generate. In each of the loop turn, we using a 4 bits output from the previous compare (DINL-DINR or DINL) & 1 bit from the dividend to make the input of the comparator. The other input of comparator is divisor in each turn. Then each turn, it generates a isGreaterEq bit for the ouput of the divider which is quotient. The remainder of the divider which is the output (DINL-DINR or DINL) of the comparator in the last ever turn in this loop. The start is the activate signal of this divider and the overflow signal for detecting whether the divisior is 0 or not.



- Test and Simulation

In this case, we create a testbench file for the simulation and make sure the logic of divider is correct. We test three sets of data 32-bits 16-bits and 8-bits input. Here is the output files of the testbench and its simulation waves shown below.

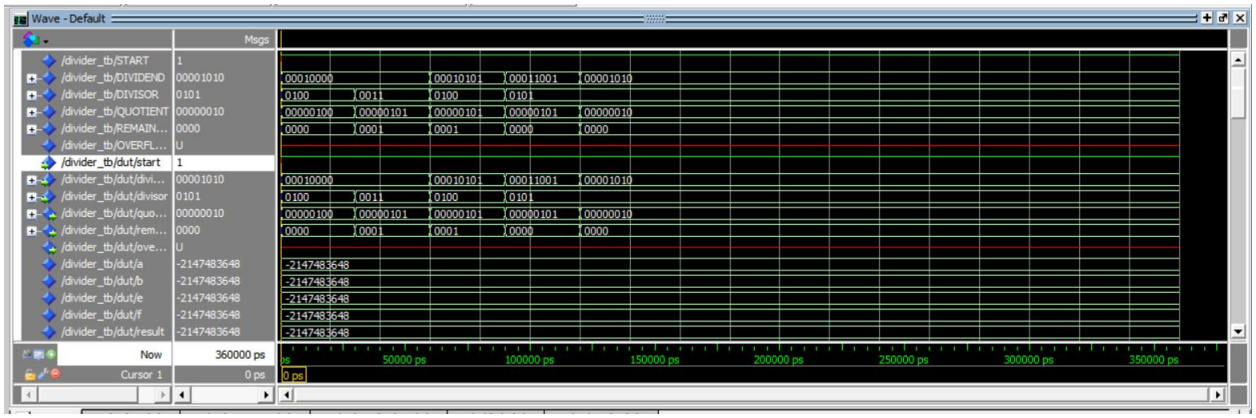


Figure 1 Simulation result (dividend 8 bits)

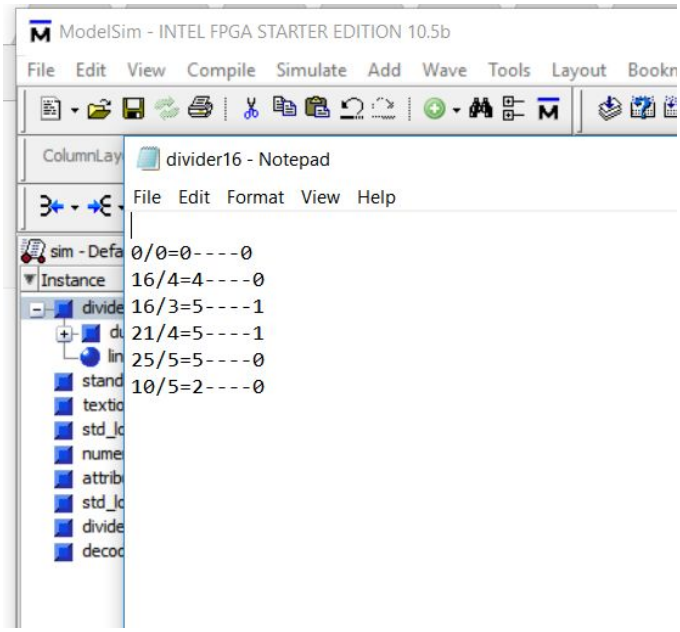


Figure 2 Output file (dividend 8 bits)

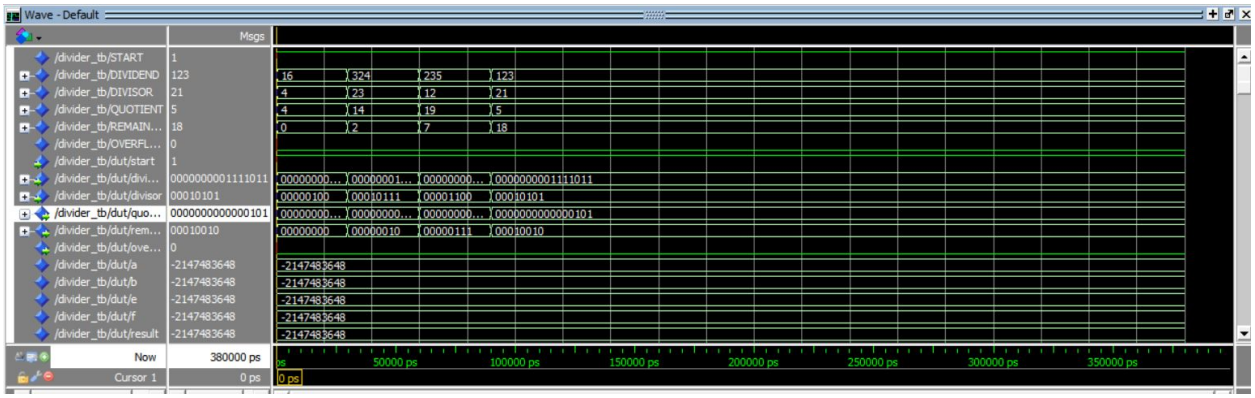


Figure 3 Simulation result (dividend 16 bits)

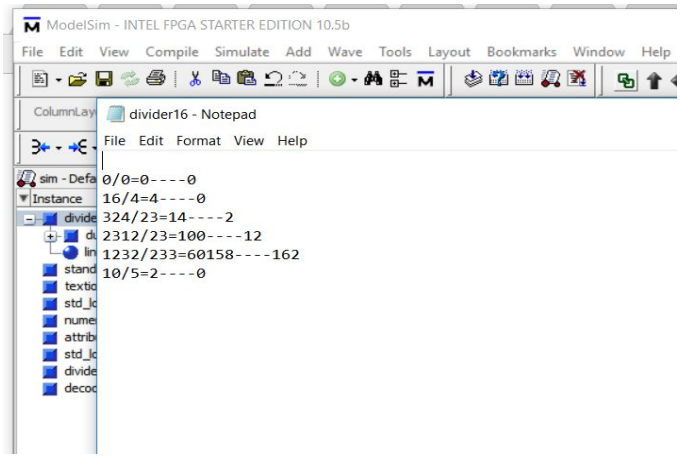


Figure 4 Output file (dividend 16 bits)

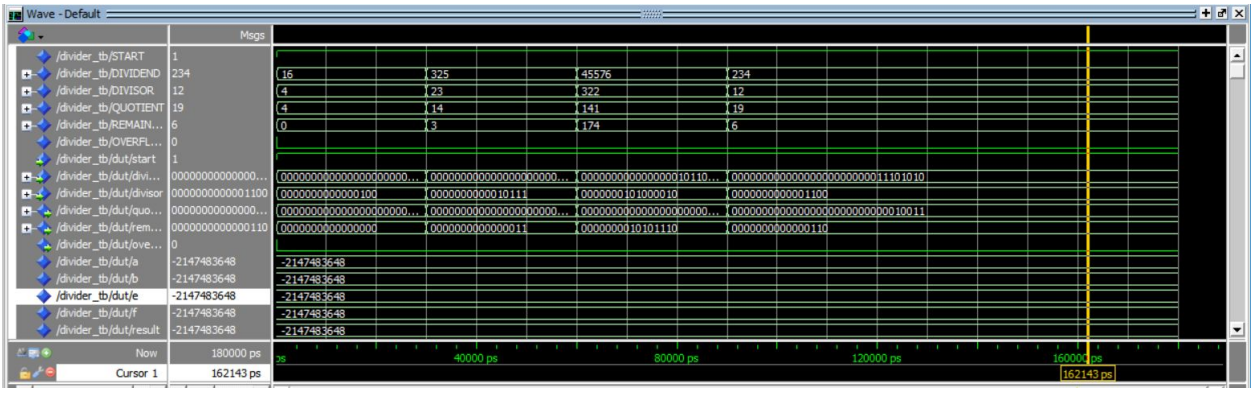


Figure 5 Simulation result (dividend 32 bits)

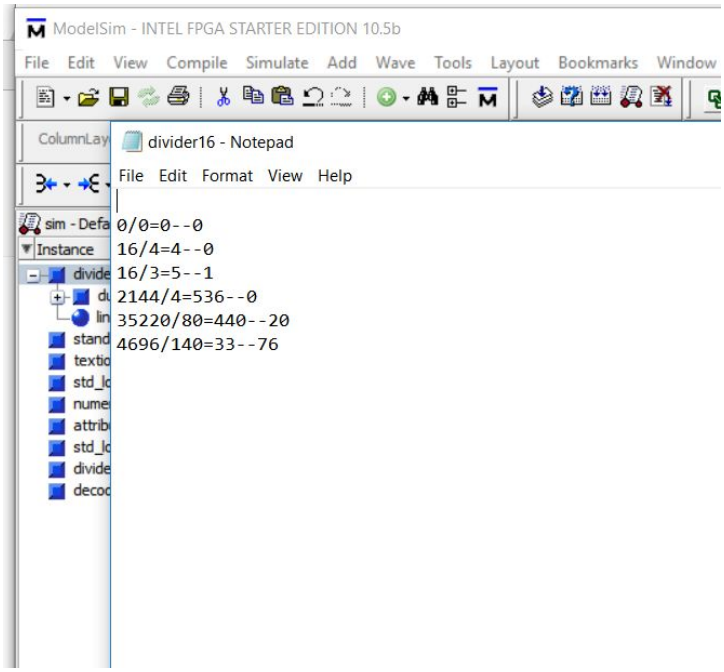


Figure 6 Output file (dividend 32bits)

For the top-level design, we implement a display_divider entity as we learned from the previous lab which has the divider component and led decoder. We use 1 bit input for the start signal, 1 led for showing whether the divisor is 0 which is overflow, 1 led for divisor and two led for the dividend, 1 led for quotient and 1 led for remainder.