SAI SRINIVASAN

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Experienced professional pursuing graduate studies in Electrical and Computer Engineering, seeking internship opportunities in **Hardware Engineering ASIC/RTL Design & Verification**.

WORK EXPERIENCE

Verizon, Chennai, India ***July 2016 – June 2018***

Software Engineer

- Development of backend microservices application for MyVerizon®
  Worked on migration of a monolith application, to multiple scalable and light-weight Microservices.
  Key Achievements: Increase site availability to 99% for 1.2 million customers, Net Adds:4600 New Lines.
  Tools: Java, RESTful API's/ Microservices, JSON, Tomcat Server, Oracle DB(SQL).
- Debugging, Unit-Testing, Application Security of some critical projects.
  Tools: HP ALM, HP Fortify, Junit.

SKILLS

Software: ModelSim, HP ALM, HP Fortify, Oracle DB.
Languages: Verilog, SystemVerilog(ongoing), C++, Java, Python, VHDL.
Tools: Synopsys DesignVision, G-Suite**,** Version Control-Git (BitBucket), Build & Deploy-Jenkins, Ticketing-JIRA, Collaboration- Confluence.
OS: Windows, Linux.
Hardware: Atmega Chips, Arduino Uno, Linux Based Raspberry Pi, ARM based boards.

EDUCATION

North Carolina State University, Raleigh, NC ***Expected May 2020***
M.S in Electrical Engineering

- *Courses:*

Computer Architecture (micro-architecture concepts), ASIC and FPGA Design with Verilog (Understanding of FPGA and RTL Design), Digital Imaging Systems.
Spring 19: ASIC Verification with System Verilog (ongoing).

SRM Institute of Science and Technology, Chennai, India ***Aug 2012 – May 2016***
B.Tech. Electronics and Communication Engineering

- *Relevant Courses:* Digital Electronics, VLSI Design, Micro-controller and Micro-processors.

ACADEMIC PROJECTS

Out of Order Super Scalar Pipeline Simulator ***Nov 2018 – Dec 2018***

•Simulated the dynamic scheduling mechanism for an out-of-order superscalar processor that fetches multiple instructions per cycle.
•The effect of Micro architectural parameters such as pipeline width, size of issue queue and re-order buffer on the IPC of the superscalar processor were explored.

Cache Simulator ***Sep 2018 – Oct 2018***

•Design of multi-level cache simulator with L1, L2 caches and augmented L1 cache with a Victim Cache.
• Studied trends such as miss rate, average access time, performance and area for various cache configurations on the SPEC2000 Benchmark.

RTL Simulation and Synthesis of SHA-256 Encryption in Verilog ***Oct 2018 – Nov 2018***

• Designed the SHA-256 cryptographic hash function in Verilog HDL, wherein 256-bit hash of a message stored in SRAM was computed in Separate Modules. Modular approach was chosen to optimize for either the performance or area depending on the user.
• The design was simulated using ModelSim which reported 160 clock cycles for hash computation of a message with maximum message length of 55 characters. Synthesis of the design using Synopsys Design Compiler reported an area of 32000 um2 at the fastest clock of 24 ns.
• *Simulation:* ***ModelSim****. Synthesis:* ***Synopsys DesignVision****. Other Tools:* ***Python, Linux, Tcl****.*

Branch Prediction Simulator ***Nov 2018 – Nov 2018***

• Constructed a branch predictor module in Java to simulate GShare, Bimodal and a hybrid branch predictor, with configurable parameters.
• Explored trends in misprediction rate with GCC, JPEG, PERL benchmarks for the above configurations

ACHIEVEMENTS:

- Awarded "Central Sector Scheme of Scholarship for College and University students" by MHRD Govt. of India
- Awarded 1st place at Regional level of Image processing contest ROBO-TRYST by IIT Delhi.
- Awarded 10th place for National Level Mathematics Olympiad in class X.