

Multi-Mode 60-GHz Radar Transmitter SoC in 45-nm SOI CMOS

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Abstract—This article introduces an architecture for a millimeter-wave multi-mode radar transmitter IC, which supports three key radar waveforms: 1) continuous-wave (CW/FMCW); 2) pulse; and 3) phase-modulated continuous-wave (PMCW), all from a single front end. The proposed IC, implemented in a 45-nm CMOS silicon-on-insulator (SOI) process for operation in the 60-GHz band, integrates a broadband frequency tripler, a two-stage pre-amplifier, two power mixers, and mixed-signal baseband waveform generation circuitry. The transmitter radar operation in multiple modes is enabled by configuring the power mixers and the associated waveform baseband circuitry. An important advantage of this approach is that the overall signal bandwidth, a key performance metric in radar, is limited only by the RF output nodes in pulse generation. A novel broadband frequency tripler design technique based on a current-reuse topology is also proposed for LO generation with >59% output fractional bandwidth. On-wafer measurement results for the full TX IC in CW mode show an average output power of 12.8 dBm from 54 to 67 GHz with a peak power of 14.7 dBm and the harmonic rejection ratio >27 dB. The measurement in pulse mode demonstrates programmable pulselwidth from 20 to 140 ps, which translates to >40-GHz radar signal bandwidth. The PMCW mode operation is also demonstrated in this case with 10-Gb/s PRBS modulated radar signal. The IC consumes 0.51 W and occupies 2.3 × 0.85 mm² of die area excluding pads.

Index Terms—CMOS, FMCW radar, frequency tripler, gesture recognition, medical imaging, millimeter-wave radar, phase-modulated continuous-wave (PMCW) radar, pulse radar, sensing, transmitter, ultra-short pulse.

I. INTRODUCTION

SINCE the introduction of Si-based mmWave ICs, more than a decade ago [1], [2], radar has been considered as one of the main applications for this technology, in particular, for the automotive electronics market [3], [4]. In comparison to discrete component-based solutions, key advantages of Si-based integrated radars include: 1) low cost in large

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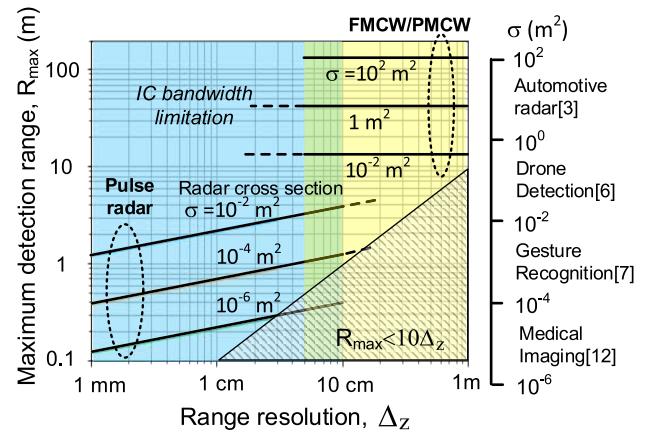


Fig. 1. Radar waveform selection for different applications based on trade-off between range resolution and detection range for given TX peak output power, RX noise figure, integration time, and SNR_{RX}.

volumes; 2) the opportunity to integrate mmWave and digital functions on the same IC to form a radar SoC; and 3) small form factor in comparison to the wavelength of operation, which in turn enables the support of multiple antennas from a single IC [5]. These advantages have motivated research on key circuit building blocks, systems, and applications beyond automotive navigation, including drone detection [6], gesture recognition [7], [8], industrial inspection [9], vital signal monitoring [10], and medical imaging [11], [12].

Adaptability and multi-functionality are strong general trends for electronic systems. In the case of radar systems, a critical element that drives key performance trade-offs, including detection range versus range resolution, is the transmitted waveform. Fig. 1 presents the maximum detection range that could be achieved with a given waveform for various target radar cross sections (RCSs) and waveforms. This plot, which is described in greater detail in Section II, also presents example applications over a range of RCS values in this trade-off space. A single-chip multi-mode radar solution, which supports different radar waveforms, is desirable not only to address multiple applications with the same hardware and antenna aperture but also to enable real-time adaptability, as shown in Fig. 2(a); the increased flexibility offered by such a design allows exploration of a very broad optimization space. In general, on-chip configurability is a strong inherent advantage of Si-integrated radars, which has not been fully explored. Such opportunity arises from the ability to co-integrate high-performance digital, mixed-signal, and mmWave circuits on the same die.

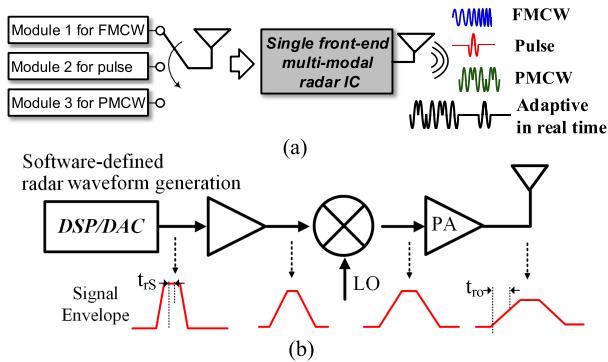


Fig. 2. (a) Concept of single front-end multi-modal radar and (b) DSP-driven multi-modal radar and radar signal bandwidth limitation through the transmitter chain.

Prior work on radar systems with configurable waveforms has typically involved fixed transmit and receive signal chains and waveform definition in software [13], [14]. Even though this approach leads to the maximum flexibility in terms of waveform generation, one of its key drawbacks is that the bandwidth of the transmitted signal will be limited by the digital-to-analog converter (DAC) and the system bandwidth of the cascaded blocks. The decrease in bandwidth through a signal chain is shown as rise/fall time degradation of the signal envelope, as illustrated in Fig. 2(b). Assuming that each stage has a Gaussian frequency response, the output rise/fall time t_{ro} is given by [15]

$$t_{ro} = \sqrt{t_{rS}^2 + t_{r1}^2 + t_{r2}^2 + \dots + t_{rN}^2} \quad (1)$$

where t_{rS} is the rise(fall) time at the DAC output, and t_{rk} is the rise(fall) time at the output of the k th stage for $k = 1 \dots N$. This limitation is critical since the range resolution, a key performance metric, is inversely proportional to the transmitted signal bandwidth.

This article introduces a novel architecture for a V-band multi-mode radar transmitter capable of supporting: 1) continuous wave (CW/FMCW); 2) pulse; and 3) phase-modulated continuous-wave (PMCW) radar waveforms while accommodating a very wide radar signal bandwidth. This article is an expansion of a prior conference publication [16]. Beyond the general description of the implemented IC reported in the conference article, this article provides: 1) a discussion of radar waveform selection to optimize performance; 2) circuit implementation details of the design's broadband frequency tripler and front-end circuitry; 3) design and simulation of the waveform generation circuitry; and 4) comprehensive measurement results of the design operating in pulse mode. This article is organized as follows. Section II discusses radar system consideration for radar waveform selection. Section III describes the proposed transmitter architecture and radar waveform generation principles. Details of the 45-nm silicon-on-insulator (SOI) CMOS IC implementation of the design are described in Section IV, with a focus on key building blocks such as the broadband frequency tripler, the power mixer, and the baseband waveform generator. Section V shows on-wafer measurement results, and Section VI provides a summary and conclusion.

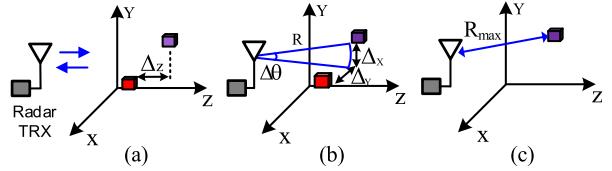


Fig. 3. Radar performance metrics. (a) Range resolution. (b) Lateral resolution. and (c) Maximum detection range.

II. RADAR SYSTEM CONSIDERATION FOR RADAR WAVEFORM SELECTION

In general, radar performance metrics include range resolution, lateral resolution, and maximum detection range, as illustrated in Fig. 3. The range resolution Δ_z improves with radar signal bandwidth B , given by $\Delta_z = c/2B$, and the lateral resolution $\Delta_{X,Y} = R\lambda/D$ improves with a smaller wavelength λ for a given antenna aperture D and distance R , which clearly indicates the benefit of using mmWave frequencies for radar. The maximum detection range R_{max} is determined by the minimum receiver signal-to-noise ratio SNR_{RX} for given requirement of probability of detection and probability of false alarm [17], given by

$$R_{max} = \left[\frac{P_{AV} T_{int} G_{ANT}^2 \lambda^2 \sigma}{(4\pi)^3 SNR_{RX}(kTF)} \right]^{1/4} \quad (2)$$

where P_{AV} is the average transmitter output power given by $\alpha \cdot P_{TX}$, P_{TX} is the transmitter peak power, α is a duty ratio, T_{int} is the integration time, G_{ANT} is the antenna gain, σ is the radar target cross section, k is Boltzmann's constant, T is temperature, and F is the receiver noise factor. α is given by $\tau \cdot PRF$ for pulse, where τ is the pulsedwidth and PRF is the pulse repetition frequency. α is unity for CW radar signals. It is noted that lateral resolution $\Delta_{X,Y}$ and maximum detection range R_{max} can be further improved by using multiple radar transceivers in a phased array architecture, which provides a narrower beamwidth and improved SNR [18].

Fig. 1 shows the calculated R_{max} with respect to Δ_z for different radar waveforms and RCSs σ , here computed using (2) with values of $PRF = 10$ MHz, $f_c = 60$ GHz, $P_{TX} = 13$ dBm, $G_{ANT} = 5$ dB, $T_{int} = 1$ mS, $SNR_{RX} = 15$ dB, and $NF = 8$ dB. In this calculation, RCS σ ranges from 10^{-6} to 10^2 m 2 , which corresponds to targets in different radar applications from medical imaging to automotive radar [3], [6], [7], [12]. It is noted that applications with smaller σ generally require higher range resolution (smaller Δ_z) within a shorter detection range. Pulse waveforms, which provide a high range resolution within a short detection range, show a trade-off between R_{max} and Δ_z : a smaller τ , which is translated into a larger B for higher range resolution, reduces P_{AV} for a given PRF , thereby decreasing R_{max} . On the contrary, modulated CW radar waveforms, such as FMCW and PMCW, which are suitable for applications with moderate resolution and longer detection range requirements than pulse radar, ideally present constant R_{max} over Δ_z as the receiver noise bandwidth is given by $1/T_{int}$ and P_{AV} does not change with Δ_z . However, it is challenging to improve Δ_z to values below a few centimeters

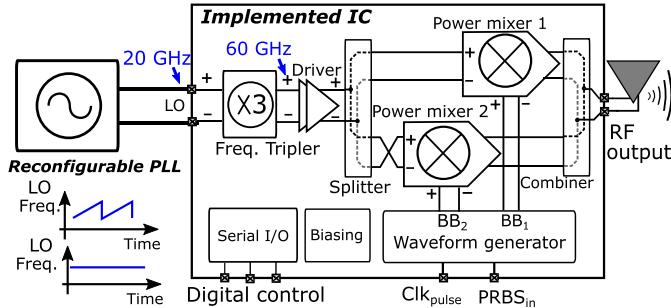


Fig. 4. Proposed 60-GHz multi-mode transmitter architecture.

(e.g., $B > 10$ GHz) due to the difficulties in achieving a wide bandwidth performance in: 1) frequency-chirping LO generation for FMCW radar and 2) analog baseband, data converters, and digital front end for PMCW radar. Hence, it is desirable to choose different waveforms and radar parameters (which offer different trade-offs between R_{\max} and Δ_z) for different usage scenarios and applications. Section III will introduce a single-chip multi-mode radar transmitter that enables such radar waveform reconfigurability with a wide bandwidth.

III. MULTI-MODE TRANSMITTER ARCHITECTURE

A new transmitter architecture is proposed to support different radar waveforms of types CW/FMCW, pulse, and PMCW with a wide signal bandwidth from a single-mmWave front end, as shown in Fig. 4. The proposed IC consists of a broadband frequency tripler, the transmitter front-end circuitry, and the baseband waveform generator. The design includes programmable biasing and serial I/O circuitry for digital control; the latter supports 52 control bits. Blocks in the high-frequency signal path are implemented differentially to suppress even-order harmonics and to enable drive of a broadband differential antenna at the output. A potential antenna topology that could be used with the proposed design is described in [19].

The design is intended to operate with an LO input signal of frequency 17–22 GHz, a signal that can be sinusoidal or frequency-modulated. This signal is first applied to a broadband frequency tripler to generate an internal 51–66-GHz LO signal. A programmable 20-GHz frequency synthesizer with frequency chirp capability and wide tuning range [20] can be potentially integrated with the proposed transmitter IC for the generation of the LO input signal. Such a 60-GHz generation scheme using a 20-GHz frequency synthesizer followed by a frequency tripler provides better phase noise and wider frequency tuning range than the direct 60-GHz frequency synthesis [22]. The output of the frequency tripler is applied to a two-stage broadband pre-amplifier to drive the two power mixers. The two power mixers are directly modulated with different baseband signals generated by the waveform generator to support different radar waveforms—CW/FMCW, pulse, and PMCW—as shown in Fig. 5. For CW mode, the waveform generator provides an appropriate level of dc to the two power mixers to operate them as a two-way current-combined power amplifier. It is noted that the polarity

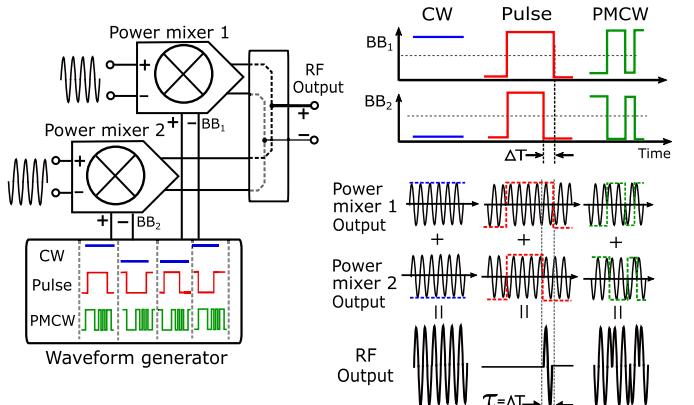


Fig. 5. Multiple radar waveform generation concept by modulating the two power mixers with different baseband signals from the waveform generator.

of the differential baseband input is contrary between the two power mixers to yield constructive combining as the LO input polarity is swapped for the second power mixer.

For pulse mode, two clock signals with aligned rising edges but time-shifted falling edges (by ΔT) are applied to the power mixers. The output currents from the two power mixers are combined constructively only when they are in opposite phase to generate pulses with a pulselength of $\tau = \Delta T$, as shown in Fig. 5. The achievable minimum pulselength is only limited by the bandwidth of the RF output node as the pulse is shaped after the currents are combined at the passive combiner. In general, turning on and off a system with a memory in a short period of time (e.g., 25 ps) is challenging for pulse generation. In [7] and [11], a hybrid switching technique was proposed where the ON and OFF transitions, which correspond to the rising and falling edges of pulses, occur at the final-stage PA and antenna to achieve a pulselength of 25 ps in a SiGe process. On the contrary, this article proposes a cancellation-based programmable pulse generation method using two power mixers combined in parallel to generate a comparable pulselength in a CMOS process. In PMCW mode, complementary radar code waveforms are applied to the power mixers to operate them as a high-speed BPSK modulator, where the modulated output currents from the two power mixers are combined constructively at the output. Since signal modulation in PMCW mode occurs only at the final stage, the proposed architecture can support a high data-rate radar code (>10 Gb/s) without being limited by the system bandwidth of the signal chain.

Table I shows the comparison of the proposed front-end architecture to a DSP-driven RF transmitter architecture, as described in Fig. 2(b), and mmWave RF-DACs [23]–[25]. In general, an M -bit RF-DAC generates 2^M output levels to enable high output power and high efficiency with large peak-to-average ratio for high-order quadrature amplitude modulation (QAM) modulation. RF-DACs, are therefore, attractive for the generation of communication waveforms [26]. Although the operation of the architecture proposed in this article in the PMCW mode is similar to a 1-bit RF-DAC, the operation principle in the pulse mode is different from RF-DACs, in which the minimum pulselength is limited by the maximum

TABLE I
COMPARISON OF DIFFERENT ARCHITECTURE APPROACHES
FOR MULTIPLE RADAR WAVEFORM GENERATION

	DSP-driven RF transmitter	M-bit I/Q RF-DAC	Proposed Architecture
# of supported amplitude levels	Arbitrary*	2^M	2
Supported code modulation	Arbitrary*	High-order QAM	BPSK
Minimum pulse width limit for pulse generation	Maximum sampling rate @ baseband + Cascaded bandwidth in signal chain	Maximum sampling rate @ RF-DAC + Final stage bandwidth	Output network bandwidth at the final stage

*limited by baseband DAC resolution.

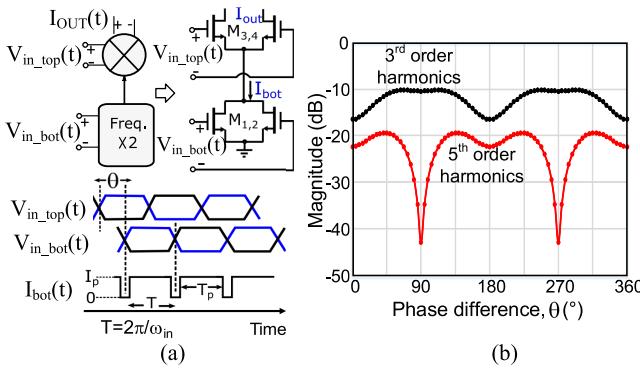


Fig. 6. (a) Current-reuse frequency tripler and (b) calculated conversion gain at $3\omega_{in}$ and $5\omega_{in}$ with respect to the phase difference between top and bottom driving signals θ .

sampling rate. The minimum pulselength achievable in the proposed architecture is only limited by the bandwidth of the output matching network, which will be further discussed in Section IV.

IV. IC IMPLEMENTATION

The proposed multi-mode transmitter IC is implemented in a 45-nm CMOS SOI process, and this section discusses the implementation details of key building blocks including frequency tripler, front-end circuitry, and baseband waveform generation circuitry.

A. Broadband Frequency Tripler

A broadband frequency tripler is designed based on a current-reuse topology [21] to upconvert LO input around 20 GHz to frequency-tripled output around 60 GHz while achieving high conversion gain and harmonic suppression over a broad frequency range. Rather than generating the third-order harmonic 3ω directly from a differential pair, the second-order harmonic 2ω is generated first from the bottom differential pair $M_{1,2}$ through a push-push operation and then is upconverted into 3ω through the commutating top differential pair $M_{3,4}$, as shown in Fig. 6(a). Assuming: 1) an ideal square-wave switching of $M_{3,4}$ and 2) a rectangular waveform of the combined drain current of $M_{1,2}$, $I_{bot}(t)$, with a duty ratio of $\alpha = T_p/T$ and the peak amplitude of I_p , the output current

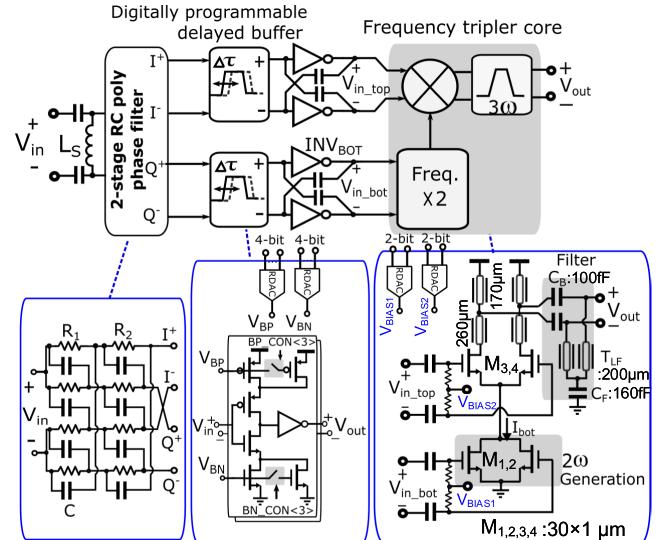


Fig. 7. Block diagram and schematic of the proposed broadband frequency tripler.

$I_{OUT}(t)$ for an input frequency of ω_{in} is written as

$$I_{OUT}(t) = \frac{4}{\pi} \sum_{n=0} I_n \cos(2n(\omega_{in}t + \theta)) \times \sum_{m=1} \frac{\sin((2m-1)\omega_{in}t)}{2m-1} \quad (3)$$

where $I_0 = \alpha I_p$, $I_n = I_p/(n\pi) \sin(2n\pi\alpha)$ for $n > 1$, and θ is the phase difference between driving voltages of $M_{1,2}$ and $M_{3,4}$, as shown in Fig. 6(a). Equation (3) indicates that the k th harmonic frequency component of the output current results from the combination of different mixing processes, which meets $k = |2m \pm 2n - 1|$ as a function of θ . To find out the optimum θ for the maximum conversion gain, Fig. 6(b) shows the calculated $3\omega_{in}$ and $5\omega_{in}$ components of the output current across θ for $m, n \leq 3$ and $\alpha = 0.65$ using (3). $\theta = 90^\circ$, where the dips of $I_{bot}(t)$ at $2\omega_{in}$ are aligned to the peaks of $V_{in_top}(t)$, provides the maximum conversion gain at $3\omega_{in}$ and the minimum conversion gain at $5\omega_{in}$, which is the dominant unwanted harmonic for low input frequencies. Although the conversion at 3ω has a good tolerance for phase deviation from 90° , harmonic suppression at 5ω is sensitive to θ around 90° . This requires accurate I/Q generation as 5ω harmonic component for an input frequency < 14 GHz stays within the bandwidth of the output matching network.

The block diagram and schematic of the proposed frequency tripler are shown in Fig. 7; key challenges for the design are to: 1) achieve the optimum phase difference of 90° over a wide bandwidth and 2) suppress unwanted harmonics at the output through a filtering network. The input LO signal is first applied to a two-stage staggered-tuning polyphase filter to generate in-phase and quadrature signals over a broad input frequency range [27]. $R_1 = 78 \Omega$, $C_1 = 82 fF$, $R_2 = 137 \Omega$, and $C_2 = 94 fF$ are chosen to achieve an I/Q phase difference within $90 \pm 4^\circ$ from 12 to 35 GHz in simulation. The shunt inductor L_s is added at the input to resonate out parasitic capacitance, and Fig. 8 shows the simulated input return loss.

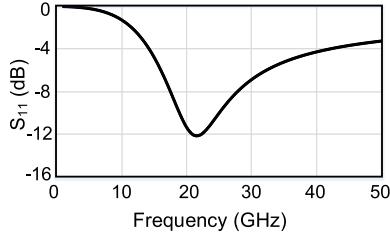


Fig. 8. Simulated input return loss of the proposed frequency tripler.

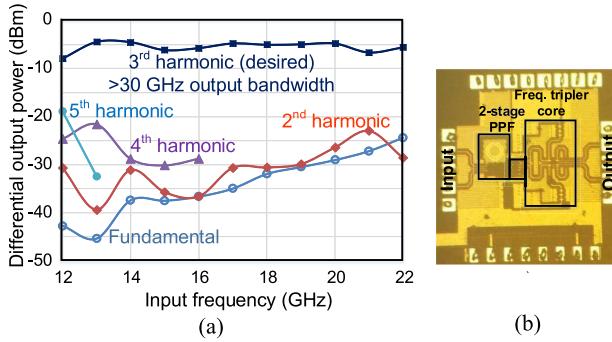


Fig. 9. (a) Measured differential output power at different harmonic components with respect to input frequency and (b) frequency tripler breakout.

The output of the polyphase filter is applied to programmable current-starved inverters to enable fine phase tuning between the I and Q paths to maintain the desired 90° relationship over frequency in the presence of process, voltage, and temperature (PVT) variations. The ON-resistance of the top PMOS and bottom NMOS is independently controlled with 4-bit digital controls, and the simulated delay tuning range is ± 3 ps with ~ 0.4 -ps resolution, which is translated into $\pm 14.4^\circ$ with 2° resolution at 20 GHz. The output signals from the programmable current-starved inverters are applied to inverters with neutralization capacitors to drive $M_{1,2}$ and $M_{3,4}$ in the frequency tripler core. The bias voltages V_{BIAS1} and V_{BIAS2} are digitally programmable through two-bit RDACs for the maximum conversion gain. At the output, C_B , TL_F , and C_F form a harmonic rejection filter to suppress ω_{in} and $4\omega_{in}$. TL_F and C_B form a high-pass filter to suppress ω_{in} as C_F is not present due to the central virtual ground for the differential signal. TL_F and C_F form a notch filter with series resonance to suppress $4\omega_{in}$ as $4\omega_{in}$ component is in common mode for differential outputs. The frequency tripler is based on a fully differential structure with a good layout symmetry to minimize deterministic phase imbalance between the differential output ports. The simulated standard deviation of phase imbalance due to random device mismatch is 0.07° at 60 GHz based on 50 samples in Monte Carlo simulation.

Fig. 9(a) shows the measured differential output power with respect to frequency at different harmonic frequencies using the frequency tripler breakout circuitry shown in Fig. 9(b). A broad output signal bandwidth greater than 30 GHz at $3\omega_{in}$ was measured with a peak output power of -4.4 dBm, and the measured harmonic rejection ratio up to $5\omega_{in}$ is better than 20 dB at input frequencies from 14 to 20 GHz, which

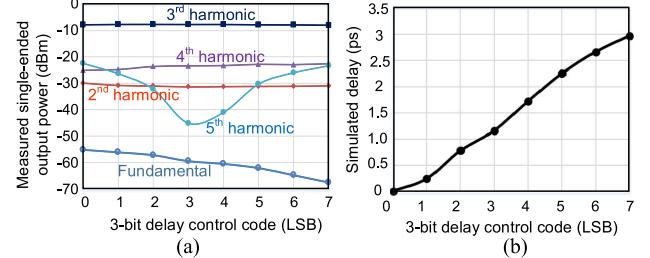
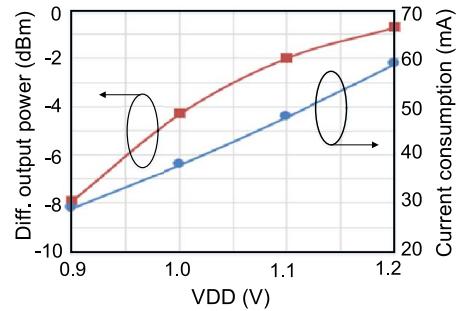
Fig. 10. (a) Measured single-ended output power across 3-bit LSB delay tuning control for $f_{in} = 13$ GHz. (b) Simulated relative delay between I/Q signal paths across 3-bit LSB delay tuning control.Fig. 11. Measured differential output power at $3f_{in}$ and power consumption across VDD for $f_{in} = 20$ GHz.

TABLE II
MEASUREMENT RESULT SUMMARY OF FREQUENCY TRIPLEXER
BREAKOUT AND COMPARISON TO PRIOR WORKS

	This work	[28]	[29]
Output frequency with 3-dB BW (GHz) (fractional BW)	36 ~ 66* (59 %)	51.3~70.2 (31 %)	57~78 (31 %)
Peak conversion gain(dB)	0 @ 60 GHz	-5.2 @ 60 GHz	1.3 @ 63 GHz
Saturated output Power(dBm)	-4.6 @ 60 GHz	1.8 @ 60 GHz	-2**
Power consumption (mW)	38	44.3	60
Harmonic suppression up to 2nd order harmonic (dBc)	>17 for 36-66G >21.6 for 36-60G	>29.2	>20
Process	45-nm SOI CMOS	90-nm CMOS	65-nm CMOS

*The measurement of the maximum output frequency is limited by the spectrum analyzer.

** Measured frequency is not reported.

will be further improved throughout the following front-end circuitry. The measured power consumption of the frequency tripler ranges from 33 to 39 mW from a 1-V power supply for input frequencies from 12 to 22 GHz. Fig. 10(a) shows the measured single-ended output power across a three-bit (LSB) fine delay tuning control for different harmonic components for an input frequency of 13 GHz. As expected from Fig. 6(b), the selection of the fine delay tuning code is critical to achieve the best harmonic rejection at $5\omega_{in}$ in the measurement: the maximum harmonic rejection, which is greater than 37 dB, is measured at the optimum fine delay code while other harmonics, including $3\omega_{in}$, are affected negligibly. The power consumption and output power at $3\omega_{in}$ also measured across different power supply voltages, as shown in Fig. 11.

Table II summarizes the measured performance compared to prior wideband frequency triplers in the V-band. The proposed

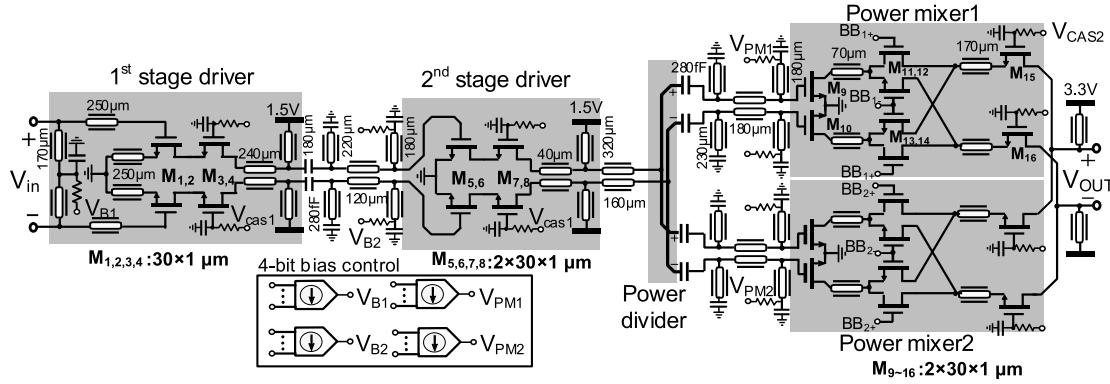


Fig. 12. Schematic of the 60-GHz differential transmitter front end consisting of two-stage pre-amplifier and two power mixers.

frequency tripler presents a much wider output bandwidth (fractional bandwidth $>59\%$) with comparable conversion gain and power dissipation versus prior works.

B. RF Transmitter Front-End

Fig. 12 shows the block diagram and schematic of the 60-GHz differential transmitter front end consisting of a two-stage pre-amplifier, a power splitter, and two identical reconfigurable power mixer segments whose output currents are combined. Each stage of the pre-amplifier is implemented as a stacked topology to both boost output power by increasing supply voltage to 1.5 V and also improve stability [30]. It is noted that the maximum VDD is ~ 1.1 V for thin-oxide devices in a 45-nm SOI CMOS. Each pre-amplifier stage is biased at the current density of 0.5 mA/ μ m, where the maximum available gains of the cascode devices at the first and second stages are 15.7 and 16.7 dB, respectively, at 60 GHz in simulation.

All the matching networks are implemented using ground-shielded co-planar waveguide (CPW) transmission lines on the 2.1- μ m-thick top aluminum layer (LB) with 10- μ m width and 10- μ m spacing from the side ground walls, resulting in a characteristic impedance of $\sim 50 \Omega$ and a loss of ~ 0.6 dB/mm at 60 GHz. Ground-shield CPW transmission line is chosen for design as it provides better accurate electromagnetic (EM) modeling and isolation than does transformer-based matching network. The two stages of the pre-amplifier are stagger-tuned to extend the bandwidth. A degeneration inductor, which is implemented as a shunt transmission line, is employed in the first stage to present a 50- Ω load to the frequency tripler over a wide frequency range. The power divider, which is implemented with a resistor-less Wilkinson power divider for a shorter interconnect in layout, feeds the two identical power mixer segments with differential signals in opposite polarity.¹ The simulated loss of the power divider is 4.1 dB; 3 dB from ideal two-way splitting and 1.1 dB from insertion loss of the transmission line.

Each power mixer segment is implemented as a Gilbert-cell switched transconductance mixer [32], where the

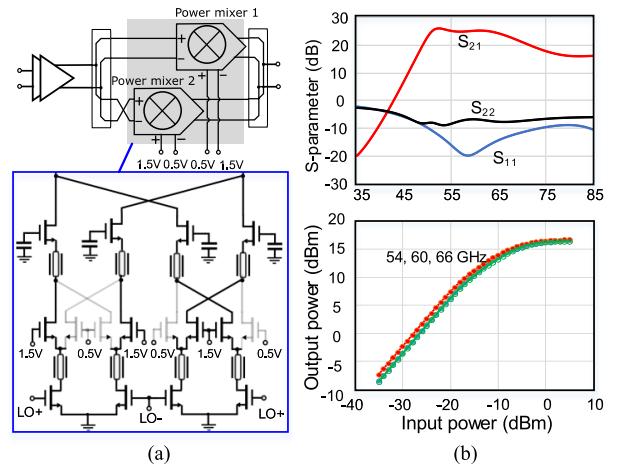


Fig. 13. (a) CW-mode configuration of the power mixers and (b) small- and large-signal simulation results of the RF front end, which includes the two-stage driver and power mixers in CW mode.

common-source transistors are driven with the 60-GHz LO signal and the baseband signals are applied to the gates of the switching quad transistors. A third level of stacked transistors is added above the switching quad devices to increase the output voltage swing and correspondingly the output power (as in [33] which was not yet published when this design was carried out). This approach allows an increase in the supply voltage to $3 \times$ VDD while keeping the voltage swing across each device within reliability limits: a large output voltage stress is distributed equally over all the transistors in the stack by inducing appropriate voltage swings at the stacking device gates through the shunt gate capacitors [30], [31]. Series transmission lines are employed between the stacked devices for interstage matching, along with source and drain device parasitic capacitances. Fig. 13 shows the CW-mode configuration of the power mixers and the simulation results of the RF front-end circuitry that includes the two-stage driver and power mixers in CW mode. The simulated small-signal gain is 27.7 dB at 60 GHz with a 3-dB bandwidth of 17 GHz, and the simulated input return loss is better than 10 dB over a 24-GHz bandwidth. The simulated saturation output power is around 17 dBm, and the simulated OP1dB ranges from 9.8 to

¹An isolation resistor is not required since any reflections at the power mixer inputs would be equal amplitude and in-phase.

TABLE III
SUMMARY OF THE SIMULATED PERFORMANCE
OF EACH FRONT-END STAGE

@ 60 GHz	Small signal gain (dB)	Peak PAE (%)	DC power consumption (mW) @ peak PAE
1 st stage pre-amplifier	5.7	21	30
2 nd stage pre-amplifier	11.1	26	59
Power splitter+two power mixers+output combiner in CW mode	11.7	6.4	343

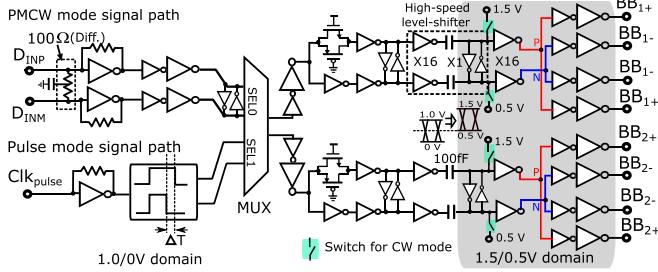


Fig. 14. Baseband waveform generation circuitry schematic.

10.6 dBm from 54 to 66 GHz. The simulated output power drops by <1 dB when the temperature increases from 25 °C to 100 °C at the output frequency of 60 GHz as the power mixer chain still operates in the saturation power across temperature. The simulated drain efficiencies are 9.4% for power mixer only and 7.7% drain efficiency for the entire front-end circuitry at 60 GHz in the saturation power. The efficiency of the power mixer could be further improved by using techniques demonstrated in prior SOI stacked power amplifiers [36], [37]. Table III summarizes the simulated performance of each front-end stage.

C. Baseband Waveform Generation Circuitry

Baseband waveform generation circuitry provides the quad-switching devices of the two power mixers with different baseband signals for CW, PMCW, and pulse modes, as illustrated in Fig. 5. As shown in Fig. 14, the waveform generation circuitry has two separate signal paths for PMCW and pulse mode before the selection point at the MUX. A differential radar code signal is provided as the input to the PMCW signal path and then amplified through a CMOS buffer chain with 100-Ω differential input termination. A clock signal $\text{Clk}_{\text{pulse}}$, which determines the pulse repetition frequency, is the input to the pulse mode path and then applied to a programmable pulse generation block [described in Fig. 15(a)] after resistor-feedback inverters. After the MUX selects one of the two input paths, the output signal is converted into a differential signal and level shifted from 0/1.0 to 0.5/1.5 V to properly drive the quad-switching devices. Decoupling capacitors, which are implemented with vertical natural capacitors and MOS capacitors, are placed between ground and different power supply planes for establishing a low impedance. CW mode is supported by turning on the dc switches connected to either 0.5 or 1.5 V after the level shifters.

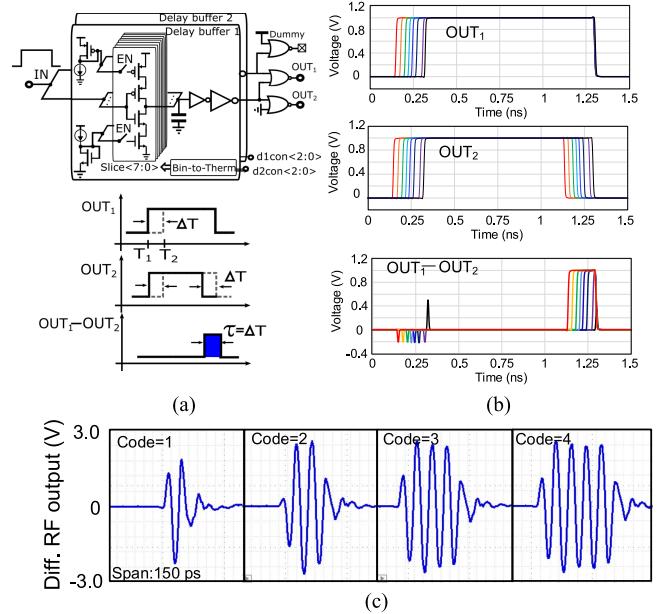


Fig. 15. (a) Programmable pulse generation circuitry schematic and pulse generation principle. (b) Pulse mode baseband simulation results. (c) Simulated differential RF output for different pulselength settings.

The pulse generation circuitry consists of two programmable delay buffers followed by NOR gates to generate two output signals with aligned rising edges and falling edges time-shifted by ΔT , as shown in Fig. 15(a). Each delay buffer has differently weighted eight slices of current-starved inverters that are independently controlled with 3-bit digital signal. The r_{ON} resistance of each slice is controlled using the top PMOS and bottom NMOS devices biased with programmable reference currents; these controls can be used for fine-tuning of the pulselength. The envelope of the RF pulse waveform is shaped at the combiner output as $|\text{OUT}_1 - \text{OUT}_2|$ since the LO input polarity is swapped for the second power mixer. Therefore, ΔT between the two falling edges determines the pulselength, as shown in Fig. 15(a). Fig. 15(b) shows the simulated OUT_1 , OUT_2 , and $\text{OUT}_1 - \text{OUT}_2$ in pulse mode while sweeping the 3-bit digital control. The simulated tuning range of the pulselength is 165 ps with ~24-ps resolution. A small timing mismatch at rising edges between OUT_1 and OUT_2 generates glitches from $\text{OUT}_1 - \text{OUT}_2$. The biggest glitch is observed when the two delay buffers have the same pulselength settings, which is not used in a practical use with a non-zero pulselength. The small glitches have the peak amplitude of around 0.2 V, resulting in short RF pulses. The measured peak amplitude of those RF pulses is 15 dB lower than the main pulses, as shown in Fig. 23(c). Fig. 15(c) shows the simulated pulse waveform at the differential RF output for different pulselength settings. The pulse delay is also programmable by shifting the two falling edges of T_1 and T_2 of the two delay buffers together for a given pulselength. This feature can be potentially useful when multiple pulse mode transmitters need to be synchronized in the air for beam-forming applications [34].

Fig. 16 describes the effect of mismatches in LO phase, amplitude, and baseband timing between the two power

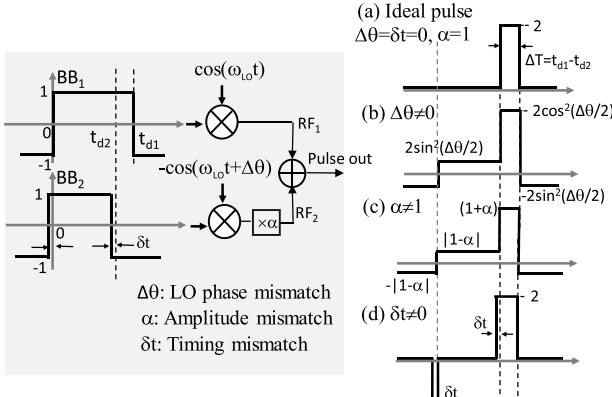


Fig. 16. Mismatch effect between the two power mixers for pulse generation in (b) LO phase, (c) amplitude, and (d) baseband timing compared to (a) ideal pulse generation.

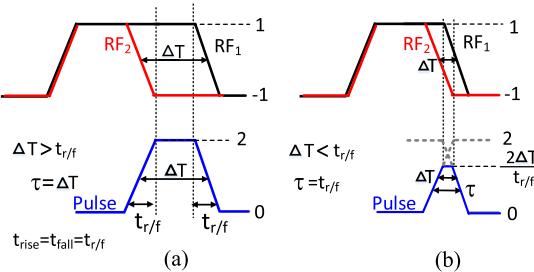


Fig. 17. RF pulse waveform considering a rise/fall time of the RF signal envelope for (a) $\Delta T > t_{r/f}$ and (b) $\Delta T < t_{r/f}$, assuming symmetric rise/fall time given by $t_{rise} = t_{fall} = t_{r/f}$.

mixers due to deterministic layout mismatch, random device mismatch, and uneven current flow from the power supply. LO phase mismatch $\Delta\theta$ increases the low-level amplitude from 0 to $2\sin^2(\Delta\theta/2)$ and reduces the high-level amplitude from 2 to $2\cos^2(\Delta\theta/2)$. Amplitude mismatch also increases the low-level amplitude to $|1 - \alpha|$, where α is the ratio of RF_1 and RF_2 amplitudes. Such increase in low-level amplitude degrades SNR in the pulse radar detection. The baseband timing mismatch δt generates unwanted short pulses with the pulselength of δt and changes the main pulselength to $\Delta T + \delta t$, where ΔT is the time delay between the falling edges of BB_1 and BB_2 given by $t_{d1} - t_{d2}$. The unwanted pulse will be suppressed through the limited bandwidth of the output matching network if δt is small enough. Fig. 17 illustrates the effect of a finite rise or fall time of the RF signal envelope on the pulse generation, assuming symmetric rise/fall time given by $t_{rise} = t_{fall} = t_{r/f}$. When ΔT is larger than $t_{r/f}$, the pulselwidth τ , which is defined as full-width half maximum (FWHM), is equal to ΔT , which is expected from the proposed pulse generation principle. As ΔT decreases below $t_{r/f}$, the pulselwidth is not reduced with ΔT and is limited to $t_{r/f}$ with the reduced peak amplitude by a factor of $\Delta T/t_{r/f}$. It is noted that $t_{r/f}$ is mainly determined by the output network bandwidth. Fig. 18 shows the simulated RF pulse envelope along with the baseband waveforms generated from $BB_1 - BB_2$ as ΔT decreases from 25 to 5 ps with 5-ps step. As expected in Fig. 17(b), the simulated minimum RF pulselwidth is limited to around 15 ps, which is close to the simulated rise/fall time at the RF output in Fig. 19(b).

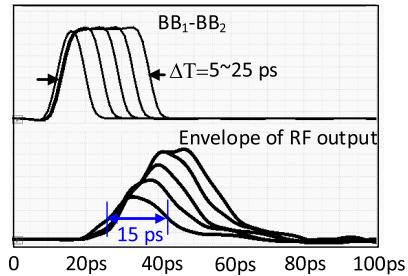


Fig. 18. Simulated RF output pulse envelope along with the baseband waveform generated from $BB_1 - BB_2$ as ΔT decreases from 25 to 5 ps with 5-ps step.

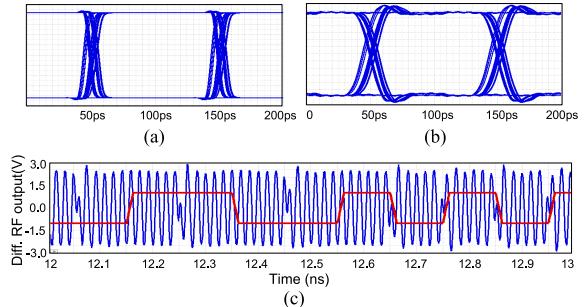


Fig. 19. Simulated PMCW-mode operation using 10-Gb/s PRBS signal. (a) Eye diagram at differential baseband output. (b) Eye diagram of RF signal envelope at RF output. (c) Differential RF output signal (blue) along with input PRBS signal (red).

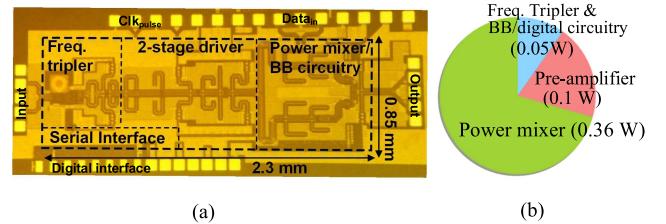


Fig. 20. (a) Chip photograph. (b) DC power consumption.

Fig. 19(a) shows the simulated 10-Gb/s eye diagram at the differential baseband output in PMCW mode when the output is loaded with the quadrature switching devices and demonstrates the simulated rise/fall time <10 ps. The eye diagram of the RF output signal envelope is plotted in Fig. 19(b), presenting rise/fall time of ~ 14 ps. Fig. 19(c) shows the simulated differential RF output along with the baseband input signal. To allow fast signal transition at the output of the baseband waveform generation circuitry, interconnects between final-stage inverters and quad-switching devices are minimized in layout.

V. MEASUREMENT RESULTS

The proposed IC was fabricated in a 45-nm CMOS SOI process. The chip photograph is shown in Fig. 20(a); it has an active area of 2.3×0.85 mm 2 excluding pads. All measurements reported in this section have been performed on wafer at 25 °C. The average dc power consumption is 0.51 W with power breakdown, as illustrated in Fig. 20(b). The IC is measured in CW, pulse, and PMCW modes using an experimental setup, as shown in Fig. 21.

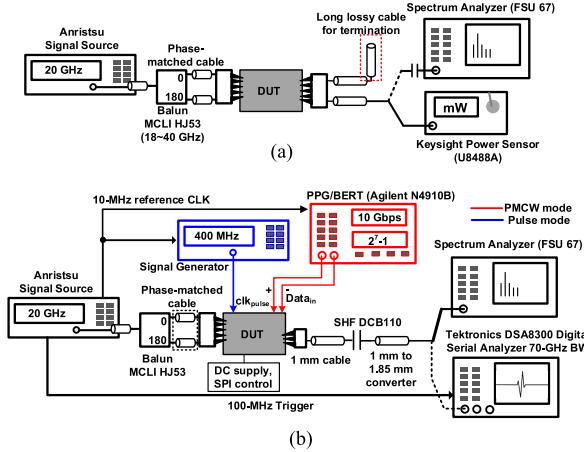


Fig. 21. Experimental setup to measure (a) CW mode and (b) PMCW and pulse mode operation.

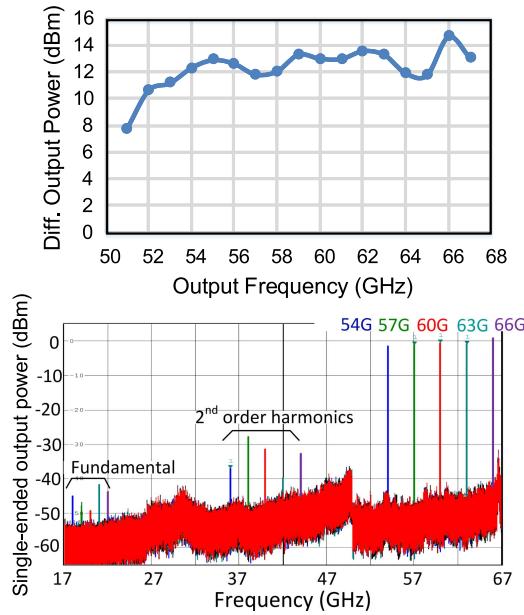


Fig. 22. (a) Measured differential output power and (b) single-ended frequency spectrum in CW-mode operation before de-embedding the output cable loss.

Fig. 22 shows the measured differential output power and frequency spectrum in CW mode using a Keysight U8488A power sensor and FSU67 spectrum analyzer with a 0-dBm frequency tripler input power. The measured average output power from 54 to 67 GHz was approximately 12.8 dBm with a peak power of 14.7 dBm at 66 GHz. The power variation from 54 to 64 GHz is less than ± 0.9 dB; this low output power variation allows support for 10-GHz FMCW radar bandwidth while keeping side-lobe suppression ratio <-13.5 dB in the IF spectrum [35].² The frequency spectrum measured at a single-ended output demonstrates harmonic rejection ratio

²In the FMCW radar system, the RF amplitude ripple within the chirp bandwidth contributes the side lobe in the IF spectrum response. The side-lobe magnitude due to the amplitude ripple is given by $SL_{a-err} = 20 \log(10^{A_e/20} - 1)$, where A_e is the amplitude error [35]. According to this equation, the maximum allowable power variation is ± 0.9 dB to keep $SL_{a-err} <-13.5$ dB, where -13.5 dB is IF side-lobe suppression ratio without windowing in the ideal FMCW radar.

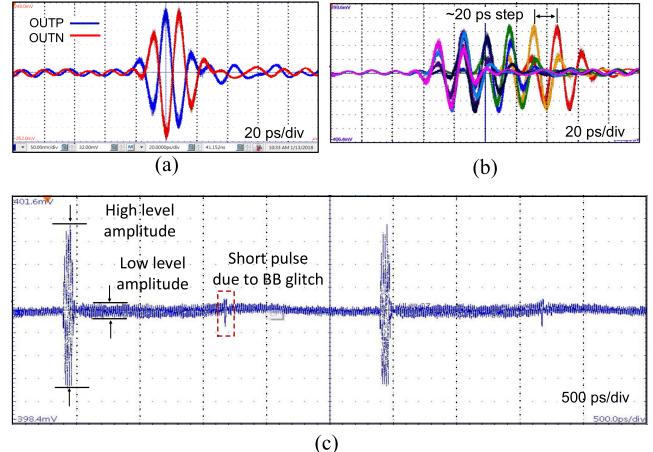


Fig. 23. (a) Measured differential pulse waveform, (b) measured pulse delay control, and (c) measured pulse waveform with a pulse repetition frequency of 400 MHz over 5-ns time span.

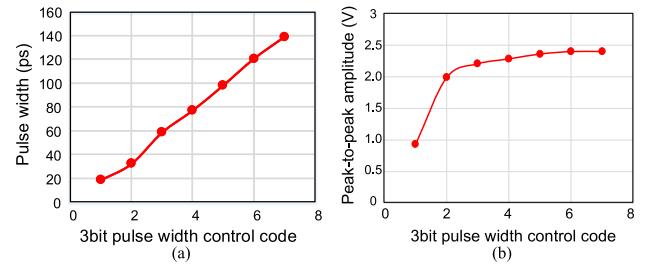


Fig. 24. (a) Measured programmable pulselength and (b) measured single-ended peak-to-peak pulse amplitude across 3-bit pulselength control.

greater than 27 dB over a wide bandwidth. It is noted that this result could be further improved if measured differentially considering that dominant harmonic component at the single-ended output is the second-order harmonic frequency.

Fig. 23(a) shows the differential output waveforms in pulse mode directly measured using a 70-GHz BW DSA8300 Digital Serial Analyzer (DSA) for a 400-MHz pulse repetition frequency and an input frequency of 22 GHz into the frequency tripler. The signal sources for LO and Clk_{pulse} generation and the DSA are synchronized, as shown in Fig. 21(b). Fig. 23(b) demonstrates the programmable pulse delay with 20-ps step for a fixed pulselength. Fig. 23(c) shows the measured pulse waveform with a pulse repetition frequency of 400 MHz over 5-ns time span. The low-level amplitude is 20.1 dB lower than the high-level amplitude, which implies a good matching between the two power mixers, as discussed in Fig. 16. Fig. 24(a) shows the measured programmable pulselength across 3-bit digital control ranging from 140 to 20 ps with approximately 20 ps of resolution. The peak output power drops less than 1 dB compared to the CW mode until the pulselength is reduced to <45 ps, as shown in Fig. 24(b). Fig. 25 shows the measured output signal at the single-ended output in pulse mode in time and frequency domains for different pulselength settings. The measured signal bandwidth changes from 7 to 40 GHz as the pulselength changes from

TABLE IV
MEASUREMENT RESULT SUMMARY AND COMPARISON TO PUBLISHED SINGLE- AND MULTI-MODE RADAR TRANSMITTERS

	This Work	G. Pyo MCWL2016[39]	A. Arbabian JSSC2010[7]	D. Guermandi JSSC2017[38]	B.P. Ginsburg ISSCC2018[4]	E. Ozturk TMTT2017[40]	S. Shopov TMTT2017[41]
Supported Waveforms	Pulse, FMCW/CW, Code (PMCW)	Pulse, FMCW/CW	Pulse	Code (PMCW)	FMCW	FMCW	CW (Doppler)
Frequency	60 GHz	24/26 GHz	90GHz	79GHz	77GHz	58.3-63.9 GHz	63.8-70.2 GHz
Pulse Width	25 ps-140 ps	500ps-1ns	26ps- 220ps	N/A	N/A	N/A	N/A
Demonstrated FMCW BW	N/A	0.32GHz	N/A	N/A	4GHz	5.6 GHz	N/A
Bandwidth available for FMCW radar	10 GHz*	N/A	N/A	N/A	N/A	N/A	N/A
CW Output Power	+12.8 dBm (ave.) +14.7 dBm (peak)	-0.56 dBm	+17.2 dBm (PA Psat)	+8.5dBm#	>+10.8dBm**	+6.4	-7
Code Mod. Rate	>10 Gb/s	N/A	N/A	2 Gb/s	N/A	N/A	N/A
Integration level	Freq. tripler, waveform gen., TX front-end	VCO, freq. divider, waveform gen., drive amp	VCO, PA, antenna, waveform gen.	PLL, 2TX, 2RX, A2D, custom digital core	PLL, 3TX, 4RX, Baseband, A2D, MCU	VCO/frequency divider, PA, power detector, LNA, I/Q down converter	TX, 4RX, VCO/ frequency divider, down- converter
Chip Area	1.95 mm²	3.64 mm ²	1.2 mm ²	7.9 mm ²	22 mm ²	1.03 mm ²	1.6 mm ²
Technology	45 nm RFSOI	0.13 μm CMOS	0.13 μm SiGe	28 nm CMOS	45 nm CMOS	0.13 μm SiGe	45 nm RFSOI
Power Cons.	0.51 W	0.14 W	0.74 W	1 W	3.5 W	0.52 W	0.042W

*BW for output power variation ± 0.9 dB to achieve side-lobe suppression <-13.5 dB in the IF spectrum of FMCW radar.

**Across -40°C to 125°C, ~13.1dBm peak power at 25°C #Including flip-chip assembly and module loss

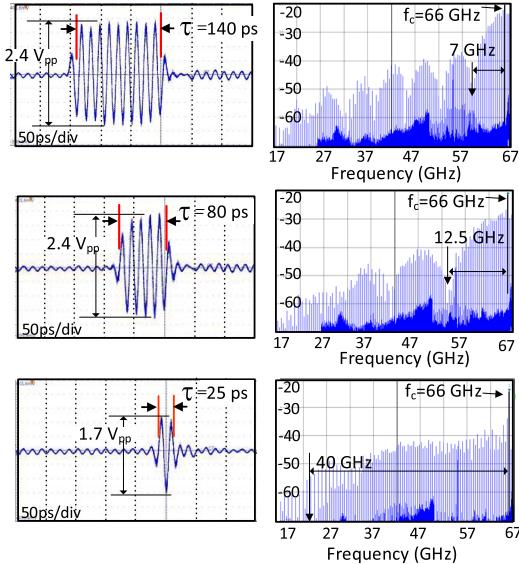


Fig. 25. Measured single-ended pulse output in time and frequency domains for different pulselength settings.

140 to 25 ps. It is noted that 40 GHz of BW can be translated into a \sim 4-mm spatial resolution.

The PMCW mode of operation was also measured using a 10-Gb/s PRBS baseband signal with the PRBS length of $2^7 - 1$, which was generated from an Agilent N4910B. The time and frequency domain measurements are shown in Fig. 26(a) and (b). A 1100 pattern at 10 Gb/s is used for close observation of one/zero signal transition, as shown

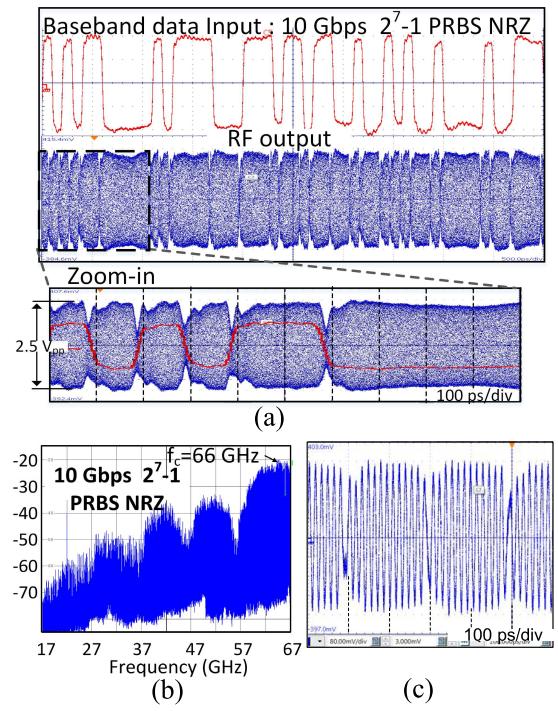


Fig. 26. Measured PMCW-mode operation at single-ended output in (a) time and (b) frequency domains using 10-Gb/s PRBS code signal and in (c) time domain using 1100 pattern at 10 Gb/s.

in Fig. 26(c). The measurement results demonstrate that the rise and fall times of the output amplitude envelope are fast enough to support >10-Gb/s data rate. Table IV summarizes

the measured performance of the proposed design compared to prior single-mode and multi-modal radar transmitter ICs and modules. This article is the first multi-mode transmitter IC to support three different radar waveforms with a very wide signal bandwidth and comparable output power to prior works.

VI. CONCLUSION

We have presented a new architecture of a multi-mode mmWave radar transmitter to enable a single front end to generate FMCW/CW, pulse, and PMCW radar signals with a wide signal bandwidth. The proposed IC has demonstrated a 54–67-GHz CW power generation with a high harmonic suppression ratio >27 dB, a programmable pulse generation with pulsedwidths down to 25 ps corresponding to 40-GHz signal bandwidth, while a pulse amplitude drops by <3 dB, and 10-Gb/s PMCW-mode radar signals. We expect that the proposed transmitter IC in this article will motivate further development of multi-mode radar modules to cover a wide variety of applications and to provide a real-time adaptability in radar detection.

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