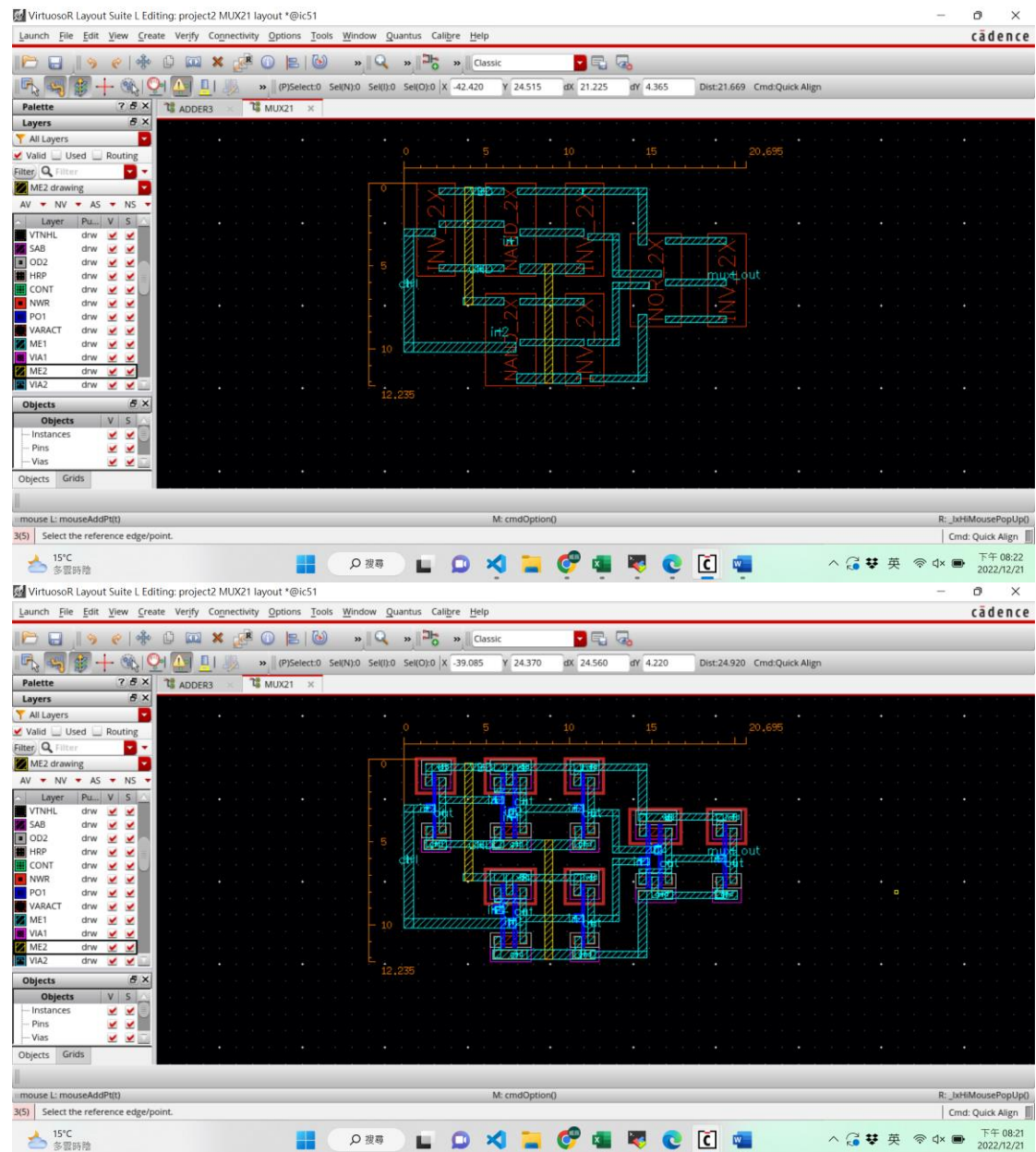


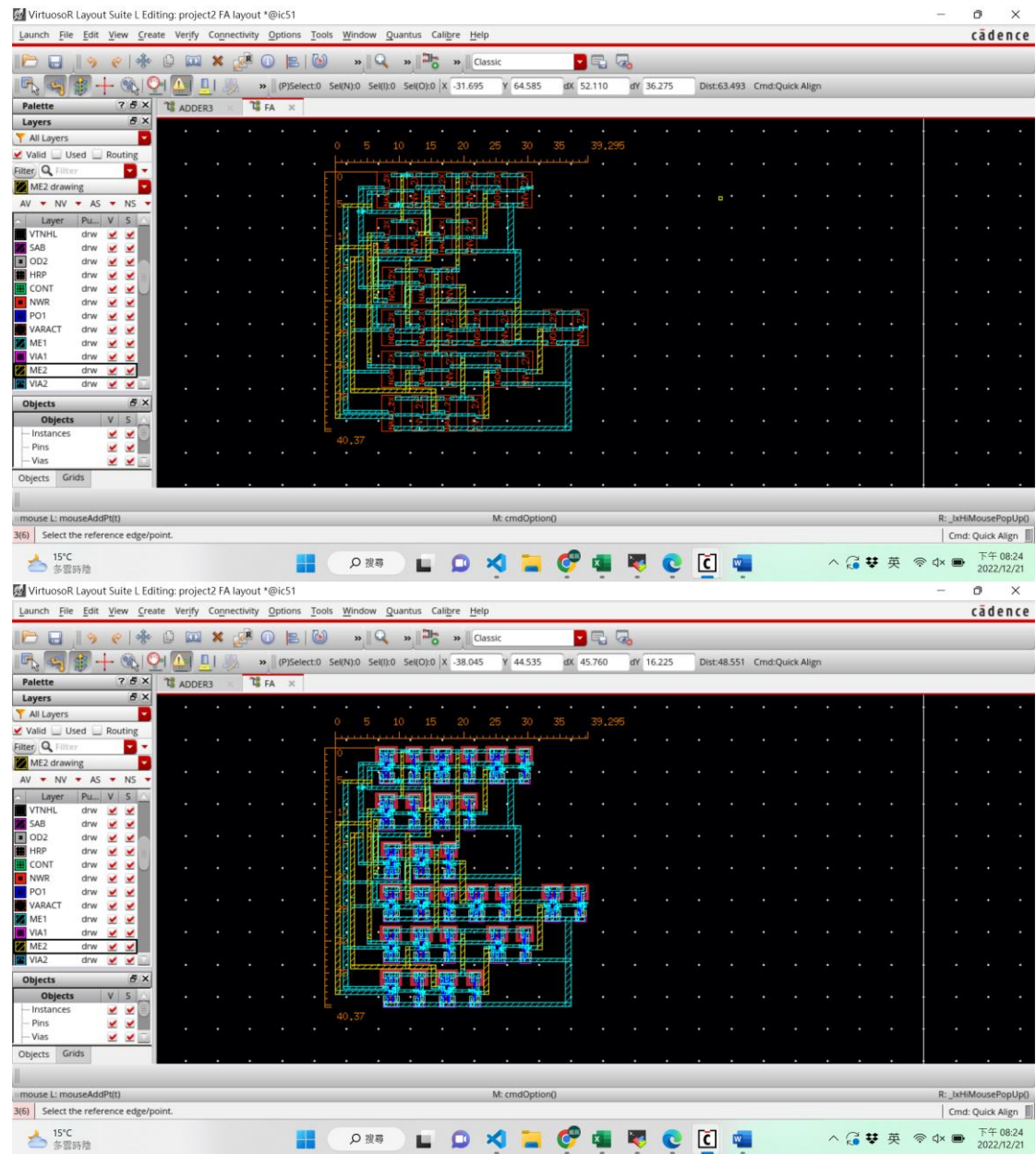
108081032 李威辰

Layout:

MUX21:



FA:

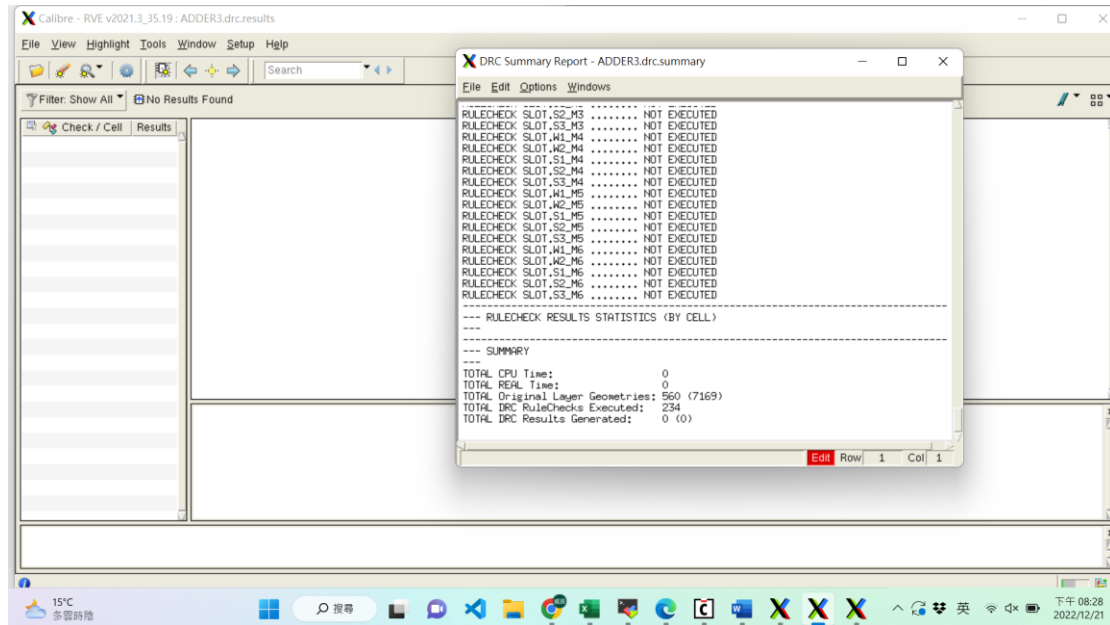


The image displays two screenshots of the Cadence Virtuoso Layout Suite L interface, showing the design of a PCB layout for a project named 'project2 ADDER3 layout *@ic51'.

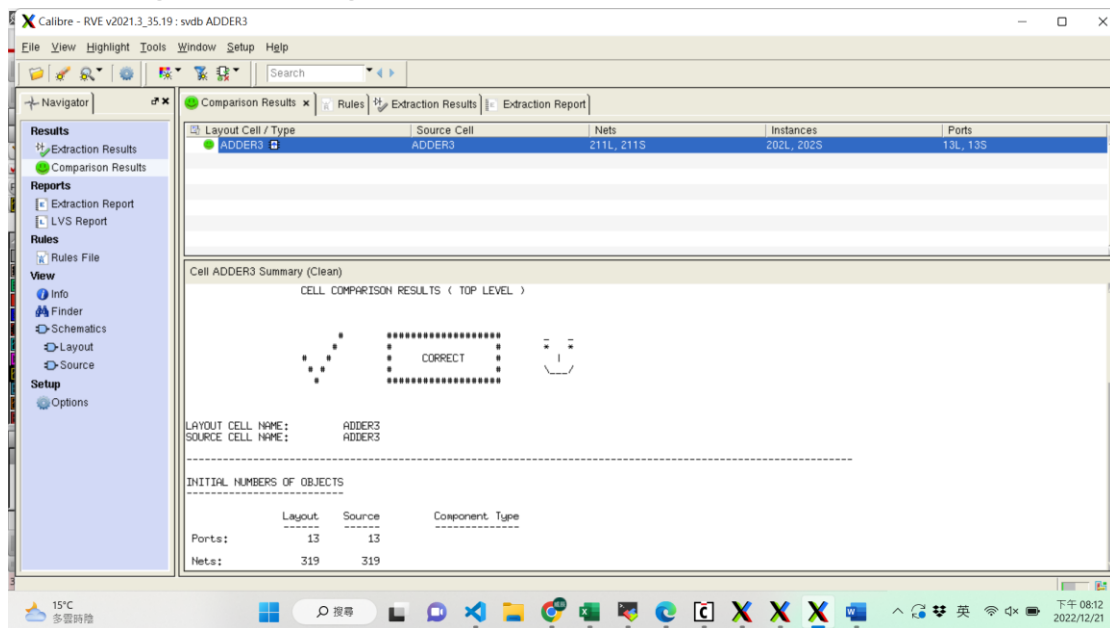
Top Screenshot: The main workspace shows a schematic-like view of the layout. Components are labeled 'U1X21' and 'U1X21'. The interface includes a layer palette on the left, a command window at the bottom, and a status bar at the top.

Bottom Screenshot: The main workspace shows a more detailed layout view, likely a top or bottom layer view. Components are labeled 'U1X21' and 'U1X21'. The interface includes a layer palette on the left, a command window at the bottom, and a status bar at the top.

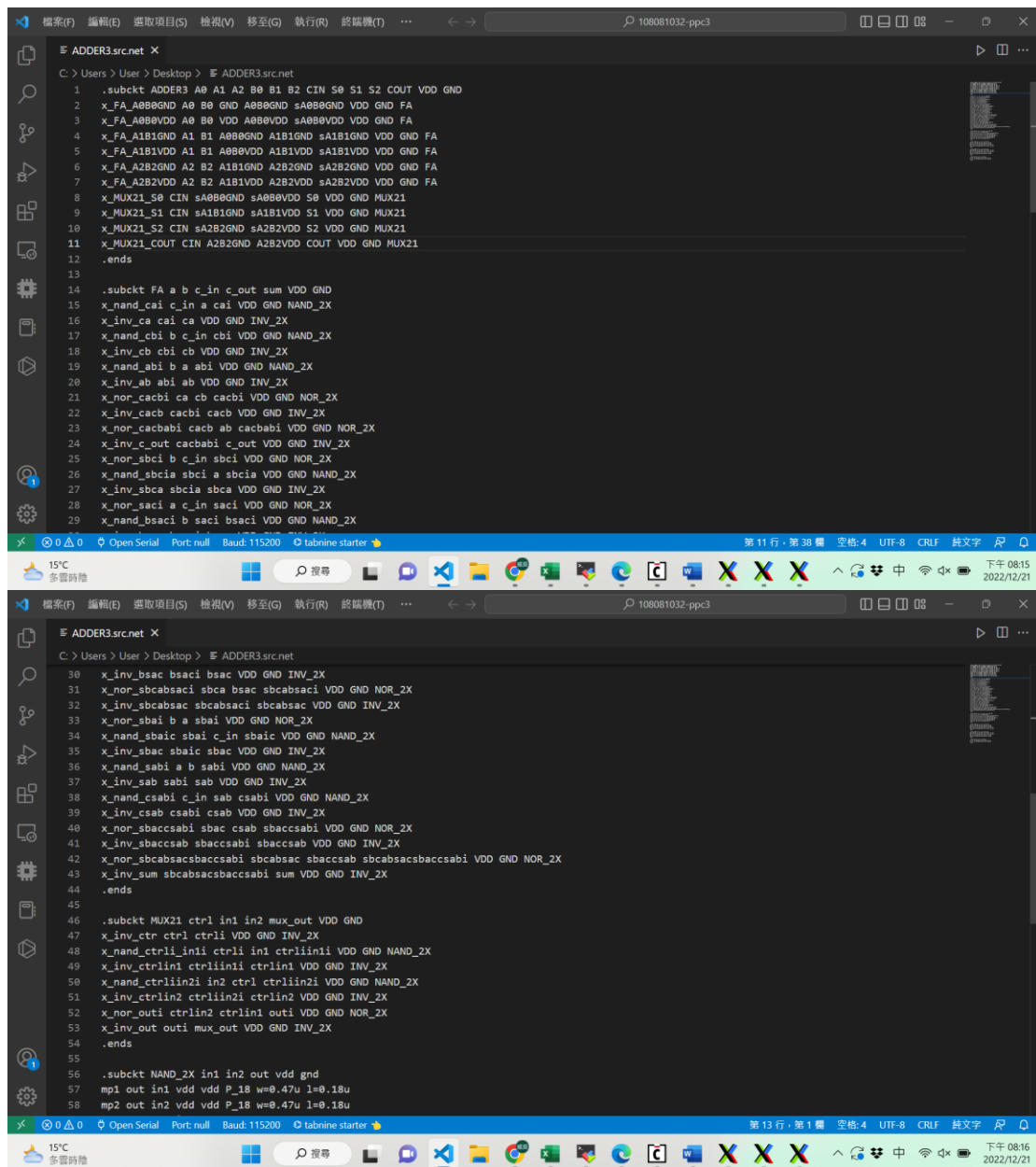
DRC summary report of ADDER3:



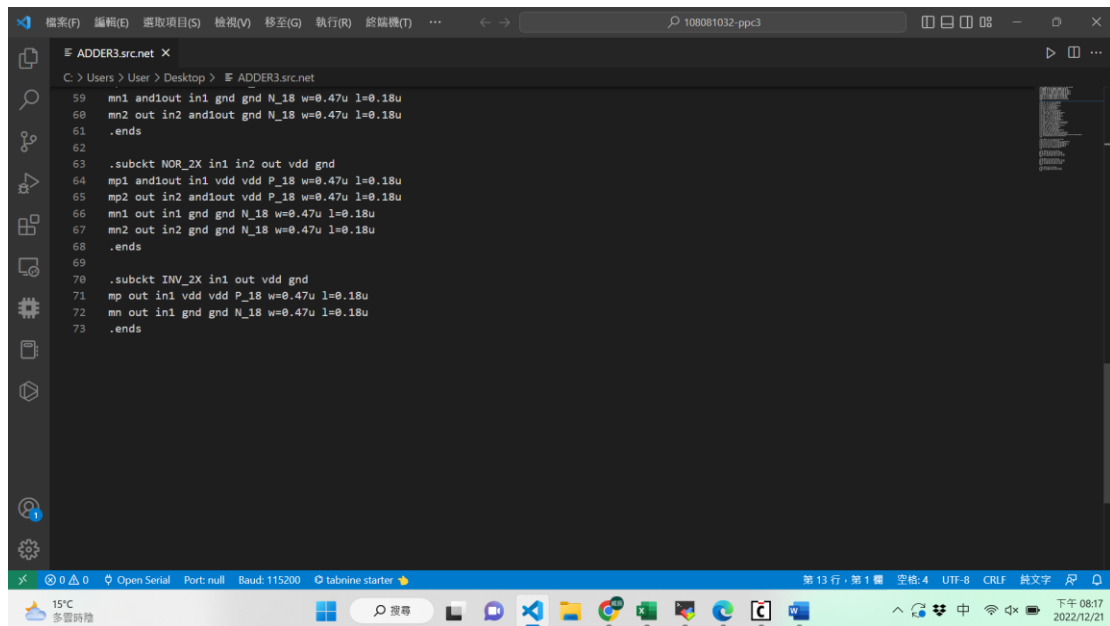
The message of passing LVS of ADDER3:



LVS schematic of ADDER3.src.net (screenshot of the text file):



```
1 .subckt ADDER3 A0 A1 A2 B0 B1 B2 CIN S0 S1 S2 COUT VDD GND
2 x_FA_A0B0GND A0 B0 GND A0B0GND sA0B0GND VDD GND FA
3 x_FA_A0B0VDD A0 B0 VDD A0B0VDD sA0B0VDD VDD GND FA
4 x_FA_A1B1GND A1 B1 A0B0GND A1B1GND sA1B1GND VDD GND FA
5 x_FA_A1B1VDD A1 B1 A0B0VDD A1B1VDD sA1B1VDD VDD GND FA
6 x_FA_A2B2GND A2 B2 A1B1GND A2B2GND sA2B2GND VDD GND FA
7 x_FA_A2B2VDD A2 B2 A1B1VDD A2B2VDD sA2B2VDD VDD GND FA
8 x_MUX21_S0 CIN sA0B0GND sA0B0VDD S0 VDD GND MUX21
9 x_MUX21_S1 CIN sA1B1GND sA1B1VDD S1 VDD GND MUX21
10 x_MUX21_S2 CIN sA2B2GND sA2B2VDD S2 VDD GND MUX21
11 x_MUX21_COUT CIN A2B2GND A2B2VDD COUT VDD GND MUX21
12 .ends
13
14 .subckt FA a b c_in c_out sum VDD GND
15 x_nand_cai c_in a cai VDD GND NAND_2X
16 x_inv_ca cai ca VDD GND INV_2X
17 x_nand_cbi b c_in cbi VDD GND NAND_2X
18 x_inv_cb cbi cb VDD GND INV_2X
19 x_nand_abi b a abi VDD GND NAND_2X
20 x_inv_ab abi ab VDD GND INV_2X
21 x_nor_cacbi ca cb cacbi VDD GND NOR_2X
22 x_inv_cacb cacbi cacb VDD GND INV_2X
23 x_nor_cacbab cacb ab cacbab VDD GND NOR_2X
24 x_inv_c_out cacbab c_out VDD GND INV_2X
25 x_nor_sbci b c_in sbci VDD GND NOR_2X
26 x_nand_sbci sbci a sbcia VDD GND NAND_2X
27 x_inv_sbca sbcia sbca VDD GND INV_2X
28 x_nor_saci a c_in saci VDD GND NOR_2X
29 x_nand_bsaci b saci bsaci VDD GND NAND_2X
30 x_inv_bsac bsaci bsac VDD GND INV_2X
31 x_nor_sbcbbsaci sbca bsac sbcbbsaci VDD GND NOR_2X
32 x_inv_sbcbbsac sbcbbsaci sbcbbsac VDD GND INV_2X
33 x_nor_sbai b a sbai VDD GND NOR_2X
34 x_nand_sbaic sbai c_in sbaic VDD GND NAND_2X
35 x_inv_sbac sbaic sbac VDD GND INV_2X
36 x_nand_sabi a b sabi VDD GND NAND_2X
37 x_inv_sab sabi sab VDD GND INV_2X
38 x_nand_csabi c_in sab csabi VDD GND NAND_2X
39 x_inv_csab csabi csab VDD GND INV_2X
40 x_nor_sbaccsabi sbac csab sbaccsabi VDD GND NOR_2X
41 x_inv_sbaccsab sbaccsabi sbaccsab VDD GND INV_2X
42 x_nor_sbcbbsacsbsabi sbcbbsac sbaccsab sbcbbsacsbsabi VDD GND NOR_2X
43 x_inv_sum sbcbbsacsbsabi sum VDD GND INV_2X
44 .ends
45
46 .subckt MUX21 ctrl in1 in2 mux_out VDD GND
47 x_inv_ctr ctrl ctrl VDD GND INV_2X
48 x_nand_ctrli in1 ctrl in1 ctrliin1 VDD GND NAND_2X
49 x_inv_ctrliin1 ctrliin1 ctrliin1 VDD GND INV_2X
50 x_nand_ctrliin2 in2 ctrl ctrliin2 VDD GND NAND_2X
51 x_inv_ctrliin2 ctrliin2 ctrliin2 VDD GND INV_2X
52 x_nor_outi ctrliin2 ctrliin1 outi VDD GND NOR_2X
53 x_inv_outi outi mux_out VDD GND INV_2X
54 .ends
55
56 .subckt NAND_2X in1 in2 out vdd gnd
57 mp1 out in1 vdd vdd P_18 w=0.47u l=0.18u
58 mp2 out in2 vdd vdd P_18 w=0.47u l=0.18u
```

```
59 mn1 and1out in1 gnd gnd N_18 w=0.47u l=0.18u
60 mn2 out in2 and1out gnd N_18 w=0.47u l=0.18u
61 .ends
62
63 .subckt NOR_2X in1 in2 out vdd gnd
64 mp1 and1out in1 vdd vdd P_18 w=0.47u l=0.18u
65 mp2 out in2 and1out vdd P_18 w=0.47u l=0.18u
66 mn1 out in1 gnd gnd N_18 w=0.47u l=0.18u
67 mn2 out in2 gnd gnd N_18 w=0.47u l=0.18u
68 .ends
69
70 .subckt INV_2X in1 out vdd gnd
71 mp out in1 vdd vdd P_18 w=0.47u l=0.18u
72 mn out in1 gnd gnd N_18 w=0.47u l=0.18u
73 .ends
```

What else did you do to enhance your layout quality?

用 A 去對齊，並且盡可能地將 metal2 縮短以便其他線路也可用 metal2

What have you learned from this homework?

這個作業讓我體會到 layout 真的有夠難畫，要想辦法縮面積又要讓線路好接，總之花了我非常多時間。

What problem(s) have you encountered in this homework?

面積一直縮不小，因為線路要想辦法接順，而且 MUX、FA 的邏輯化簡可能我還要顯辦法再縮短，總之總面積的部分我還要取學習改進。