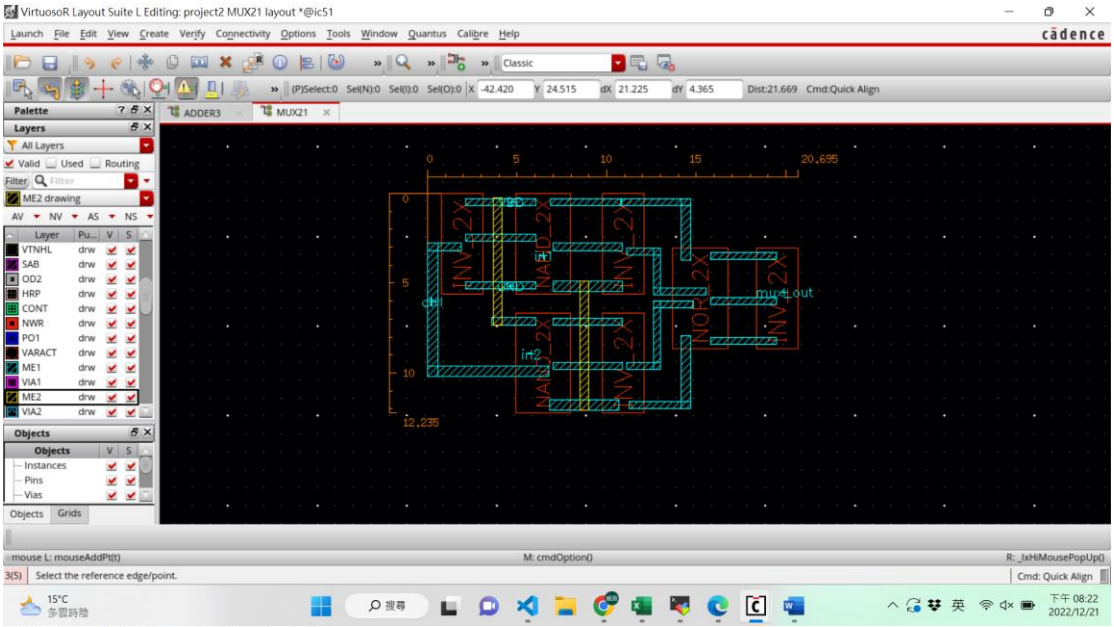
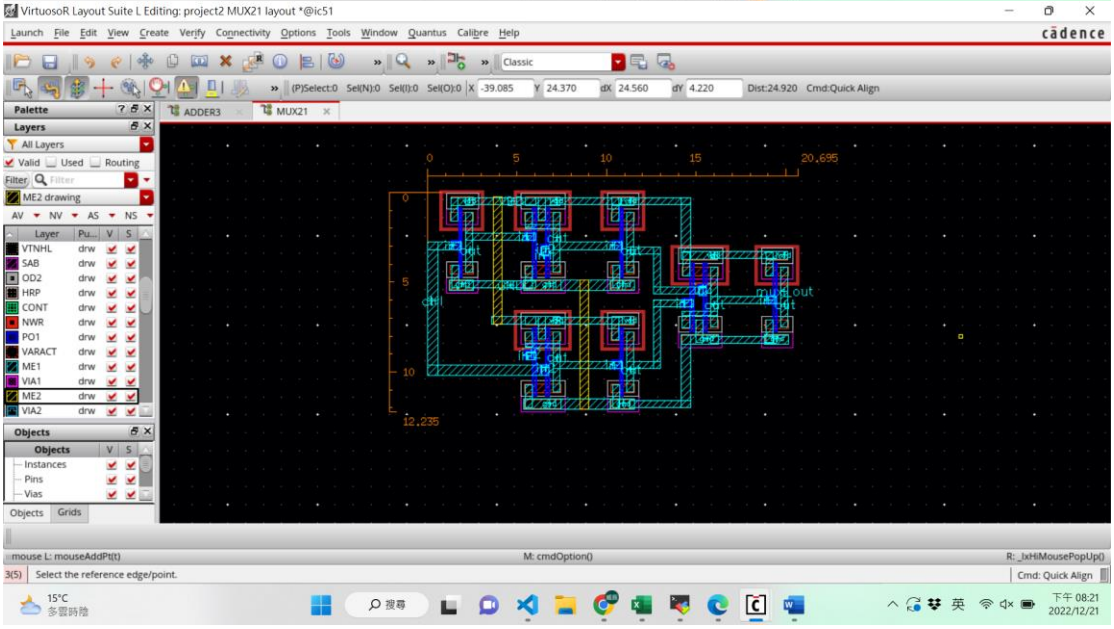
108081032 李威辰

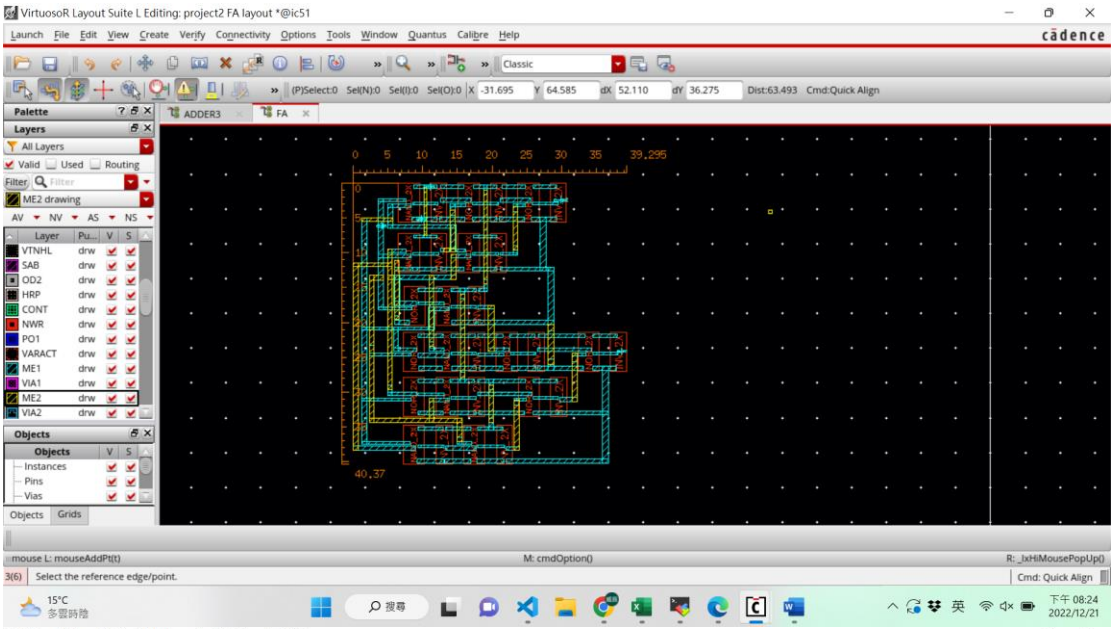
Layout:

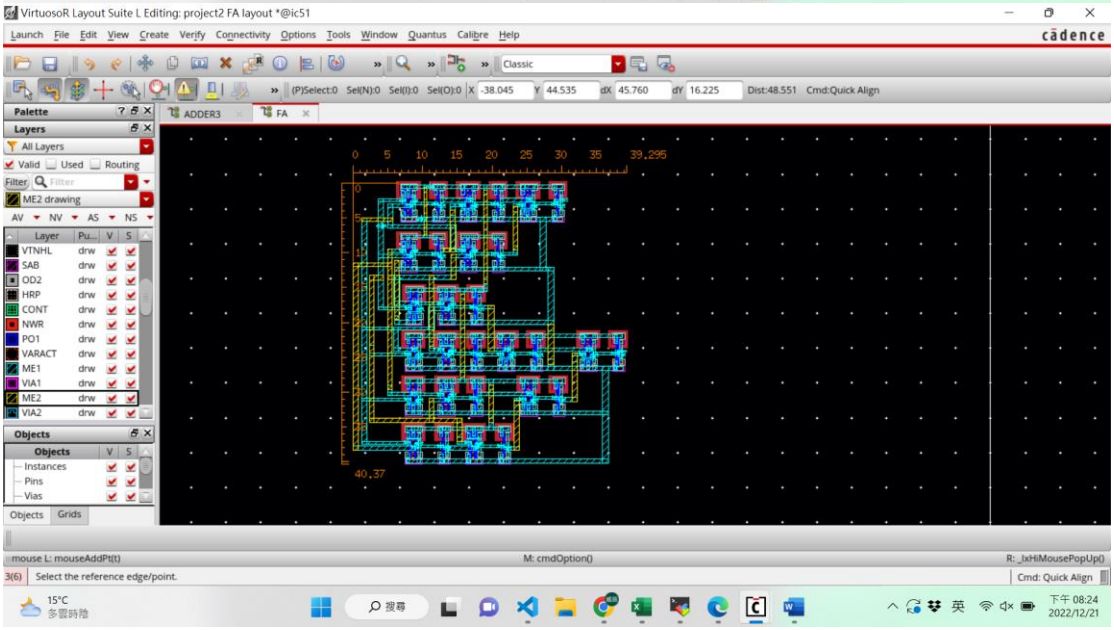
MUX21:



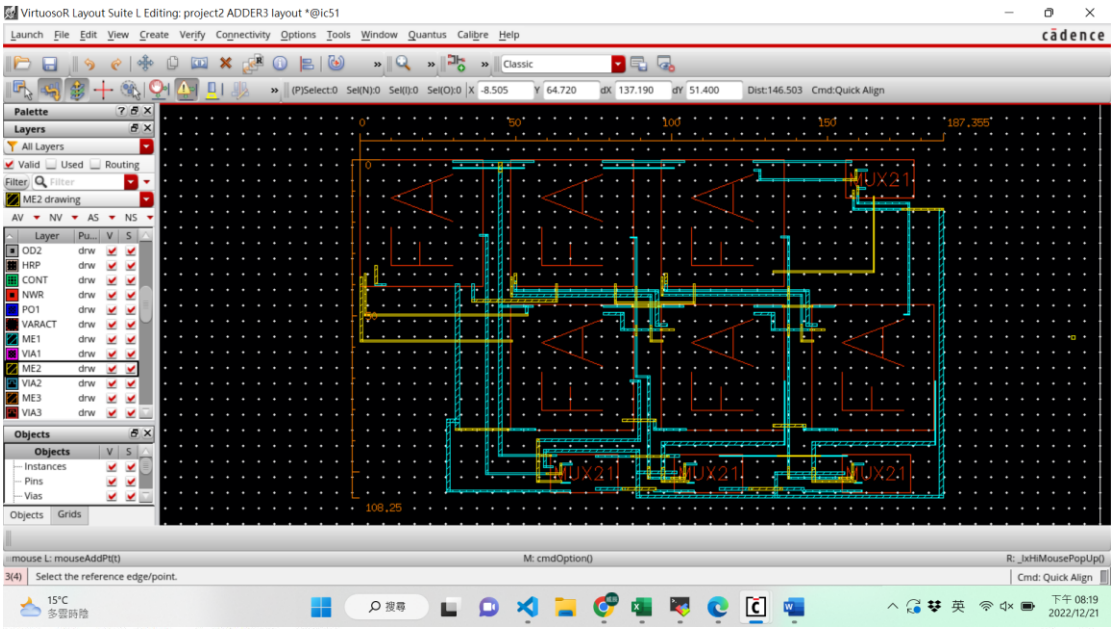


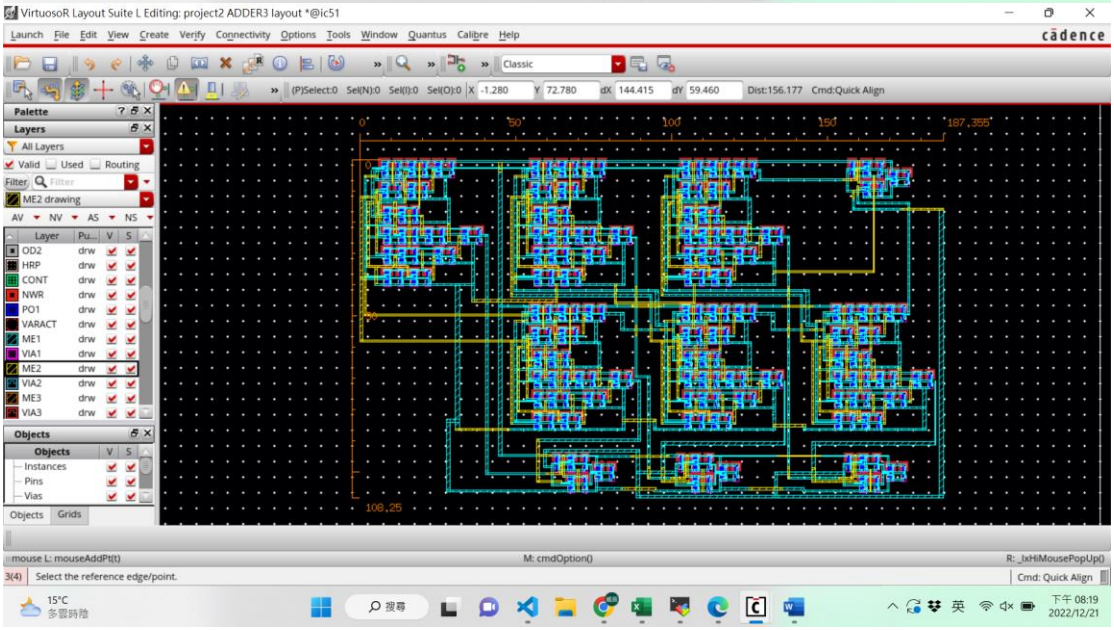
FA:


VirtuosoR Layout Suite L Editing: project2 FA layout *@ic51
Launch File Edit View Create Verify Connectivity Options Tools Window Quantus Calibre Help
cadence
ADDER3
FA
mouse L: mouseAddPt(t)
M: cmdOption()
Select the reference edge/point.
Cmd: Quick Align

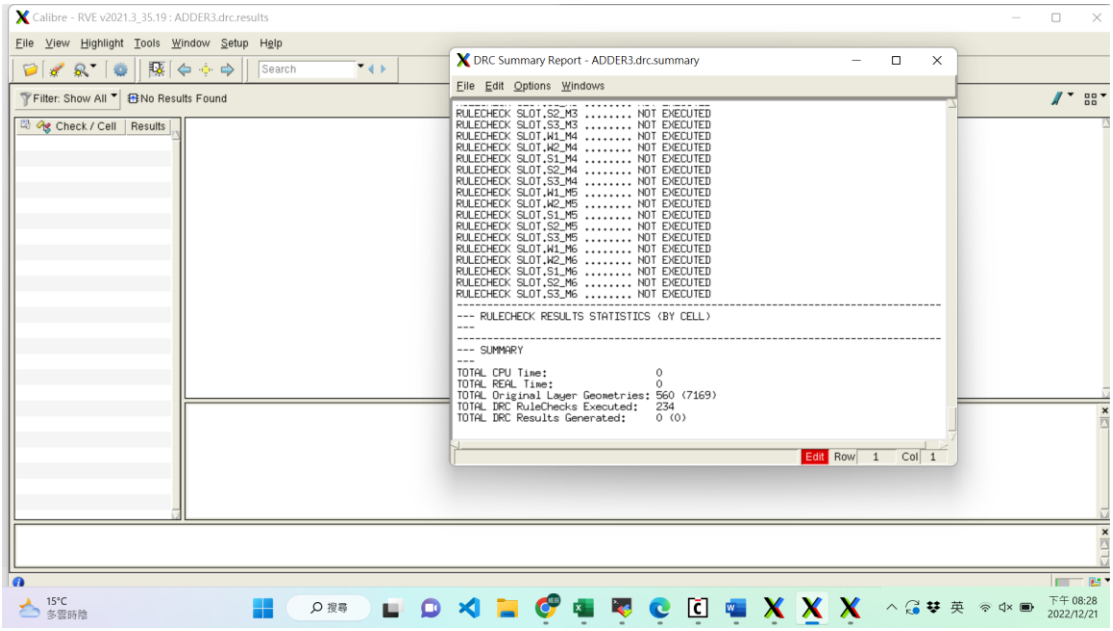

VirtuosoR Layout Suite L Editing: project2 FA layout *@ic51
Launch File Edit View Create Verify Connectivity Options Tools Window Quantus Calibre Help
cadence
ADDER3
FA
mouse L: mouseAddPt(t)
M: cmdOption()
Select the reference edge/point.
Cmd: Quick Align

ADDER3:

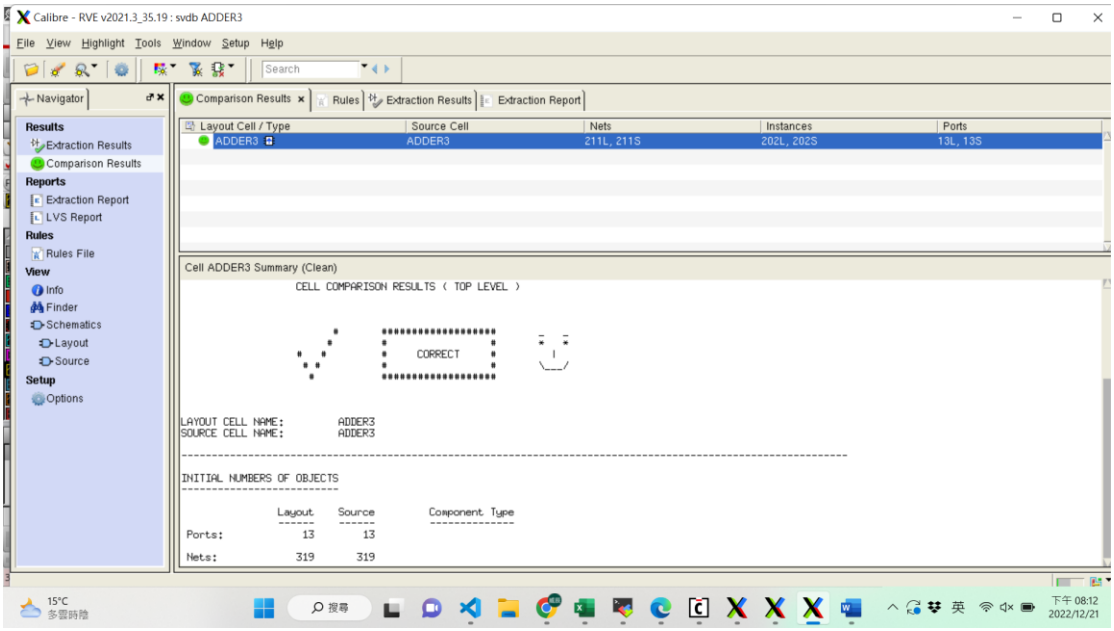

VirtuosoR Layout Suite L Editing: project2 ADDER3 layout *@ic51
Launch File Edit View Create Verify Connectivity Options Tools Window Quantus Calibre Help
cadence
MUX21
MUX21
MUX21
MUX21


VirtuosoR Layout Suite L Editing: project2 ADDER3 layout *@ic51
Launch File Edit View Create Verify Connectivity Options Tools Window Quantus Calibre Help
cadence

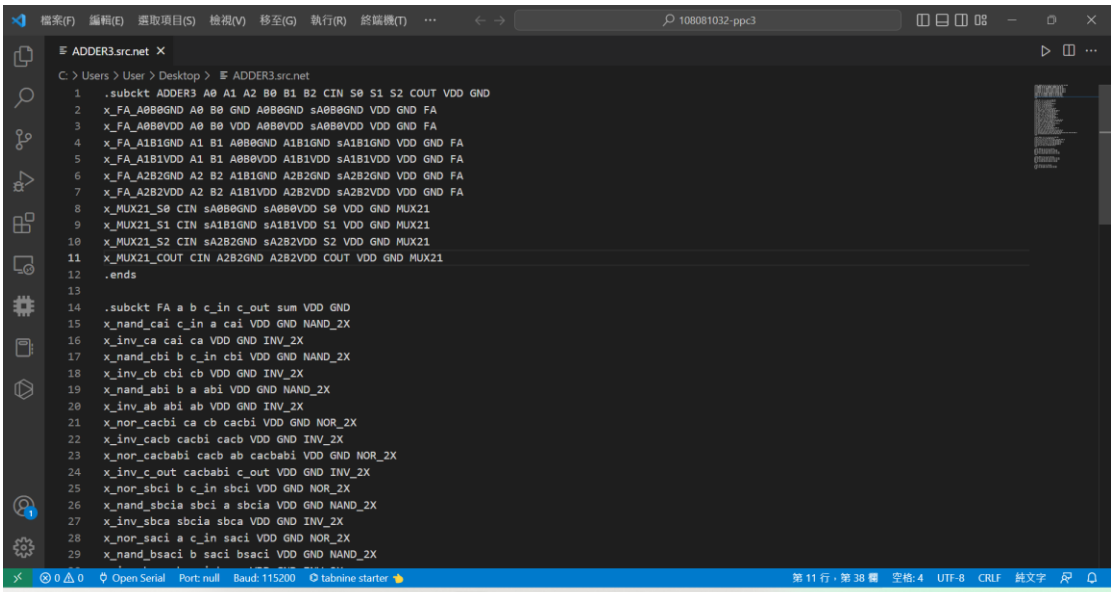
DRC summary report of ADDER3:



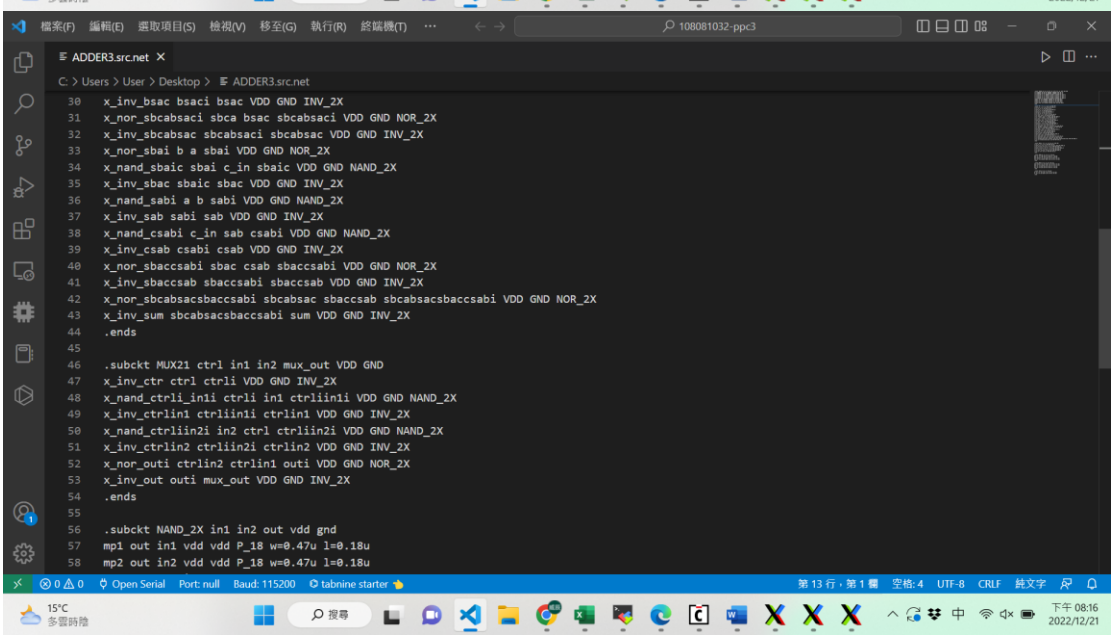
The message of passing LVS of ADDER3:



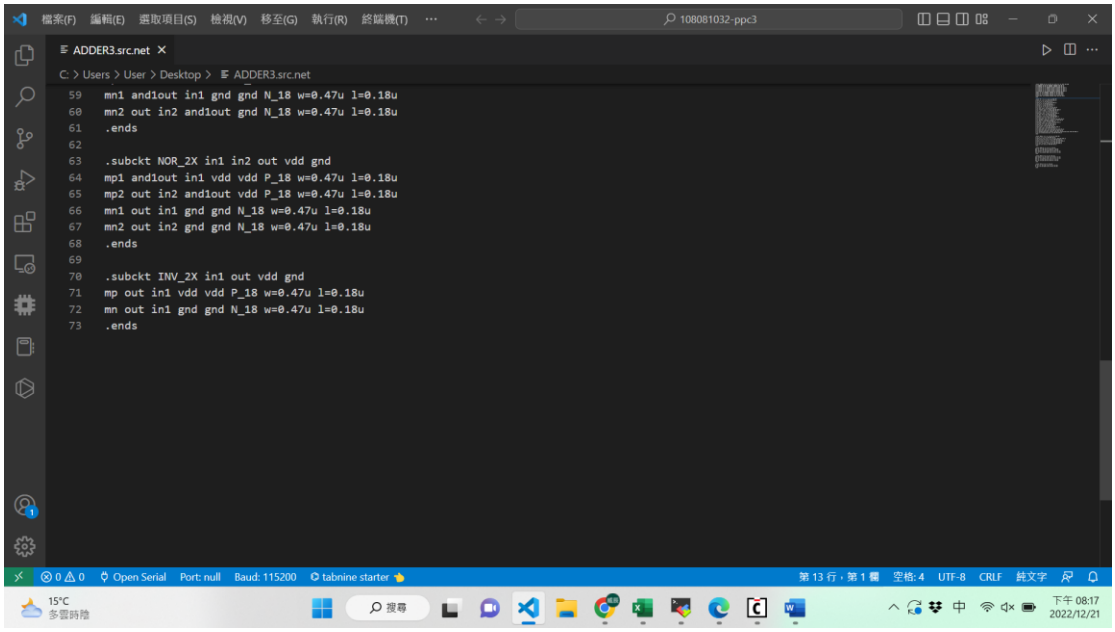
LVS schematic of ADDER3.src.net (screenshot of the text file):



```
.subckt ADDER3 A0 A1 A2 B0 B1 B2 CIN S0 S1 S2 COUT VDD GND
x_FA_A0B0GND A0 B0 GND A0B0GND sA0B0GND VDD GND FA
x_FA_A0B0VDD A0 B0 VDD A0B0VDD sA0B0VDD VDD GND FA
x_FA_A1B1GND A1 B1 A0B0GND A1B1GND sA1B1GND VDD GND FA
x_FA_A1B1VDD A1 B1 A0B0VDD A1B1VDD sA1B1VDD VDD GND FA
x_FA_A2B2GND A2 B2 A1B1GND A2B2GND sA2B2GND VDD GND FA
x_FA_A2B2VDD A2 B2 A1B1VDD A2B2VDD sA2B2VDD VDD GND FA
x_MUX21_S0 CIN sA0B0GND sA0B0VDD S0 VDD GND MUX21
x_MUX21_S1 CIN sA1B1GND sA1B1VDD S1 VDD GND MUX21
x_MUX21_S2 CIN sA2B2GND sA2B2VDD S2 VDD GND MUX21
x_MUX21_COUT CIN A2B2GND A2B2VDD COUT VDD GND MUX21
.ends

.subckt FA a b c_in c_out sum VDD GND
x_nand_cai c_in a cai VDD GND NAND_2X
x_inv_ca cai ca VDD GND INV_2X
x_nand_cbi b c_in cbi VDD GND NAND_2X
x_inv_cb cbi cb VDD GND INV_2X
x_nand_abi b a abi VDD GND NAND_2X
x_inv_ab abi ab VDD GND INV_2X
x_nor_cacbi ca cb cacbi VDD GND NOR_2X
x_inv_cacb cacbi cacb VDD GND INV_2X
x_nor_cacbabi cacb ab cacbabi VDD GND NOR_2X
x_inv_c_out cacbabi c_out VDD GND INV_2X
x_nor_sbci b c_in sbci VDD GND NOR_2X
x_nand_sbcia sbci a sbcia VDD GND NAND_2X
x_inv_sbca sbcia sbca VDD GND INV_2X
x_nor_saci a c_in saci VDD GND NOR_2X
x_nand_bsaci b saci bsaci VDD GND NAND_2X
```



```
x_inv_bsac bsaci bsac VDD GND INV_2X
x_nor_sbcabsaci sbca bsac sbcabsaci VDD GND NOR_2X
x_inv_sbcabsac sbcabsaci sbcabsac VDD GND INV_2X
x_nor_sbai b a sbai VDD GND NOR_2X
x_nand_sbaic sbai c_in sbaic VDD GND NAND_2X
x_inv_sbac sbaic sbac VDD GND INV_2X
x_nand_sabi a b sabi VDD GND NAND_2X
x_inv_sab sabi sab VDD GND INV_2X
x_nand_csabi c_in sab csabi VDD GND NAND_2X
x_inv_csab csabi csab VDD GND INV_2X
x_nor_sbaccsabi sbac csab sbaccsabi VDD GND NOR_2X
x_inv_sbaccsab sbaccsabi sbaccsab VDD GND INV_2X
x_nor_sbcabsacsbaccsabi sbcabsac sbaccsab sbcabsacsbaccsabi VDD GND NOR_2X
x_inv_sum sbcabsacsbaccsabi sum VDD GND INV_2X
.ends

.subckt MUX21 ctrl in1 in2 mux_out VDD GND
x_inv_ctr ctrl ctrli VDD GND INV_2X
x_nand_ctrli_in1i ctrli in1 ctrliin1i VDD GND NAND_2X
x_inv_ctrlin1 ctrliin1i ctrlin1 VDD GND INV_2X
x_nand_ctrliin2i in2 ctrl ctrliin2i VDD GND NAND_2X
x_inv_ctrlin2 ctrliin2i ctrlin2 VDD GND INV_2X
x_nor_outi ctrlin2 ctrlin1 outi VDD GND NOR_2X
x_inv_out outi mux_out VDD GND INV_2X
.ends

.subckt NAND_2X in1 in2 out vdd gnd
mp1 out in1 vdd vdd P_18 w=0.47u l=0.18u
mp2 out in2 vdd vdd P_18 w=0.47u l=0.18u
```



What else did you do to enhance your layout quality?

用 A 去對齊，並且盡可能地將 metal2 縮短以便其他線路也可用 metal2

What have you learned from this homework?

這個作業讓我體會到 layout 真的有夠難畫，要想辦法縮面積又要讓線路好接，總之花了我非常多時間。

What problem(s) have you encountered in this homework?

面積一直縮不小，因為線路要想辦法接順，而且 MUX、FA 的邏輯化簡可能我還要去顯辦法再縮短，總之總面積的部分我還要取學習改進。