**FPGA Implementation document**

**1. Higher level overview and Connections:**

FPGA\_Random\_Walk\_Module can are defnied in bram\_random\_walk.v file (Verilog to be found in github repository), and it can be instantiated into multiple instances depending on how many processing is needed for the application (the following picture shows the 2 FPGA\_Random\_Walk\_Module instantiation)

Diagram

Description automatically generated

The connections to ZCU102 PS is described in section 4.

**2. What and how Data are stored in each BRAM Block:**

The following diagram shows what stores in each BRAM Block. In each BRAM block, seed node is stored from the 0x0 to 0x(K-1) address (K is the number of seed node). From 0xK to 0x(K+2\*N), it stores the first and last neighbour’s address for each node in the subgraph (N is number of nodes in the subgraph). Starting from Ox(K+2\*N + 1), it stores the neighbours for each node in the subgraph.

The following picture shows 3 rectangular boxes and the first box is ranging from 0x0 to 0x(K-1), and the second box ranging is from 0xK to 0x(K+2\*N), and the third box is starting from Ox(K+2\*N+1)

A picture containing text

Description automatically generated

**3. Verilog files and modules:**

Under <https://github.com/lixali/FPGA_PPR/tree/master/FPGA/ultra96_random_walk/>, the following Verilog files are created and used to constructed the above circuits.

*BRAM.v (module definition of BRAM block)*

*Clock\_divider.v (clock divider modulethat make main clocks into various clocks with various frequency)*

*LFSR.v (linear feedback shift register to mimic generating random numbers in FPGA)*

*BRAM\_random\_walk.v (random walk module that read data from BRAM and calculate the counter table)*

**4. Simulations Waveform**

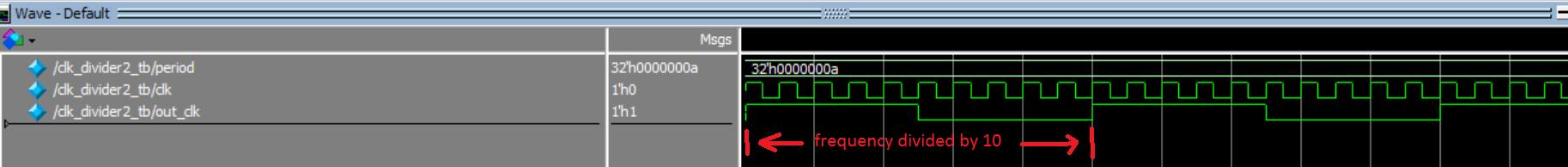
The following waveforms the simulations result from various block (all test bench files are committed to the same directory as the verilog module files)

BRAM basic read and write simulation

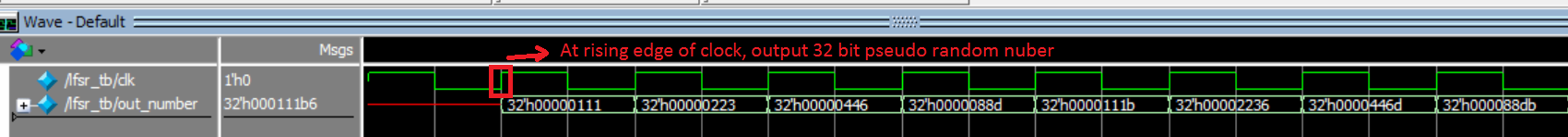
A picture containing graphical user interface

Description automatically generated

Clock frequency divider (clock\_divider.v)



Linear Feedback Shift Register (lfsr.v)



Modelsim simulation project (modelsim is running faster in simulation than vivado; But synthesis is still done is vivado)

Graphical user interface, text, application, Word

Description automatically generated

Simulation waveform of BRAM\_random\_walk module (bram\_random\_walk.v)

A screenshot of a computer

Description automatically generated

**4. Connections to zcu102’s PS**