

Computer Architecture and Design Practical 1 – RISC-V ALU Design

Preparing your submission

October 2019

The submission for practical 1 should consist of a signed lab sheet stapled on top of a brief written report, with a listing of your Verilog code at the back. There is no hard limit on the length of the report, but it will typically require no more than 4 sides of A4.

The entire practical is marked out of 30 and is worth 30% of the practical marks for this course. Up to 10 marks are allocated in class, comprising 1 mark for each ticked check-box on the lab sheet. The remaining 20 marks are allocated for the write-up.

The writeup should be in two main parts, firstly to explain the *operation of your design*, and secondly to present a *quantitative evaluation of the design* in terms of timing and resource utilization. Each of these parts is worth up to 6 marks. The first part should explain how each ALU operation works and should give the rationale for any design decisions you made. The second part should:

- give the critical path through your design, and explain which of the 10 operations are implemented by that path (3 marks)
- tabulate the resource utilization on the FPGA for your design (3 marks)

The remaining 8 marks are allocated for an assessment of code quality (which is why it is important that you submit a listing). Among the criteria considered in assessing code quality are: clarity, appropriate use of language constructs, brevity, indentation, appropriate and informative use of comments.