Computer Architecture and Design Practical 1 Lab Sheet
October 2019

Name	Matric No.

Part (a) – Designing and Simulating an ALU module

☐ Logical operations passing tests ☐ Add, subtract operations passing tests ☐ Set operations passing tests ☐ Shift operations passing tests ☐ At least 10,000 tests run
Demonstrator Signature
Demonstrator Comments

Part (b) – Synthesising the ALU Module

☐ Synthesis completes without error ☐ No inferred latches ☐ No combinational loops ☐ Critical path has been demonstrated, and is less than 20ns ☐ FPGA resource utilization has been demonstrated
Demonstrator Signature
Demonstrator Comments

Attach this lab sheet as the cover page to your report before handing to ITO before the deadline. Please ensure you include a listing of the Verilog code for your ALU design.