Computer Architecture and Design – Practical 2
Dependency Checking and Data Forwarding

Preparing your submission

October 2019

The submission for practical 2 should consist of a signed lab sheet stapled on top of a brief written report, with a listing of your Verilog code at the back. There is no hard limit on the length of the report, but it will typically require no more than 5 sides of A4.

The entire practical is marked out of 35 and is worth 35% of the practical marks for this course. Up to 15 marks are allocated in class, comprising 5 marks for each of parts (a), (b) and (c) that are signed off on the lab sheet. The remaining 20 marks are allocated for the write-up.

The writeup should have one section per part, and cover two aspects for each part; firstly to explain the *operation of your design*, and secondly to present a *quantitative evaluation of the design*. The evaluation should cover aspects such as CPI measurements, benchmark timings, and resource utilization of the design on the FPGA.

Of the 20 marks for the writeup, 7 are allocated for Part (a), 7 are allocated for Part (b) and 6 are allocated for Part (c). The overall mark allocation summary is shown below in Table 1.

		Part (a)	Part (b)	Part (c)	Total
Signed labsheet		5	5	5	15
Written report					
	Explain the design	2	2	3	7
	Evaluate the design	3	3	3	9
	Code quality	2	2	-	4
Total		12	12	11	**35**

Table 1: Allocation of marks for Parts (a), (b) and (c)

Among the criteria considered in assessing the quality of your explanation are: clarity and completeness of your explanation.

Among the criteria considered in assessing the quality of your evaluation are: inclusion of all relevant aspects of evaluation, such as CPI, actual execution time, critical paths and extracts from timing reports, and extracts from resource utilisation reports.

Among the criteria considered in assessing code quality are: clarity, appropriate use of language constructs, brevity, indentation, appropriate and informative use of comments.