

## BLG222E Computer Organization

### Project 3

Due Date: 17.05.2017

Design a **hardwire-control unit** for the following architecture. Use the structure that you have designed in project #2.

#### Instruction format

There are two types of instructions as described below.

(1) Instructions with address reference has the format shown in Figure 1:

- The OPCODE is a 5-bit field (See Table 1 for the definition).
- The REGSEL is a 2-bit field (See left side of Table 2 for the definition).
- The ADDRESSING MODE is a 1-bit field (See Table 3 for the definition).
- The ADDRESS is 8 bits

OPCODE	REGSEL	ADDRESSING MODE	ADDRESS
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*Figure 1: Instructions with an address reference*

(2) Instructions without address reference has the format shown in Figure 2:

- The OPCODE is a 5-bit field (See Table 1 for the definition).
- DESTREG is a 3-bit field which specifies the destination register (See right side of Table 2 for the definition).
- SRCREG1 is a 3-bit field which specifies the first source register (See right side of Table 2 for the definition).
- SRCREG2 is a 3-bit field which specifies the second source register (See right side of Table 2 for the definition).

OPCODE	DESTREG	SRCREG1	SRCREG2
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*Figure 2: Instructions without an address reference*

*Table 1: OPCODE field and SYMBols for opertions and their descriptions*

OPCODE (HEX)	SYMB	ADDRESSING MODE	DESCRIPTION
0x00	LD	IM, D	$R_x \leftarrow \text{Value}$ (Value is described in Table 3)
0x01	ST	D	$\text{Value} \leftarrow R_x$
0x02	MOV	N/A	$\text{DESTREG} \leftarrow \text{SRCREG1}$
0x03	PSH	N/A	$M[\text{SP}] \leftarrow R_x, \text{SP} \leftarrow \text{SP} - 1$
0x04	PUL	N/A	$\text{SP} \leftarrow \text{SP} + 1, R_x \leftarrow M[\text{SP}]$
0x05	ADD	N/A	$\text{DESTREG} \leftarrow \text{SRCREG1} + \text{SRCREG2}$
0x06	SUB	N/A	$\text{DESTREG} \leftarrow \text{SRCREG2} - \text{SRCREG1}$
0x07	DEC	N/A	$\text{DESTREG} \leftarrow \text{SRCREG1} - 1$
0x08	INC	N/A	$\text{DESTREG} \leftarrow \text{SRCREG1} + 1$
0x09	AND	N/A	$\text{DESTREG} \leftarrow \text{SRCREG1} \text{ AND } \text{SRCREG2}$
0x0A	OR	N/A	$\text{DESTREG} \leftarrow \text{SRCREG1} \text{ OR } \text{SRCREG2}$
0x0B	NOT	N/A	$\text{DESTREG} \leftarrow \text{NOT SRCREG1}$
0x0C	LSL	N/A	$\text{DESTREG} \leftarrow \text{LSL SRCREG1}$
0x0D	LSR	N/A	$\text{DESTREG} \leftarrow \text{LSR SRCREG1}$
0x0E	BRA	IM	$\text{PC} \leftarrow \text{Value}$
0x0F	BEQ	IM	IF $Z=1$ THEN $\text{PC} \leftarrow \text{Value}$
0x10	BNE	IM	IF $Z=0$ THEN $\text{PC} \leftarrow \text{Value}$
0x11	CALL	IM	$M[\text{SP}] \leftarrow \text{PC}, \text{SP} \leftarrow \text{SP} - 1, \text{PC} \leftarrow \text{Value}$
0x12	RET	N/A	$\text{SP} \leftarrow \text{SP} + 1, \text{PC} \leftarrow M[\text{SP}]$

*Table 2: REGSEL (Left) and DESTREG/SRCREG1/SRCREG2 (Right) select the register of interest for a particular instruction*

REGSEL	REGISTER	DESTREG/SRCREG1/SRCREG2	REGISTER
00	R0	000	R0
01	R1	001	R1
10	R2	010	R2
11	R3	011	R3
		100	PC
		101	PC
		110	AR
		111	SP

Table 3: Addressing modes

ADDRESSING MODE	MODE	SYMB	Value
0	Immediate	IM	ADDRESS Field
1	Direct	D	M[AR]

**Example Code:**

The code given below adds data that are stored at M[A0]+M[A1]+M[A2]+M[A3]+M[A4] and stores the total at M[A5]. It is written as a loop that iterates 5 times.

ORG 0x20	# Write the program starting from the address 0x20
LD R0 IM 0x05	# R0 is used for iteration number
LD R1 IM 0x00	# R1 is used to store total
LD R2 IM 0xA0	
MOV AR R2	# AR is used to track data address: starts from 0xA0
LABEL: LD R2 D	# R2 <- M[AR] (AR = 0xA0 to 0xA4)
INC AR AR	# AR <- AR + 1 (Next Data)
ADD R1 R1 R2	# R1 <- R1 + R2 (Total = Total + M[AR])
DEC R0 R0	# R0 <- R0 - 1 (Decrement Iteration Counter)
BNE IM LABEL	# Go back to LABEL if Z=0 (Iteration Counter > 0)
INC AR AR	# AR <- AR + 1 (Total will be written to 0xA5)
ST R1 D	# M[AR] <- R1 (Store Total at 0xA5)