# H264 High Profile Decoder 2.0 on HDVICP2 and Media Controller Based Platform Data Sheet

## FEATURES

- Supports all features of Main Profile(MP) and High Profile (HP)
- Supports resolutions up to 4320 x 4096
- Supports progressive, interlaced, Picture Adaptive Frame Field (PicAFF) and Macro-block Adaptive Frame Field (MBAFF) type picture decoding
- Supports multiple slices and multiple reference frames
- Supports CAVLC and CABAC decoding
- Supports all intra prediction and inter prediction modes
- Supports up to 16 MV per MB
- Supports frame based decoding
- Supports picture width and height (resolutions) greater than 64 pixels including all standard resolutions. In case of high resolution(Max Width or Max Height in create time parameters is more than 2048), the minimum supported picture width is 336 pixels.
- Tested for compliance with JM version 10.1 reference decoder
- Supports reference picture list reordering
- Supports PCM macroblock decoding
- Supports graceful exit and error reporting under error conditions
- Supports error concealment
- Supports parse header functionality
- Supports access to parsed Supplemental Enhancement Information (SEI) and Video Usability Information (VUI) data
- Supports memory management and control operations (MMCO)
- Supports gaps in frame number
- Supports skip functionality
- Supports dynamic change in resolution
- Supports configurable display delay for low delay applications
- Supports low DDR footprint in closed loop scenario
- Supports low latency features – sub frame level synchronization for input and output. Input data synchronization is based upon slices and fixed length of bit-stream and output data synchronization is based on MB rows.
- Supports decoding of one frame each of multiple channels in a single process call
- Supports dual YUV dump
- Limited support for decoding of Scalable Video Coding (SVC) streams
- Supports parsing of stereo SEI and frame packing SEI
- Supports decrypting of embedded watermark in closed loop scenario
- Supports decoding of only specific frame types requested by user. User can choose decoding of only I/IDR, IP or all frame types.
- The other explicit features that TI's H.264 Decoder supports are
  - eXpressDSP Digital Media (XDM IVIDDEC3) interface compliant
  - Multiple instances of the decoder can be run simultaneously
  - Supports booting of HDVICP2
  - Implements different power optimization schemes
  - Supports YUV 420 semi-planar color subsampling format
  - Independent of any operating system
  - Ability to get plugged in any multimedia frameworks (eg. Codec Engine, OpenMax, GStreamer, etc)

PRODUCT PREVIEW

## Description

H.264 is the latest video compression standard from the ITU-T Video Coding Experts Group and the ISO/IEC Moving Picture Experts Group. This H.264 Decoder is validated on HDVICP2 and Media Controller based platform with code generation tools version 4.5.1 for HDVIPCP2 processor and code generation tools version 5.0.3 for Media controller processor.

## Performance and Memory Summary

This section describes the performance and memory usage of H.264 High Profile Decoder.

**Table 1 Configuration Table**

| CONFIGURATION | ID |
|---|---|
| H.264 High Profile Universal Decoder: Resolutions up to 1920 x 1080 | H264_DEC_001 |
| H.264 High Profile Universal Decoder: Resolutions between 2048 x 2048 and 4320 x 4096 | H264_DEC_002 |
| H.264 High Profile Universal N-Channel Decoder: Resolutions up to 1280 x 720, 4 channels are decoded with the same input for all the channels | H264_DEC_003 |
| H.264 High Profile Universal Decoder: Resolutions - 1920 x 1080 and 4096 x 4096 with decoding only I/IDR and IP frame types | H264_DEC_004 |
| H.264 High Profile Universal Decoder: Resolutions - 1920 x 1080 and 4096 x 4096 with decoding only I/IDR frame types | H264_DEC_005 |

**Table 2 Cycles Information - Profiled on DM816x REV-A2 EVM with Code Generation Tools Version 5.0.3**

| CONFIGURATION ID | HDVICP2 PERFORMANCE STATISTICS (MEGA CYCLES PER SECOND) (1) | | |
|---|---|---|---|
| | TEST DESCRIPTION (2) | AVERAGE(3) | PEAK(4) |
| H264_DEC_001 | mobcal_p640x360_1mbps_IPB_30fps.264 | 22.25 | 23.34 |
| | akiyo_p640x480_100kbps_IPP_30fps.264 | 29.45 | 29.71 |
| | lambo_p720x480_2mbps_IPB_30fps.264 | 30.52 | 31.54 |
| | cvmpMot_i720x480_3mbps_IPB_30fps.264 | 32.30 | 36.76 |
| | mov817_p1280x720_5mbps_IPB_30fps.264 | 71.79 | 73.88 |
| | station_p1920x1080_7mbps_IPB_30fps.264 | 155.67 | 160.63 |
| | station_i1920x1080_9mbps_IPB_30fps.264 | 160.63 | 166.87 |
| H264_DEC_002 | sample_p4096x2048_38mbps_IPB_30fps.264 | 621.78 | 632.20 |
| | bbccrowded_i4096x2320_47mbps_IPB_30fps.264 | 705.79 | 730.83 |
| | vqeghd1_src01_original_p4096x4096_25mbps_IPP_30fps.264 | 1239.75 | 1300.06 |
| | airshow_p4320x2048_35mbps_IPB_30fps.264 | 676.93 | 731.52 |
| H264_DEC_003 | foreman_p352x288_512kbps_IPB_30fps_4Ch.264 | 48.66 | 50.71 |
| | mobcal_p640x360_1mbps_IPB_30fps_4Ch.264 | 87.06 | 91.83 |
| | akiyo_p640x480_100kbps_IPP_30fps_4Ch.264 | 112.66 | 113.81 |
| | lambo_p720x480_2mbps_IPB_30fps_4Ch.264 | 117.97 | 121.61 |
| | campMot_i720x480_3mbps_IPBB_30fps_4Ch.264 | 129.28 | 143.28 |
| | mov817_p1280x720_5mbps_IPB_30fps_4Ch.264 | 285.25 | 296.23 |
| H264_DEC_004 | station_p1920x1080_12Mbps_IPP_30fps.264 | 156.88 | 163.62 |
| | station_i1920x1080_16Mbps_IPP_30fps.264 | 164.25 | 168.56 |
| | vqeghd1_csrc12_original_p4096x4096_30Mbps_IPP_30fps.264 | 1251.08 | 1300.76 |
| | vqeghd1_csrc12_original_i4096x4096_44Mbps_IPP_30fps.264 | 1259.57 | 1305.34 |
| H264_DEC_005 | station_p1920x1080_9Mbps_IIII_30fps.264 | 164.05 | 164.15 |
| | station_i1920x1080_12Mbps_IIII_30fps.264 | 169.32 | 169.41 |
| | vqeghd1_csrc12_original_p4096x4096_76Mbps_III_30fps.264 | 1301.10 | 1301.29 |
| | vqeghd1_csrc12_original_i4096x4096_98Mbps_III_30fps.264 | 1306.12 | 1306.35 |



(1) Measured on DM816x REV-A2 EVM having Cortex-A8 @ 1GHz, HDVICP2 @ 533MHz, Media Controller @ 250 MHz, L3 interconnect @ 500 MHz and DDR2 @ 400 MHz and there could be a variation of around 1-2% in the numbers.
   a) Media Controller code is placed in cacheable memory region in DDR.
   b) No latency from system at process call and processing unit as frame (no sub-frame level communication) is assumed.
   c) All Luma 2D Video buffers of codec being in TILED_8 Bit Memory and all Chroma 2D Video buffers of codec being in TILED_16 Bit Memory
(2) Cycles have been measured across process call.
(3) Intra frame period is 30, number of slices per picture is 1, frame rate is 30 fps.
(4) Average is computed based on worst case cycles having 2 extra output frame buffers.
(5) Peak is based on worst case cycles having no extra output frame buffer. It is computed as peak among 30 frames.

**Table 3 Memory Statistics of Media Controller - Generated with Code Generation Tools Version 5.0.3**

| CONFIGURATION ID | RESOLUTION | MEMORY STATISTICS[1] | | | | | | | TOTAL |
|---|---|---|---|---|---|---|---|---|---|
| | | PROGRAM MEMORY | DATA MEMORY | | | | | | |
| | | | INTERNAL | EXTERNAL[2] | | | | STACK | |
| | | | | PERSISTENT[3] | | | CONST | | |
| | | | | TILED8 (numBufs x Width x Height) | TILED16 (numBufs x Width x Height) | TILED PAGE / RAW | RAW | | |
| H264_DEC_001 | Level 3.0 – 720x480 | 20 | 0 | 0 | 0 | 2311 | 520 | 2 | 2853 |
| | Level 4.1 – 720x480 | 20 | 0 | 0 | 0 | 5053 | 520 | 2 | 5595 |
| | Level 4.1 – 1280x720 | 20 | 0 | 0 | 0 | 7704 | 520 | 2 | 8246 |
| | Level 4.1 – 1920x1080 | 20 | 0 | 0 | 0 | 8679 | 520 | 2 | 9221 |
| | Level 5.0 – 1920x1080 | 20 | 0 | 0 | 0 | 23596 | 520 | 2 | 24138 |
| | Level 5.0 – 2048x2048 | 20 | 0 | 0 | 0 | 23687 | 520 | 2 | 24229 |
| | Level 5.1 – 1920x1080 | 20 | 0 | 0 | 0 | 28569 | 520 | 2 | 29111 |
| | Level 5.1 – 2048x2048 | 20 | 0 | 0 | 0 | 40327 | 520 | 2 | 40869 |
| H264_DEC_002 | Level 5.1 – 4096x2048 | 20 | 0 | 0 | 0 | 40327 | 520 | 2 | 40869 |
| | Level 5.1 – 4096x4096 | 20 | 0 | 0 | 0 | 40327 | 520 | 2 | 40869 |
| | Level 5.1 – 4320x4096 | 20 | 0 | 0 | 0 | 42511 | 520 | 2 | 43053 |
| H264_DEC_004 | Level 4.1 – 1920x1080 | 20 | 0 | 0 | 0 | 392 | 520 | 2 | 934 |
| | Level 5.1 – 4096x4096 | 20 | 0 | 0 | 0 | 13702 | 520 | 2 | 14244 |
| H264_DEC_005 | Level 4.1 – 1920x1080 | 20 | 0 | 0 | 0 | 392 | 520 | 2 | 934 |
| | Level 5.1 – 4096x4096 | 20 | 0 | 0 | 0 | 13702 | 520 | 2 | 14244 |

(1) All memory requirements are expressed in kilobytes (1 K-byte = 1024 bytes) and there might be rounding to next integer K-byte. Stack can be kept in internal/external memory, negligible performance impact can be observed in Media Controller cycles if it is placed in external memory.

(2) Codec's request of memory container can be over-ridden by application, adhering to the below rules
   a. TILED PAGE can be overridden by RAW
   b. TILED8, TILED16 can be overridden by TILED PAGE, RAW
   c. TILED16 can be overridden by TILED8, RAW, TILED PAGE

   However, in case of overriding of 2B and 2C, there can be some performance impact.

(3) Persistent memory is instance specific and does not include I/O buffers.

(4) For N-channel case, the persistent memory requirement (TILEDPAGE/RAW) should be computed as the sum of the memory requirement for the individual channels.

**Table 4 Split-up of Media Controller Internal Data Memory Statistics**

| CONFIGURATION ID | DATA MEMORY - INTERNAL(1) | | |
|---|---|---|---|
| | SHARED | | INSTANCE |
| | CONSTANTS | SCRATCH | |
| H264_DEC_001, H264_DEC_002, H264_DEC_003, H264_DEC_004, H264_DEC_005 | 0 | 0 | 0 |

(1) Internal memory refers to on chip memory. If the system doesn't have enough internal memory, then external memory can also be used. Memory requirements are expressed in kilobytes.

**Notes**

- I/O buffers:
  - Input buffer size = 1000 KB (average case for 1920x1088)
  - Output buffer size = 3441 KB (for 1920x1088 resolution)
- None of the buffers at input and output level is accessed by Media Controller processor hence the data should be valid in DDR (not in cache)
- Total data memory for N non pre-emptive instances = Constants + Runtime Tables + Scratch + N * (Instance + I/O buffers + Stack)
- Total data memory for N pre-emptive instances = Constants + Runtime Tables + N * (Instance + I/O buffers + Stack + Scratch)
- MAIL BOX FIFO #0 and #1 are used and user numbering for Media Controller as 2 and for HDVICP2 as 3 is assumed
- It is assumed that RTS library from ARM is available in system because few symbols like memcpy are used in codec
- All constants and Input/Output Buffers to decoder are assumed to be in VDMA addressable space in DDR

**References**

- ISO/IEC 14496-10:2005 Information technology -- Coding of audio-visual objects -- Part 10: Advanced Video Coding
- eXpressDSP Algorithm Interoperability Standard (TMS320 Algorithm Interface Standard)
- H.264 High Profile Decoder on HDVICP2 and Media Controller Based Platform User's Guide (Literature Number: SPRUGN9)

## Glossary

| Term | Description |
|---|---|
| Constants | Elements that go into .const memory section |
| Scratch | Memory space that can be reused across different instances of the algorithm |
| Shared | Sum of Constants and Scratch |
| Instance | Persistent-memory that contains persistent information - allocated for each instance of the algorithm |

## Acronyms

| Acronym | Description |
|---|---|
| AIR | Adaptive Intra Refresh |
| CIF | Common Intermediate Format |
| CPB | Coded Picture Buffer |
| D1 | SDTV image resolution (720x480) |
| QCIF | Quarter Common Intermediate Format |
| ISO | International Organization for Standardization |
| ITU | International Telecommunication Union |
| VDMA | Video Direct Memory Access |
| SDTV | Standard Definition Television |
| SEI | Supplemental Enhancement Information |
| VUI | Video Usability Information |
| XDAIS | eXpressDSP Algorithm Interface Standard |
| XDM | eXpressDSP Digital Media |
| VGA | Video Graphics Array (640x480 resolution) |

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have not been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

| **Products** | | **Applications** | |
|---|---|---|---|
| Audio | www.ti.com/audio | Automotive & Transportation | www.ti.com/automotive |
| Amplifiers | amplifier.ti.com | Communications & Telecom | www.ti.com/communications |
| Data Converters | dataconverter.ti.com | Computers & Peripherals | www.ti.com/computers |
| DLP® Products | www.dlp.com | Consumer Electronics | www.ti.com/consumer-apps |
| DSP | dsp.ti.com | Energy and Lighting | www.ti.com/energyapps |
| Clocks and Timers | www.ti.com/clocks | Industrial | www.ti.com/industrial |
| Interface | interface.ti.com | Medical | www.ti.com/medical |
| Logic | logic.ti.com | Security | www.ti.com/security |
| Power Mgmt | power.ti.com | Space, Avionics & Defense | www.ti.com/space-avionics-defense |
| Microcontrollers | microcontroller.ti.com | Video & Imaging | www.ti.com/video |
| RFID | www.ti-rfid.com | | |
| OMAP Applications Processors | www.ti.com/omap | **TI E2E Community** | e2e.ti.com |
| Wireless Connectivity | www.ti.com/wirelessconnectivity | | |

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265