MPEG2 Decoder (v01.00.15.01) on HDVICP2 and Media Controller Based Platform

FEATURES

- **Supports up to High level of Main Profile (MP)**
- **Supports decoding of MPEG1 constrained video streams**
- **Supports progressive and interlaced type picture decoding**
- **Supports P and B frames**
- **Supports optional out-of-loop deblocking**
- **Supports error concealment while decoding erroneous streams**
- **Supports picture width and height (resolutions) greater than 64 pixels including all standard resolutions up to 2048x2048**
- **Graceful exit under error conditions is supported**
- **Has logic and checks to help application to support trick mode playback**
- **Return of macroblock properties is supported in transcode mode**
- **Does not support sub frame level data synchronization**
- **The other explicit features that TI's MPEG2 Decoder supports are**
  - **eXpressDSP Digital Media (XDM IVIDDEC3) interface compliant**
  - **Supports multi-channel functionality**
  - **Supports booting of HDVICP2**
  - **Implements different Power optimization schemes**
  - **Supports YUV420 semi planar color sub-sampling formats**
  - **Independent of any operating system**
  - **Ability to get plugged in any multimedia frameworks (eg. Codec Engine, OpenMax, GStreamer etc)**

DESCRIPTION

MPEG-2 is an international standard for video compression. This standard is defined in the ISO/IEC-13838-2 document. This MPEG2 is validated on the HDVICP2 and Media Controller Based Platform with Code Composer Studio version 4.2.0.09000 and code generation tools version 4.5.1 for HDVICP2 and code generation tools version 5.0.3 for Media Controller.

PRODUCT PREVIEW

Performance and Memory Summary

This section describes the performance and memory usage of the MPEG2 Decoder

Table 1 Configuration Table

CONFIGURATION	ID
MPEG-2 Main Profile Decoder (supports up to High level)	MPEG2_DEC_001
MPEG-2 Main Profile Decoder (supports up to High level) with optional out-of-loop deblocking ON (`outloopDeBlocking` field in IMPEG2VDEC_Params is set to 3)	MPEG2_DEC_002

Table 2 Cycles Information - Profiled on DM816x REV-A2 EVM with Code Generation Tools Version 4.5.1 for HDVICP2 and Version 5.0.3 for Media Controller.

CONFIGURATION ID	HDVICP2 PERFORMANCE STATISTICS (MEGA CYCLES PER SECOND) (1)		
	TEST DESCRIPTION	AVERAGE(2)	PEAK(3)
MPEG2_DEC__001	Motion1_640x360_P_1385kbps_420P_IPP.mpv	14.65	14.84
	LAMBORGHINI_640x480_P_2Mbps_420P_IPB_MPEG1.mpv	18.19	20.00
	office_720x480_P_2Mbps_420P_IPB.mpv	20.00	21.57
	ParkJoy_1280x720_P_5.3mbps_420P_IPB.mpv	48.93	52.10
	5D2_PORTRAIT_1920x1080_P_10Mbps_420P_IPB.mpv	109.00	112.77
	stockholm_720x480_I_2Mbps_420P_IPB.mpv	23.90	26.76
	RALLI_1920x1080_I_28mbps_420P_IPB.mpv	123.83	136.36
MPEG2_DEC__002	Motion1_640x360_P_1385kbps_420P_IPP.mpv	20.28	20.73
	LAMBORGHINI_640x480_P_2Mbps_420P_IPB_MPEG1.mpv	26.35	26.47
	office_720x480_P_2Mbps_420P_IPB.mpv	28.24	28.66
	ParkJoy_1280x720_P_5.3mbps_420P_IPB.mpv	69.78	70.16
	5D2_PORTRAIT_1920x1080_P_10Mbps_420P_IPB.mpv	154.75	154.83
	stockholm_720x480_I_2Mbps_420P_IPB.mpv	28.80	29.80
	RALLI_1920x1080_I_28mbps_420P_IPB.mpv	155.89	158.72

(1) Measured on DM816x REV-A2 EVM having Cortex-A8 @ 1GHz, HDVICP2 @ 533MHZ, Media Controller @ 250 MHZ, L3 interconnect @ 500 MHZ and DDR2 @ 400 MHZ and there could be a variation of around 1-2% in the numbers.
   a) Media Controller code is placed in cacheable memory region in DDR.
   b) No Latency from system at process call and processing unit as frame (no sub-frame level communications) is assumed.
   c) All Luma 2D Video buffers of codec being in TILED_8 Bit Memory and all Chroma 2D Video buffers of codec being in TILED_16 Bit Memory

(2) It is computed based on worst case cycles having 2 extra output frame buffer. Average is calculated @ 30fps

(3) It is based on worst case cycles having no extra output frame buffer. It is computed based on peak among 30 frames @ 30fps.

Table 3 Memory Statistics of Media Controller - Generated with Code Generation Tools Version 5.0.3

CONFIGURATION ID	RESOLUTION	MEMORY STATISTICS[1]							
		PROGRAM MEMORY	DATA MEMORY						TOTAL
			INTERNAL	EXTERNAL[2]				STACK	
				PERSISTENT[3]			CONST		
				TILED8 (numBufs x Width x Height)	TILED16 (numBufs x Width x Height)	TILED PAGE / RAW	RAW		
MPEG2_DEC_001	All	21	0	0	0	1.5	412	2	436.5
MPEG2_DEC_002	352x288	21	0	3x354x290	3x354x146	1.5	412	2	888.7
	720x480	21	0	3x722x482	3x722x242	1.5	412	2	1967.9
	1920x1088	21	0	3x1922x1090	3x1922x546	1.5	412	2	9648.6

(1) All memory requirements are expressed in kilobytes (1 K-byte = 1024 bytes) and there might be rounding to next integer K-byte. Stack can be kept in internal/external memory, negligible performance impact can be observed in Media Controller cycles if it is placed in external memory

(2) Codec's request of memory container can be over-ridden by application, adhering to the below rules
   a. TILED PAGE can be overridden by RAW
   b. TILED8, TILED16 can be overridden by TILED PAGE, RAW
   c. TILED16 can be overridden by TILED8, RAW, TILED PAGE

   However, in case of overriding of 2B and 2C, there can be some performance impacts

(3) Persistent memory is instance specific and does not include I/O buffers.

Table 4 Split-up of Media Controller Internal Data Memory Statistics

CONFIGURATION ID	DATA MEMORY - INTERNAL[1]		
	SHARED		INSTANCE
	CONSTANTS	SCRATCH	
MPEG2_DEC_001/ MPEG2_DEC_002	0	0	0

(1) Internal memory refers to on chip memory. If the system doesn't have enough internal memory, then external memory can also be used. Memory requirements are expressed in kilobytes.

Notes

- I/O buffers:
  - Input buffer size = 2040 K-bytes (for 1920x1088 resolution, YUV420)
  - Output buffer size = 3070.7 K-bytes (for decoding 1920x1088 resolution)
- None of the buffers at input and output level is accessed by Media Controller processor hence the data should be valid in DDR (not in cache). This is not valid incase of decoding erroneous frames with outloopDeblocking enabled, where the output buffer is accessed by Media Controller processor and the valid data might be in cache not in DDR.
- Total data memory for N non pre-emptive instances = Constants + Runtime Tables + Scratch + N * (Instance + I/O buffers + Stack)
- Total data memory for N pre-emptive instances = Constants + Runtime Tables + N * (Instance + I/O buffers + Stack + Scratch)
- MAIL BOX FIFO #0 and #1 are used and user numbering for Media Controller as 2 and for HDVICP2 as 3 is assumed
- It is assumed that RTS library from ARM is available in system because few symbols like memcpy, div are used in codec
- All constants and Input Output Buffer to decoder is assumed in vDMA addressable space in

DDR

References

- ISO/IEC-13838-2: MPEG-2 Standard Specification
- eXpressDSP Algorithm Interoperability Standard (TMS320 Algorithm Interface Standard)
- MPEG-2 Decoder on HDVICP2 and Media Controller Based Platform User's Guide

Glossary

Term	Description
Constants	Elements that go into .const memory section
Scratch	Memory space that can be reused across different instances of the algorithm
Shared	Sum of Constants and Scratch
Instance	Persistent-memory that contains persistent information - allocated for each instance of the algorithm

Acronyms

Acronym	Description
CCITT	Committee Consultative International Telephone and Telegraph
DCT	Discrete Cosine Transform
DSP	Digital Signal Processing
HDTV	High Definition Television
IEC	International Electrotechnical Commission
ISO	International Organization for Standardization
ITU	International Telecommunication Union
MPEG	Motion Picture Experts Group
XDM	eXpressDSP Digital Media

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products	
Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications	
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Transportation and Automotive	www.ti.com/automotive
Video and Imaging	www.ti.com/video
Wireless	www.ti.com/wireless-apps

TI E2E Community Home Page e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265