DIGITAL LOGIC SPECIFICATIONS

Table 7.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Units
Input Voltage High	V_{IH}		1.4			V
Input Voltage Low	V_{IL}				0.70	V
Output Voltage High	V_{OH}	I_{OH} = −100 µA	2.3			V
Output Voltage Low	V_{OL}	I_{OL} = 100 µA			0.2	V
Serial Clock Period	t_{CLK}		38			ns
Setup Time Between Data and Rising Edge of SCLK	t_{DS}		8			ns
Hold Time Between Data and Rising Edge of SCLK	t_{DH}		8			ns
Setup Time Between Falling Edge of $\overline{CS}$ and SCLK	t_S		10			ns
Hold Time Between Rising Edge of $\overline{CS}$ and SCLK	t_H		10			ns
Minimum Period for SCLK to Be in a Logic High State	t_{HIGH}		10			ns
Minimum Period for SCLK to Be in a Logic Low State	t_{LOW}		10			ns
Maximum Delay Between Falling Edge of SCLK and Output Data Valid for a Read Operation	t_{ACCESS}				231	ns
Maximum Delay Between $\overline{CS}$ Deactivation and SDIO Bus Return to High Impedance	t_Z				5	ns

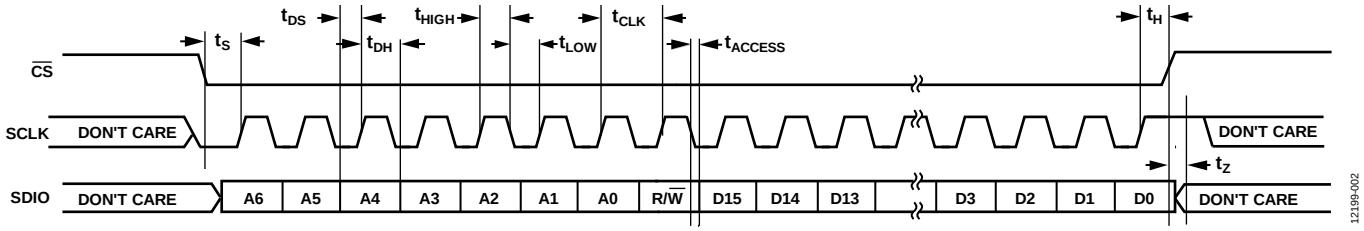

Figure 2. Setup and Hold Timing Measurements