RX Board Pin Assignments

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| CPLD | | | PCB | On-board Device | |  |
| Module | Pin | Pin Loc | Net | Chip | Pin | Pin Loc |
| ADRF\_brg | spi0\_spck | G8 | SPISCK | ATSAMG55 (SPI0) | PB0 | U54.37 |
| spi0\_npcs0 | B1 | **RESET\_M** | PA15 | U54.56 |
| spi0\_mosi | H4 | TXD0 **TP** | PA10/TXD0 | U54.48 |
| spi0\_miso | H5 | RXD0 **TP** | PA9/RXD0 | U54.49 |
| ADRF\_brg | ad\_spi\_cs | B8 | SPI0\_CS | ARF6612 | CS | U65.19 |
| ad\_spi\_sclk | B7 | SPI0\_SPCK | SCLK | U65.18 |
| ad\_spi\_sdio | B2 | SPI0\_MISO | SDIO | U65.17 |
| TS\_brg | spi5\_spck | F8 | SPI\_CLK | ATSAMG55 (SPI5) | PA14/SPICLK | U54.41 |
| spi5\_npcs0 | C5 | SPI\_CS | PA11/SPICS0 | U54.44 |
| spi5\_mosi | C8 | SPI\_DI | PA13/MOSI | U54.42 |
| spi5\_miso | C6 | SPI\_DO | PA12/MISO | U54.43 |
| TS\_brg | TS\_CLK | F5 | TS\_CLK | SMS4470 | TS\_CLK | U33.A5 |
| TS\_D0 | F3 | TS\_D0 | TS\_D0 | U33.A6 |
| TS\_VALID | F1 | TS\_VALID | TS\_VALID | U33.B4 |
| TS\_SYNC | D2 | TS\_SYNC | TS\_SYNC | U33.B5 |

Note:

1. CPLD to ATSAMG55's SPI0 need Jump wires

Evaluation Board Pin Assignments

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| CPLD | | | PCB | On-board Device | |  |
| Module | Pin | Pin Loc | Net | Chip | Pin | Pin Loc |
| ADRF\_brg | spi0\_spck | L1 | J6.13 | ATSAMG55 (SPI0) | PB0 | U54.37 |
| spi0\_npcs0 | L2 | **J6.14** | PA25 | U54.56 |
| spi0\_mosi | K2 | J6.15 | PA10/TXD0 | U54.48 |
| spi0\_miso | K3 | J6.16 | PA9/RXD0 | U54.49 |
| ADRF\_brg | ad\_spi\_cs | J3 | J6.17 | ARF6612 | CS | U65.19 |
| ad\_spi\_sclk | K1 | J6.18 | SCLK | U65.18 |
| ad\_spi\_sdio | J1 | J6.19 | SDIO | U65.17 |
| TS\_brg | spi5\_spck | H2 | J6.21 | ATSAMG55 (SPI5) | PA14/SPICLK | U54.41 |
| spi5\_npcs0 | H3 | J6.22 | PA11/SPICS0 | U54.44 |
| spi5\_mosi | G3 | J6.23 | PA13/MOSI | U54.42 |
| spi5\_miso | H1 | J6.24 | PA12/MISO | U54.43 |
| TS\_brg | TS\_CLK | G1 | J6.25 | SMS4470 | TS\_CLK | U33.A5 |
| TS\_D0 | G2 | J6.26 | TS\_D0 | U33.A6 |
| TS\_VALID | F2 | J6.27 | TS\_VALID | U33.B4 |
| TS\_SYNC | F3 | J6.28 | TS\_SYNC | U33.B5 |

Note: clock 24MHz Y1 connect to CPLD's pin E1