Example 1 (Embedded system). The embedded system comprises a processor, sensors and an actuator. The main processor, connected to ports M_{in} and M_{out} , reads data coming from sensors, and passes instructions to the actuator through port Input and Output, respectively. The system fails to get an input only when no data flows through each probabilistic filter. A complete round, which starts when a data comes in and stops when the output data is written successfully, should be accomplished in a certain period of time, otherwise the system sends out a timeout signal.

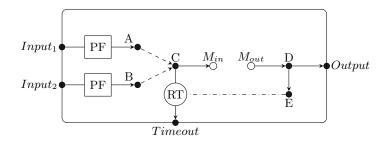


Fig. 1. Embedded System

A probabilistic filter, **PF** in short, drops data with a certain probability, i.e. 1 - p; while **RT** with time bound t_{max} , which stands for reset timer, can be reset.

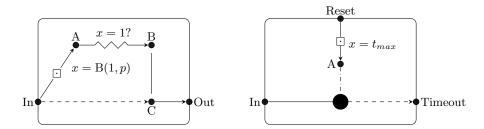


Fig. 2. Probablistic Filter (left) and Reset Timer (right)

There are 8 locations in the STA_r of the embedded system, consisting of triples which symbolizes the configuration of two probabilistic filters and the reset timer. The STA_r is represented by JANI; elements are ommitted except locations and edges.

```
\begin{verbatim}
// the embedded system
{
```

```
locations:
  // loc_num [inv] < initial > : loc_conf
  1 <initial >: (init, init, waiting),
  2: (init, ready, waiting),
  3: (ready, init, waiting),
  4: (ready, ready, waiting),
  5 [t \le t_max] : (init, init, timing),
   6 \quad [t \leftarrow \max] : (init, ready, timing), 
  7 \ [\, t \, <= \, t \text{\_max} \,] \ : \ (\, ready \, , \ init \, , \ timing \,) \, ,
  8 [t \le t_max] : (ready, ready, timing)
edges: [
  // src\_loc \rightarrow dst\_loc (act) [guard] <: update\_func>
  1 \rightarrow 2 (i) : buf_2 = B(1, p),
  2 \rightarrow 1 (Input_2),
  1 \rightarrow 3 (i) : buf_1 = B(1, p),
  3 \rightarrow 1 (Input_1),
  1 \rightarrow 4 (i) : buf_1 = B(1, p), buf_2 = B(1, p),
  4 \rightarrow 1 (Input_1, Input_2),
  2 \rightarrow 4 (i) : buf_1 = B(1, p),
  4 \rightarrow 2 (Input_1),
  3 \rightarrow 4 (i) : buf_2 = B(1, p),
  4 \rightarrow 3 (Input_2),
  2 \rightarrow 3 \text{ (i, Input_2)} : buf_1 = B(1, p),
  3 \rightarrow 2 (i, Input_1) : buf_2 = B(1, p),
  5 \rightarrow 6 (i) : buf_2 = B(1, p),
  6 \rightarrow 5 \text{ (Input_2)},
  5 \rightarrow 7 (i) : buf_1 = B(1, p),
  7 \rightarrow 5 (Input_1),
  5 \rightarrow 8 \ (i) : buf_1 = B(1, p), buf_2 = B(1, p),
  8 \rightarrow 5 \text{ (Input_1, Input_2)},
  6 \rightarrow 8 (i) : buf_1 = B(1, p),
  8 \rightarrow 6 (Input_1),
  7 \rightarrow 8 \ (i) : buf_2 = B(1, p),
  8 \rightarrow 7 \text{ (Input_2)}
  6 \rightarrow 7 \text{ (i, Input_2)} : buf_1 = B(1. p),
  7 \rightarrow 6 \text{ (i, Input_1)} : buf_2 = B(1, p),
  1 \rightarrow 1 \text{ (M_out, Output)} : Output = M_out,
  2 \rightarrow 2 \text{ (M_out, Output)} : Output = M_out,
  3 \ -\!\!\!> \ 3 \ \left(\,\mathrm{M\_out}\,,\ \mathrm{Output}\,\right) \ : \ \mathrm{Output} \ = \ \mathrm{M\_out}\,,
  4 \rightarrow 4 \text{ (M_out, Output)} : Output = M_out,
  7 \rightarrow 5 \text{ (Input_1, M_in) [buf_1 = 1, t = t_max] : t = 0,}
```

```
7 \rightarrow 5 (Input_1, M_in, Timeout) [buf_1 = 1, t = t_max] :
     t = 0, M_in = Input_1, Timeout = TIMEOUT,
7 \rightarrow 5 \text{ (Input_1, M_in, M_out, Output) [buf_1 = 1]}:
    t = 0, M_{in} = Input_{1}, Output = M_{out},
7 -> 5 (Input_1, M_in, M_out, Output, Timeout)
     [buf_1 = 1, t = t_max]:
     t = 0, M_in = Input_1, Output = M_out, Timeout = TIMEOUT,
6 \rightarrow 5 \text{ (Input_2, M_in) [buf_2 = 1, t = t_max]} : t = 0,
6 \rightarrow 5 (Input_2, M_in, Timeout) [buf_2 = 1, t = t_max] :
     t = 0, M_{in} = Input_{2}, Timeout = TIMEOUT,
6 \rightarrow 5 \text{ (Input-2, } M_{-in}, M_{-out}, Output) [buf-2 = 1] :
     t = 0, M_{in} = Input_2, Output = M_{out},
6 -> 5 (Input_2, M_in, M_out, Output, Timeout)
     [buf_2 = 1, t = t_max]:
     t = 0, M_in = Input_2, Output = M_out, Timeout = TIMEOUT,
8 \rightarrow 6 \text{ (Input_1, M_in) [buf_1 = 1, t = t_max]} : t = 0,
8 \rightarrow 6 (Input_1, M_in, Timeout) [buf_1 = 1, t = t_max] :
     t \ = \ 0 \, , \ \ M\_in \ = \ Input\_1 \, , \ \ Timeout \ = \ TIMEOUT,
8 \rightarrow 6 \text{ (Input-1, } M_{in}, M_{out}, \text{ Output) } [buf_1 = 1] :
     t = 0, M_{in} = Input_{-1}, Output = M_{out},
8 \rightarrow 6 \text{ (Input_1, M_in, M_out, Output, Timeout)}
     [buf_1 = 1, t = t_max]:
     t = 0, M_{in} = Input_{-1}, Output = M_{out}, Timeout = TIMEOUT,
8 \to 7 \ (Input_2 \, , \, M_{in}) \ [buf_2 = 1, \ t = t_max] : t = 0, \\ 8 \to 7 \ (Input_2 \, , \, M_{in} \, , \, Timeout) \ [buf_2 = 1, \ t = t_max] :
     t = 0, M_in = Input_2, Timeout = TIMEOUT,
8 \rightarrow 7 \text{ (Input_2, M_in, M_out, Output) [buf_2 = 1]}:
     t = 0, M_{in} = Input_{2}, Output = M_{out},
8 -> 7 (Input_2, M_in, M_out, Output, Timeout)
     [buf_{-2} = 1, t = t_{-max}]:
     t \, = \, 0 \, , \ M\_in \, = \, Input\_2 \, , \ Output \, = \, M\_out \, , \ Timeout \, = \, TIMEOUT ,
8 \rightarrow 5 \text{ (Input_1, Input_2, M_in) [buf_1 = 1, t = t_max]}:
     t \; = \; 0 \; , \; \; M\_in \; = \; Input\_1 \; , \; \;
8 \rightarrow 5 \text{ (Input_1, Input_2, M_in) [buf_2 = 1, t = t_max]}:
     t = 0, M_{in} = Input_2,
8 \rightarrow 5 \text{ (Input_1, Input_2, M_in, M_out, Output) [buf_1 = 1]}:
     t = 0, M_{in} = Input_{1}, Output = M_{out},
8 \rightarrow 5 (Input_1, Input_2, M_in, M_out, Output) [buf_2 = 1] :
     t = 0, M_{in} = Input_{2}, Output = M_{out},
8 \rightarrow 5 \text{ (Input_1, Input_2, M_in, Timeout) [buf_1 = 1, t = t_max]}:
     t = 0, M_{in} = Input_{1}, Timeout = TIMEOUT,
8 \rightarrow 5 \text{ (Input_1, Input_2, M_in, Timeout) [buf_2 = 1, t = t_max]}:
     t = 0, M_{in} = Input_{2}, Timeout = TIMEOUT,
8 -> 5 (Input_1, Input_2, M_in, M_out, Output, Timeout)
     [buf_1 = 1, t = t_max]:
```

```
t = 0, M_in = Input_1, Output = M_out, Timeout = TIMEOUT,
8 \rightarrow 5 \text{ (Input_1, Input_2, M_in, M_out, Output, Timeout)}
     [buf_2 = 1, t = t_max]:
     t = 0, M_in = Input_2, Output = M_out, Timeout = TIMEOUT,
5 \rightarrow 1 \text{ (M_out, Output) } [t < t_max] : Output = M_out,
    5 \rightarrow 1 (i) [t = t_max]
5 \rightarrow 1 \text{ (Timeout)} [t = t_max] : Timeout = TIMEOUT,
5 \rightarrow 1 \text{ (M_out, Output, Timeout) } [t = t_max] :
    Output = M_out, Timeout = TIMEOUT,
6 \rightarrow 2 \text{ (M\_out, Output) } [t < t\_max] : Output = M\_out,
    6 \rightarrow 2 (i) [t = t_max]
6 \rightarrow 2 (Timeout) [t = t_max] : Timeout = TIMEOUT,
6 \rightarrow 2 \text{ (M_out, Output, Timeout) } [t = t_max]:
    Output = M_out, Timeout = TIMEOUT,
7 \rightarrow 3 \text{ (M\_out, Output) } [t < t\_max] : Output = M\_out,
    7 -> 3 (i) [t = t_max]
7 \rightarrow 3 (Timeout) [t = t_max] : Timeout = TIMEOUT,
7 \rightarrow 3 \text{ (M_out, Output, Timeout) } [t = t_max]:
    Output = M_out, Timeout = TIMEOUT,
8 \rightarrow 4 \text{ (M_out, Output) } [t < t_max] : Output = M_out,
    8 \rightarrow 4 (i) [t = t_max]
8 \rightarrow 4 (Timeout) [t = t_max] : Timeout = TIMEOUT,
8 \rightarrow 4 \text{ (M_out, Output, Timeout) } [t = t_max]:
    Output = M_out, Timeout = TIMEOUT,
3 \rightarrow 5 \text{ (Input_1, M_in) [buf_1 = 1] : } t = 0, M_in = Input_1,
3 \rightarrow 5 \text{ (Input-1, M-in, M-out, Output) [buf-1 = 1]}:
    t = 0, M_{in} = Input_{1}, Output = M_{out},
2 \rightarrow 5 \text{ (Input_2, M_in) [buf_2 = 1]} : t = 0, M_in = Input_2,
2 \rightarrow 5 \text{ (Input_2, M_in, M_out, Output) [buf_2 = 1]}:
    t = 0, M_{in} = Input_2, Output = M_{out},
4 \rightarrow 6 \text{ (Input_1, M_in) [buf_1 = 1]} : t = 0, M_in = Input_1,
4 \rightarrow 6 \text{ (Input_1, M_in, M_out, Output) [buf_1 = 1]}:
    t = 0, M_{in} = Input_{1}, Output = M_{out},
4 \rightarrow 7 \text{ (Input_2, M_in) [buf_2 = 1]} : t = 0, M_in = Input_2,
4 \rightarrow 7 \text{ (Input_2, M_in, M_out, Output) } [buf_2 = 1] :
    t = 0, M_in = Input_2, Output = M_out,
3 \rightarrow 6 \ (i, Input_1, M_{in}) \ [buf_1 = 1] :
    t \ = \ 0 \, , \ M\_in \ = \ Input\_1 \, , \ buf\_2 \ = \ B(1 \, , \ p) \, ,
3 \rightarrow 6 \ (i, Input_1, M_in, M_out, Output) \ [buf_1 = 1] :
    t = 0, M_{in} = Input_{-1}, buf_{-2} = B(1, p), Output = M_{out},
2 \rightarrow 7 \ (i, Input_2, M_in) \ [buf_2 = 1] :
    t = 0, M_{in} = Input_{2}, buf_{1} = B(1, p),
2 \rightarrow 7 (i, Input_2, M_in, M_out, Output) [buf_2 = 1] :
```