# Per-Location Simulation – Appendix

Liyi Li, Elsa L. Gunter {liyili2,egunter}@illinois.edu

Department of Computer Science, University of Illinois at Urbana-Champaign

Abstract. Simulation/bisimulation is one of the most widely used frameworks for proving program equivalence/semantic preservation. In this paper, we propose a new per-location simulation (PLS) relation that is simple and suitable for proving that a compiled program semantically preserves its original program under a CFG-based language with a real-world, C/C++ like, weak memory model. To the best of our knowledge, PLS is the first simulation framework weaker than the CompCert [5]/CompCertTSO [9] one that is used for proving compiler correctness. With a combination of PLS, the compiler proof-framework Morpheus [7], and a language semantics with a weak memory model, we are able to prove that programs are semantically preserved through a transformation. All the definitions and proofs have been implemented in Isabelle/HOL.

## 1 Appendix

### 1.1 Morpheus Syntax

Here we introduce the syntax of Morpheus. More details can be found at the work of Mansky et~al. [7]. The basic approach of the Morpheus specification language is modeled after the TRANS language of Kalvala et~al. [2]. Optimizations are specified as conditional compositions of rewrites on a generalized control flow graph (GCFG) containing the program's code. The language is partitioned into three largely independent components: core graph transformations (H below), conditions given in a variant of Computation Tree Logic (CTL) ( $\varphi$  below), and a strategy language (T below) for building complex transformations out of component transformations and conditions.

Intuitively, the rewrite portion of an optimization expresses the local transformation to be made, the condition characterizes the situations in which the optimization should be applied, and the strategy language allows us to build whole-system transformations out of collections of local ones. Morpheus is a special-purpose language for the transformation of GCFGs, and as such is parametrized by aspects of GCFGs, namely node names, node labels (program instructions), and edge labels (marking control flow). Transformation specifications may mention aspects of GCFGs concretely, but more generally, they use pattern variables that will be instantiated with control flow graph components in each specific application. We will use the term "expressions" to refer to patterns built from both

concrete entities and metavariables (which will be instantiated with concrete entities when the transformation is applied). We use the term metavariable (a) to refer to the variables in the patterns and expressions in Morpheus transformations, as opposed to the concrete programming variables that will be found in instructions.

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\begin{split} H & \triangleq \mathsf{add\_node}(\pi, B, (l_1, \pi_1), \dots, (l_n, \pi_n)) \mid \mathsf{add\_node}(\pi) \\ & \mid \mathsf{relabel\_node}(\pi, B) \mid \mathsf{move\_edge}((\pi, l, \pi_1), \pi_2) \\ \varphi & \triangleq \mathsf{true} \mid p(\overrightarrow{x}) \mid \varphi \land \varphi \mid \neg \varphi \mid \exists \ a. \ \varphi \mid \mathcal{AX} \ \varphi \mid \mathcal{AY} \ \varphi \mid \mathcal{EX} \ \varphi \mid \mathcal{EY} \ \varphi \\ & \mid \mathcal{A} \ \varphi \ \mathcal{U} \ \varphi \mid \mathcal{E} \ \varphi \ \mathcal{U} \ \varphi \mid \mathcal{A} \ \varphi \ \mathcal{S} \ \varphi \mid \mathcal{E} \ \varphi \ \mathcal{S} \ \varphi \\ T & \triangleq H \mid \mathsf{SATISFIED\_AT} \ \pi \ \varphi \mid \mathsf{NOT} \ T \mid T \setminus T \mid \mathsf{EXISTS} \ a. \ T \mid T + T \mid T \ ; \ T \mid T \ast T \mid T \ast T \mid T \ \end{split}
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The syntax of Morpheus consists of actions (H), conditions  $(\varphi)$ , and transformations (T). The atomic actions H begin with add\_node and remove\_node, which add and remove nodes that have no incoming edges. In the case of add\_node, the addition only takes place if the node description is well-formed as a CFG node (i.e., it has the right number and kind of outgoing edges for its instruction label). The relabel\_node action relabels an existing node with a new instruction, as long as that new instruction is compatible with the existing edge structure. The only action that operates directly on edges (rather than nodes) is move\_edge, which moves the destination of an edge from one node in the graph to another. The conditions  $\varphi$  of Morpheus are based on First-Order CTL (FOCTL). Starting from a set of atomic predicates p, they include all of the usual propositional and temporal operators. The  $\mathcal{S}$  ("since") and  $\mathcal{Y}$  ("yesterday") operators are the past-time counterparts to the  $\mathcal{U}$  ("until") and  $\mathcal{X}$  ("next") operators respectively; for instance,  $\mathcal{E} \varphi_1 \mathcal{S} \varphi_2$  holds when there exists some path backwards through the graph such that  $\varphi_1$  holds until a previous point at which  $\varphi_2$  holds. The existential quantifier  $\exists$  is used to quantify over metavariables in a formula: these metavariables may then appear in the atomic predicates of a formula, enhancing the expressive power of the conditions. At the top level, a transformation T combines conditions and rewrites using strategies. Strategies are inherently non-deterministic, as is reflected by their returning a set of possible transformed graphs. The simplest strategy is just to perform an action H. The strategy SATISFIED\_AT  $\pi \varphi$  acts as the identity transformation if  $\varphi$  holds of the GCFG at the node  $\pi$ , and returns the empty set if  $\varphi$  fails to hold on  $\pi$ . Thus SATISFIED\_AT  $\pi \varphi$  acts as filter, allowing through only those GCFGs and nodes  $\pi$  that satisfy  $\varphi$ . On the other hand, NOT T and  $T_1 \setminus T_2$  allow us to deselect graphs by the ability to perform a transformation. The transformation NOT Tselects those graphs that T cannot transform, i.e., those not in the domain of T, and deselects those that it can transform. The transformation  $T_1 \setminus T_2$  restricts the output of  $T_1$  to those graphs that could not be produced by  $T_2$ , i.e., those not in the image of  $T_2$ . Note the difference between these two filters: NOT Tfilters based on the complement of the domain of a transformation, while  $T_1 \setminus T_2$ filters based on the complement of the range of a transformation. The strategy **EXISTS** a. T binds a in T, limiting its scope to the free occurrences of a in the conditions and actions of T. Finally, the constructs + and ; allow for choice between and sequencing of two transformations respectively, and the iteration

operator \* allows for the repeated application of a transformation any number of times.

For a simple example of a Morpheus transformation, assume we have a language of instructions that supports assign- ments and binary arithmetic expressions. In this setting, if we have a variable assigned the result of applying an arithmetic operation to two constants, we might want to replace the operation with its result. This can be done by the following transformation:

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\begin{split} & \texttt{simple\_constant\_folding}(\pi) \triangleq \texttt{EXISTS} \ x \ a \ b \ c \ oper. \\ & \texttt{SATISFIED\_AT} \ \pi \ \texttt{stmt}( \ x = oper( \ a,b)) \land \texttt{is\_const}(a) \land \texttt{is\_const}(b) \land \texttt{is\_const}(c) \land \texttt{eval}(oper(a,b),c) \ ; \ \texttt{relabel\_node}(\pi,x=c) \end{split}
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This is an existentially quantified sequence of a condition and an action. (Note that oper is a metavariable that will be bound to an arithmetic operator appearing in the program syntax, and eval(e,c) is a predicate asserting that the expression e evaluates to the constant e.) We may apply  $simple\_constant\_folding$  to a program with a node labeled diff = 10 - 2, and the transformation will match  $\pi$  to (the name of) this node, e to e diff, e to e 10, e to 2, e oper to (op - ), and e to 8 (because of the clause is e (e, e), and relabel the node to e diff = 8.

#### 1.2 Memory Model

Here we introduce the memory model described in Sec. ??. The model is supposed to be in the format of an axiomatic candidate execution model [1]. By defining a set of binary relations and predicates, a candidate execution model selects a valid set of memory executions from a set of candidate executions. Here, we use a subset of a model from the ATRCM model [6], which has been proved to be sound with respect to the C/C++ memory model defined by Lahav *et al.* [4] and the IMM model [8].

We first show a set of useful conventions.  $R^2$ ,  $R^+$  and  $R^*$  represent the reflexive, transitive, and reflexive-transitive closures of relation R. A memory execution (memory trace) in this paper is viewed as a sequence of memory events  $(\mathcal{E}_{\mathcal{V}})$  in Fig. ??) representing interactions between program executions and the main memory. The structure of a memory event is a triple of a thread-ID (type Tid), a unique memory action-ID (type Aid described in Fig. ??), and a memory action (type l). Each non- $\tau$  memory event (W and R) comes from a memory instruction (store and load instructions) in a program execution produced by the program semantics. A memory execution is defined as a triple of  $(T, \rho, rf)$ , where T is a downward closed natural number set excluding 0 representing time points,  $\rho$  is a partial function from natural numbers to memory events and a reads from relation (rf, type  $T \times T$ ) determining the write-read pairs in the execution. To determine if a memory execution is valid, we need other entities: a set of threads (Tid, type TID set), a family (sbs, type  $TID \to T \times T$ ) of sequencedbefore relations sb, each of which is based on the information from a CFG, and a family (dds, type  $TID \to T \times T$ ) of data dependency relations dd. For a CFG

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Domain
 Time Points: T \subseteq \mathbb{N}
                                                                          Action-IDs: Aid ≜ Name
                                                                                                                                                            Thread-IDs: tid \in Tid \subseteq Tid
Memory Concurrency Model
 Execution Map: \rho \subseteq T \to (Tid \times Aid \times Act)
                                                                                                                                                             Data Dependency: dd \subseteq T \times T
Data Dependency Family: \operatorname{dds} \subseteq Tid \to (T \times T)
Sequenced-Before Family: \operatorname{sbs} \subseteq Tid \to (T \times T)
                                                                                                                                                            Sequenced-Before Relation: \mathtt{sb} \subseteq T \times T
 acq(T, \rho, sb) \triangleq \{(s, t) \in T^2 | (s, t) \in sb \land is\_read(\rho(s)) \land is\_acq(\rho(s)) \}
 \begin{array}{l} \operatorname{dcd}(T,\rho,\operatorname{sb}) = \{(s,t) \in T \mid (s,t) \in \operatorname{sb} \wedge \operatorname{is\_red}(\rho(s)) \wedge \operatorname{is\_acq}(\rho(s))\} \\ \operatorname{rel}(T,\rho,\operatorname{sb}) \triangleq \{(s,t) \in T^2 | (s,t) \in \operatorname{sb} \wedge \operatorname{is\_rel}(\rho(t)) \wedge \operatorname{is\_write}(\rho(t))\} \\ \operatorname{po}(T,\rho,\operatorname{sb},\operatorname{dd}) \equiv \operatorname{dd} \cup \operatorname{acq}(T,\rho,\operatorname{sb}) \cup \operatorname{rel}(T,\rho,\operatorname{sb}) \\ \operatorname{pos}(Tid,T,\rho,\operatorname{sbs},\operatorname{dds}) \equiv \bigcup_{tid \in Tid} \operatorname{po}(T,\rho,\operatorname{sbs}(tid),\operatorname{dds}(tid)) \\ & = \bigcup_{tid \in Tid} \operatorname{po}(T,\rho,\operatorname{sbs}(tid),\operatorname{dds}(tid)) \\ \end{array} 
 co\_cw(T, \rho, rf) \triangleq
     \begin{array}{l} \exists \exists (s,t) \mid (s,t) \in \texttt{rf} \land (\exists (r,r') \in \texttt{rf}.r < s \land t < r' \land \texttt{same\_loc}(\rho(s),\rho(r)) \land \texttt{same\_thread}(\rho(r'),\rho(t))) \} \\ \cup \{(s,t) \mid \exists r \ r'.(s,r) \in \texttt{rf} \land (t,r') \in \texttt{rf} \land \texttt{same\_thread}(\rho(s),\rho(t)) \end{array} 
                                \land \mathtt{same\_thread}(\rho(r), \rho(r')) \land ((s < t \land r > r') \lor (s > t \land r < r')) \}
 \texttt{single\_prop}(Tid, T, \rho, \texttt{sbs}, \texttt{dds}, \texttt{rf}) \triangleq \forall (s, t) \in (\texttt{rf} \cup \texttt{pos}(Tid, T, \rho, \texttt{sbs}, \texttt{dds})).s < t
\mathtt{at\_co}(T,\rho,\mathtt{rf}) \triangleq \mathtt{co\_cw}(T,\rho,\mathtt{rf}) = \emptyset
 \mathtt{sat}(Tid, T, \rho, \mathtt{sbs}, \mathtt{dds}, \mathtt{rf}) \triangleq \ \mathtt{single\_prop}(Tid, T, \rho, \mathtt{sbs}, \mathtt{dds}, \mathtt{rf}) \wedge \mathtt{at\_co}(T, \rho, \mathtt{rf})
\mathsf{mo}_x(T,\rho) \triangleq \{(s,t) \in T^2 | a < b \land \mathsf{same\_loc}(\rho(s),\rho(t)) \land \mathsf{is\_write}(\rho(s)) \land \mathsf{is\_write}(\rho(s)) \}
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Fig. 1: Parts of the Definition of the Memory Model

G, sb describes the relations on memory instructions in the CFG that simulate the instruction evaluation order relations from an in-order execution machine to execute G, while dd describes the data, control, and alias dependencies that can be generated by traditional data flow, control flow, and alias analysis algorithms.

In Fig. 1, we describe how we judge if a memory execution is valid. We first define the program order relation po for a thread as the union of all singlethreaded instruction dependency relations in the thread. It is a function taking in a time point set T, a  $\rho$  function and sb for the thread, and it outputs a relation set defining the instruction dependency. For simplicity, throughout this paper, we use refer to po as the relation set generated by the  $po(T, \rho, sb, dd)$ . The po relation for a set of memory executions represents the exact order of evaluation based on the program meaning. The sequenced-before relation (sb) represents an approximation of the order of evaluation in a memory execution, but it does not mean that an instruction must happen before another instruction only because the programmer writes them in that order. For example, program (a) in Fig. ?? has the read from y sequenced-before the write to x in the left thread, but the program allows the write to happen before the read. In this paper, po is defined as a union of the dd, acq, and rel relations. dd is the data dependence relation for a memory execution including all dependency generated by data flow analysis, control flow analysis, alias analysis and dynamic or static methods that determine the data dependency of instructions in a CFG. acq and rel relations are defined in Fig. 1. Here, is\_something is a predicate checks if a memory event has the property described as something, acq defines the binary relations between all acq reads and all memory operations (reads and writes) after it in a thread; rel defines the relations between a rel write in a thread and all operations prior to it. We also define pos as the union of all po in each thread. A valid C/C++ memory model has the property that there is a global

total order (modification order) on observations of writes for each location. We define modification order for each location  $(mo_x)$  in Fig. 1, and mo is the union of all per-location modification orders. To guarantee the valid multi-threaded behaviors, the predicate  $at_co$  (Fig. 1) ensures that bad behaviors defined by the  $co_cw$  relation do not happen. The  $co_cw$  relation collects bad relations in an execution that violates two execution orders: first, every two read instructions in the same thread (by the  $same_thread$  function) at the same location (by the  $same_loc$  function) read from writes in a timely order. Second, the sends (writes) and receives (reads) between two threads are in FIFO order. Finally, the predicate  $sat(Tid, T, \rho, sbs, rf)$  checks if an execution is valid by checking an execution satisfy the  $at_co$  predicate, as well as checking if all edges in the union of program order relations and the reads-from relation on a program are from an early time to a later time.

We have introduced the memory model briefly. The model is a C/C++ like weak memory model because we have proved that the model is sound with respect to the RC11 model [3]. More specifically, the model is SRA-consistent as the proof below. The details of the proof are in the technical report [6].

**Lemma 1.** For any valid execution  $\operatorname{sat}(T, Tid, \rho, \operatorname{sbs}, \operatorname{dds}, \operatorname{rf})$  in ATRCM, and a location set (Loc) given as collecting all locations used in  $\rho$ , then  $\operatorname{pos} \cup \operatorname{mo} \cup \operatorname{rf}$  is acyclic.

#### 1.3 Program Transition Semantics

Here, we define the semantics for a program based on the program syntax in Fig. ?? and instruction semantics in Sec. ??. The program semantics is building an abstract machine executing single threaded instructions through a family of conceptual CPUs (one for each thread), and multi-threaded instructions through a conceptual memory machine. We assume that a CPU execute a basic block of instructions at a time, and any one of executing basic blocks in an program execution, named dynamic basic block, can be identified as a unique number  $m \in \mathbb{N}$  in a program execution. We use a pair of a unique number and a basic block number of a block  $(m,\pi) \in \mathbb{N} \times \mathbb{N}$  to refer to the **dynamic basic block number** (as  $\overline{\pi}$ ) for a dynamic block whose content is the basic block whose node is  $\pi$  in a CFG. Then, a pair of dynamic block number and an instruction number  $(\mathbb{N} \times \mathbb{N} \times \mathbb{N})$ , named action-ID (as d having type  $A = \mathbb{N} \times \mathbb{N} \times \mathbb{N}$ ), can uniquely identify an executing instruction in a thread in a program execution. In Sec. 1.2, we have described a po relation (or a family pos), we extend the idea to a relation  $\overline{po}$  (or a family  $\overline{pos}$ , one for each thread) describing similar program order relations as po.  $\overline{po}$  for a thread is a relation on  $A \times A$ , and it describes the program order relations on different instructions instead of memory events in po. Every  $\overline{po}$  in  $\overline{pos}$  is generated along with program semantics transitions.

The operational transition semantics in Fig. 2 is combination of the instruction level semantics and memory concurrency model. It is represented as a labeled transition system whose states are pairs of programs  $(\mu)$  and the state environment  $(\omega)$ , and whose labels are memory events. A state environment is

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\begin{split} & \text{form}\_\mathsf{D}(\overline{\pi},\beta) \equiv \{d | \exists e \: i.d = (\overline{\pi},i) \land e = \text{ins}(\beta,d) \} \quad \text{gen}(\overline{\mathsf{po}},\mathsf{D},W) \equiv \{d \in \mathsf{D}| (\neg \exists d' \in W.(d',d) \in \overline{\mathsf{po}}) \} \\ & \qquad \qquad (N,\pi_0,\lambda,E) = C \land \pi = \text{snd}(\overline{\pi}) \land \text{ins}(\beta,d) = e \land \text{is}\_\mathsf{CInst}(\beta,d) \land \lambda(\pi) = \beta \\ & \qquad \land l = \eta(e,\phi) \land (\pi,l,\pi') \in E \land \lambda(\pi') = \beta' \land \overline{\pi}' = (\mathsf{fst}(\overline{\pi}) + 1,\pi') \land D = \mathsf{form}\_\mathsf{D}(\overline{\pi}',\beta') \\ & \qquad \land \rho' = \rho[\mathsf{max}(T) + 1 \mapsto (tid,d,\tau)] \land \overline{\mathsf{po}}' = \mathsf{gen}\_\bar{\mathsf{po}}(G,\overline{\pi}',\overline{\mathsf{po}},\rho',D,\beta',\varphi) \land W = \mathsf{gen}(\overline{\mathsf{po}},D,D) \\ & \qquad \qquad \mathsf{trans}(C,tid,\overline{\pi},\overline{\mathsf{po}},\mathsf{sb},\mathsf{dd},T,\rho,\varphi,\Gamma,(\{d\},S)) \\ & \qquad \qquad = (\overline{\pi}',\overline{\mathsf{po}}',\mathsf{sb},\mathsf{dd},T \cup \{\mathsf{max}(T) + 1\},\rho',\varphi,\Gamma,(W,\emptyset),\emptyset) \\ \\ & \qquad \qquad (N,\pi_0,\lambda,E) = C \land \lambda(\mathsf{snd}(\overline{\pi})) = \beta \land \mathsf{ins}(\beta,d) = e \land \neg \mathsf{is}\_\mathsf{CInst}(\beta,d) \land \Gamma(tid) = \gamma \\ & \qquad \land \Gamma(tid') = \gamma' \land \gamma'(x) = (t,v) \land (\varphi',\mathsf{R}^x_{v,o}) = \psi(e,\varphi,\gamma[x \mapsto (t,v)]) \\ & \qquad \land W' = \mathsf{gen}(\overline{\mathsf{po}},D - (S \cup \{d\}),W) \land \mathsf{rf} = \{\mathsf{fst}(\gamma'(x)),\mathsf{max}(T) + 1)\} \\ & \qquad \land \mathsf{bb}' = \mathsf{gen}\_\mathsf{sb}(\mathsf{sb},\overline{\mathsf{po}},\mathsf{d}) \land \mathsf{dd}' = \mathsf{gen}\_\mathsf{dd}(\mathsf{dd},\overline{\mathsf{po}},\mathsf{d}) \\ & \qquad \qquad \mathsf{trans}(C,tid,\overline{\pi},\overline{\mathsf{po}},\mathsf{sb},\mathsf{dd},T,\rho,\varphi,\Gamma,(W \cup \{d\},S)) \\ & \qquad \qquad = (\overline{\pi},\overline{\mathsf{po}},\mathsf{sb}',\mathsf{dd}',T \cup \{\mathsf{max}(T) + 1\},\rho[\mathsf{max}(T) + 1 \mapsto (tid,d,\mathsf{R}^x_{v,o})],\varphi',\Gamma,(W',S \cup \{d\}),\mathsf{rf}) \\ & \qquad \qquad \mathsf{tid} \in Tid \land \overline{\mathsf{pos}}' = \overline{\mathsf{pos}}[tid \mapsto \overline{\mathsf{po}}'] \land \mathsf{sbs}' = \mathsf{sbs}[tid \mapsto \mathsf{sb}'] \land \mathsf{das}' = \mathsf{dds}[tid \mapsto \mathsf{dd}'] \\ & \qquad \land \overline{\Pi}' = \overline{\Pi}[tid \mapsto \overline{\pi}] \land \Phi' = \Phi[tid \mapsto \varphi'] \land \theta' = \Theta[tid \mapsto \theta'] \land \mathsf{sat}(Tid,T',\rho,\mathsf{sbs}',\mathsf{dds}',\mathsf{rf} \cup \mathsf{rf}') \\ & \qquad \land \mathsf{trans}(\mu(tid),tid,\overline{\Pi}(tid),\overline{\mathsf{pos}}(tid),\mathsf{sbs}(tid),\mathsf{dds}(tid),T,\rho,\Phi(tid),\Gamma,\Theta(tid)) \\ & \qquad \qquad (\mathsf{c}) = (\overline{\pi}',\overline{\mathsf{po}}',\mathsf{sb}',\mathsf{dd}',T',\rho',\varphi',\Gamma',\theta',\mathsf{rf}') \end{aligned}
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Fig. 2: The Program Semantics

 $\xrightarrow{\rho'(\max(T'))} \left(\mu, Tid, \overline{\texttt{pos}}', \texttt{sbs}', \texttt{dds}', \overline{\varPi}', \varPhi', \varTheta', \Gamma', \Gamma', \rho', \texttt{rf} \cup \texttt{rf'}\right)$ 

 $(\mu, Tid, \overline{pos}, sbs, dds, \overline{\Pi}, \Phi, \Theta, \Gamma, T, \rho, rf)$ 

a long tuple of a set of thread-IDs (Tid), a program order family (pos, one for each thread), a sequenced-before relation family (sbs), a data dependency family (dds), a current dynamic block number family  $(\overline{H})$ , a registers family  $(\Phi)$ , a heap snapshot family  $(\Gamma)$  representing different views of the threads of the main memory, a program pointer family  $(\Theta)$  representing the current executing instruction of each thread, a time point set (T), a  $\rho$  mapping, and a reads-from relation (rf). We show the rule (c) as the top-most rule of the transition system in Fig. 2. This rule selects a thread tid, applies the one-step transition to see if the accumulated result satisfies the predicate of the memory model (sat), and then moves forward to a new step via the memory event label  $\rho'(\max(T'))$ . The function max produces the maximum number in T'. We can retrieve the memory event by the max function because the trans function always creates a map entry in  $\rho$  from the maximum time point plus 1 to the current memory event.

We show two rules ((a) and (b)) of trans in Fig. 2. It needs to finish several tasks as a one step evaluation for a thread tid with a CFG C. First, if its program pointer  $\Theta(tid)$  points to the end of a basic block (no instructions left for execution), it selects a new basic block according to the edge information in C (applying function  $\eta$  to it with registers ( $\Phi(tid)$ ) to get the edge label), and assigns a new dynamic basic block number with a new program pointer pointing to the top of the new block. In this case, trans also adds new relations of program order, sequenced-before, and data dependency to the existing relation sets inside the new basic block. Second, if  $\Theta(tid)$  indicates that there are instructions in the basic block waiting for execution, an instruction is randomly selected for execution (applying function  $\psi$  to it with registers ( $\Phi(tid)$ ) and heap snapshot

 $(\Gamma(tid))$ ) if the instruction satisfies the program order relation on the basic block. Third, for a step, **trans** also picks a new time point (the maximum number of the time point set T plus 1) to add to the set T, and assigns the new time point to a new memory event. The creation of the event is to combine the thread-ID tid, a newly generated action-ID (the action-ID is calculated by combining the dynamic block number with the instruction number), and a memory action calculated from the function  $\psi$  (if the instruction is a termination, we assume that the action is  $\tau$ ). Fourth, **trans** also generates a new **rf** pair if the action is a read, and modifies the memory snapshot by inserting the current time point and write value if the action is a write.

Rules (a) and (b) (Fig. 2) are sample rules of the trans function that connects between the transition function  $(\rightarrow)$  and the single-instruction semantics defined in Sec. ??. trans transitions from a tuple of a CFG C, a thread-ID tid, a current dynamic block number  $\overline{\pi}$ , a program order  $\overline{po}$ , a sequenced-before relation sb, a data dependency relation dd, a time point n, a mapping  $\rho$ , a register  $\phi$ , a family of memory snapshots  $\Gamma$ , and a program counter  $\theta$ ; to another tuple of a possible new dynamic block number  $\overline{\pi}'$ , an updated program order  $\overline{po}'$ , an updated sequencedbefore relation sb', an updated data dependency relation dd', a new time point n', a new mapping  $\rho'$ , a possible new register  $\phi'$ , an updated family of memory snapshots  $\Gamma'$ , an updated program counter  $\theta$ , and a set of reads-from relations rf containing a possible write-read pair generated by a load instruction. In a thread tid, trans selects one of the possible next instructions in  $\theta$  to execute. The (a) rule deals with the transition after executing a branching state at the end of a basic block, while rule (b) deals with the case of a load instruction. In these rules, ins is a function producing the instruction expression from a basic block and an action-ID.  $\gamma|_v$  means to form a new mapping by getting rid of the time point in the value pair  $T \times val$ . The function gen\_ $\overline{po}$  takes the existing  $\overline{po}$  and a basic block and generates a new po' containing all relations in the po relation, all program order relations between instructions in the basic block, and the program order relations between the old-instructions in  $\overline{po}$  and the instruction in the new basic block. gen\_\overline{\rho}\overline{\rho} happens once when a new dynamic basic block is generated. The function gen\_sb generates an updated sb relation based on the information in the updated po relation, while gen\_dd generates an updated dd relation based on the information in the updated  $\overline{po}$  relation.

### References

- Alglave, J., Maranget, L., Tautschnig, M.: Herding Cats: Modelling, Simulation, Testing, and Data Mining for Weak Memory. ACM Trans. Program. Lang. Syst. 36(2), 7:1-7:74 (Jul 2014). https://doi.org/10.1145/2627752, http://doi.acm.org/ 10.1145/2627752
- Kalvala, S., Warburton, R., Lacey, D.: Program transformations using temporal logic side conditions. ACM Trans. Program. Lang. Syst. 31 (05 2009). https://doi.org/10.1145/1516507.1516509
- Lahav, O., Giannarakis, N., Vafeiadis, V.: Taming release-acquire consistency. SIG-PLAN Not. 51(1), 649–662 (Jan 2016). https://doi.org/10.1145/2914770.2837643, http://doi.acm.org/10.1145/2914770.2837643

- 4. Lahav, O., Vafeiadis, V., Kang, J., Hur, C.K., Dreyer, D.: Repairing sequential consistency in c/c++11. SIGPLAN Not. **52**(6), 618-632 (Jun 2017). https://doi.org/10.1145/3140587.3062352, http://doi.acm.org/10.1145/3140587.3062352
- Leroy, X.: A Formally Verified Compiler Back-end. J. Autom. Reason. 43(4), 363–446 (Dec 2009). https://doi.org/10.1007/s10817-009-9155-4, http://dx.doi.org/10.1007/s10817-009-9155-4
- Li, L., Gunter, E.: The axiomatic timed relaxed memory model (2019), https://github.com/liyili2/timed-relaxed-memory-model
- Mansky, W., Gunter, E.L., Griffith, D., Adams, M.D.: Specifying and executing optimizations for generalized control flow graphs. Science of Computer Programming 130, 2–23 (Nov 2016). https://doi.org/10.1016/j.scico.2016.06.003
- 8. Podkopaev, A., Lahav, O., Vafeiadis, V.: Bridging the Gap Between Programming Languages and Hardware Weak Memory Models. Proc. ACM Program. Lang. **3**(POPL), 69:1-69:31 (Jan 2019). https://doi.org/10.1145/3290382, http://doi.acm.org/10.1145/3290382
- 9. Ševčík, J., Vafeiadis, V., Zappa Nardelli, F., Jagannathan, S., Sewell, P.: CompCertTSO: A Verified Compiler for Relaxed-Memory Concurrency. J. ACM 60(3), 22:1-22:50 (Jun 2013). https://doi.org/10.1145/2487241.2487248, http://doi.acm.org/10.1145/2487241.2487248