REVISIONS							
REV	ZONE	NO.	DESCRIPTION	E.C.	BY	APVD.	DATE
			RELEASE PER PPD #				

X-5
CARRIER BOARD SCHEMATIC EV1
REV 1D

TABLE OF CONTENTS

CLOCK TABLE

SIGNAL ATTRIBUTES

CRITICAL SIGNALS

ITEM	QTY.	PART NO.	DESCRIPTION	REMARKS/REF.SYMBOL

PARTS LIST

UGSI CORPORATION

CONFIDENTIAL RESTRICTED

DIMENSIONS ARE IN INCHES

UNLESS OTHERWISE SPECIFIED

	MM	INCH
XX	±	± .01
XXX	±	± .005

ANGLES ± 1° FRACTIONS ± 1/64

MATERIAL:

FINISH:

APPROVALS	DATE
DRAWN	
CHECKED	
ENGINEER	
MFG. ENG.	
PRODUCT	
QUALITY	
TEST ENG.	

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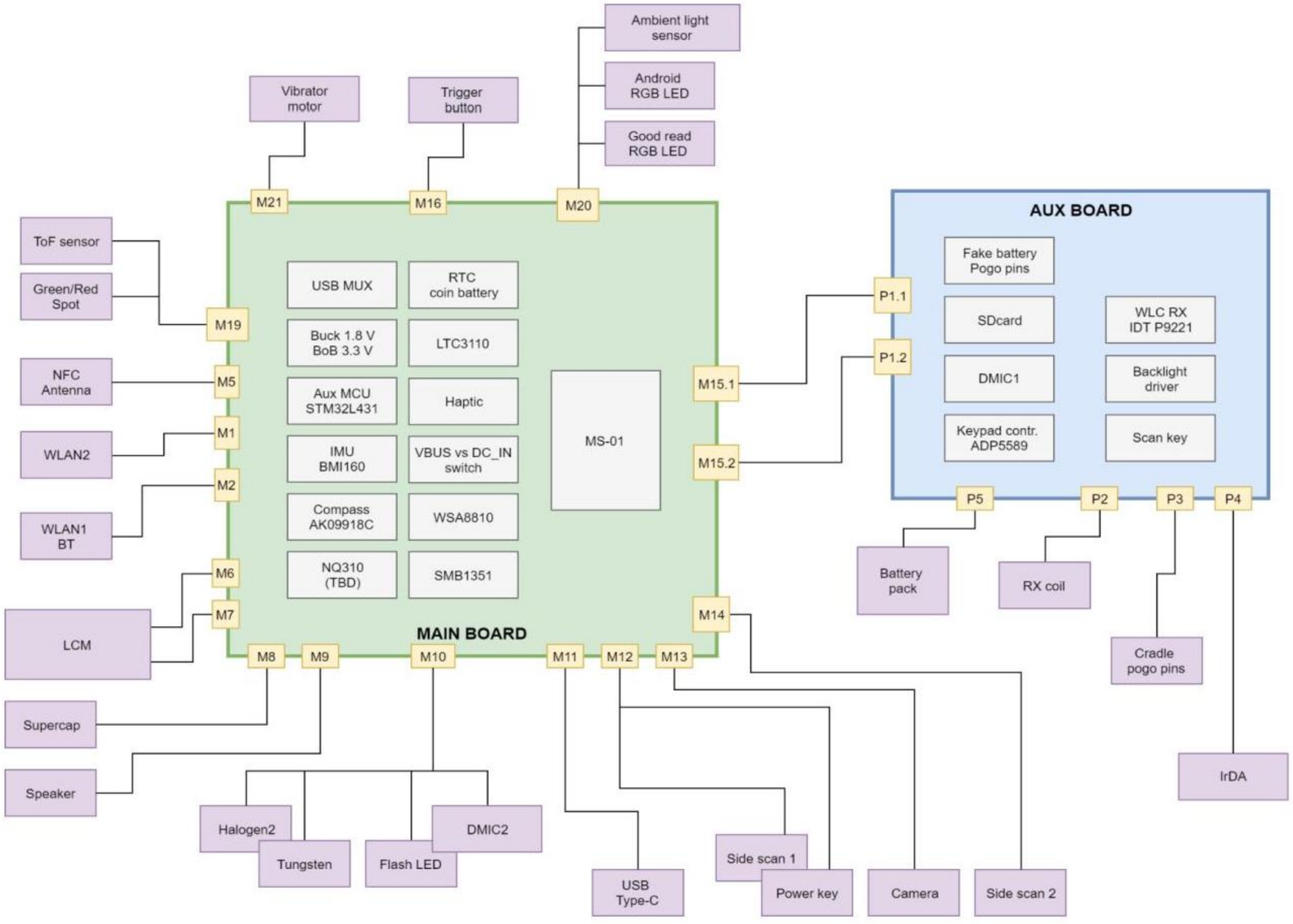
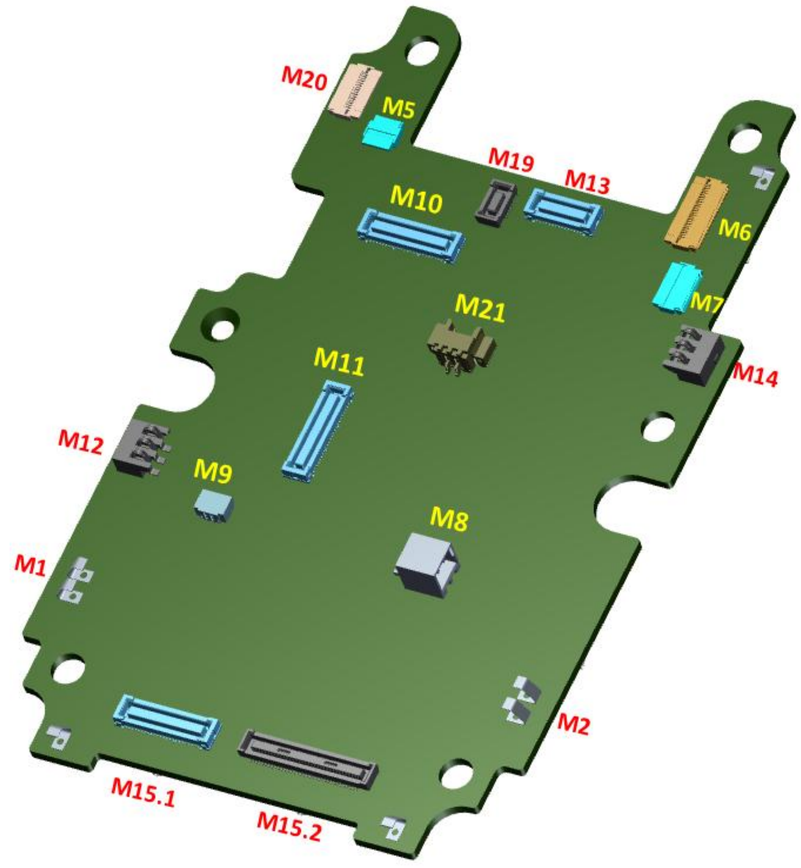
NEXT ASSY	USED ON

DO NOT SCALE DRAWING

BOARD LEVEL BLOCK DIAGRAM

REVISIONS							
REV	ZONE	NO.	DESCRIPTION	E.C.	BY	APVD.	DATE
			SEE SHEET 1				





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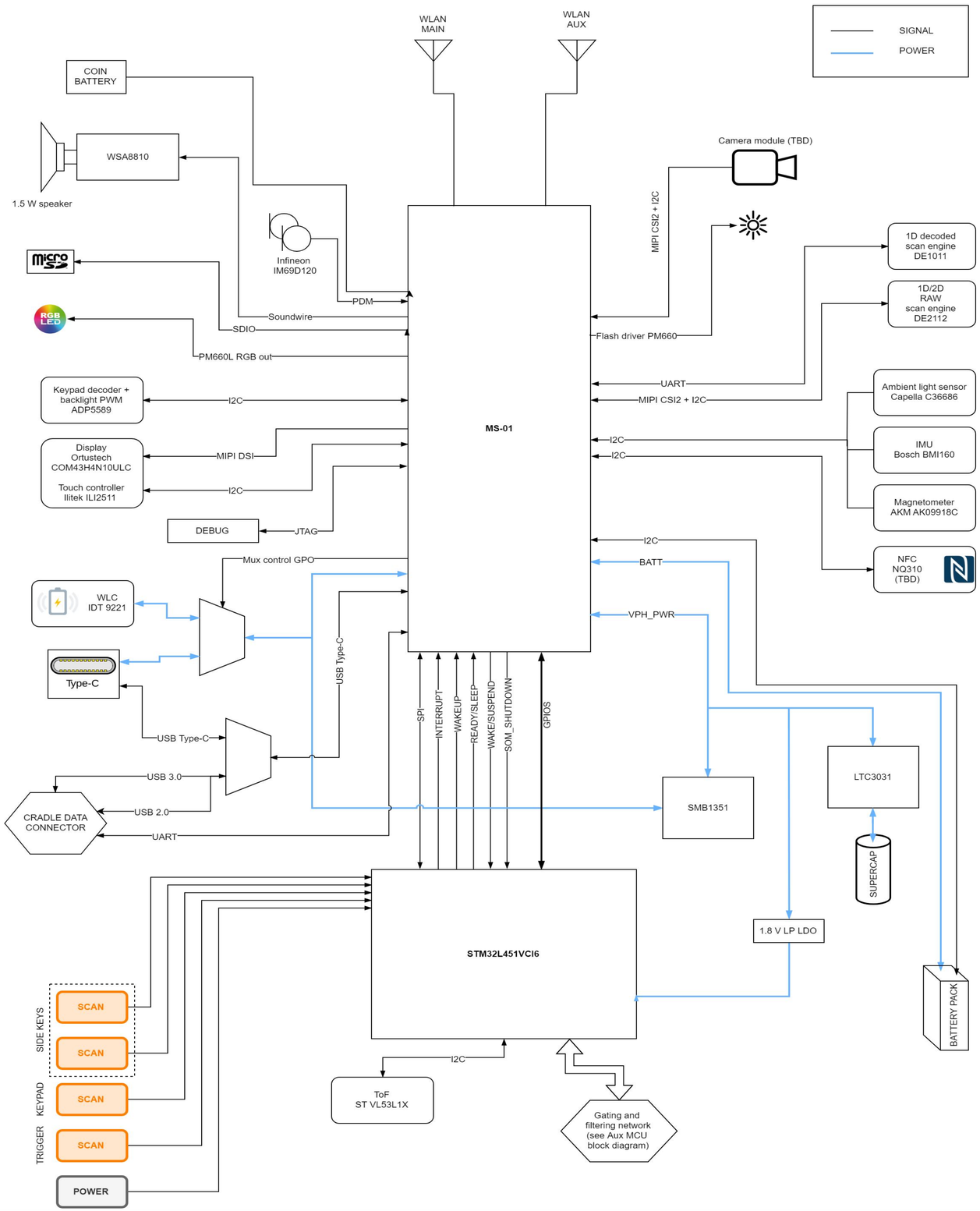
BLOCK DIAGRAM

REVISIONS							
REV	ZONE	NO.	DESCRIPTION	E.C.	BY	APVD.	DATE
			SEE SHEET 1				



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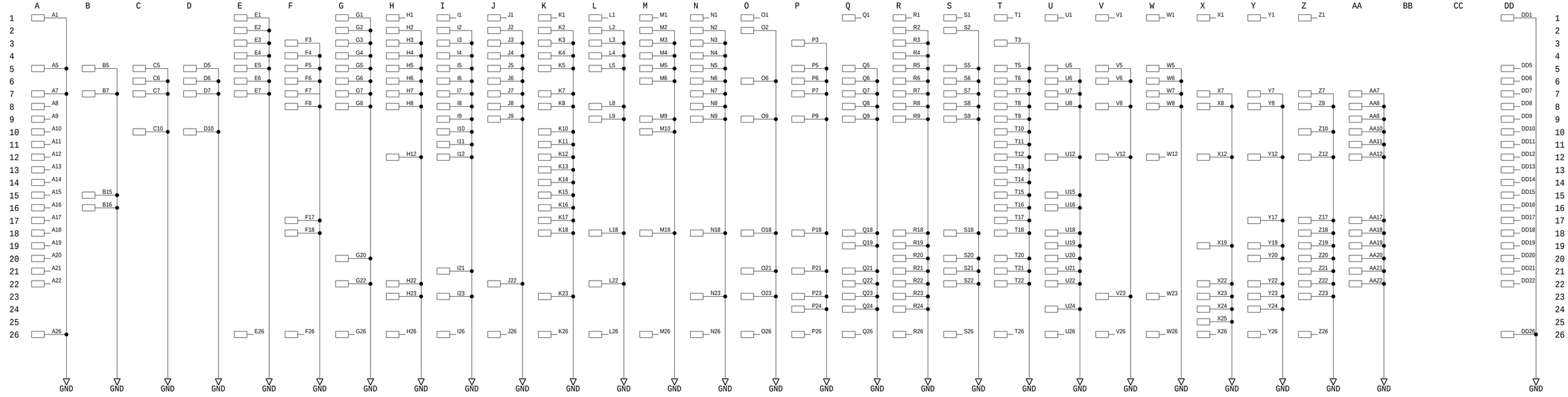
SOM660 WAN MODULE GND AND DUMMY PAD

REVISIONS							
REV	ZONE	NO.	DESCRIPTION	E.C.	BY	APVD.	DATE
			SEE SHEET 1				

U401

DUMMY_PAD
GND



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SIZE D	DWG. NO. REV V1D
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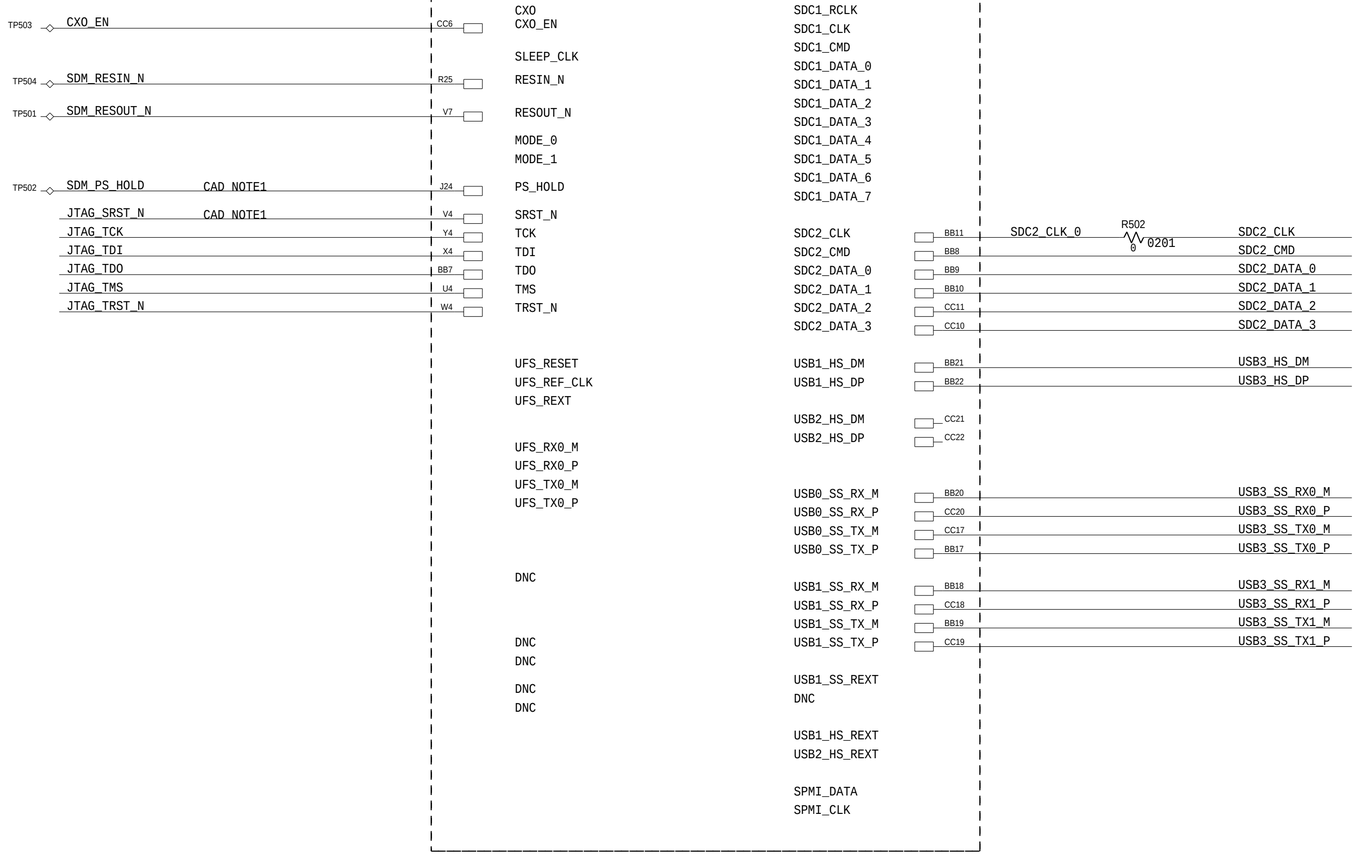
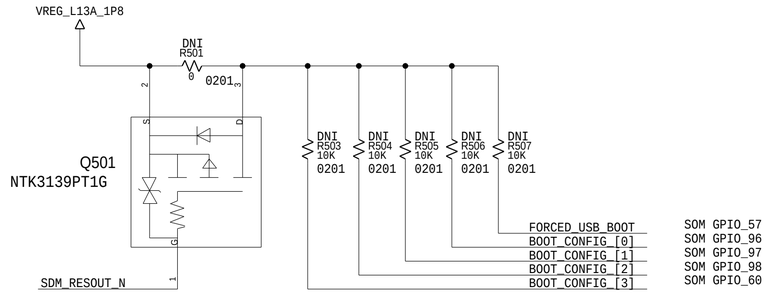
SDM660: CONTROL

REVISIONS						
REV	ZONE	NO.	DESCRIPTION	E.C.	BY	APVD.	DATE
			SEE SHEET 1				

CAD NOTE1
KEY SIGNAL, AWAY FOR NOISY TRACE



BOOT CONFIG



FASTBOOT_SEL[3:0]	BOOT OPTIONS
0b0000	eMMC @SDC1 --> SD @SDC2 --> USB
0b0001	SD @SDC2 -> eMMC @SDC1
0b0010	SD @SDC2
0b0011	USB
0b0100	UFS HS-G1
0b0101	SD @SDC2 --> UFS

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SDM660: GPIOS

REVISIONS							
REV	ZONE	NO.	DESCRIPTION	E.C.	BY	APVD.	DATE
			SEE SHEET 1				

SCAN ENGINE BLSP1

SPI	I2C	UART
MISO	N/C	RX
MOSI	N/C	TX
CS_N	SDA	CTS
CLK	SCL	RTS

GPIO

GPIO						
GPIO_0	Y6	TP633	BLSP1_SPI_MOSI	SCAN ENGINE SPI, I2C, UART		
GPIO_1	V17	TP634	BLSP1_SPI_MISO			
GPIO_2	X6	TP635	BLSP1_SPI_CS_N			
GPIO_3	X5	TP636	BLSP1_SPI_CLK			
GPIO_4	Y2		BLSP2_UART_TX	DEBUG UART		
GPIO_5	Z2		BLSP2_UART_RX			
GPIO_6	U10	TP603	BLSP2_I2C_SDA	SMB&NFC&TOUCH I2C		
GPIO_7	U11	TP604	BLSP2_I2C_SCL			
GPIO_8	AA13		NFC_EN			
GPIO_9	Y18	TP606	WSA_SPKR_SD_N			
GPIO_10	V2	TP607	BLSP3_I2C_SDA	BATTERY I2C		
GPIO_11	W2	TP608	BLSP3_I2C_SCL			
GPIO_12	T4	TP609	MCU_STAT_CTRL			
GPIO_13	AA6	TP610	MCU_WAKEUP			
GPIO_14	S4	TP611	BLSP4_I2C_SDA	TOUCH I2C		
GPIO_15	S3	TP612	BLSP4_I2C_SCL			
GPIO_16				BT/FM HCI UART		
GPIO_17						
GPIO_18						
GPIO_19						
GPIO_20	U17	TP637	MCU_STAT_FB			
GPIO_21	BB5	TP613	SMB_STAT	SMB1351 STATE		
GPIO_22	O7	TP655	BLSP6_SPI_CS_N	MCU SPI		
GPIO_23	O8	TP656	BLSP6_SPI_CLK			
GPIO_24	CC7		WSA_SWR_CLK	WSA8810 SWR		
GPIO_25	CC8		WSA_SWR_DAT			
GPIO_26	CC9	TP614	BLSP7_I2C_SDA	AUX BOARD I2C		
GPIO_27	BB6	TP615	BLSP7_I2C_SCL			
GPIO_28	O5	TP616	BLSP8_UART_TX	CRADLE UART		
GPIO_29	P4	TP617	BLSP8_UART_RX			
GPIO_30	O4		NFC_DWL_REQ			
GPIO_31	O3		NFC_INT_N			
GPIO_32	M22		CAM0_MCLK	CAM_MCLK	R601 0 0201	SDM_CAM0_MCLK
GPIO_33	N22		NOT USE			
GPIO_34	U9	TP632	SOM_GPIO_34			
GPIO_35	P25	TP654	SOM_GPIO_35			
GPIO_36	M19		CCI_I2C_SDA0	CAMERA I2C		
GPIO_37	M20		CCI_I2C_SCL0			
GPIO_38	T24		NOT USE			
GPIO_39	T23		NOT USE			
GPIO_40	S23	TP657	KEYBOARD_INT_FIL			
GPIO_41						
GPIO_42	V9	TP620	BATT_DET_FIL			
GPIO_43	L23		KEYPAD_ESC			
GPIO_44	J23		WLC_INT			
GPIO_45	S24	TP640	MCU_INT			
GPIO_46	O22		CAM0_RST_N			
GPIO_47	P22	TP641	USB_MUX_N_EN			
GPIO_48	S25	TP642	USB_MUX_SEL			
GPIO_49	N21	TP621	BLSP6_SPI_MOSI	MCU SPI		
GPIO_50	W9		CAM_AFVDD_EN			
GPIO_51	M21		CAM_AVDD_EN			
GPIO_52	K22	TP622	BLSP6_SPI_MISO	MCU SPI		
GPIO_53	AA14		LCD_RST_N	NOTE1	BOOT_CONFIG [14]	
GPIO_54	V15		SD_CARD_DET_N			
GPIO_55	AA5	TP623	CRADLE_CC1_RP			
GPIO_56	Z5	TP624	CRADLE_CC1_RD			

VDD_P3 POWER DOMAIN	GPIO_57	X20		FORCED_USB_BOOT		
	GPIO_58	Z24		ST_USB_PHY_PS		
	GPIO_59	T2		MCU_PROG_BOOT	TP625	
	GPIO_60	Z4	BOOT_CONFIG [3]	BOOT_CONFIG_[3]	TP649	NC
	GPIO_61	M8		KYPD_RST		
	GPIO_62	U2		MCU_PROG_RST	TP626	
	GPIO_63	Z6	BOOT_CONFIG [115]	NOTE1 GRN_SPOT_ON	TP643	
	GPIO_64	Y5	BOOT_CONFIG [12]	NOTE1 RED_SPOT_ON	TP644	
	GPIO_65	U23	BOOT_CONFIG [6]			
	GPIO_66	U3		TS_RESET_N		
	GPIO_67	X2		TS_INT_N		
	GPIO_68	W3		ACCL_GYRO_DRDY_INT	TP627	
	GPIO_69	Y3		ACCL_GYRO_EVENT_INT	TP628	
	GPIO_70	X3		MAG_INT_N	TP629	NC
	GPIO_71	Z3		ALPS_INT_N		
	GPIO_72	V3				
	GPIO_73	M7		SOM_GPIO_73	TP645	
	GPIO_74	X18		SOM_GPIO_74	TP650	
	GPIO_75	V16				
	GPIO_76	Z14		SCAN_N_SCAN_EN	TP646	
	GPIO_77	Z13		SCAN_N_ILLUM_EN	TP630	
	GPIO_78					
	GPIO_79	T25	[SDM_HAPT_PWM]			
	GPIO_80	J25	BOOT_CONFIG [9]	SOM_GPIO_80	TP647	
	GPIO_81					
	GPIO_82					
VDD_P6	GPIO_83	W24				
	GPIO_84	W25				
	GPIO_85	T19				
	GPIO_86	G24				
VDD_P5	GPIO_87	W17				
	GPIO_88	X17				
	GPIO_89	F24				
	GPIO_90	E25				
VDD_P3 POWER DOMAIN	GPIO_91	I17	[BUA}			
	GPIO_92	V24	BOOT_CONFIG [10]	NOTE1		
	GPIO_93	V25	BOOT_CONFIG [11]	NOTE1		
	GPIO_94	I24	BOOT_CONFIG [7]			
	GPIO_95	Y25	BOOT_CONFIG [8]			
	GPIO_96	Q25	BOOT_CONFIG [0]	BOOT_CONFIG [0]	TP651	
	GPIO_97	Z25	BOOT_CONFIG [1]	BOOT_CONFIG [1]	TP652	
	GPIO_98	U25	BOOT_CONFIG [2]	BOOT_CONFIG [2]	TP653	
	GPIO_99					
	GPIO_100					
	GPIO_101					
	GPIO_102					
	GPIO_103					
	GPIO_104					
	GPIO_105					
	GPIO_106					
	GPIO_107					
	GPIO_108					
	GPIO_109					
	GPIO_110					
	GPIO_111					
	GPIO_112					
	GPIO_113	CC5	BOOT_CONFIG [13]	NOTE1 SOM_GPIO_113	TP648	

TP631 — R603 0 0201 — USB_PHY_PS

DNI R602 10K 0201 — GND

RESISTOR	TYPE C	MICRO USB
R602	DNI	MOUNT
R603	MOUNT	DNI

SENSOR LOW POWER ISLAND (SLPI)
SNAPDRAGON SENSORS CORE (SSC)

WCI UART

UIM2 NC IN SX5

UIM1 NC IN SX5

RFFE

SW NOTE:
WLC_INT
DEFAULT PU OR NP

SW NOTE:
MCU_INT
DEFAULT PU OR NP

NOTE1: ENSURE THAT THERE ARE NO EXTERNAL PULLS ON THE GPIOS (53, 63, 64, 92, 93,113)
THE EXTERNAL PULLS CAN FORCE THE SDM DEVICE TO ENTER SECURE BOOT OR TO SELECT A DIFFERENT BOOT DEVICE.

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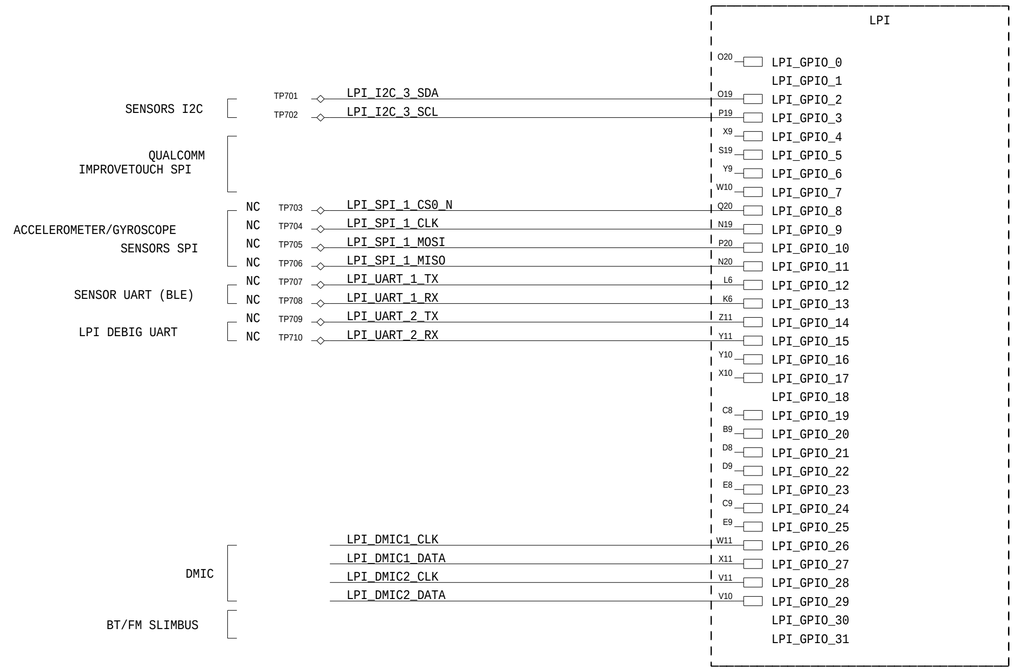
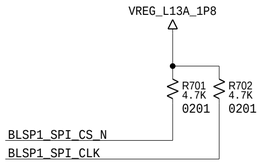
SDM660: LPI GPIOS

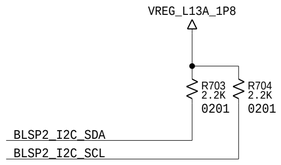
REVISIONS							
REV	ZONE	NO.	DESCRIPTION	E.C.	BY	APVD.	DATE
			SEE SHEET 1				



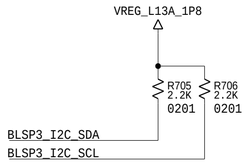


BLSP1
SCANNER

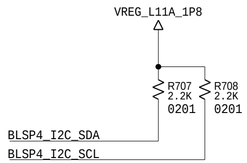
SCANNER INTERNAL 10K PULLUP TO VCC_IO
4.7K ADDITIONAL EXTERNAL PULLUP IS SUGGESTED



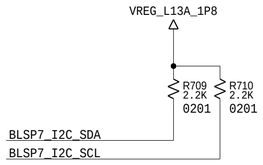
BLSP2
NFC & SMB



BLSP3
BATTERY PACK

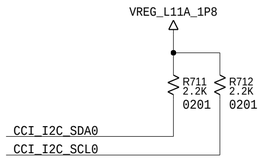


BLSP4
TOUCH

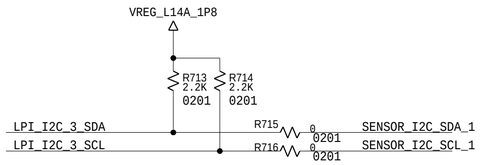


BLSP7
KEYPAD CONTROLLER
WIRELESS P9221

P9221 ADDRESS:	0X61
ADP5589	0X34



CC1
REAR CAMERAS



LPI I2C
SENSORS CORE

ALS ADDRESS:	0X60
GYRO ADDRESS:	0X68
E-COMPASS ADDRESS:	0X0C

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SDM660: MIPI-CSI/DSI

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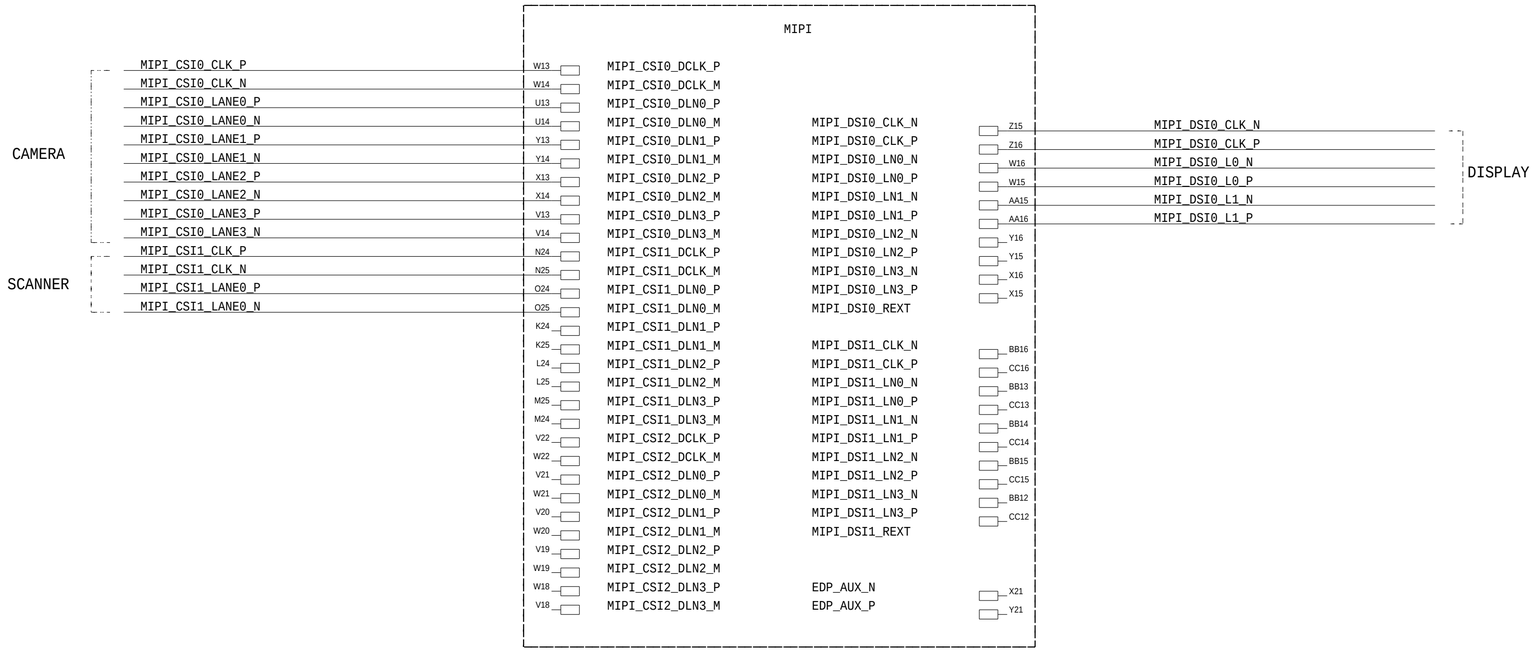
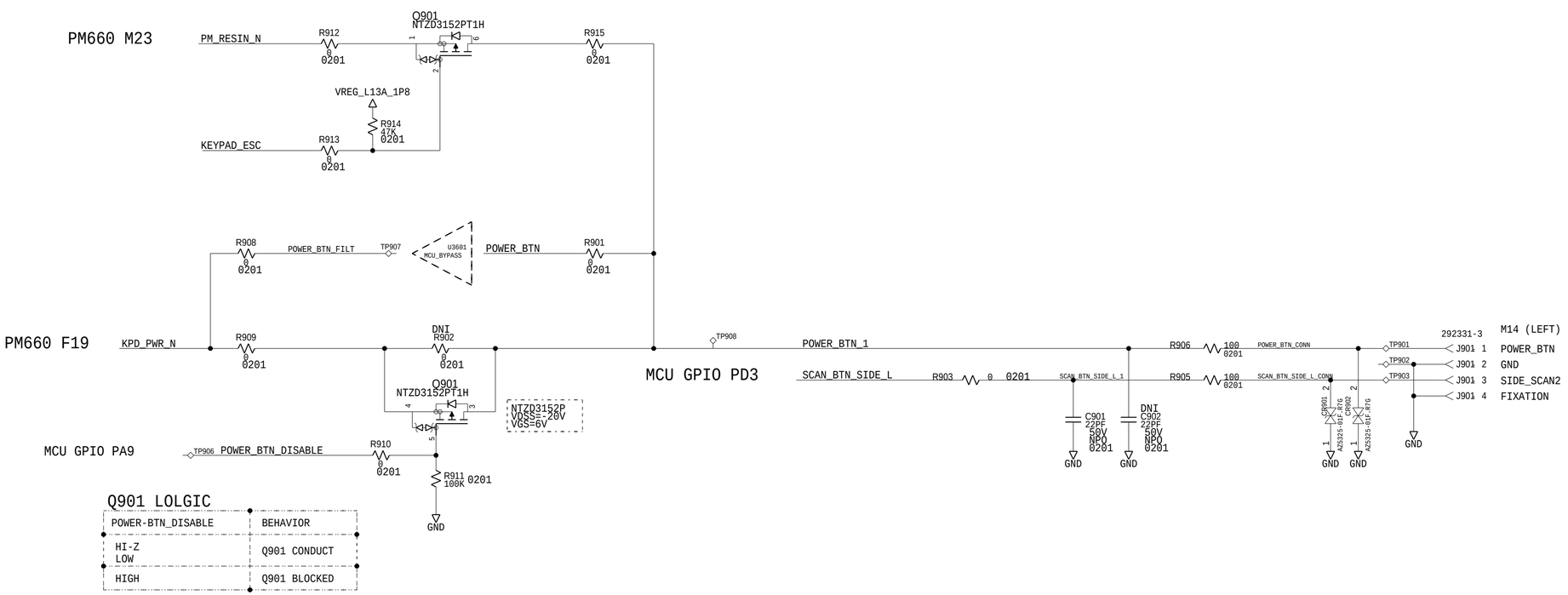


NOTE:IF BEST EMI PRACTICES ARE FOLLOWED FOR MIPI CSI/DSI SIGNALS, THERE IS NO NEED FOR COMMON MODE CHOKE FILTERS. YOU MAY CHOOSE TO HAVE PLACEHOLDERS FOR COMMON MODE DEPENDING UPON YOUR DESIGN CONSTRAINTS.

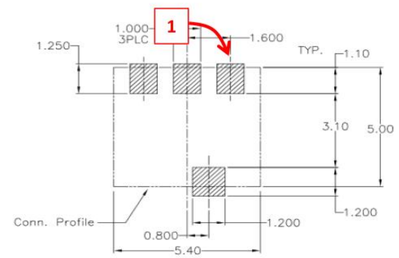
EXTREME CARE MUST BE TAKEN THAT NO STUBS ARE CREATED BY DOING SO.

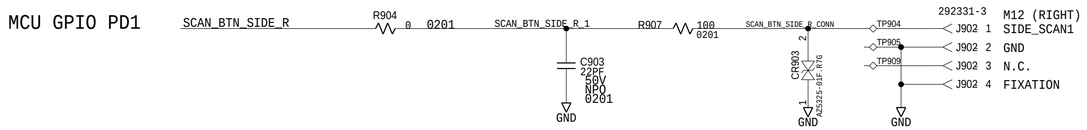
SIDE KEY(M12,M14)

REVISIONS							
REV	ZONE	NO.	DESCRIPTION	E.C.	BY	APVD.	DATE
			SEE SHEET 1				



TE 292331-3





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PM660: CHARGER

REVISIONS							
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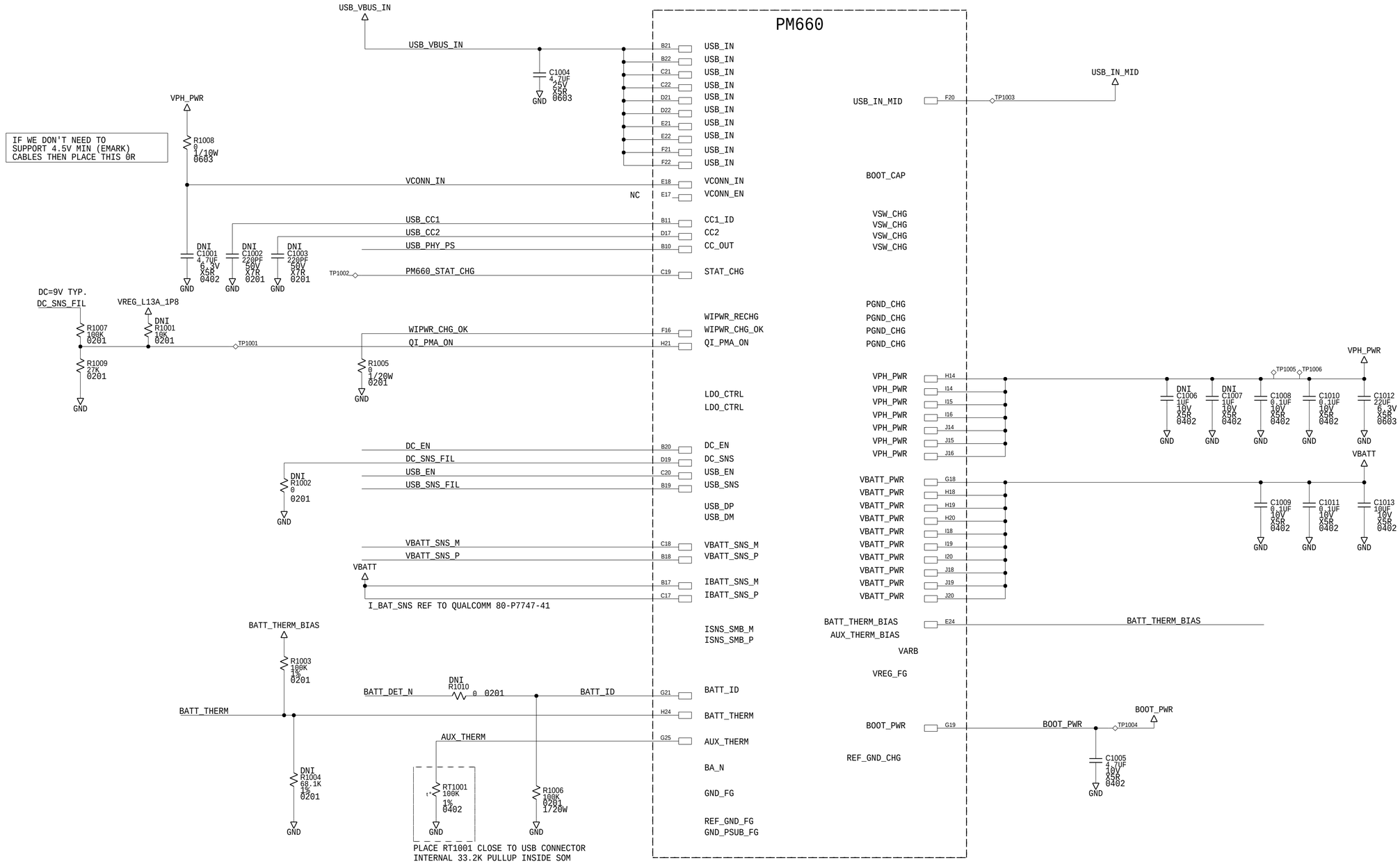
			SEE SHEET 1				



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USI CONFIDENTIAL MS-01 PRO DEV. BOARD	
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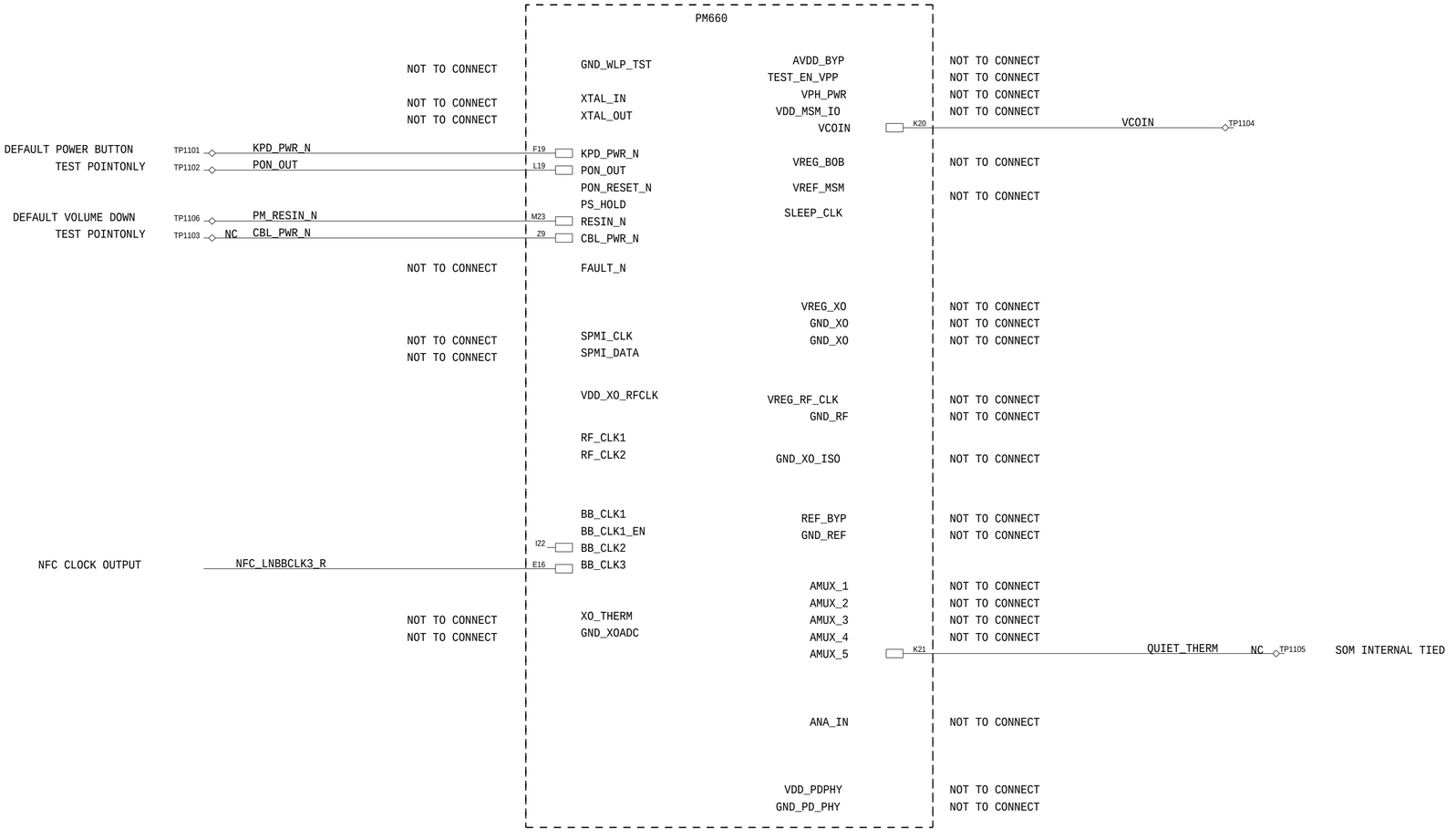
PM660:CONTROL/CLOCKS

REVISIONS							
REV	ZONE	NO.	DESCRIPTION	E.C.	BY	APVD.	DATE
			SEE SHEET 1				



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MS-01 PRO DEV. BOARD

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D		V1D

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REVISIONS							
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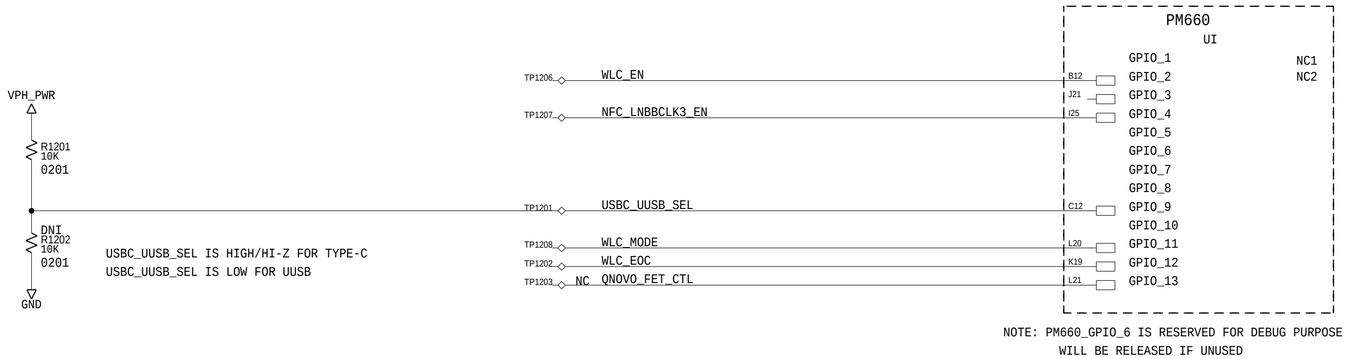
PM660:GPIOS

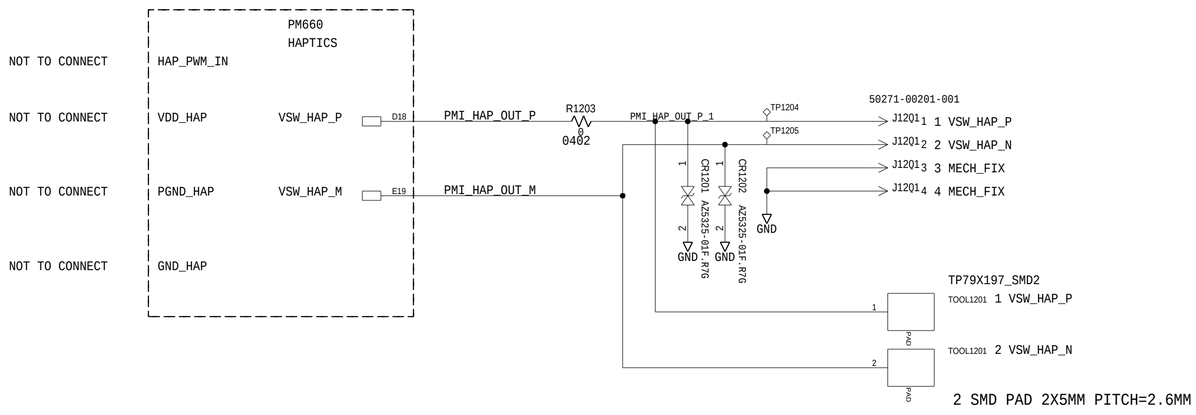


NOTE: PM660_GPIO_6 IS RESERVED FOR DEBUG PURPOSE
WILL BE RELEASED IF UNUSED

PM660 GPIO Configuration For QRD660

GPIO_1	OPTION1	GPIO_8	SLB
GPIO_2	DIV_CLK2	GPIO_9	uUSB_TYPEC
GPIO_3	DIV_CLK1	GPIO_10	WCSS_VCTRL
GPIO_4	NFC_CLK_REQ	GPIO_11	HOMEKEY_FP_PM_INT
GPIO_5	WLAN_SW_CTRL	GPIO_12	WIPWR_MODE
GPIO_6	SLP_CLK	GPIO_13	PM_A_GPIO_13
GPIO_7	UIM_BATT_ALARM		

PM660:HAPTICS(M21)



ACES 50271-00201-001

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PM660:SMPS

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PM660
VREG1

NOT TO CONNECT	VIN_S1	VREG_S1	NOT TO CONNECT
NOT TO CONNECT	VDD_S1		
		VSW_S1	NOT TO CONNECT
		VSW_S1	NOT TO CONNECT
NOT TO CONNECT	GND_S1	VSW_S1	NOT TO CONNECT
NOT TO CONNECT	GND_S1		
		VREF_NEG_S1	NOT TO CONNECT
NOT TO CONNECT	VDD_S2	VREG_S2	NOT TO CONNECT
NOT TO CONNECT	VDD_S2		
		VSW_S2	NOT TO CONNECT
		VSW_S2	NOT TO CONNECT
NOT TO CONNECT	GND_S2	VSW_S2	NOT TO CONNECT
NOT TO CONNECT	GND_S2	VSW_S2	NOT TO CONNECT
		VREF_NEG_S2	NOT TO CONNECT
NOT TO CONNECT	VDD_S3	VREG_S3	NOT TO CONNECT
NOT TO CONNECT	VDD_S3		
NOT TO CONNECT	GND_S3	VSW_S3	NOT TO CONNECT
NOT TO CONNECT	GND_S3	VSW_S3	NOT TO CONNECT
		VSW_S3	NOT TO CONNECT
		VREF_NEG_S3	NOT TO CONNECT
			NOT TO CONNECT
NOT TO CONNECT	VDD_S4	VREG_S4	NOT TO CONNECT
NOT TO CONNECT	VDD_S4		NOT TO CONNECT
NOT TO CONNECT	VDD_S4		
		VSW_S4	NOT TO CONNECT
		VSW_S4	NOT TO CONNECT
		VSW_S4	
NOT TO CONNECT	GND_S4		
NOT TO CONNECT	GND_S4		
NOT TO CONNECT	VDD_S5	VREG_S5	
NOT TO CONNECT	VDD_S5		
		VSW_S5	NOT TO CONNECT
		VSW_S5	NOT TO CONNECT
NOT TO CONNECT	GND_S5		
NOT TO CONNECT	GND_S5		
NOT TO CONNECT	VDD_S6	VREG_S6	NOT TO CONNECT
			NOT TO CONNECT
		VSW_S6	NOT TO CONNECT
NOT TO CONNECT	GND_S6	VSW_S6	NOT TO CONNECT

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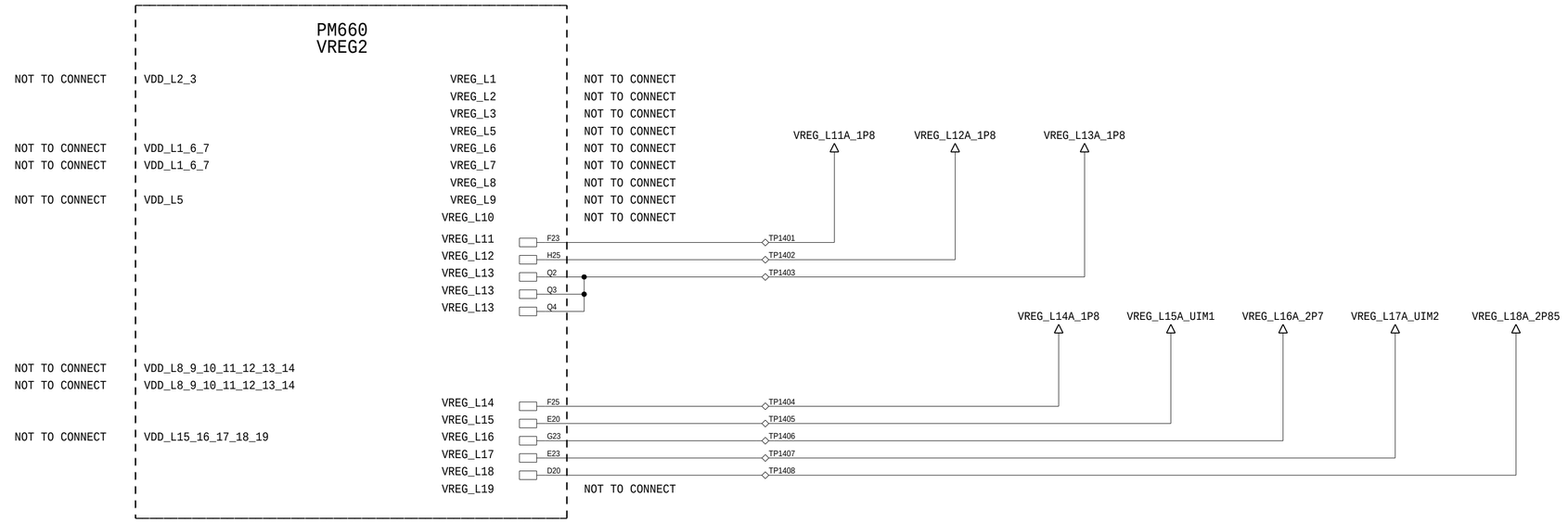
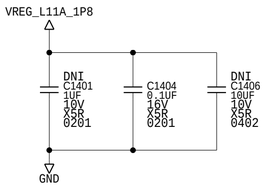
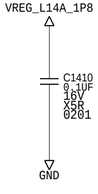
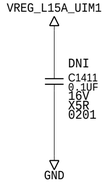
REV	ZONE	NO.	DESCRIPTION	E.C.	BY	APVD.	DATE
			SEE SHEET 1				

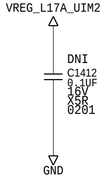
PM660:LDO

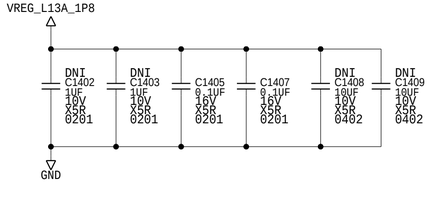












PSEUDO CAPLESS LDOS

(LDO8A , LDO9A, LDO11A , LDO12A , LDO14A , LDO15A , LDO16A , LDO17A , LDO18A , LDO19A)

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SIZE	DWG. NO.	REV
D		V1D

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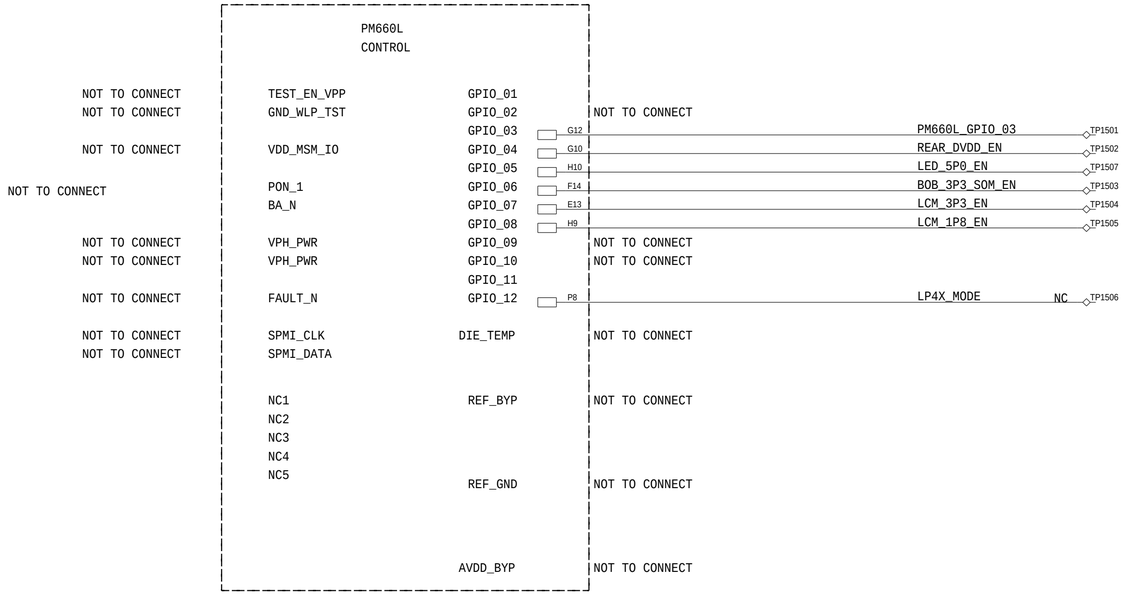
PM660L:GPIOS

REVISIONS							
REV	ZONE	NO.	DESCRIPTION	E.C.	BY	APVD.	DATE
			SEE SHEET 1				



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MS-01 PRO DEV. BOARD

SIZE	DWG. NO.	REV
D		V1D

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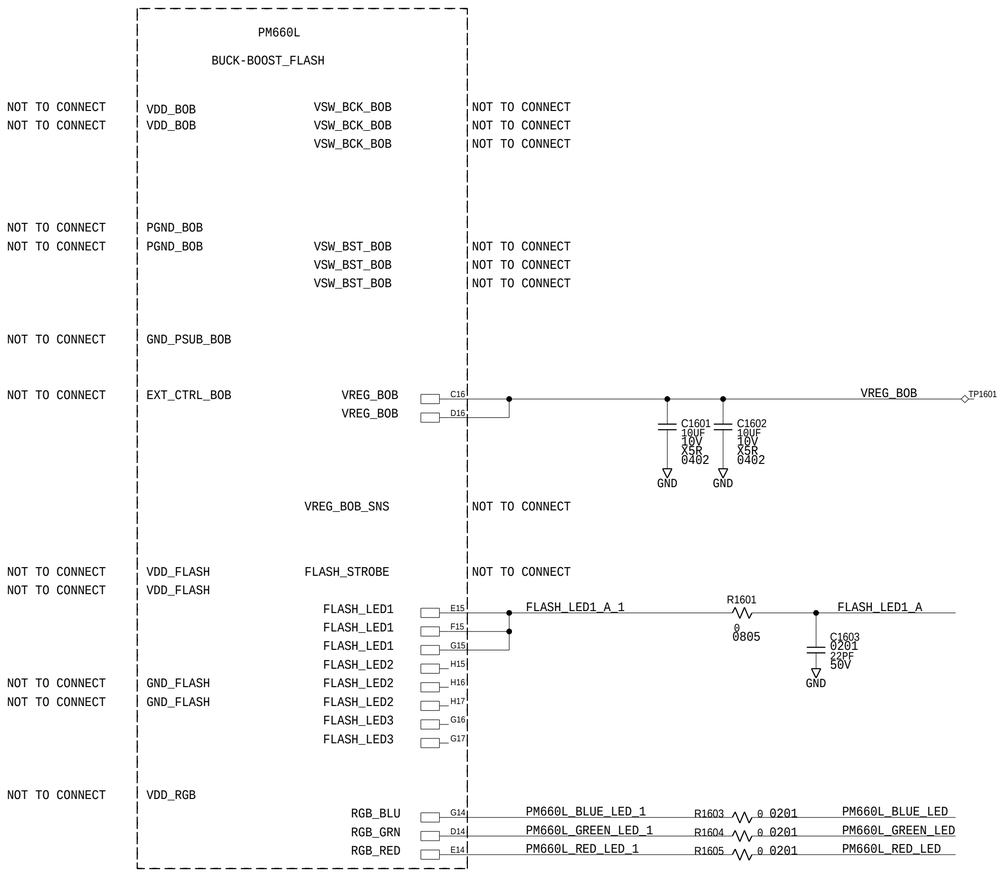
PM660L:BOB_FLASH

REVISIONS							
REV	ZONE	NO.	DESCRIPTION	E.C.	BY	APVD.	DATE
			SEE SHEET 1				



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MS-01 PRO DEV. BOARD

SIZE	DWG. NO.	REV
D		V1D

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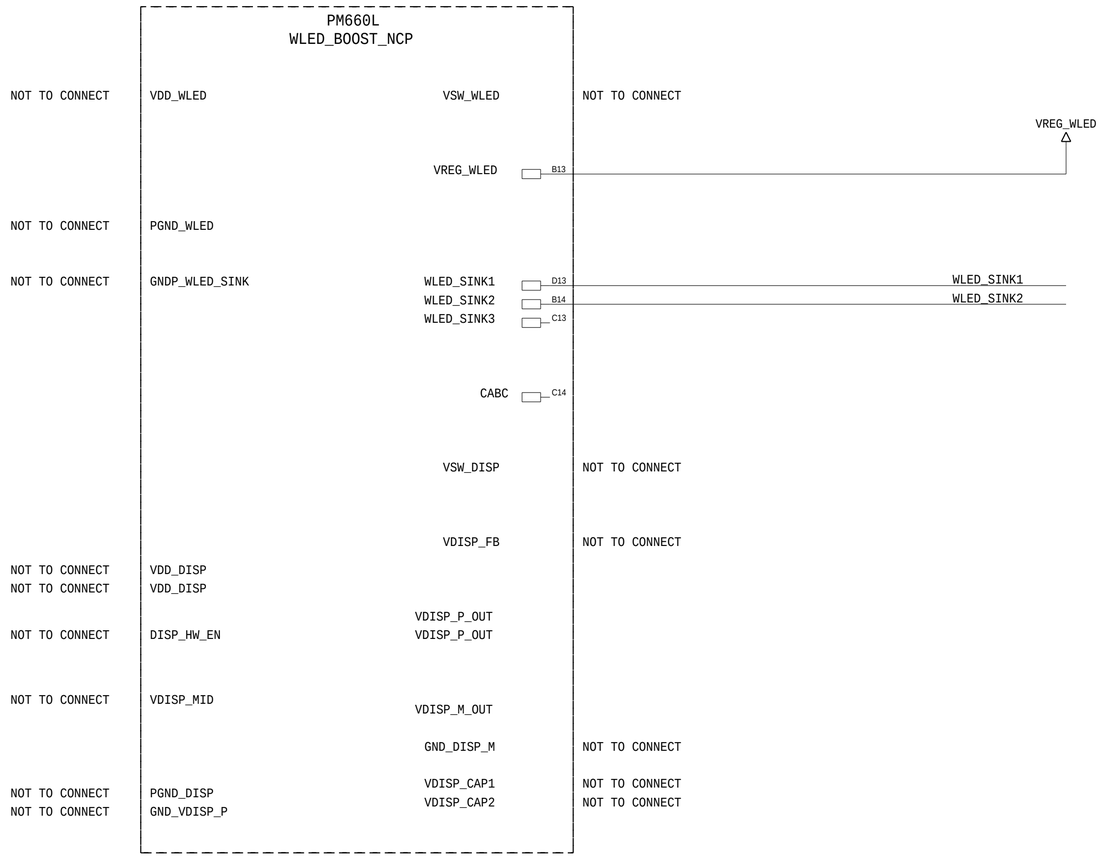
PM660L:WLED_LAB/IBB

REVISIONS							
REV	ZONE	NO.	DESCRIPTION	E.C.	BY	APVD.	DATE
			SEE SHEET 1				



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MS-01 PRO DEV. BOARD

SIZE	DWG. NO.	REV
D		V1D

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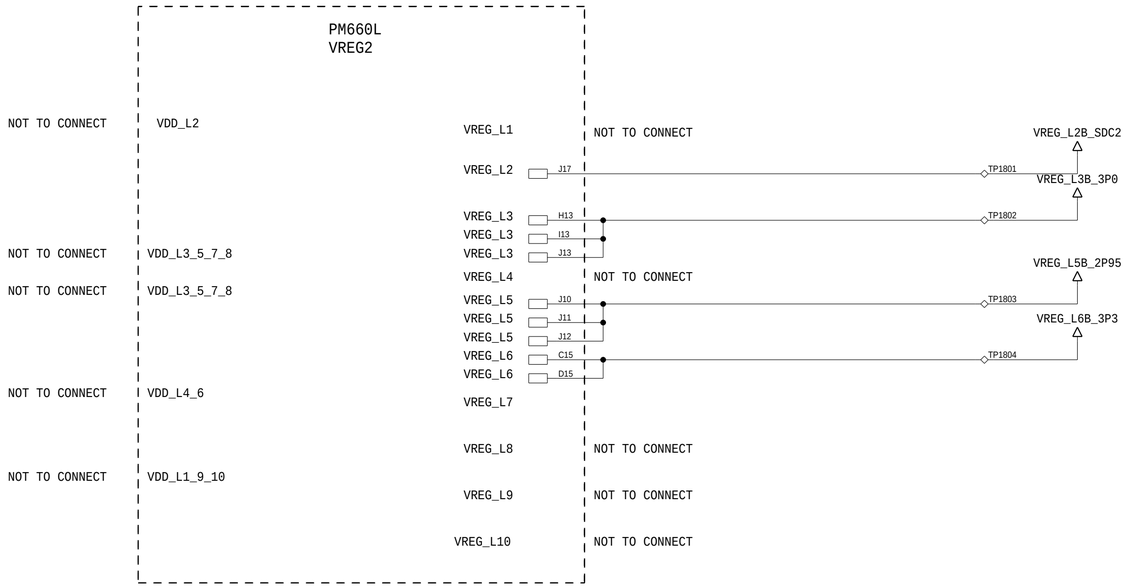
PM660L:LDOS

REVISIONS							
REV	ZONE	NO.	DESCRIPTION	E.C.	BY	APVD.	DATE
			SEE SHEET 1				



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MS-01 PRO DEV. BOARD

SIZE	DWG. NO.	REV
D		V1D

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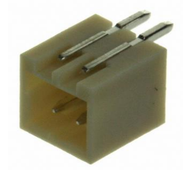
SUPERCAP(M9)

REVISIONS							
REV	ZONE	NO.	DESCRIPTION	E.C.	BY	APVD.	DATE
			SEE SHEET 1				



SUPERCAP CONN

5-1775444-2

J1901 1 SCAP_POS

J1901 2 SCAP_NEG

CR1901 AZ5325-01F.R7G

VCAP=2.595V

$V_{CAP} = 1.095V \cdot \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$

U1901 LTC3110IUF#TRPBF

L1901 0624CDMCCDS-2R2MC 2.2UH

SCAP_MODE
HIGH=PWM MODE
LOW=BURST MODE

SCAP_RUN
HIGH=RUN
LOW=DISABLE

SGND TIE TOGETHER FIRST

BACKUP MODE VOLTAGE

LOGIC	VPH_PWR_SCAP
LOPOWER=0	3.099V
LOPOWER=1	3.197V

$V_{SYS} = 0.6V \cdot \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$

BACKUP MODE THRESHOLD

NCHRG=0	3.254V
NCHRG=1	3.354V

$V_{TH(DIR\_RISING)} = 1.095V \cdot \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$

$V_{TH(DIR\_FALLING)} = 1.045V \cdot \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$

CAP CHARGE CURRENT SETTING

PLACE R1939 R1940 C1906 C1918 CLOSE TO IC U1901

CTRL TABLE

BIT0	BIT1	IVSYS
HI-Z	HI-Z	0.2A
0	0	0.2A
0	1	1A
1	0	0.55A
1	1	1A

$I_{VSYS} = \frac{3k\Omega}{R_{PROG}}$

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SIZE	DWG. NO.	REV
D		V1D

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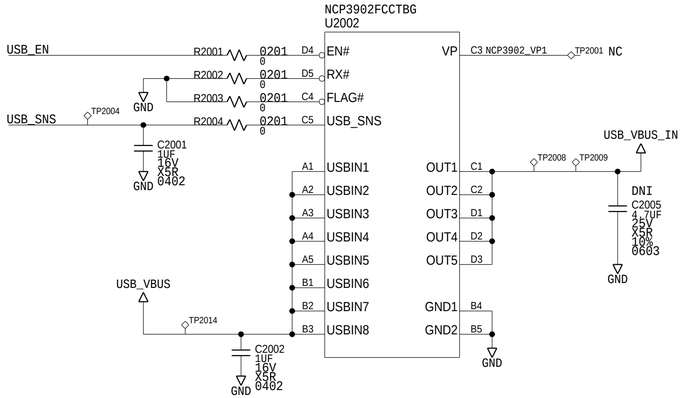
NCP3902 POWER MUX

REVISIONS						
REV	ZONE	NO.	DESCRIPTION	E.C.	BY	APVD.	DATE
			SEE SHEET 1				

USB POWER MUX



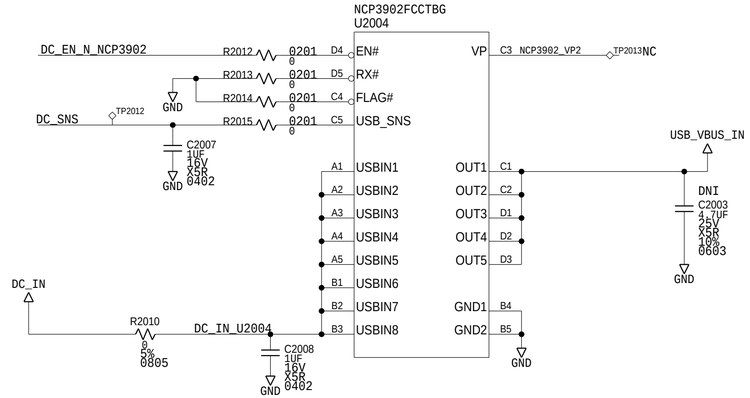
NCP3902 VP SETTING

VP PIN	OVP THRESHOLD
FLOATING	13V
GND	17V

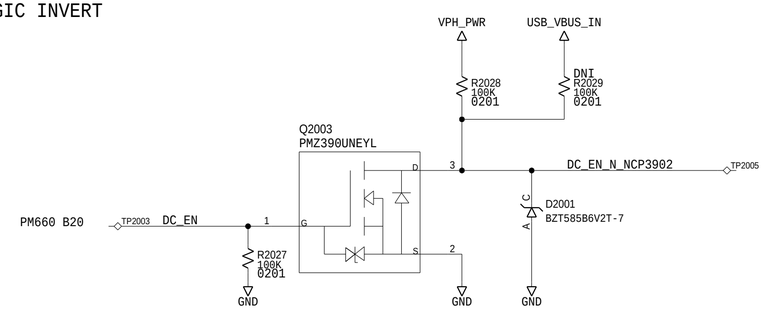
NCP3902 SWITCH

NET NAME	LOGIC	BEHAVIOR
NCP3902_EN#	LOW	USBIN CONDUCT TO OUT
	HIGH	OUT DISCONNECT OUT DISCHARGE

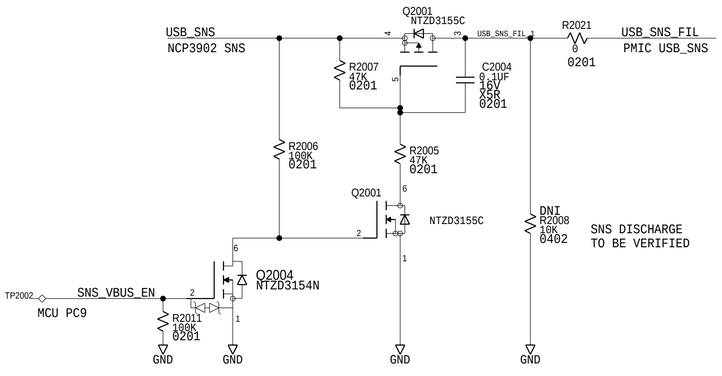
DC POWER MUX



DC_EN LOGIC INVERT

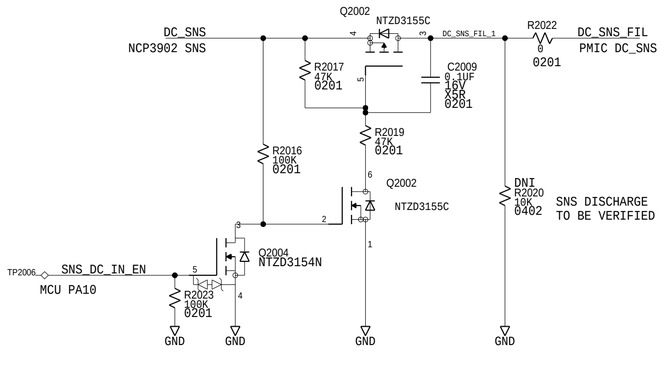


SNS BYPASS BY MCU



Q2001, Q2002 LOGIC

NET NAME	LOGIC	BEHAVIOR
SNS_VBUS_EN SNS_DC_IN_EN	LOW HI-Z	Q2001 CONDUCT Q2002 CONDUCT
	HIGH	Q2001 BLOCK Q2002 BLOCK



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MS-01 PRO DEV. BOARD

SIZE	DWG. NO.	REV
D		V1D

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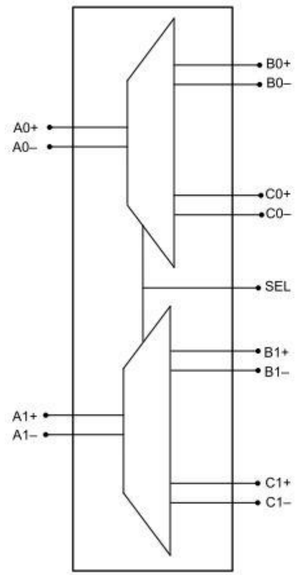
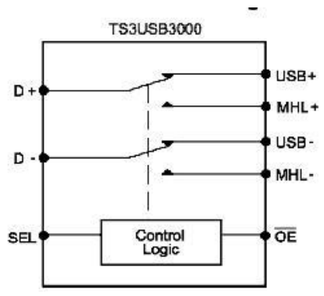
USB MUX

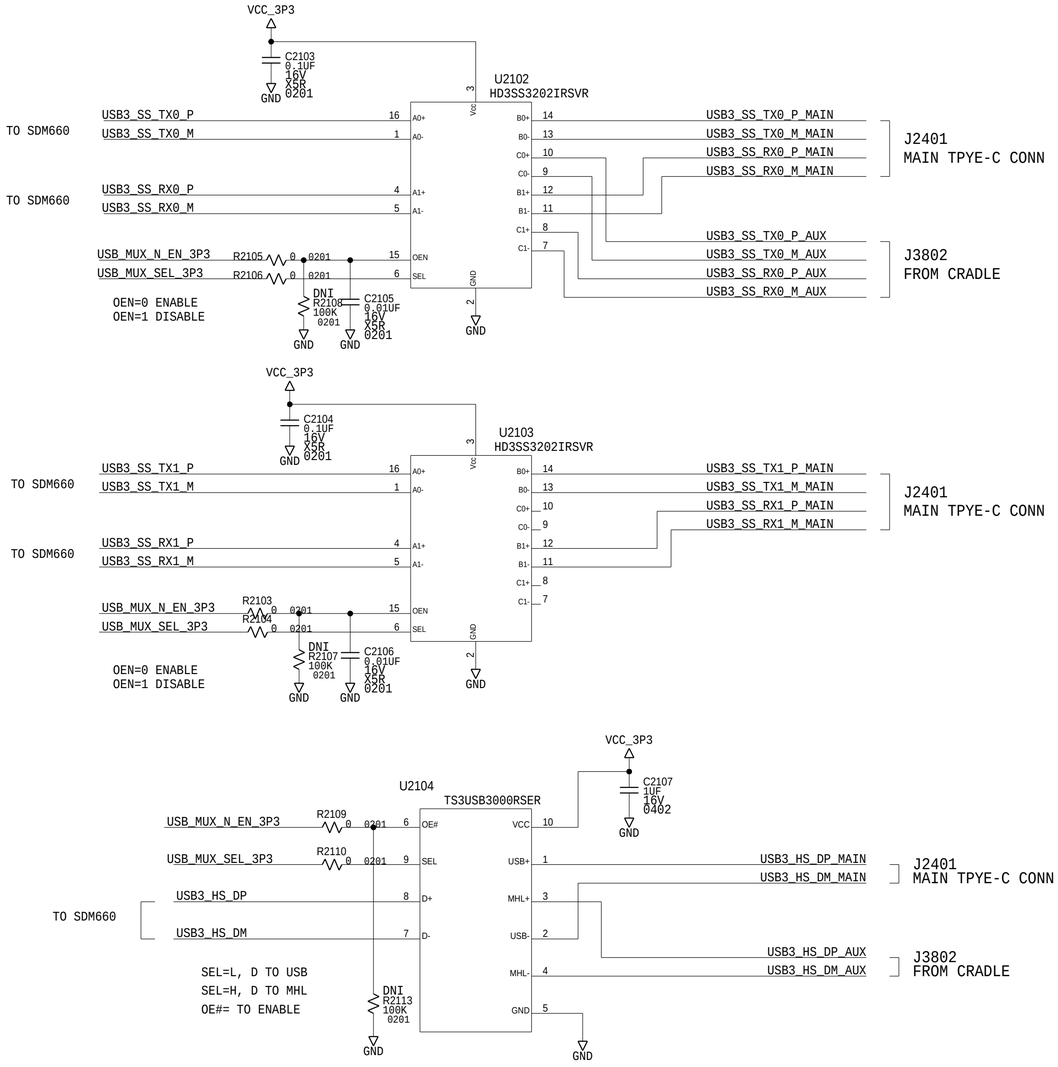
REVISIONS							
REV	ZONE	NO.	DESCRIPTION	E.C.	BY	APVD.	DATE
			SEE SHEET 1				

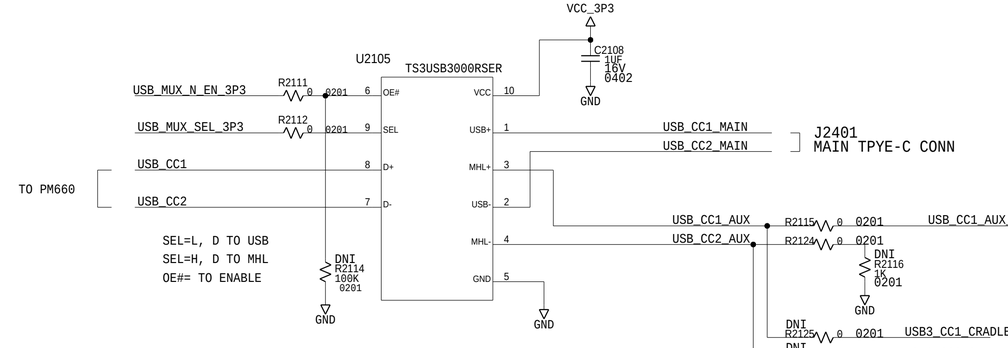


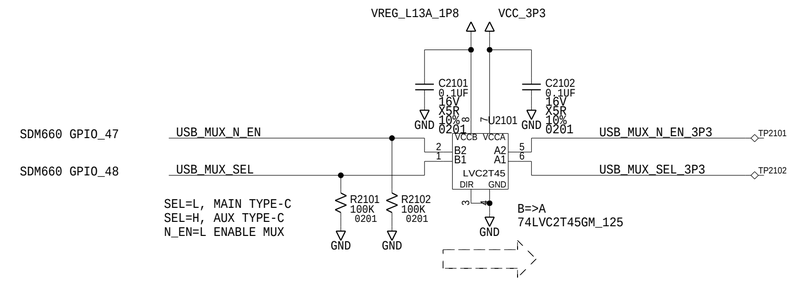
PORT A CHANNEL	PORT B OR PORT C CHANNEL CONNECTED TO PORT A CHANNEL	
	SEL = L	SEL = H
A0p	B0p	C0p
A0n	B0n	C0n
A1p	B1p	C1p
A1n	B1n	C1n



SEL	$\overline{OE}$	SWITCH STATUS
X	High	Both USB and MHL switches in High-Z
Low	Low	D+/D– to USB+/USB–
High	Low	D+/D– to MHL+/MHL–







H = HIGH voltage level;
L = LOW voltage level;
Z = high-impedance OFF-state.

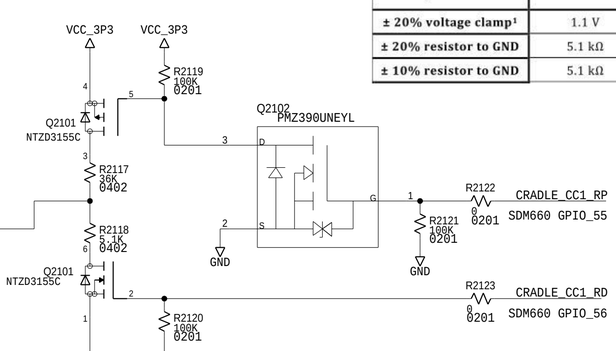
State	DIR CTRL	I/O-1	I/O-2	Description
1	H	output	input	system-1 data to system-2
2	H	Z	Z	system-2 is getting ready to send data to system-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on bus hold
3	L	Z	Z	DIR bit is set LOW. I/O-1 and I/O-2 still are disabled. The bus-line state depends on bus hold
4	L	input	output	system-2 data to system-1

Table 4-20 Source CC Termination (Rp) Requirements

Source Advertisement	Current Source to 1.7 – 5.5 V	Resistor pull-up to 4.75 – 5.5 V	Resistor pull-up to 3.3 V ± 5%
Default USB Power	80 µA ± 20%	56 kΩ ± 20% (Note 1)	36 kΩ ± 20%
1.5 A @ 5 V	180 µA ± 8%	22 kΩ ± 5%	12 kΩ ± 5%
3.0 A @ 5 V	330 µA ± 8%	10 kΩ ± 5%	4.7 kΩ ± 5%

Table 4-21 Sink CC Termination (Rd) Requirements

Rd Implementation	Nominal value	Can detect power capability?	Max voltage on pin
± 20% voltage clamp[1]	1.1 V	No	1.32 V
± 20% resistor to GND	5.1 kΩ	No	2.18 V
± 10% resistor to GND	5.1 kΩ	Yes	2.04 V



CRADLE_CC1 CONFIG		
RP	RD	REMARK
L	L	NOT ATTACHED
L	H	SDM660 HOST
H	L	SDM660 SLAVE
H	H	NOT ALLOWED

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SIZE	DWG. NO.	REV
D		V1D
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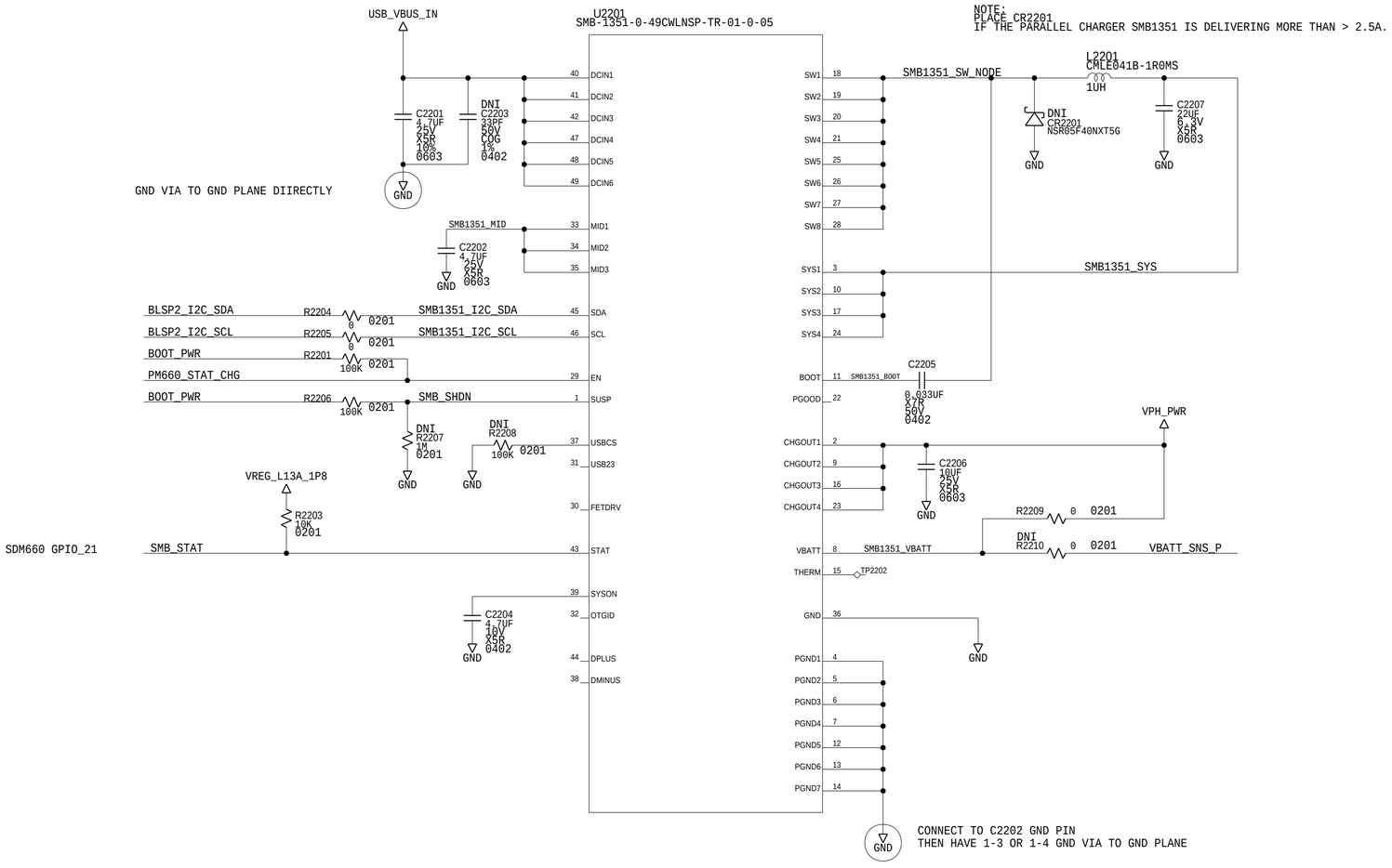
SMB1351

REVISIONS							
REV	ZONE	NO.	DESCRIPTION	E.C.	BY	APVD.	DATE
			SEE SHEET 1				



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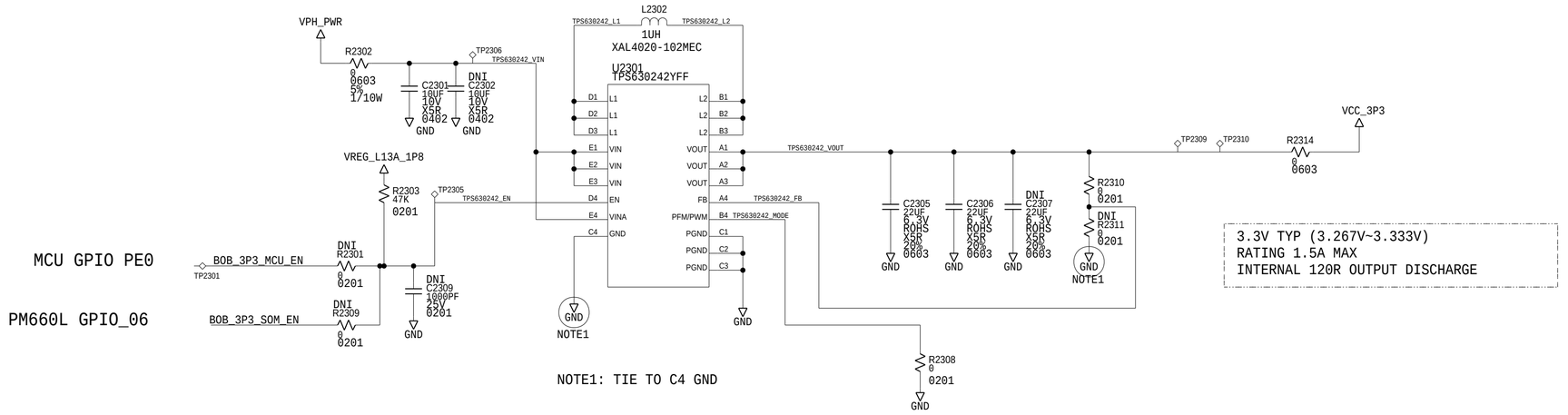
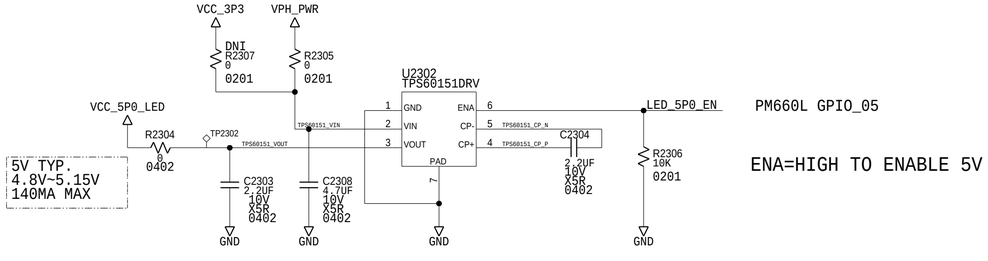
SIZE D	DWG. NO. REV V1D
Fri May 03 11:44:30 2019	SHEET 22 OF 45

POWER RAIL

REVISIONS							
REV	ZONE	NO.	DESCRIPTION	E.C.	BY	APVD.	DATE
			SEE SHEET 1				



3V3 BUCK-BOOST TPS60242



5V0 CHARGE PUMP TPS60151

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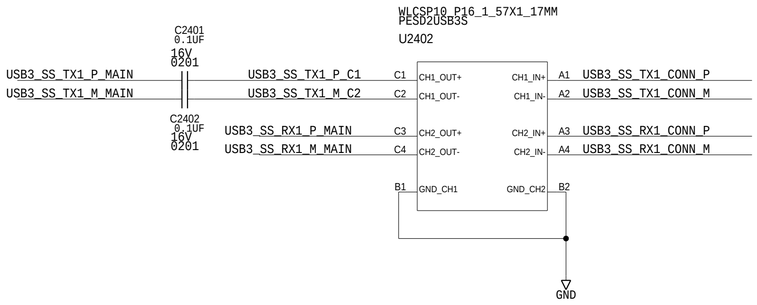
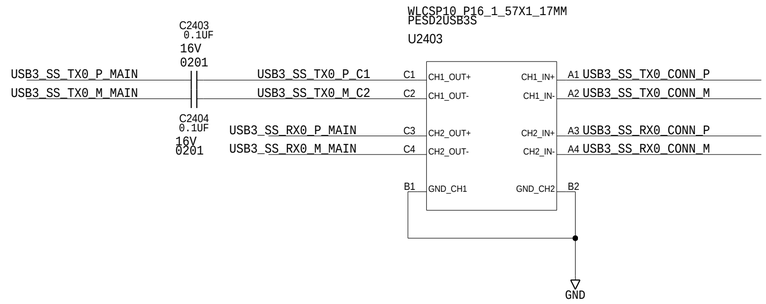
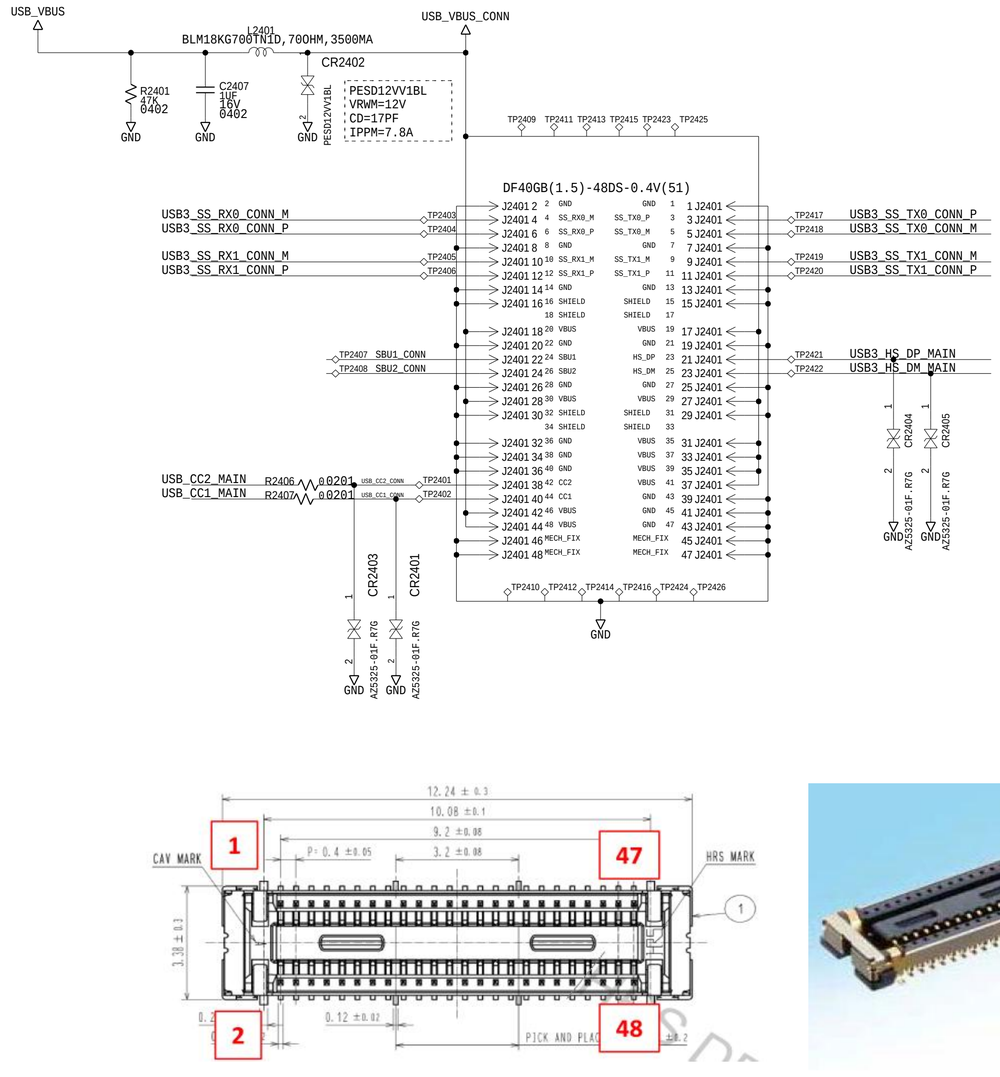
SIZE D	DWG. NO.		REV V1D
Tue Apr 30 15:04:34 2019		SHEET 23 OF 45	

MAIN TYPE C(M11)

REVISIONS							
REV	ZONE	NO.	DESCRIPTION	E.C.	BY	APVD.	DATE
			SEE SHEET 1				







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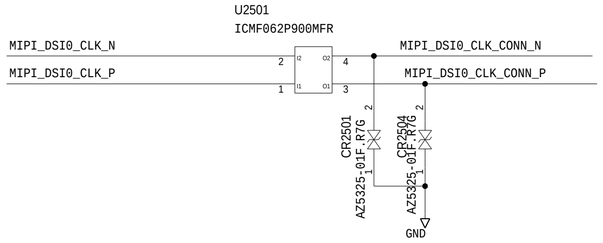
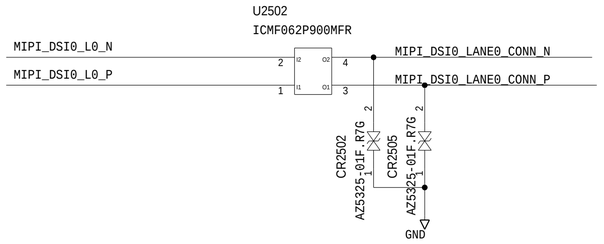
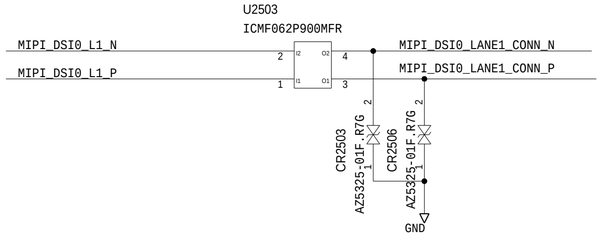
SIZE D	DWG. NO.	REV V1D
Tue Apr 30 15:04:35 2019	SHEET 24 OF 45	

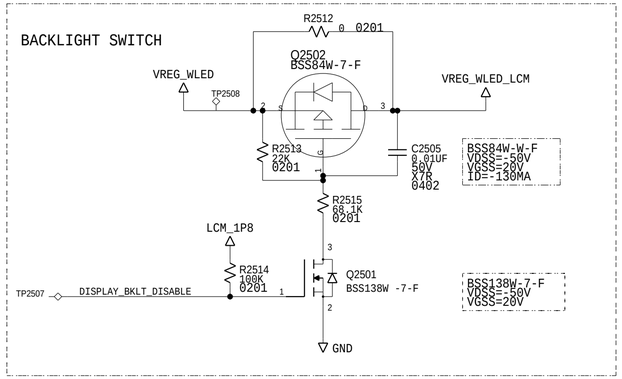
DISPLAY INTERFACE(M6)

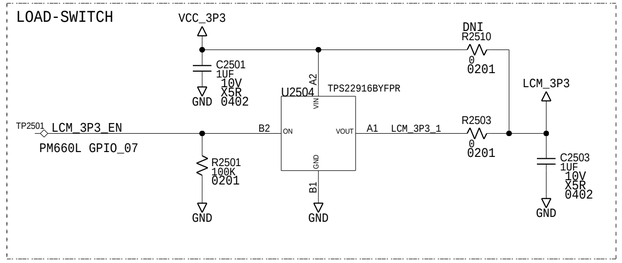
REVISIONS							
REV	ZONE	NO.	DESCRIPTION	E.C.	BY	APVD.	DATE
			SEE SHEET 1				

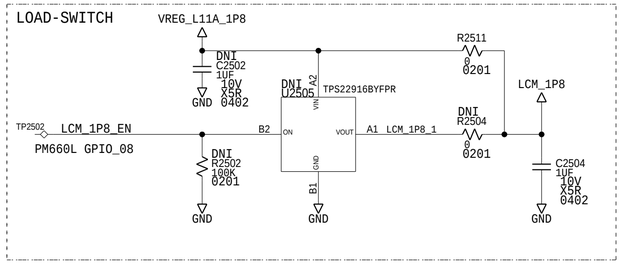


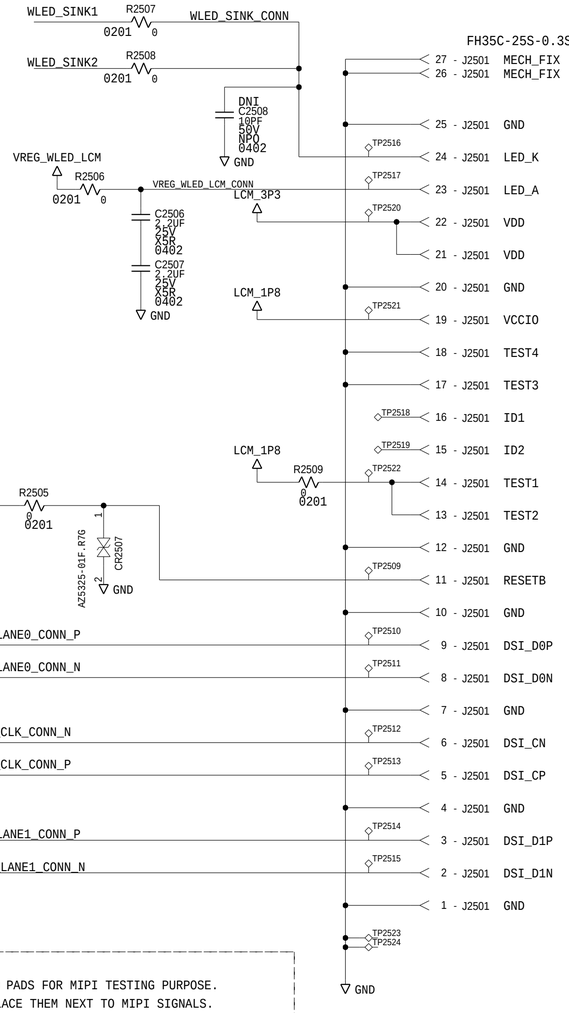










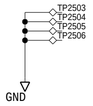


FPC PIN1 MAPPED TO CONN PIN25

FPC PINOUT

No.	Symbol	Details	Remark	IO
1	GND	Ground		P
2	LED-	Backlight LED Cathode		P
3	LED+	Backlight LED Anode		P
4	VDD	Analog Power Supply	VDD = 3.3V (TYP)	P
5	VDD	Analog Power Supply	VDD = 3.3V (TYP)	P
6	GND	Ground(PVSS)		P
7	VCCIO	DSI and I/O Power Supply	VCCIO = 1.8V (TYP)	P
8	TEST 4	Serial communication pin for shipping inspection	Please connect this pin to GND.	I
9	TEST 3	Serial communication pin for shipping inspection	Please connect this pin to GND.	I
10	ID1	ID check	Output level is GND.	O
11	ID2	ID check	Output level is GND.	O
12	TEST 1	Serial communication pin for shipping inspection	Please connect this pin to VCCIO(1.8V)	I
13	TEST 2	Serial communication pin for shipping inspection	Please connect this pin to VCCIO(1.8V)	I
14	GND	Ground		P
15	RESETB	LCD Reset	L:Initialize Power_ON Reset is Required when Turning on the Power	I
16	GND	Ground		P
17	DSI_D0P	MIPI-DSI Data differential signal input pin (Data lane 0)		IO
18	DSI_D0N	MIPI-DSI Data differential signal input pin (Data lane 0)		IO
19	GND	Ground		P
20	DSI_CN	MIPI-DSI Clock differential signal input pin		I
21	DSI_CP	MIPI-DSI Clock differential signal input pin		I
22	GND	Ground		P
23	DSI_D1P	MIPI-DSI Data differential signal input pin (Data lane 1)		I
24	DSI_D1N	MIPI-DSI Data differential signal input pin (Data lane 1)		I
25	GND	Ground		P

GND PADS FOR MIPI TESTING PURPOSE.
PLACE THEM NEXT TO MIPI SIGNALS.



7.1.1 Display Module

(Unless otherwise noted, Ta=25 °C,VDD=3.3V,VCCIO=1.8V,GND=0V)

Item	Symbol	Condition	Rating			Unit	Applicable terminal
			MIN	TYP	MAX		
Input Signal Voltage	VIH	VCCIO=1.7-1.9V	0.7×VCCIO	-	VCCIO	V	RESETB
	VIL		0	-	0.3×VCCIO	V	TEST1-4
Operating Current	IDD	fDSICLK=150 MHz	-	12.5	25.0	mA	VDD
	ICCIO	Color bar display	-	3.3	6.6	mA	VCCIO
Sleep_mode Current	IDDS	Clock/Data=LP11	-	43	100	uA	VDD
	ICCIOS	Sleep_mode	-	10	100	uA	VCCIO

7.1.3 Backlight

Item	Symbol	Condition	Rating			Unit	Applicable terminal
			MIN	TYP	MAX		
Forward current	IL25	Ta=25 °C	--	7.0	35	mA	LED+ - LED-
	IL70	Ta=70 °C	--	--	15	mA	
Forward voltage	VL	Ta=25 °C IL=7.0mA	--	18.9	21.0	V	
Estimated Life of LED	LL	Ta=25 °C IL=7.0mA Note	--	20000	--	hrs	

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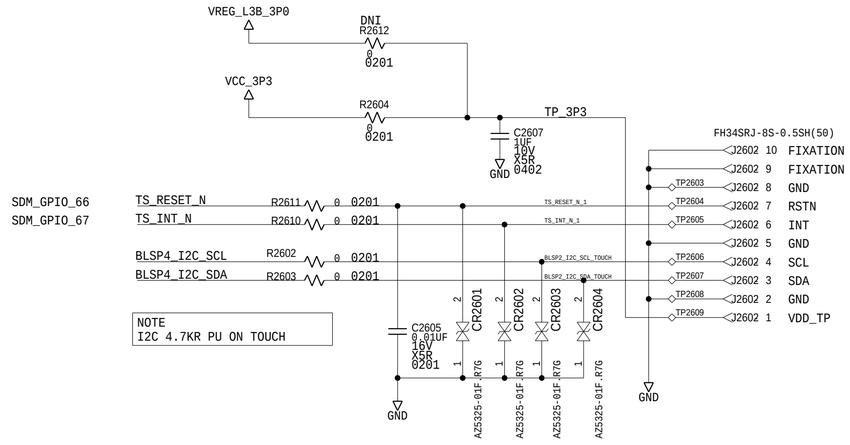
TOUCH PANNEL(M7)

REVISIONS							
REV	ZONE	NO.	DESCRIPTION	E.C.	BY	APVD.	DATE
			SEE SHEET 1				



FPC PIN1 MAPPED TO CONN PIN8

FPC PINOUT

TP_FPC

No.	Symbol	Details	Remark	IO
1	GND	Ground	GND	P
2	RSTN	External hardware reset input	I/O = 1.8V (TYP) ,Low active	I
3	INT	Interrupt output	I/O = 1.8V (TYP)	O
4	GND	Ground	GND	P
5	SCL	I2C interface, clock input	I/O = 1.8V (TYP) ,Note1	I/O
6	SDA	I2C interface, data input	I/O = 1.8V (TYP) ,Note1	I/O
7	GND	Ground	GND	P
8	VDD_TP	Power Supply	VDD_TP = 3.3V (TYP)	P

Note1: - Pull high to 1.8V.
This is implemented in the FPC circuit.

Connector: Hirose FH34SRJ-8S-0.5SH

Item	Symbol	Min	Typ.	Max	Unit	Condition
Operation current	I_{op}		100		mA	Active Mode @ 21.5"

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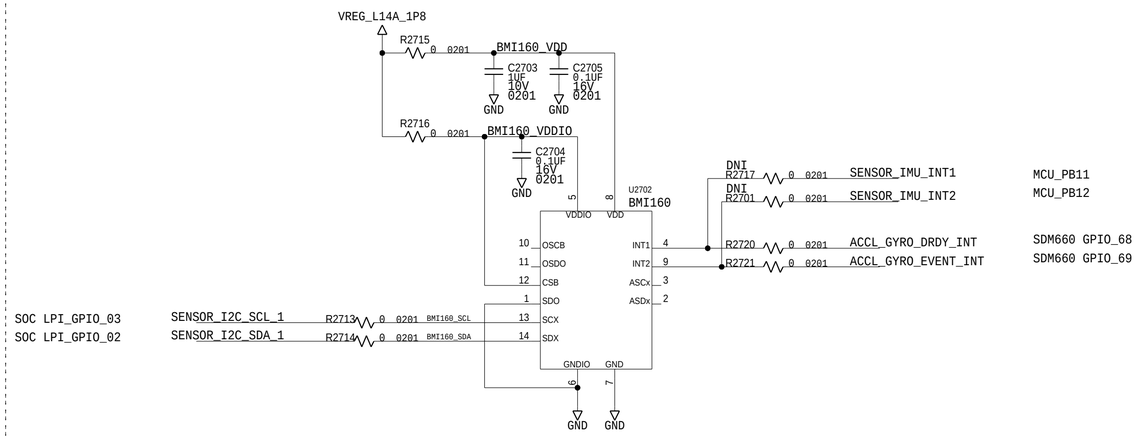
SENSOR

REVISIONS							
REV	ZONE	NO.	DESCRIPTION	E.C.	BY	APVD.	DATE
			SEE SHEET 1				

PROXIMITY SENSOR AND ALS

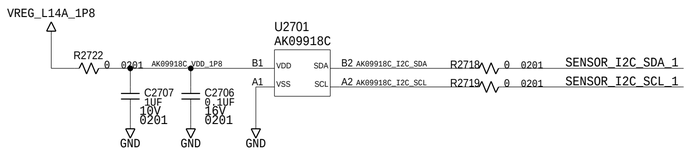
SENSOR ON NOTIFICATION FPC
CM36686M3OE
ADDRESS 0X60

GYRO,G-SENSOR



SDO=GND, ADDRESS 0X68

E-COMPASS



ADDRESS 0X0C

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SIZE	DWG. NO.	REV
D		V1D

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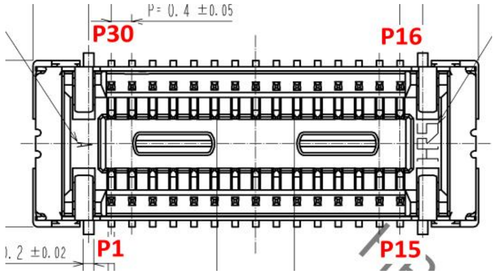
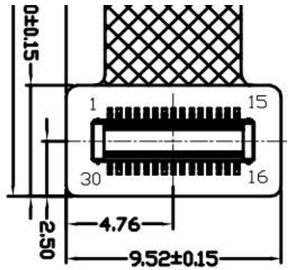
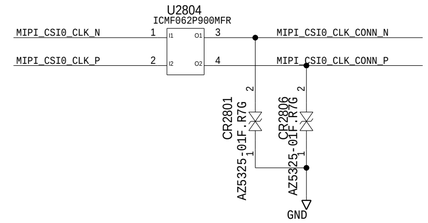
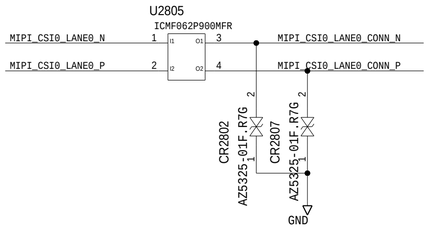
CAMERA(M13)

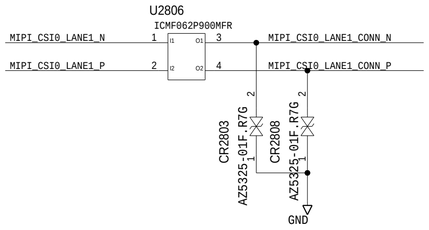
REVISIONS							
REV	ZONE	NO.	DESCRIPTION	E.C.	BY	APVD.	DATE
			SEE SHEET 1				

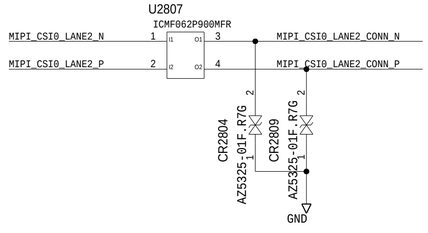


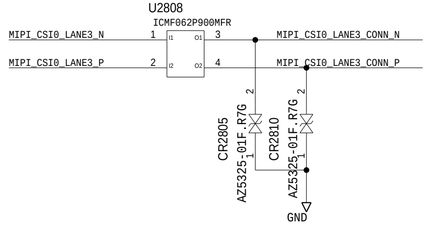


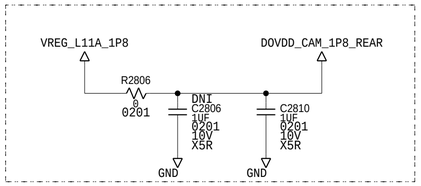


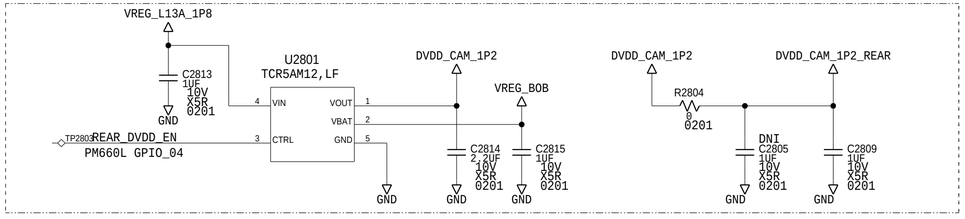


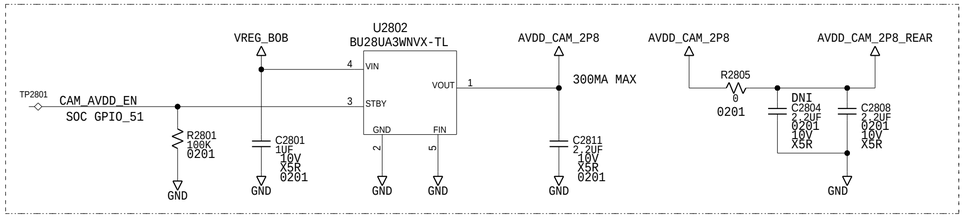


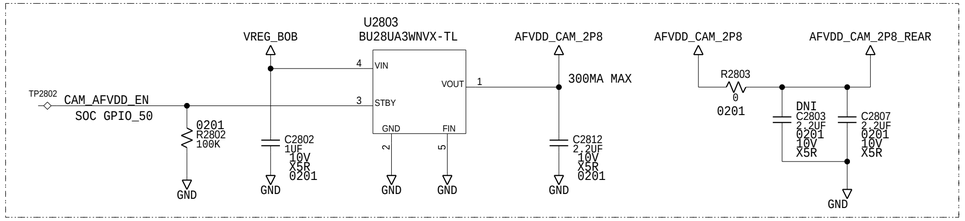












1	DGND
2	MCLK
3	DGND
4	MDP0
5	MDN0
6	DGND
7	MCP
8	MCN
9	DGND
10	MDP1
11	MDN1
12	DGND
13	DVDD
14	DGND
15	AVDD
16	DGND
17	AF_VDD
18	DOVDD
19	DGND
20	SDA
21	SCL
22	XSHUTDOWN
23	DGND
24	DGND
25	MDN2
26	MDP2
27	DGND
28	MDN3
29	MDP3
30	DGND

GND PADS FOR MIPI TESTING PURPOSE.
PLACE THEM NEXT TO MIPI SIGNALS.

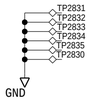


table 7-3 DC characteristics (-30°C < T_J < 85°C)

symbol	parameter	min	typ	max[a]	unit
supply					
V_{DD-A}	supply voltage (analog)	2.7	2.8	3.0	V
V_{DD-D}	supply voltage (digital core for 2-lane MIPI up to 900 Mbps/lane)	1.14	1.2	1.26	V
V_{DD-IO}	supply voltage (digital I/O)	1.7	1.8	1.9	V
I_{DD-A}	active (operating) current[b]		36	45	mA
I_{DD-IO}			3	4	mA
I_{DD-D}[c]			106	140	mA
$I_{DDS-SCCB}$	standby current[d]		1	20	mA
$I_{DDS-XSHUTDN}$			2	20	µA

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RESERVE FOR WWAN

REVISIONS							
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			SEE SHEET 1				

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SIZE	DWG. NO.	REV
D		V1D

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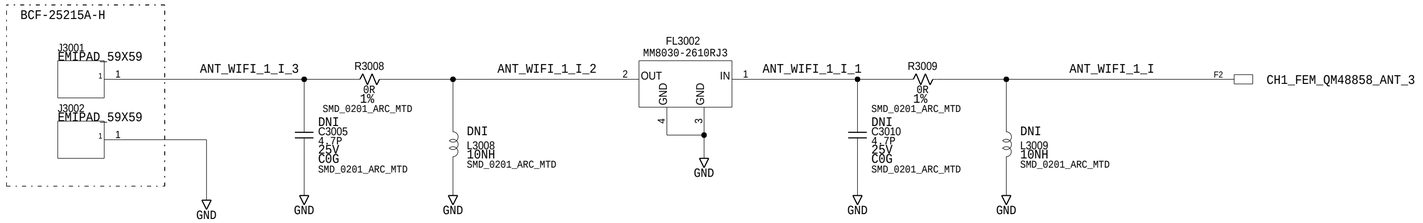
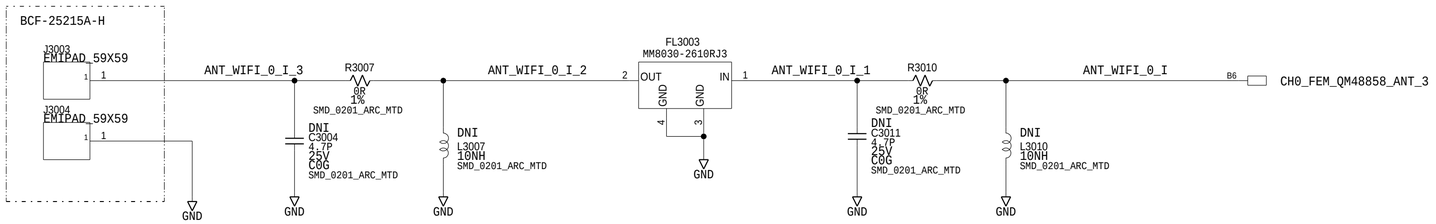
WIFI ANTENNA(M1,M2)

REVISIONS							
REV	ZONE	NO.	DESCRIPTION	E.C.	BY	APVD.	DATE
			SEE SHEET 1				

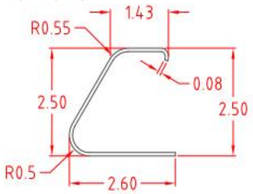


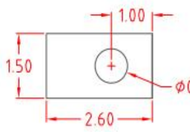


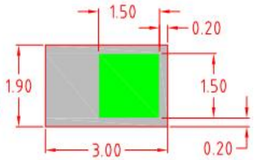
WP_IF — L7 — NC PIN

RF_TP — P2 — NC PIN

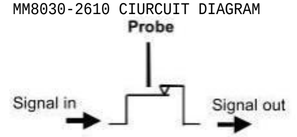
BCF-25215A-H

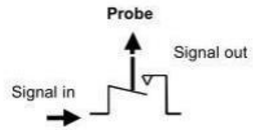






MM8030-2610 CIURCUIT DIAGRAM





RESERVE FOR GPS

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SIZE D	DWG. NO.	REV V1D
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NFC

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POWER INPUT

VREG_L15A_UIM1 — DNI R3105 0 0201 — RF_VREG_L15A_UIM1
VREG_L17A_UIM2 — DNI R3106 0 0201 — RF_VREG_L17A_UIM2
VREG_L13A_1P8 — R3107 0 0201 — RF_VREG_L13A_1P8
VPH_PWR — R3108 0 0402 — RF_NFC_VBAT

RF_VREG_L13A_1P8 — DNI R3110 0 0201 — R3111 0 0201 — GND

Table 12. I²C-bus interface addressing

HIF2	HIF1	I²C-bus address (R/W = 0, write)	I²C-bus address (R/W = 1, read)
0	0	0x50	0x51
0	1	0x52	0x53
1	0	0x54	0x55
1	1	0x56	0x57

RF_VNFC_SIM1 — OUTPUT TO USIM1 — DNI C3101 0.47UF 6.3V X5R 0201 — GND
RF_VNFC_SIM2 — OUTPUT TO USIM2 — DNI C3102 0.47UF 6.3V X5R 0201 — GND
RF_VREG_L15A_UIM1 — FROM PM660 L15A — DNI C3103 1UF 10V X5R 0201 — GND
RF_VREG_L17A_UIM2 — FROM PM660 L17A — DNI C3104 1UF 10V X5R 0201 — GND

RF_VNFC_VDD: C3110 2.2UF 10V X5R 0402 — GND; C3114 0.47UF 6.3V X5R 0201 — GND; C3116 2.2UF 10V X5R 0402 — GND

R3121 0 0201; R3123 0 0201 — *NOTE3 — GND

DNI C3108 0.22UF 10V X5R 0201 — GND *NOTE2

C3105 2.2UF 10V X5R 0402 — GND; C3106 2.2UF 10V X5R 0402 — GND
CLOSE TO PIN G7

RF_NFC_VDD_UP — DNI C3107 4.7UF 10V X5R 0402 — GND
C3109 0.1UF 16V X5R 0201 — GND

RF_VREG_L13A_1P8 — C3111 1UF 10V X5R 0402 — GND

RF_NFC_VBAT — C3115 4.7UF 10V X5R 0603 — GND; C3113 0.1UF 10V X5R 0201 — GND
CLOSE TO PIN E8

U3102
NQ310A1EV/C101Y_NSMD

VDDA	D7	HIF1	C3
VDDD	C7	HIF2	D1
VDD_SIM_1	A5	HIF3	E1 — RF_NFC_I2C_SDA — R3113 0 0201 — BLSP2_I2C_SDA — SOC GPIO_6
VDD_SIM_2	A8	HIF4	E2 — RF_NFC_I2C_SCL — R3114 0 0201 — BLSP2_I2C_SCL — SOC GPIO_7
VDD_SIM_PMU_1	A4	NFC_CLK_XTAL1	C8 — RF_NFC_CLK1
VDD_SIM_PMU_2	A7	XTAL2	D8 — RF_NFC_CLK2
VDD_SE	B8	ANT1	F7
VDD_HF	D6	ANT2	E7
VDD_TX	G7	TX1	G8 — RF_NFC_TX_1
VDD_UP	H3	TX2	H7 — RF_NFC_TX_2
VDD_MID	H4	RXP	H5 — RF_NFC_RXP
NC#IC5	C5	RXN	H6 — RF_NFC_RXN
VDD_PAD	D2	CLK_REQ	B1 — NFC_LNBBCLK3_EN_R — DNI R3115 0 0201 — NFC_LNBBCLK3_EN — PM660 GPIO_4
VDD_GPIO	G1	DWL_REQ	D3 — RF_NFC_DWL_REQ — R3116 0 0201 — NFC_DWL_REQ — TP3107 — SDM660 GPIO_30
VBAT	E8	WKUP_REQ	A1
NFC_GPIO_0	C2	TX_PWR_REQ	F8 — RF_NFC_BOOST_EN
NFC_GPIO_2	F3 — NFC_F3	NFC_GPIO_1	B2
NFC_GPIO_3	F2	IRQ	E3 — RF_NFC_INT — R3119 0 0201 — NFC_INT_N — TP3104 — SDM660 GPIO_31
NFC_GPIO_4	H2	VEN	H1 — RF_NFC_EN — R3120 0 0201 — NFC_EN — TP3105 — SDM660 GPIO_8
NFC_GPIO_5	G2		R3112 1M 0201 — GND
NFC_GPIO_6	F1	SIM_SWIO_1	A3
NFC_GPIO_7	A2	SIM_SWIO_2	A6
IC#B7	B7	SIM_IO_PULLDOWN_1	B3
NC#B5	B5	SIM_IO_PULLDOWN_2	B6
NC#D4	D4	VSSA	G3
NC#E4	E4 — NFC_E4	VSSA	G5
IC#G4	G4	VSSA	G6
NC#E5	E5	VSSD	C6
NC#D5	D5	VSS_TX	H8
ESE_SPI_MOSI	F5	NC#B4	B4 — DNI R3124 0 0201 — *NOTE2 — GND
NC#C4	C4	VSS_PAD	C1 — GND
NC#F4	F4		
NC#F6	F6		
NC#E6	E6 — NFC_E6		

NC IN SX5
NC IN SX5

DNI R3122 0 0201 — NFC_LNBBCLK3_R — PM660 BBCLK3

Y3101 27.12MHZ
RF_NFC_CLK1 — 1 — 3 — RF_NFC_CLK2
C3119 15PF 25V C0G 0201 — GND
VSS (2) — GND; VSS (4) — GND
C3120 15PF 25V C0G 0201 — GND

OPTION POWER SIM VCC FROM LDO
*NOTE3

RF_VREG_L15A_UIM1 — DNI R3103 0 0201 — SIM_VCC_1
RF_VNFC_SIM1 — DNI R3104 0 0201
RF_VREG_L17A_UIM2 — DNI R3101 0 0201 — SIM_VCC_2
RF_VNFC_SIM2 — DNI R3102 0 0201

*NOTE2

NFC_F3
NFC_E4 — DNI R3117 0 0201
NFC_E6 — DNI R3118 0 0201

IF NQ330/NQ440 IS USED
MOUNT R3124, C3108, R3117, R3118

*NOTE3

UICC NOT USED, MOUNT R3121, R3123
UICC ARE USED, DNI R3121, R3123

NFV BOOST POWER

RF_NFC_VBAT — C3112 22UF 6.3V X5R 0603 — GND
L3101 1UH ASMPH-0603-1R0M-T
U3101
PCA9410
VIN (A3); SW1 (B1); SW2 (B2); EN (B3); VOUT1 (A1); VOUT2 (A2); PGND1 (C1); PGND2 (C2); AGND (C3)
RF_NFC_BOOST_EN — TP3102
DNI C3117 100PF 25V NPO 0201 — GND
RF_NFC_VDD_UP_1 — TP3103 — R3109 0 0201 — RF_NFC_VDD_UP
C3118 10UF 10V X5R 0402
C3121 10UF 10V X5R 0402
GND

INPUT CAPACITOR 2UF@5V
OUTPUT CAPACITOR 3UF@5V

5V TYP (4.85V~5.15V)
IO=500MA

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D		V1D
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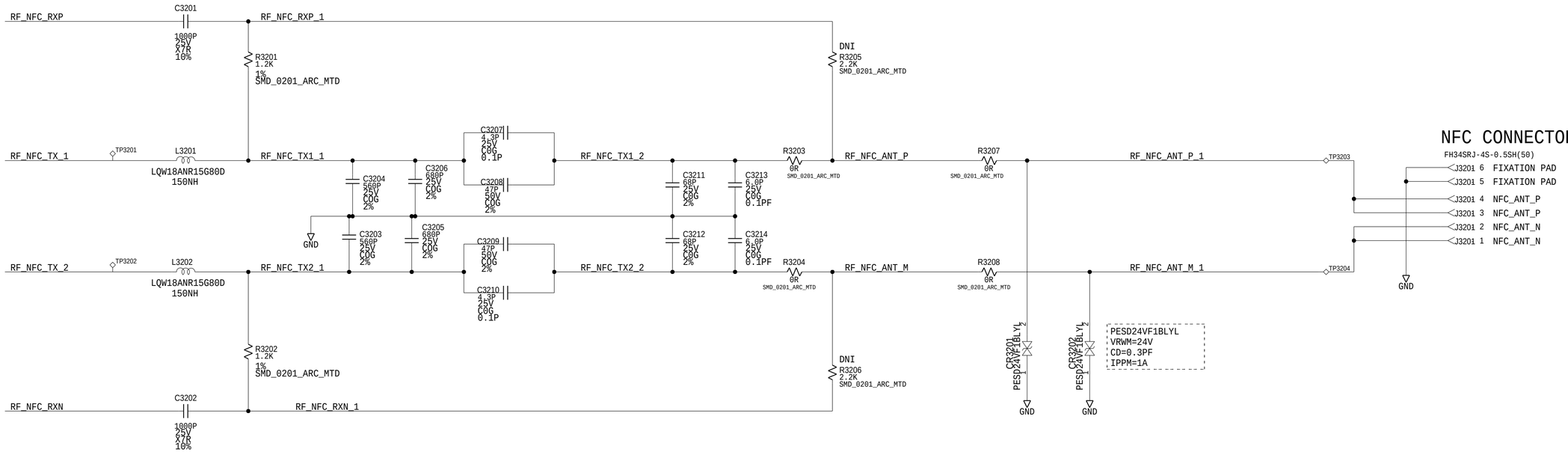
NFC ANTENNA(M5)

REVISIONS							
REV	ZONE	NO.	DESCRIPTION	E.C.	BY	APVD.	DATE
			SEE SHEET 1				



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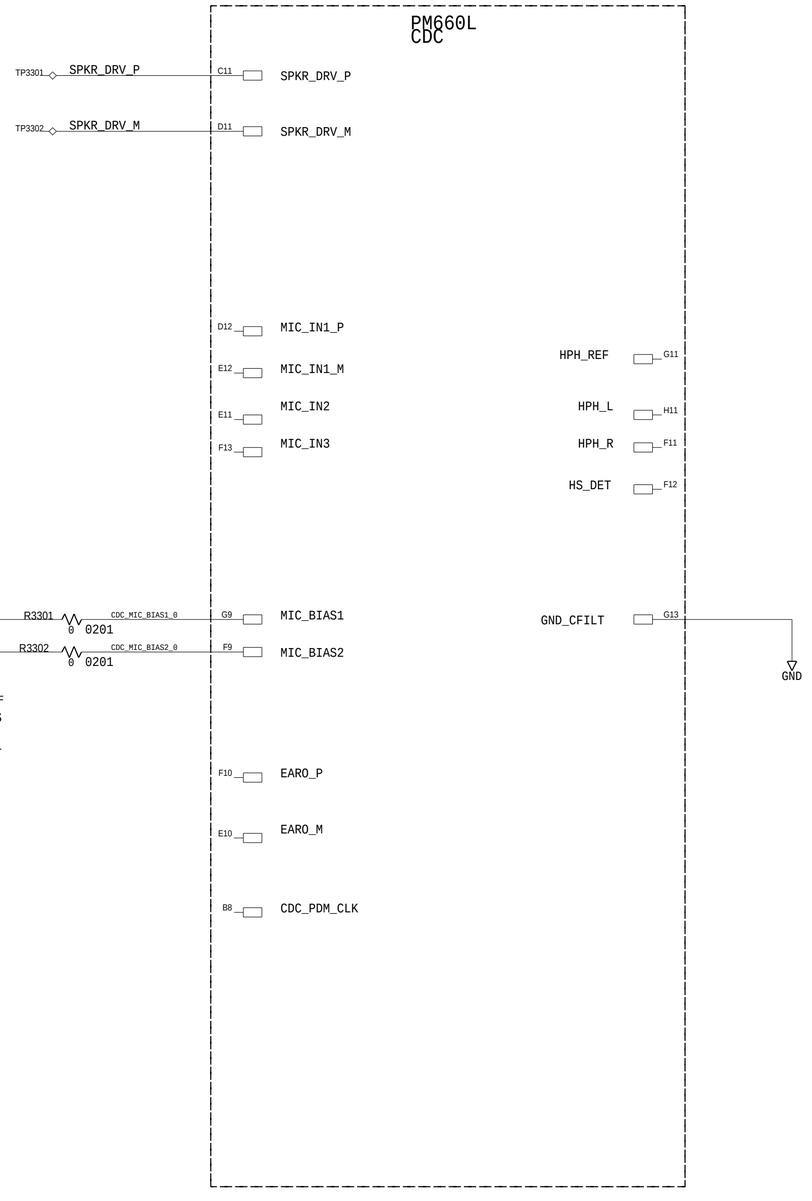
PM660L CODEC

REVISIONS							
REV	ZONE	NO.	DESCRIPTION	E.C.	BY	APVD.	DATE
			SEE SHEET 1				



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SIZE	DWG. NO.	REV
D		V1D

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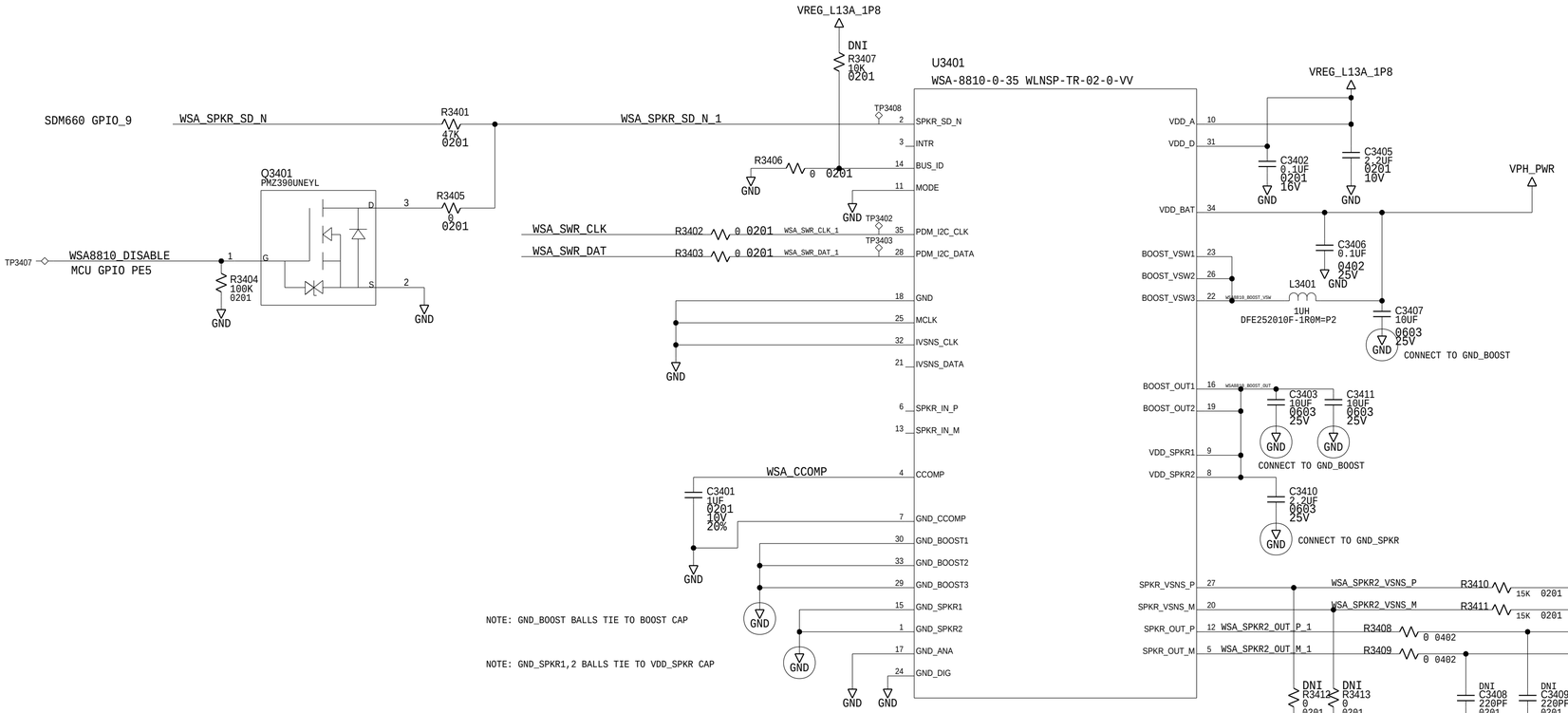
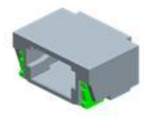
WSA8810 FOR SPEAKER(M9)

REVISIONS							
REV	ZONE	NO.	DESCRIPTION	E.C.	BY	APVD.	DATE
			SEE SHEET 1				





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SIZE D	DWG. NO.	REV V1D
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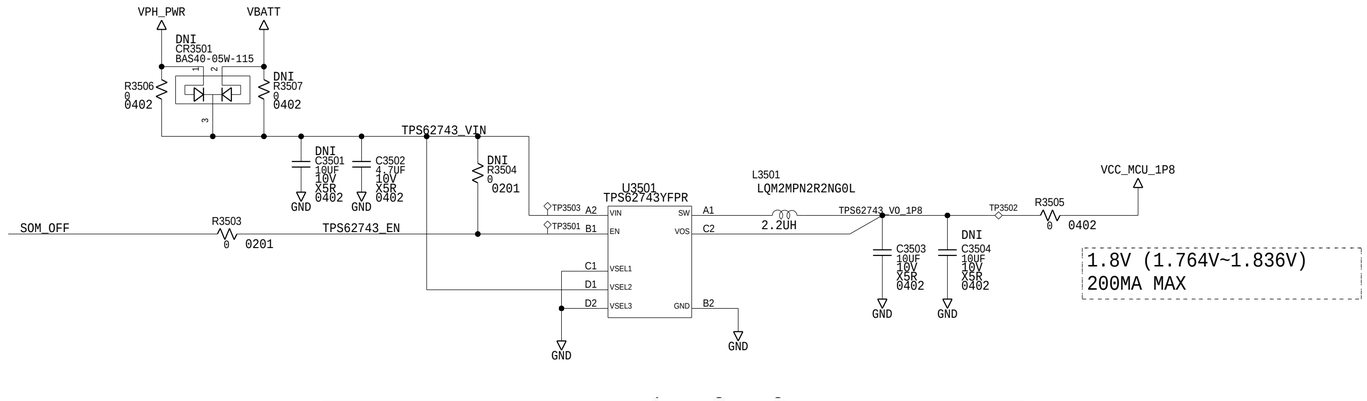
MCU 1P8 POWER

REVISIONS							
REV	ZONE	NO.	DESCRIPTION	E.C.	BY	APVD.	DATE
			SEE SHEET 1				



Output voltage setting V_{OUT} [V]		VSEL setting		
TPS62743	TPS627431	VSEL3	VSEL2	VSEL1
1.2	1.3	0	0	0
1.5	1.4	0	0	1
1.8	1.6	0	1	0
2.1	1.7	0	1	1
2.5	1.9	1	0	0
2.8	2.0	1	0	1
3.0	2.9	1	1	0
3.3	3.1	1	1	1

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D		V1D

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MCU

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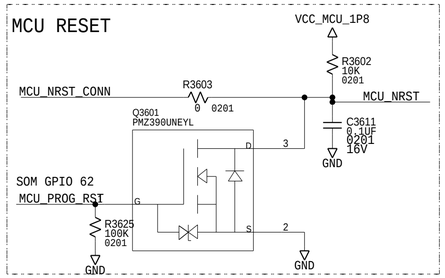
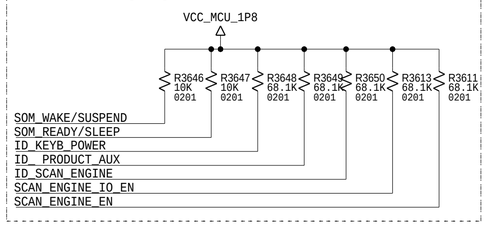
			SEE SHEET 1				

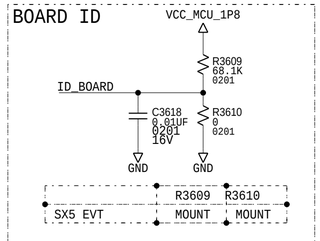
MCU RESET

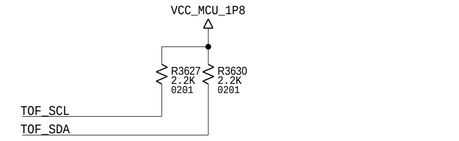


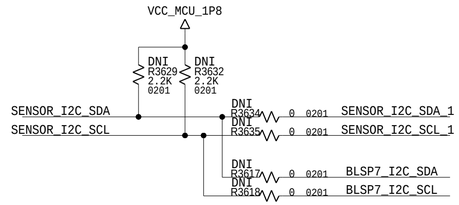
EXTERNAL PULLUP



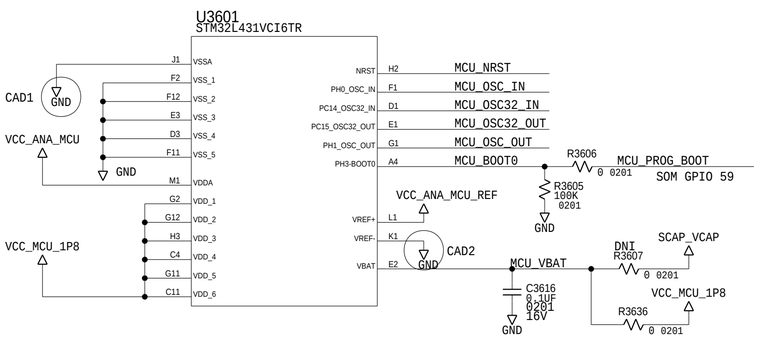
BOARD ID



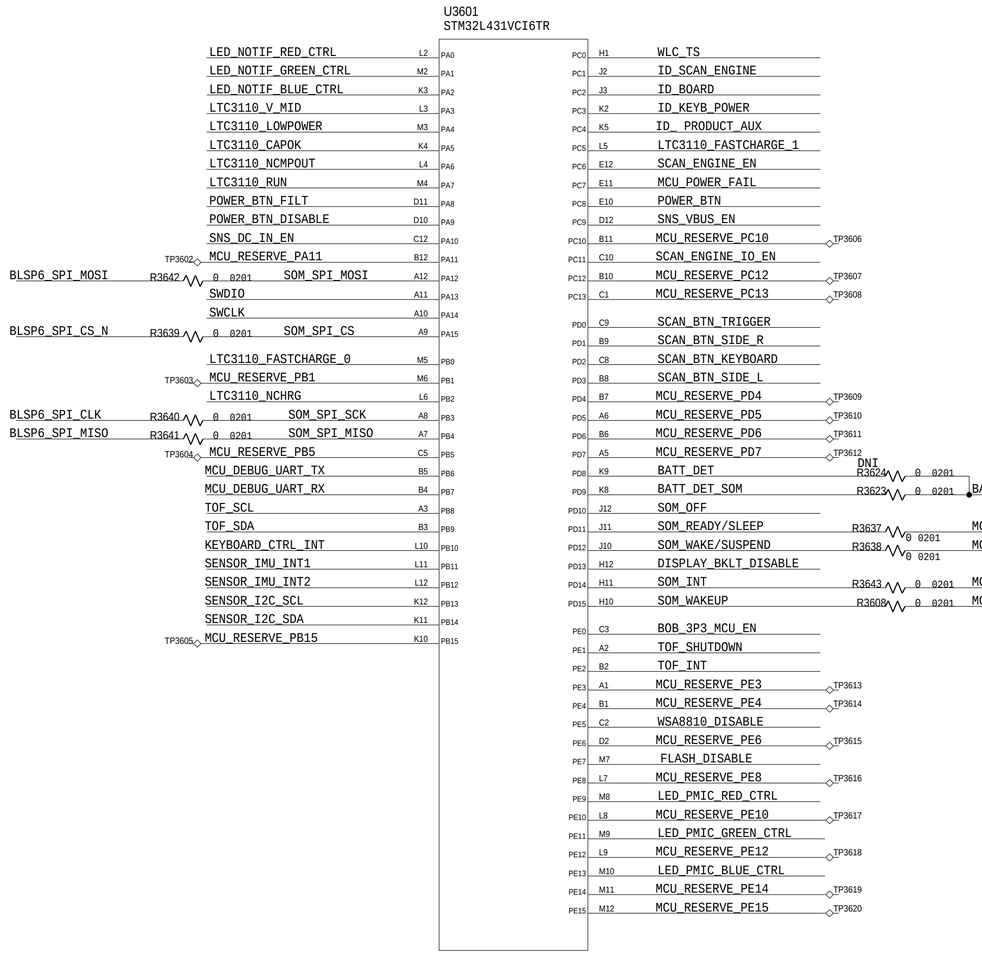




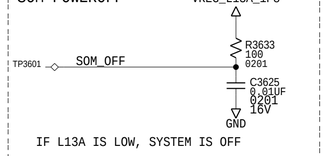
U3601 STM32L431VCI6TR



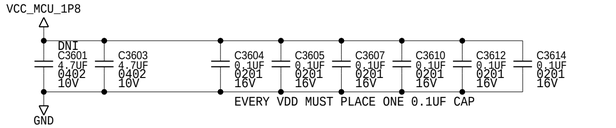
U3601 STM32L431VCI6TR

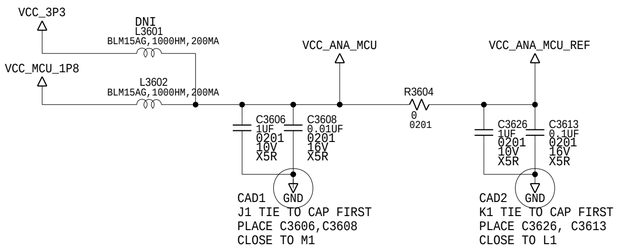


SOM POWEROFF

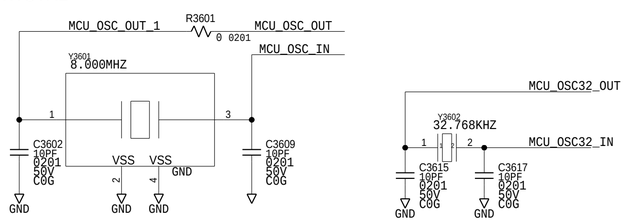


DECOUPLING CAPACITOR





CRYSTAL



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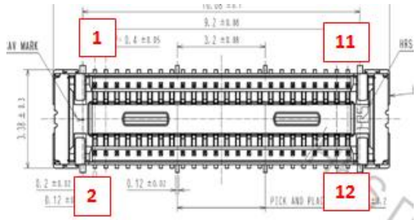
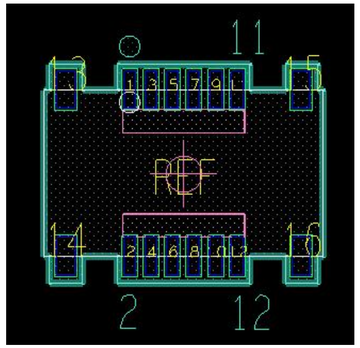
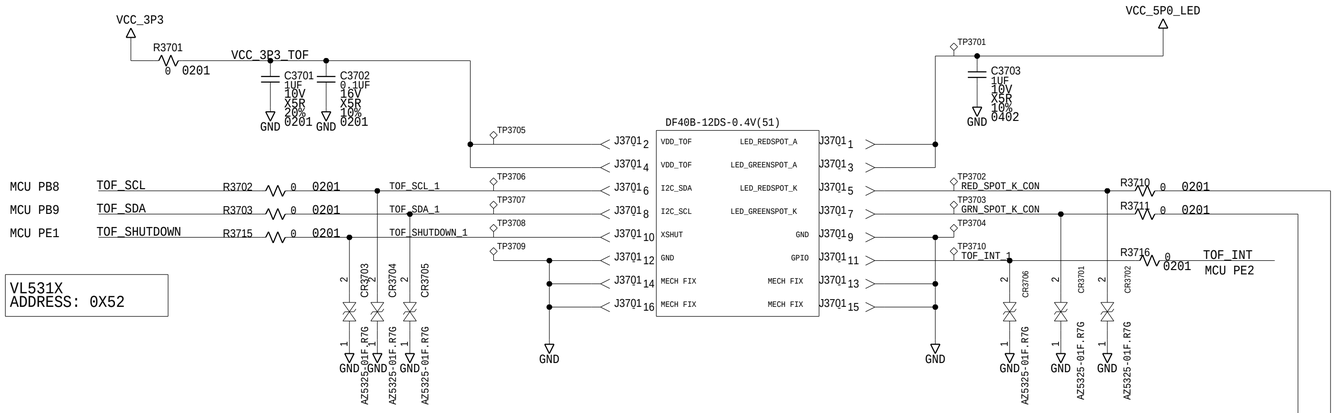
TOF & SPOT LED(M19)

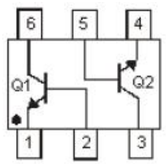
REVISIONS							
REV	ZONE	NO.	DESCRIPTION	E.C.	BY	APVD.	DATE
			SEE SHEET 1				

DF40B-12DS-0.4V(51)









ON CHARACTERISTICS (Note 4)					
DC Current Gain	h_{FE}	40 70 100 60 30	— — 300 — —	—	I_C = 100μA, V_{CE} = 1.0V I_C = 1.0mA, V_{CE} = 1.0V I_C = 10mA, V_{CE} = 1.0V I_C = 50mA, V_{CE} = 1.0V I_C = 100mA, V_{CE} = 1.0V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	—	0.20 0.30	V	I_C = 10mA, I_B = 1.0mA I_C = 50mA, I_B = 5.0mA
Base-Emitter Saturation Voltage	$V_{BE(SAT)}$	0.65 —	0.85 0.95	V	I_C = 10mA, I_B = 1.0mA I_C = 50mA, I_B = 5.0mA

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AUX BOARD CONNECTOR(M15)

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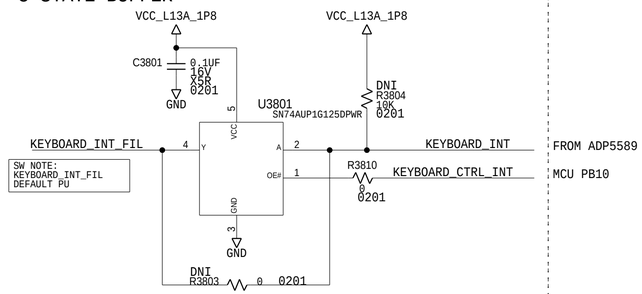
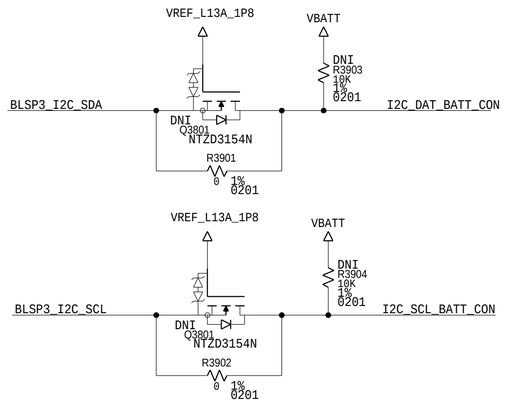
SN74AUP1G125 Table 1. Function Table

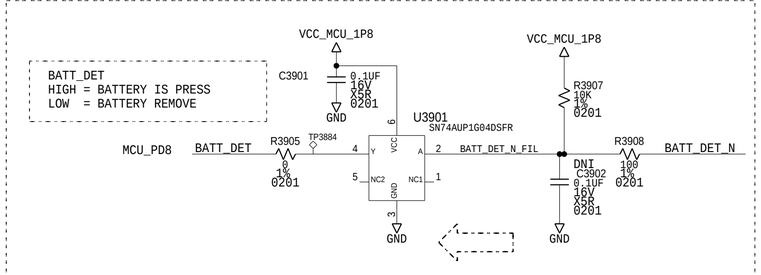
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Hi-Z

3-STATE BUFFER



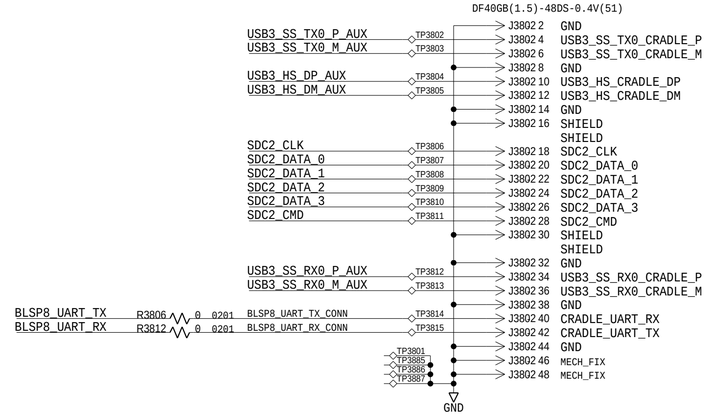
LEVEL SHIFT

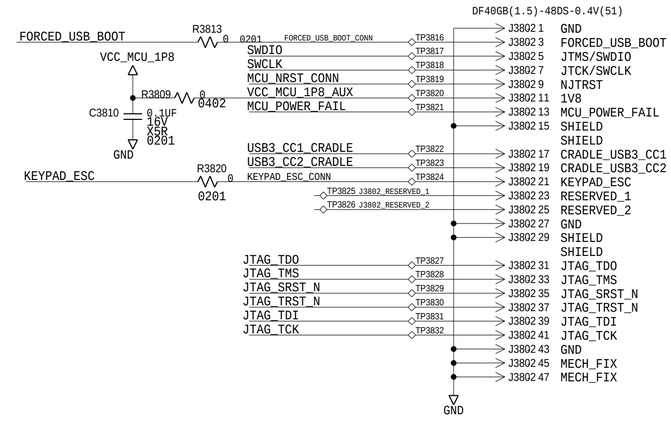




M15.1

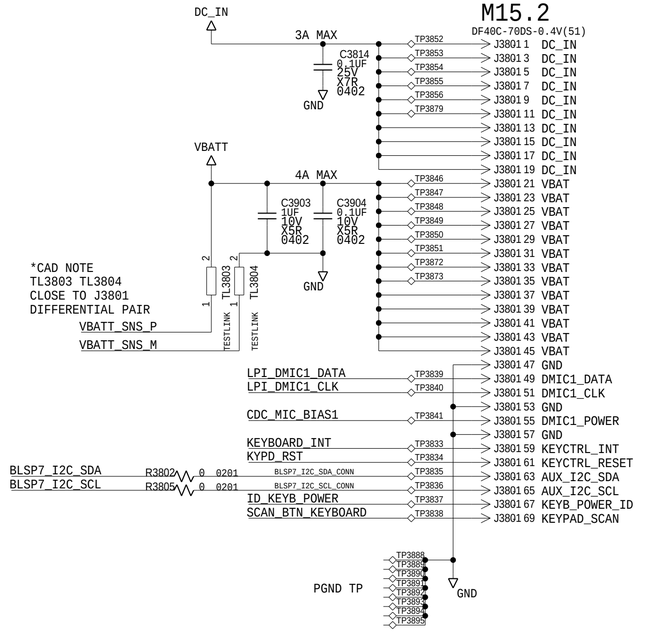
DF40GB(1.5)-48DS-0.4V(51)

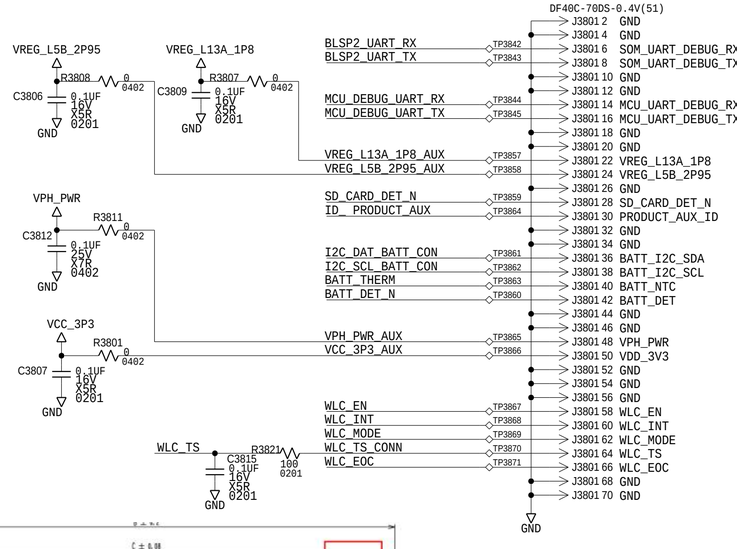


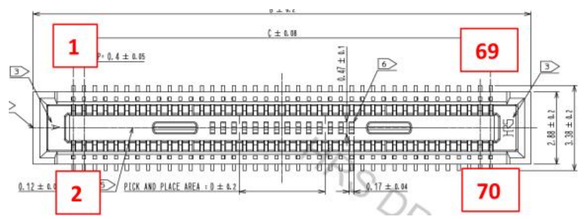


M15.2

DF40C-70DS-0.4V(51)







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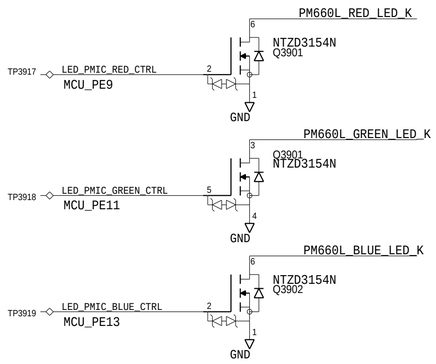
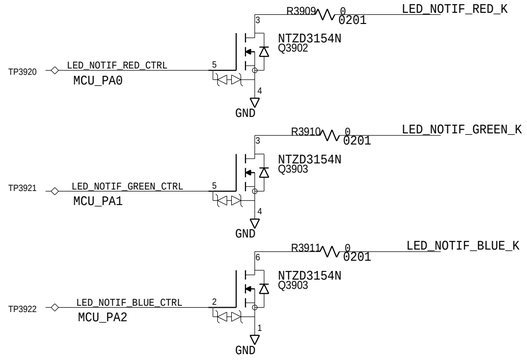
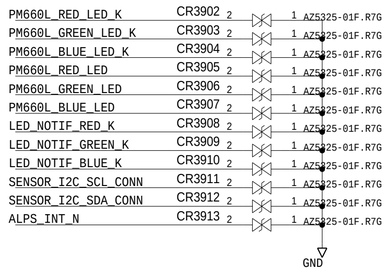
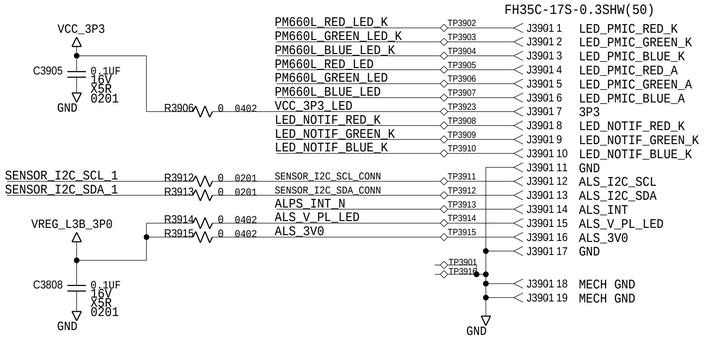
ALS & LED (M20)

REVISIONS							
REV	ZONE	NO.	DESCRIPTION	E.C.	BY	APVD.	DATE
			SEE SHEET 1				

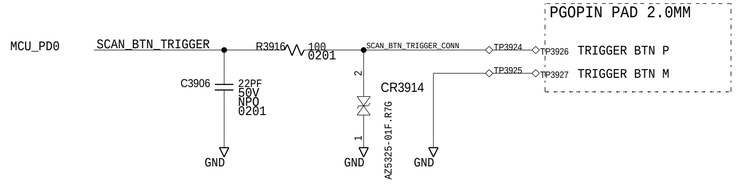








SX5 SCAN TRIGGER(M16)



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RESERVE

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D		V1D

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RESERVE

REVISIONS							
REV	ZONE	NO.	DESCRIPTION	E.C.	BY	APVD.	DATE
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SCANNER& FLASH& DMIC(M10)

REVISIONS						
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			SEE SHEET 1				

SPI, I2C, UART

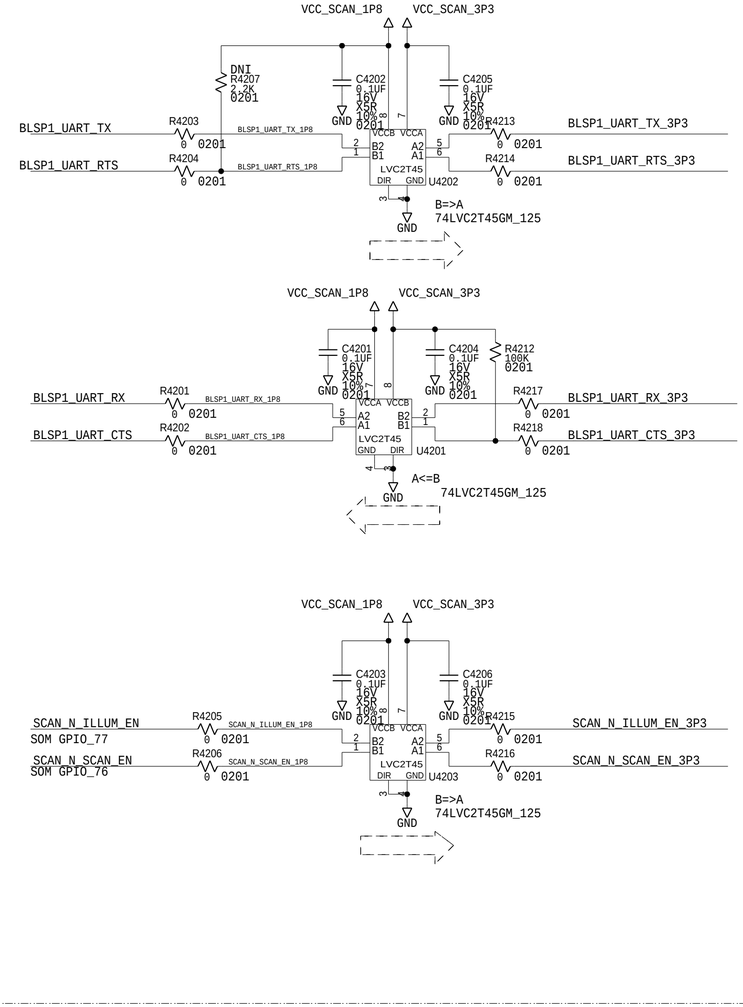
BLSP1_SPI_MISO
BLSP1_SPI_MOSI
BLSP1_SPI_CS_N
BLSP1_SPI_CLK

R4210 0 0201 BLSP1_I2C_SDA
R4211 0 0201 BLSP1_I2C_SCL

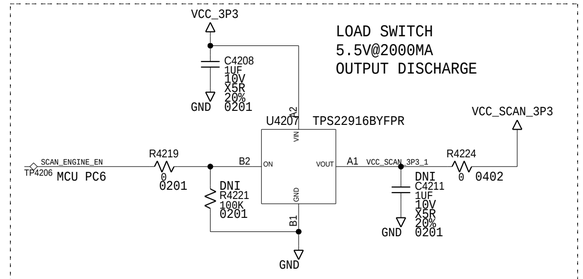
BLSP1_UART_RX
BLSP1_UART_TX
BLSP1_UART_CTS
BLSP1_UART_RTS

SPI	I2C	UART
MISO	N/C	RX
MOSI	N/C	TX
CS_N	SDA	CTS
CLK	SCL	RTS

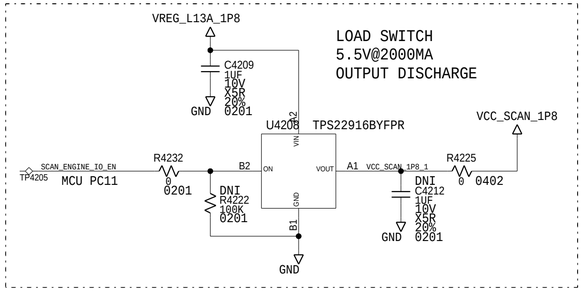
DE1011 LEVEL SHIFT



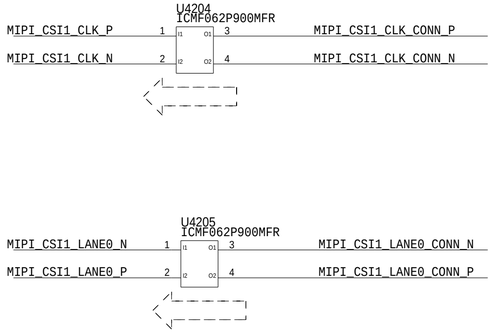
LOAD SWITCH 5.5V@2000MA OUTPUT DISCHARGE



LOAD SWITCH 5.5V@2000MA OUTPUT DISCHARGE



MIPI FILTER



ESD DIODE

BLSP1_UART_RX_3P3	CR4201	2	1	AZ5325-01F.R7G
BLSP1_UART_TX_3P3	CR4202	2	1	AZ5325-01F.R7G
BLSP1_UART_RTS_3P3	CR4203	2	1	AZ5325-01F.R7G
BLSP1_UART_CTS_3P3	CR4204	2	1	AZ5325-01F.R7G
MIPI_CSI1_CLK_CONN_N	CR4205	2	1	AZ5325-01F.R7G
MIPI_CSI1_CLK_CONN_P	CR4206	2	1	AZ5325-01F.R7G
MIPI_CSI1_LANE0_CONN_P	CR4207	2	1	AZ5325-01F.R7G
MIPI_CSI1_LANE0_CONN_N	CR4208	2	1	AZ5325-01F.R7G
BLSP1_I2C_SDA	CR4209	2	1	AZ5325-01F.R7G
BLSP1_I2C_SCL	CR4210	2	1	AZ5325-01F.R7G
CDC_MIC_BIAS2	CR4211	2	1	AZ5325-01F.R7G
LPI_DMIC2_DATA	CR4212	2	1	AZ5325-01F.R7G
LPI_DMIC2_CLK	CR4213	2	1	AZ5325-01F.R7G
ID_SCAN_ENGINE	CR4214	2	1	AZ5325-01F.R7G
FLASH_LED1_A	CR4215	2	1	AZ5325-01F.R7G
FLASH_LED1_K	CR2815	2	1	AZ5325-01F.R7G
SCAN_N_ILLUM_EN_3P3	CR2816	2	1	AZ5325-01F.R7G
SCAN_N_SCAN_EN_3P3	CR2817	2	1	AZ5325-01F.R7G

VCC_SCAN_3P3
C4214 1UF 10V X5R 20% 0201
C4217 0.1UF 16V X5R 10% 0201
VCC_SCAN_1P8
DNI C4215 1UF 10V X5R 20% 0201
C4218 0.1UF 16V X5R 10% 0201

DF40GB(1.5)-48DS-0.4V(51)

HALOGEN2	TUNGSTEN		
VCC_ILLUM_SYS	N.C.	TP4208	J4201 1
VCC_ILLUM_SYS	N.C.	TP4209	J4201 3
VCC	VCC	TP4211	J4201 5
GND	GND		J4201 7
GND	GND		J4201 9
GND	GND		J4201 11
VCC_IO	N.C.	TP4212	J4201 13
SHIELD	SHIELD		J4201 15
SHIELD	SHIELD		
GND	GND		J4201 17
FLASH_LED_K	FLASH_LED_K	TP4240	J4201 19
FLASH_LED_K	FLASH_LED_K	TP4241	J4201 21
FLASH_LED_K	FLASH_LED_K	TP4242	J4201 23
FLASH_LED_K	FLASH_LED_K		J4201 25
FLASH_LED_K	FLASH_LED_K		J4201 27
SHIELD	SHIELD		J4201 29
SHIELD	SHIELD		
N.C.	N_ILLUM_EN_3P3	TP4243	J4201 31
N.C.	N_SCAN_EN_3P3	TP4244	J4201 33
N.C.	UART_TX_3P3	TP4213	J4201 35
N.C.	UART_RX_3P3	TP4214	J4201 37
N.C.	UART_CTS_3P3	TP4215	J4201 39
N.C.	UART_RTS_3P3	TP4216	J4201 41
GND	GND		J4201 43
MECH_FIX	MECH_FIX		J4201 45
MECH_FIX	MECH_FIX		J4201 47

GND

FLASH_LED1_K
VREG_L13A_1P8
R4234 100K 0201
Q4201 SSM6K781G
FLASH_DISABLE
TP4246
MCU PE7
R4233 0 0201
GND

DF40GB(1.5)-48DS-0.4V(51)

BLSP1_I2C_SDA	TP4221	J4201 2	I2C_SDA
BLSP1_I2C_SCL	TP4222	J4201 4	I2C_CLK
		J4201 6	GND
CDC_MIC_BIAS2	TP4223	J4201 8	DMIC_POWER
		J4201 10	GND
LPI_DMIC2_DATA	TP4224	J4201 12	DMIC2_DATA
LPI_DMIC2_CLK	TP4225	J4201 14	DMIC2_CLK
		J4201 16	SHIELD
			SHIELD
ID_SCAN_ENGINE	TP4226	J4201 18	SCAN_ENGINE_ID
FLASH_LED1_A	TP4227	J4201 20	FLASH_LED_A
	TP4228	J4201 22	FLASH_LED_A
	TP4229	J4201 24	FLASH_LED_A
		J4201 26	FLASH_LED_A
		J4201 28	FLASH_LED_A
		J4201 30	SHIELD
			SHIELD
MIPI_CSI1_CLK_CONN_N	TP4217	J4201 32	GND
MIPI_CSI1_CLK_CONN_P	TP4218	J4201 34	MIPI_CLKN
		J4201 36	MIPI_CLKP
MIPI_CSI1_LANE0_CONN_P	TP4219	J4201 38	GND
MIPI_CSI1_LANE0_CONN_N	TP4220	J4201 40	MIPI_DP
		J4201 42	MIPI_DN
		J4201 44	GND
		J4201 46	MECH_FIX
		J4201 48	MECH_FIX

TP4236
TP4237
TP4238
TP4245
GND

GND FOR MIPI TP

TP4201
TP4202
TP4203
TP4204
GND

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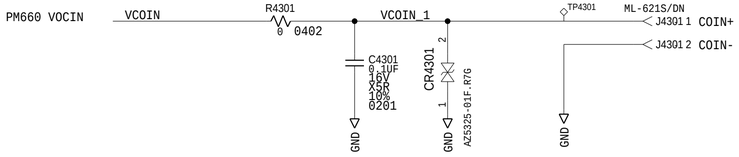
RTC BATTERY CONN



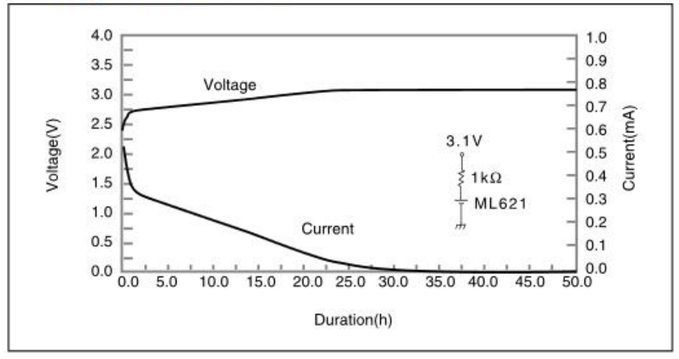
WHEN THE MAIN BATTERY IS CONNECTED TO THE PHONE WHILE A RESIDUAL VOLTAGE IS ON VCOIN, PHONES MAY NOT POWER ON.
THIS CAN OCCUR IN THE FACTORY OR WHEN A NEND USER RECONNECTS A BATTERY TO THE PHONE
DETAIL REF TO QUALCOMM KBA-170615054152

PANASONIC ML-621S/DN

■ Specification

Nominal voltage(V)	3
Nominal capacity(mAh)	5
Continuous drain(mA)	0.01
Operating temperature(˚C)	-20 to +60

■ Charge characteristics



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D		V1D

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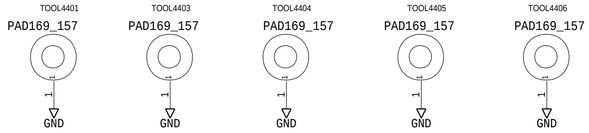
DRILLS

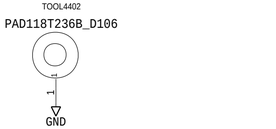
EE NOTE: FOOTPRINT TO BE UPDATED

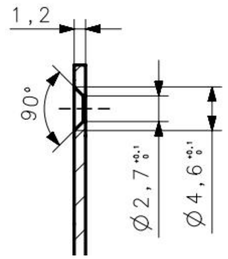
DRILL B



PTH DRILL=4MM
TOP PAD = BOTTOM PAD = 4MM

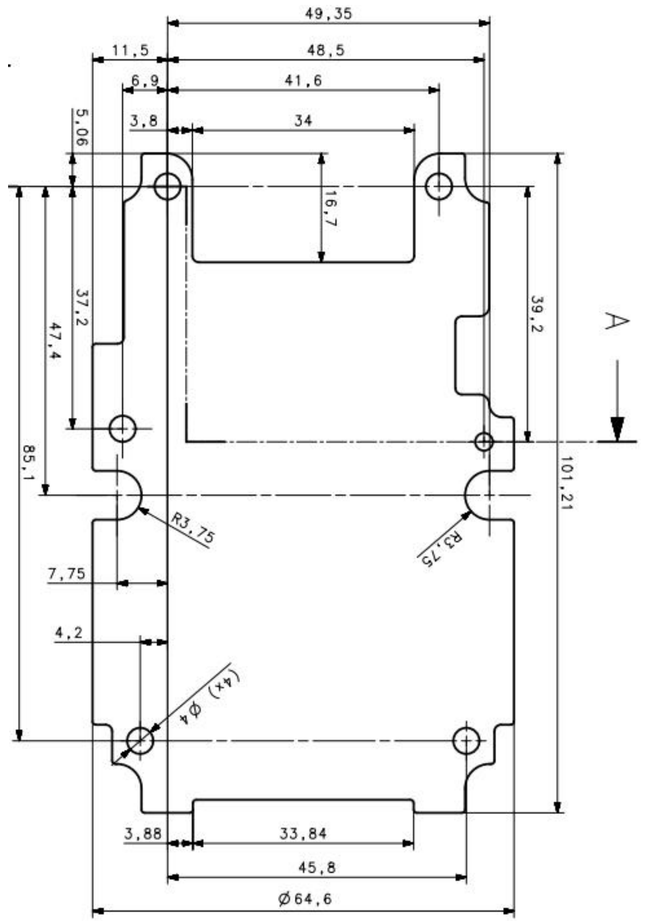
COUNTERSINK DRILL A



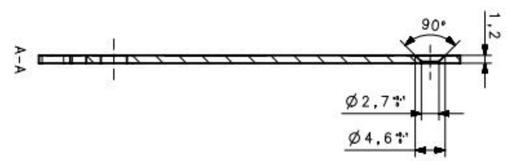


PTH DRILL= 2.7MM
BOTTOM COUNTERSINK DRILL 4.6MM 90¢X
TOP PAD=2.7MM, BOTTOM PAD=6.0MM

TOP VIEW



BOTTOM PCB SIDE



TOP PCB SIDE (DISPLAY)

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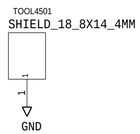
REVISIONS							
REV	ZONE	NO.	DESCRIPTION	E.C.	BY	APVD.	DATE
			SEE SHEET 1				

SHIELDING CAN

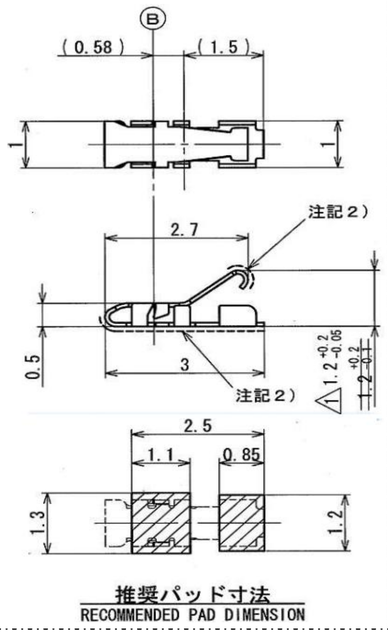
NFC SHIELDING



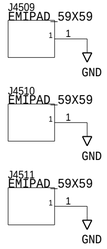
NFC SHIELD FRAME FOOTPRINT
DIMENSION=18.8X14.4X2.25MM

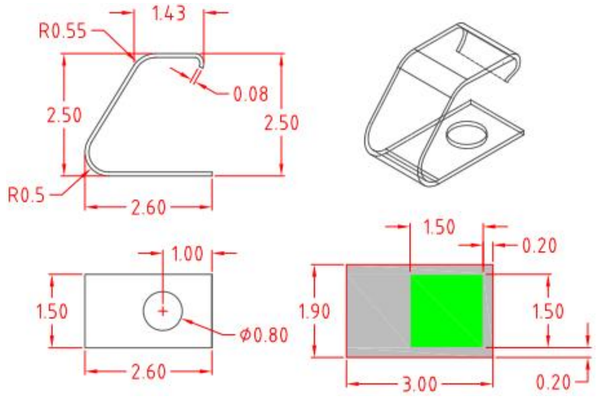
GND SPRING

TOP GND SRPING



BOTTOM GND SRPING





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