

1. Direct mapped caches

How many bytes of data can our cache hold? How many words?

CPU Cache	Index Number	Offset				Tag bits	Index bits	Offset bits	Total
		3	2	1	0				
	0					29	1	2	32
	1								

Index bits = \log_2 (Number of index rows) Offset bits = \log_2 (Number of offsets columns)

8 bytes, 2 words

2. Fill in the "Tag bits, Index bits, Offset bits" with the correct T:I:O breakdown according to the diagram.

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3. Let's say we have a 8192KiB cache with an 128B block size, what is the tag, index, and offset of 0xFEEDF00D?

FE	ED	FO	OD
1111 1110	1110 1101	1111 0000	0000 1101

$8192 = 2^{13} \text{ KiB} = 2^{23} \text{ B}$ $128 = 2^7 \text{ B}$
 offset: 7 bits \rightarrow 0001101 tag: 1 1111 1101
 index $\rightarrow 23 - 7 = 16$ bits 1101 1011 1110 0000

4. Fill in the table below. Assume we have a write-through cache, so the number of bits per row includes only the cache data, the tag, and the valid bit.

Address size (bits)	Cache size	Block size	Tag bits	Index bits	Offset bits	Bits per row
16	4KiB 12	4B 2	4	10	2	37
32	32KiB 15	16B 4	17	11	4	146
32	64KiB	16B	16	12	4	145
64	2048KiB	128B	43	14	7	1068

$4 \times 8 + 4 + 1$
 $16 \times 8 + 17 + 1$
 $16 \times 8 + 16 + 1$

$$1\text{MiB} = 2^{20} \text{ B}$$

$$1\text{KiB} = 2^{10} \text{ B}$$

$$1\text{KiB} = 2^{10} \text{ B}$$

5. Let's say you have a byte-addressed computer with a total memory of 1MiB. It features a 16KiB CPU cache with 1KiB blocks.

1) . How many bits make up a memory address on this computer?

$$20 \text{ 位}$$

2) . What is the T:I:O breakdown? tag bits: 6 index bits: 4 offset bits:

$$I: 14 - 10 = 4 \text{ 位}$$

$$O: 10 \text{ 位}$$

$$\text{tag} = 20 - 4 - 10 = 6 \text{ 位}$$

6. Given CPU base CPI = 1, clock rate = 4GHz Miss rate/instruction = 2%

Main memory access time = 100ns, With just primary cache, what is Average memory access time (AMAT)?

$$T = \frac{1}{4 \times 10^9} \times 10^9 \text{ ns} = 0.25 \text{ ns}$$

$$\text{AMAT} = 0.25 + 2\% \times 100 = 2.25 \text{ ns}$$

7. CPU with 1ns clock, hit time = 1 cycle, miss penalty = 20 cycles, I-cache miss rate = 5%, what is Average memory access time (AMAT)?

$$\text{AMAT} = 1 + 0.05 \times 20 \times 1 = 2 \text{ ns}$$

8. Given, I-cache miss rate = 2%, D-cache miss rate = 4%, Miss penalty = 100 cycles Base CPI (ideal cache) = 2, Load & stores are 36% of instructions, what is Actual CPI

$$\begin{aligned} \text{Actual CPI} &= 2 + 0.02 \times 100 + 0.36 \times 0.04 \times 100 \\ &= 5.44 \end{aligned}$$