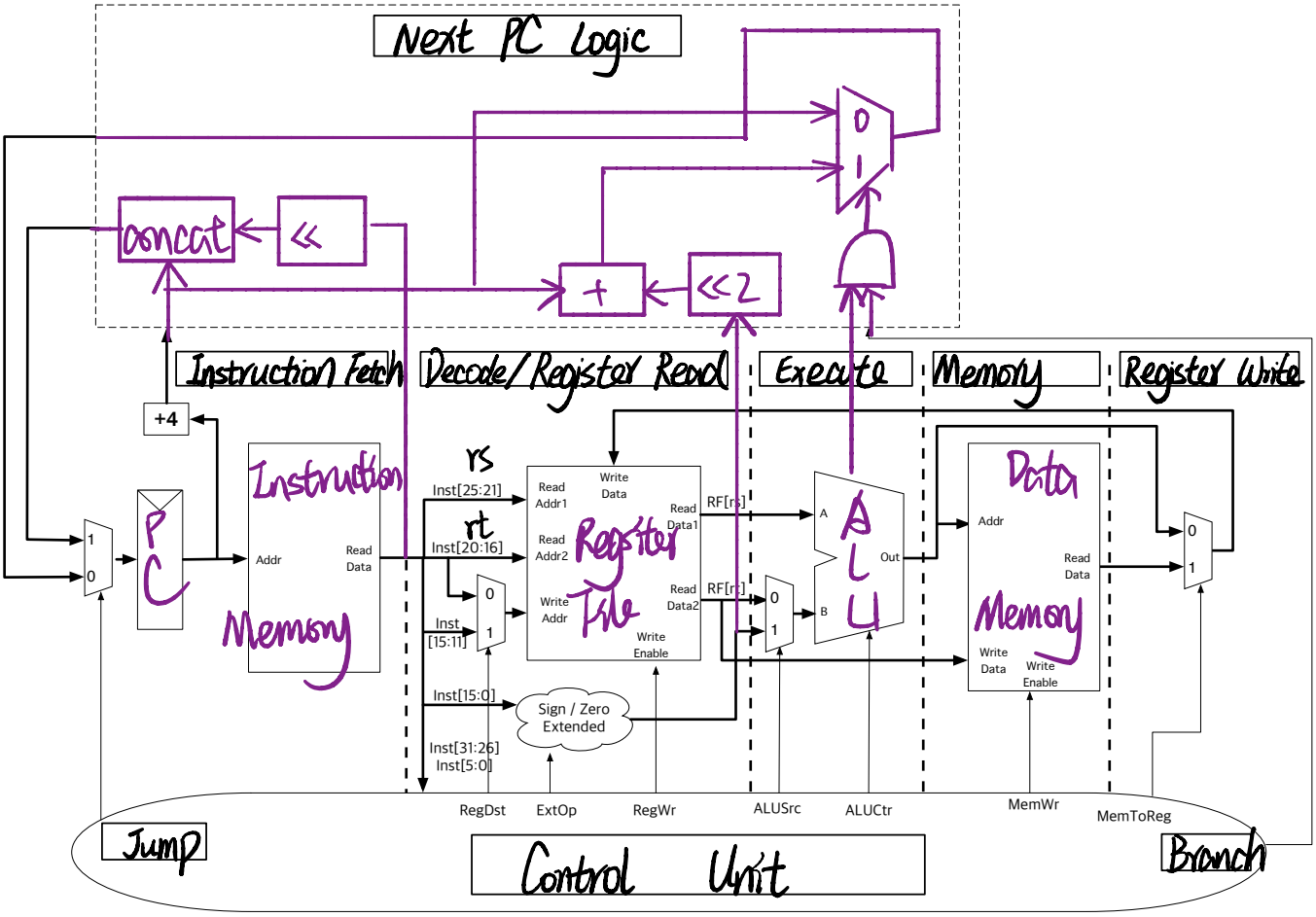
Single Cycle CPU Design

Here we have a single cycle CPU diagram. Answer the following questions:

1. Name each component.
2. Name each datapath stage and explain its functionality.

Stage	Functionality

3. Provide data inputs and control signals to the next PC logic.
4. Implement the next PC logic.



2.

Instruction Fetch <取指>	通过向指令内存中发出地址的读出指令，再改变PC的值
Decode/Register Read <指令译码>	① 通过Op以及function中的值生成控制信号 ② 读取寄存器中的值 ③ 遇到立即数操作需进行符号位扩展
Execute <执行>	完成算术或逻辑运算
Memory <访存>	load和store指令会在这里进行从内存中读出数据或者数据写入内存的操作
Register write <写寄存器>	将计算结果或从内存中读出的数写回寄存器

Single Cycle CPU Control Logic

Fill out the values for the control signals from the previous CPU diagram.

Instrs.	Control Signals								
	Jump	Branch	RegDst	ExtOp	ALUSrc	ALUCtr	MemWr	MemtoReg	RegWr
add	0	0	1	X	0	0010	0	0	1
ori	0	0	0	0	1	0001	0	0	1
lw	0	0	0	0	1	0010	0	1	1
sw	0	0	X	0	1	0010	1	X	0
beq	0	1	X	1	0	0110	0	X	0
j	1	X	X	X	X	XXXX	0	X	0

This table shows the ALUCtr values for each operation of the ALU:

Operation	AND	OR	ADD	SUB	SLT	NOR
ALUCtr	0000	0001	0010	0110	0111	1100

Clocking Methodology

- The input signal to each state element must stabilize before each rising edge.
- Critical path: Longest delay path between state elements in the circuit.
- $t_{clk} \geq t_{clk\text{-}to\text{-}q} + t_{CL} + t_{setup}$, where t_{CL} is the critical path in the combinational logic.
- If we place registers in the critical path, we can shorten the period by reducing the amount of logic between registers.

Single Cycle CPU Performance Analysis

The delays of circuit elements are given as follows:

Element	Register clk-to-q	Register Setup	MUX	ALU	Mem Read	Mem Write	RegFile Read	RegFile Setup
Parameter	$t_{clk\text{-}to\text{-}q}$	t_{setup}	t_{mux}	t_{ALU}	$t_{MEMread}$	$t_{MEMwrite}$	t_{RFread}	$T_{RFsetup}$
Delay(ps)	30	20	25	200	250	200	150	20

1. Give an instruction that exercises the critical path.

lw

2. What is the critical path in the single cycle CPU?

PC → Instruction Mem → Reg File → ALU → Data Mem

Write Data

Read Data 1

rt

3. What are the minimum clock cycle, t_{clk}, and the maximum clock frequency, f_{clk}?

Assume the $t_{clk\text{-}to\text{-}q}$ > hold time.

$T_{min} = 30 + 250 + 150 + 200 + 150 + 20 = 825ps$

$f_{max} = \frac{1}{825ps} = 1.08GHz$

4. Why is a single cycle CPU inefficient?

答：每条指令都会经过周期内所有过程，即 critical Path

执行一条指令的时候，在进行某一阶段时，其他数据 阶段处于空闲状态，

5. How can you improve its performance? What is the purpose of pipelining?

答：使用流水线模式处理

缩短时钟周期，同时进行多条指令

这时产生时间上的浪费