**Computer Organization**

**1.** The von Neumann model of a computer consists of three major components: the central processing unit (CPU), main memory, and input-output. In which of these components might we find the 32 registers of a MIPS processor?

A. CPU

B. Main memory

C. Input-output

D. CPU as well as main memory

E. Main memory as well as input-output

**2.** Suppose we want to put the 32-bit value 0x456789AB into register **$4**. Which of the following is a good sequence of assembly instructions to do so?

A. **addi $4, $0, 0x4567**

**sll $4, $4, 8**

**addi $4, $4, 0x89AB**

B. **addiu $4, $0, 0x4567**

**srl $4, $4, 8**

**addiu $4, $4, 0x89AB**

C. **lui $4, 0x4567**

**addi $4, $4, 0x89AB**

D. **lui $4, 0x4567**

**addiu $4, $4, 0x89AB**

E. All of the above

**3.** Which of the following instructions, when encoded in binary, has a field that holds an immediate/constant value that is *NOT automatically multiplied by 4* during execution by the CPU:

A. **lw $4, 4($4)**

B. **sll $4, $4, 2**

C. **bne $4, $1, 0x0100**

D. **jal 0x0100**

E. The **lw**, **bne** and **jal** instructions above

F. The **lw** and **sll** instructions above

4. Which of the following CANNOT be compiled as a single valid MIPS instruction:

A. **addu $s6, $s7, $t8**

B. **mul $2, $3, $4**

C. **lw $2, -3($4)**

D. **la $2, -3($4)**

E. None of the above

5. If **a** is of type **double\*** in C, and each double is 8 bytes long, then which of the following C Boolean expressions is *FALSE:*

A. **a == &a[0]**

B. **\*(a+i) == a[i]**

C. **&a[j] == a+j**

D. **a[4] == \*(a+32)**

E. None of the above

6. Which of the following addressing modes is available in MIPS?

A. Memory indirect

B. Displacement

C. Autoincrement

D. Indexed

E. Scaled

7. The following five assembly statements reserve space for five different variables/arrays, named A, B, C, D and E. Circle the one that reserves a different amount of space than the other four:

A. **A: .byte 1, 2, 34, 45, 0, 0, 4, 8**

B. **B: .word 0, 0**

C. **C: .asciiz “Comp 411”**

D. **D: .asciiz “Quiz #2”**

E. **E: .space 8**

8. Suppose *ProcedureA* calls *ProcedureB* with six arguments (*arg[0]—arg[5]*), and that registers **$sp** and **$fp** are properly managed by the assembly code. Within *ProcedureB,* how would the code read the argument *arg[5]* into register **$5**?

A. **lw $5, 4($fp)**

B. **lw $5, 8($fp)**

C. **lw $5, 5($sp)**

D. **lw $5, 20($sp)**

E. **ori $5, $a5, 0**

9. Suppose the **main** part of your assembly code occupies the range of memory locations 0 to 63 (0x00000000 to 0x0000003F). Now, suppose within **main** you need to call a procedure that is located at the memory address 0xFFFFFF00 (really high address). Which of the following would be a good instruction to implement this procedure call?

A. **j**

B. **jal**

C. **jr**

D. **jalr**

E. **beq**

11.Assume we have an array in memory that contains int\* arr = {1,2,3,4,5,6,0}. Let the value of arr be a multiple of 4 and stored in register $s0. What do the following programs do?

1. lw $t0, 12($s0)

add $t1, $t0, $s0

sw $t0, 4($t1)

1. addiu $s1, $s0, 27

lh $t0, -3($s1)

1. addiu $s1, $s0, 24

lh $t0$, -3($s1)

1. addiu $t0, $0, 12

sw $t0, 6($s0)

1. addiu $t0, $0, 8

sw $t0, -4($s0)

1. addiu $s1, $s0, 10 addiu $t0, $0, 6

sw $t0, 2($s1)

1. What are the instructions to branch to label: on each of the following conditions?

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| $s0 | < $s1 | | | $s0 | <= $s1 | | | $s0 > 1 | $s0 >= 1 |
| slt bne | $t0,  $t0, | $s0,  $0, | $s1 label | slt beq | $t0,  $t0, | $s1,  $0, | $s0 label | sltiu $t0, $s0, 2 beq $t0, $0, label | bgtz $s0, label |