

# F2837xD Firmware Development Package

## USER'S GUIDE



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## Revision Information

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# 1 Introduction

The Texas Instruments® F2837xD Firmware development library is a group of example applications and helper libraries that demonstrate the basics of getting started with a F2837xD device.

**The following chapter (chapter 2) provides a step by step guide for from scratch project creation for each core as well as debug. It is highly recommended that users new to the F2837xD family of devices start by reading this section first.**

Because the F2837xD devices have two cores the example applications have been broken up to distinguish which examples run on each core.

- The example applications which run exclusively on the CPU 1 core can be found in the `F2837xD_examples_Cpu1` directory.
- The example applications which require both cores to run can be found in the `F2837xD_examples_Dual` directory.

As users move past evaluation, and get started developing their own application, TI recommends they maintain a similar project directory structure to that used in the example projects. Example projects have a heirarchy as follows:

- Main project directory
  - CPU 1 project folder (cpu01)
    - \* CPU 1 project sources (\*.c, \*.h)
    - \* CCS folder (ccs)
      - CCS project specific files
  - CPU 2 project folder (cpu02)
    - \* CPU 2 project sources (\*.c, \*.h)
    - \* CCS folder (ccs)
      - CCS project specific files

TI also recommends that users append either `_cpu01` or `_cpu02` to project names to help developers differentiate between projects with similar names.

## 1.1 Detailed Revision History

### V1.90

- F2837xD\_Gpio.c - Comment correction
- can.c - Fixed case statement
- Updated IPC CPU2 examples to work for additional GSx memories
- Assigned buffer to RAM section in flash programming examples
- Fixed ePWM setup in eQEP examples
- F2837xD\_CpuTimer.c - Fixed period in ConfigCpuTimer function
- Updated missing fields in DCCAPCTL register in ePWM header file
- Updated DCSM SCC Reset example to allow CPU Timer selection
- Updates to blinky DCSM example

- General fixes to USB library
- USB Dev Mouse example fixes
- Updated SCI Flash Kernel Example
- Added UPP transmit and receive examples

#### **V1.80**

- SDFM Header - MS bit marked as reserved
- EPWM Header - DBRED and DBFED bit fields updated as union and struct. Must be accessed now using .bit or .all
- Flash Header - FBAC.BAGP marked as reserved and FPAC2 register is removed.
- I2C Header - Added I2CISRC.WRITE\_ZEROS bit field
- XBAR Header - Renamed ADCSOCA to ADCSOCOA and ADCSOCB to ADCSOCBO
- Added new example - DMA GSRAM Transfer
- Corrected issue with Blinky DCSM example
- Corrected LPM examples regarding watchdog and flash power down
- sysctl.c - Corrected SysCtlAuxClockSet driver function race condition for 120MHz SysClk

#### **V1.70**

- Fixed flash\_programming example to assign Example\_CallFlashAPI() to RAM section
- Memory Configuration header - Renamed ROM Prefetch register bit field PFDISABLE to PFENABLE
- DMA header - Removed bit fields SYNCE and SYNCSEL from DMA channel Mode register
- DMA header - Removed bit fields SYNCFRC and SYNCCLR from DMA channel Control register
- SCI header - Corrected spelling of SCI FIFO transmit register bit field from TXFIFOXRESET to TXFIFORESET
- SPI header - Removed PRIORITY bit field from SPI priority control register (SPIPRI)
- F2837xD\_defaultisr.h is no longer included in F2837xD\_device.h
- Corrected PLLCLK\_BY\_80 value in F2837xD\_Examples.h
- DCSM header - Changed GRAB\_BANK2 to GRAB\_BANK1, EXEONLY\_BANK2 to EXEONLY\_BANK1, and STATUS\_BANK2 to STATUS\_BANK1
- Added CAN Message RAM section to linker command files
- Flash header - Added PUMPREQUEST register
- Flash header - Removed FSPRD register
- Updated linker command files to support ramfunc attribute
- Updated CAN (CANA, CANB) interrupt line and ISR references from 1 and 2 to 0 and 1
- Added new BUFFDAC examples: buffdac\_ramp, buffdac\_random, buffdac\_sine, and buffdac\_square
- Added new ADC SOC EPWM temperature sensor example (adc\_soc\_epwm\_tempsensor)
- Updated example description for adc\_soc\_software
- Added new ADC synchronous software triggering example (adc\_soc\_software\_sync)
- X-Bar header - Renamed TrigRegs to SyncSocRegs and moved to the SysCtrl header



- X-Bar header - EXTADCSOCSELECT register renamed to ADCSOCOUTSELECT and SYNC-SOCLCK.EXTADCSOCSELECT field renamed to SYNC-SOCLCK.ADCSOCOUTSELECT
- SysCtrl header - Added SyncSocRegs and removed incorrect DCx and SOFTPRESx registers
- Added SafeCopyCode Reset example (dcsn\_scc\_reset)
- IPC header - Removed PUMPREQUEST register
- SDFM header - Removed SDSTATUS register and removed SDCTLPARM1.MS bit field
- F2837xD\_Examples.h - Changed FMULT\_1 to FMULT\_0

## **V1.60**

- Aligned sysctl.c SysCtlClockSet() with correct clock initialization flow
- Calling InitSysCtrl() from CPU2 will now call InitPeripheralClocks() and enable the clocks
- Removed F2837xD\_hwbistcontext.asm
- Updated F2837xD\_epwm.h with HRPCTL PWMSYNCSSEL bit
- Changed HWBIST bits to reserved in f28x7\_nmiinterrupt.h and F2837xD\_sysctrl.h
- Updated InitAuxPll() in F2837xD\_SysCtrl.c with correct initialization flow
- Updated InitSysPll() in F2837xD\_SysCtrl.c to set multipliers in a single 32-bit write
- Fixed GPIO setup options in all SCI examples
- Fixed CAN drivers to avoid issues with 32-bit reads/writes while using optimization
- Fixed adc\_soc\_epwm example and added volatile to bufferFull variable
- Added power consumption note regarding InitPeripheralClocks() in F2837xD\_SysCtrl.c
- Fixed uart.c driver issue regarding non-volatile loop conditions
- Added target configuration file to all examples
- usb.c - Updated USBIntStatus to work around USB stalling due to edge triggering issue
- Updated USBIntHandlerInternals to accept USBTXIS/USBRXIS status argument to ensure the status is handled correctly.
- Fixed offsets in USBHSCSIWrite10() of usbhscsi.c to prevent writing of incorrect commands
- Removed OTG mode section from the USB Library User Guide
- Fixed UARTprintf function in uartstdio.c to support long format

## **V1.50**

- Added EMIF 16bit SDRAM DMA example
- Added EMIF 16bit SDRAM Far memcpy example
- Added Single and Dual core hibernate wake-up examples
- Added F2837xD Peripheral Driver Library User Guide
- F2837xD\_cla.h - Reserved space added between MAR1 and MSTF
- F2837xD\_cla.h - Added a union called MR\_REG made up of an Uint32 and a float
- F2837xD\_epwm.h - Added HRCNFG2 register
- F2837xD\_epwm.h - Changed TZOSTFLG.DCx EVT2 bits to TZOSTFLG.DCx EVT1
- F2837xD\_epwm.h - Changed TZOSTCLR.DCx EVT2 bits to TZOSTCLR.DCx EVT1
- F2837xD\_spi.h - Added HS\_MODE bit
- Updated hrpwm\_prdupdown\_sfo\_v8 example so that PHSEN is disabled

- Fixed issue in IPCBootCPU2 function in F2837xD\_Ipc\_Driver\_Util.c
- Cleaned up example source and header code comments
- Cleaned up example CCS warnings
- Fixed error in mmc-F2837x.c for FATFS
- Corrected CAN Loopback interrupts example source name
- Updated CLA C compiler section in F2837xD User Guide
- Updates to F2837xD SCI Flash Kernel examples
- Renamed DCAN references to CAN
- Updated IPC ISR comments to reflect correct interrupt numbers

#### **V1.40**

- sci\_echoback example description updated
- Updated F2837xD\_Cla\_typedefs.h to include additional typedef guards
- Updated F2837xD\_device.h typedefs guards
- Updated CLA linker command files for C2000 compiler 6.4.x support
- Fixed case mismatches in various example include files
- Removed PBIST and HWBIST header files
- Updated CLA examples and removed 3 NOPs before writing to the MCTL register
- Removed CAN sections from linker header files
- Updated Flash linker command files to align on 64-bit boundary
- Cleaned up F2837xD CPU1 and Dual Examples CCS warnings
- F2837xD\_PieVect.c - Fixed comment for IPC interrupt
- Updated mcbasp\_loopback\_dma example to initialize PIE correctly
- Changed .Mux to .MUX in F2837xD\_epwm\_xbar.h and F2837xD\_output\_xbar.h
- Fixed build error in SDFM Filter Sync CLA example
- Updated EPwm.h - TRIPINPUT13 in DC submodule reserved
- Added lpm\_haltwake example
- Updated EPWM X-Bar TRIPINV misnamed fields
- Updated DCSM reserved fields in header structs to correct word size
- Added Cla1SoftIntRegs to CLA Header file
- Cleaned up code and comments in F2837xD\_device.h
- Added EMIF1 examples and associated source/header files
- F2837xD\_Dcan\_defines.h renamed to F2837xD\_Can\_defines.h

#### **V1.30**

- Removed SPI\_REG D
- Removed SDFM\_REGS 3 and 4
- Removed EQEP\_REG 4
- Removed EPWM\_REGS 13 through 16
- Removed ECAP\_REGS 7 and 8
- Removed CMPSS\_REGS 9 through 12

- Renamed OUTPUT X-XBAR OUT0-7 Registers to OUTPUT1-8
- Renamed Register \_MSTF bitfield RPC to \_RPC
- Added DmaClaSrcSelRegs for CPU2
- Fixed cla\_adc\_fir32\_cpu01 example undefined symbol
- Fixed sdfm\_filters\_sync\_cla build issue
- SysCtrl.c fixes in HALT() and HIB(). Also add DisablePeripheralClocks() function
- F28x7x\_SysCtrl.C - InitSysPll() Errata Fix
- Removed incorrect comments in Examples
- Deleted Can.h and Usb.h bit structured headers from /include
- Removed incomplete drivers from F2837xD\_common/driverlib
- Fixed SysCtrl header comment
- Fixed F2837xS Sysctrl.c references InitFlash
- Added lpm\_idlewake example
- Added lpm\_standbywake example
- Cleaned up Dual Example - Flash\_Programming
- Corrected data buffer size in Flash API example
- Added additional OTP prevention for examples
- Fixed redefined TRUE/FALSE defines from stdbool.h
- Added Example to show DMA being triggered from other CPU
- F2837xD\_sci\_io.c - Updated SCI Regs
- F2837xD\_SysCtrl.c - Removed incorrect FlashCtrlRegs reference
- Rewrote IPC driver to meet "One entry, one exit" standard
- Fixed 2837x\_RAM\_IQMATH\_Ink\_cpu1.cmd Page Issue
- SPI Module XML - Fixed missing SPICCR
- In Device .h - Extended bit definition to 32-bits
- Blinky DCSM example corrections
- Removed unused variable warning in flash programming example
- Fixed Capitalization issues preventing examples from building on Linux

## **V1.20**

- Updated eqep examples to use rts2800 for fpu32
- Corrected DCSM\_OPT\_Z1 and DCSM\_OPT\_Z2 origin addresses
- Updated usb\_dev\_serial\_cpu01 to fix CCS linking errors
- Fixed some USB examples with missing StackModeSet call
- Updated eqep examples with IQmath lib for FPU32
- Added cla\_support option to cla\_atan example
- Fixed McBSP Loopback CPU1 Example Issues for 32-bit transfers
- Updated F2837xD\_Dma\_defines.h with missing SPI and USB trigger defines
- Corrected USB guide text and formatting issues
- Removed Redundant code found in dual core examples

- Cleaned up CPU1 Example File Titles/Descriptions
- Added DMA SPI example
- Fixed McBSP\_DLB\_DMA example so both DMA CH1 and CH2 Interrupts occur
- Corrected EPWMsetup.c in eqep\_freq\_cal\_cpu01 example to output correct waveform
- Re-added the tmu\_support command line option from the tmu example
- Re-added the cla\_support command line option from the cla examples

#### **V1.10**

- IPC interrupts renumbered from 1-4 to 0-3 to match flag numbers
- BIOS linker files were missing declarations for EmuBModeVar, EmuKeyVar, and PieVectTable-File. These were added with a DSECT type to prevent warnings.
- Added missing F2837xD\_common/tools folder
- PieVect Table made to be volatile
- Removed extra copys of GlobalVariableDefs.c
- Added USB Dual Mode Example
- USB Examples - moved memcpy before PLL initialization to fix examples
- Updated example build options to use built in VCU, CLA, and TMU options
- F2837x\_Device.h - put guard macros around assert and stdarg.h to prevent the CLA from using these includes
- Added SW Prioritized Interrupt example
- GPIO Setup example now properly configures IOs for trip zones

#### **V1.00**

- This version is the first release (packaged with development tools and customer trainings) of the F2837xD header files and examples.

## 2 Getting Started and Troubleshooting

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### 2.1 Introduction

Because of the sheer complexity of the F2837xD devices, it is not uncommon for new users to have trouble bringing up the device their first time. This guide aims to give you, the user, a step by step guide for how to create and debug projects from scratch. This guide will focus on the user of a F2837xD controlCARD, but these same ideas should apply to other boards with minimal translation.

### 2.2 Project Creation

A typical F2837xD application consists of two separate CCS projects: one for CPU 1 and one for CPU2. The two projects are completely independent and have no real linking between them as far as CCS is concerned.

## CPU 1 Subsystem Project Creation

1. From the main CCS window select File -> New -> CCS Project. Name your project and choose a location for it to reside. Click Finish and your project will be created.

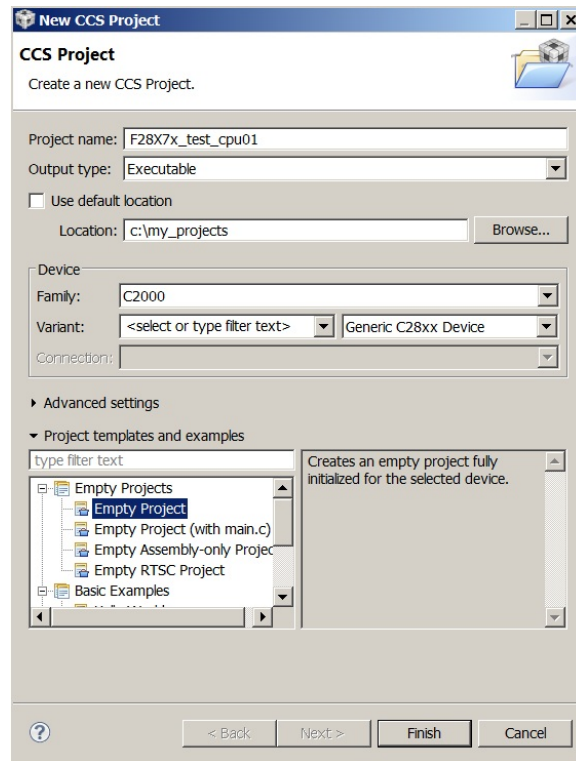


Figure 2.1: Creating a new C28 project

2. Before we can successfully build a project we need to setup some build specific settings. Right click on your project and select Properties. Look at the Processor Options and ensure they match the below image:

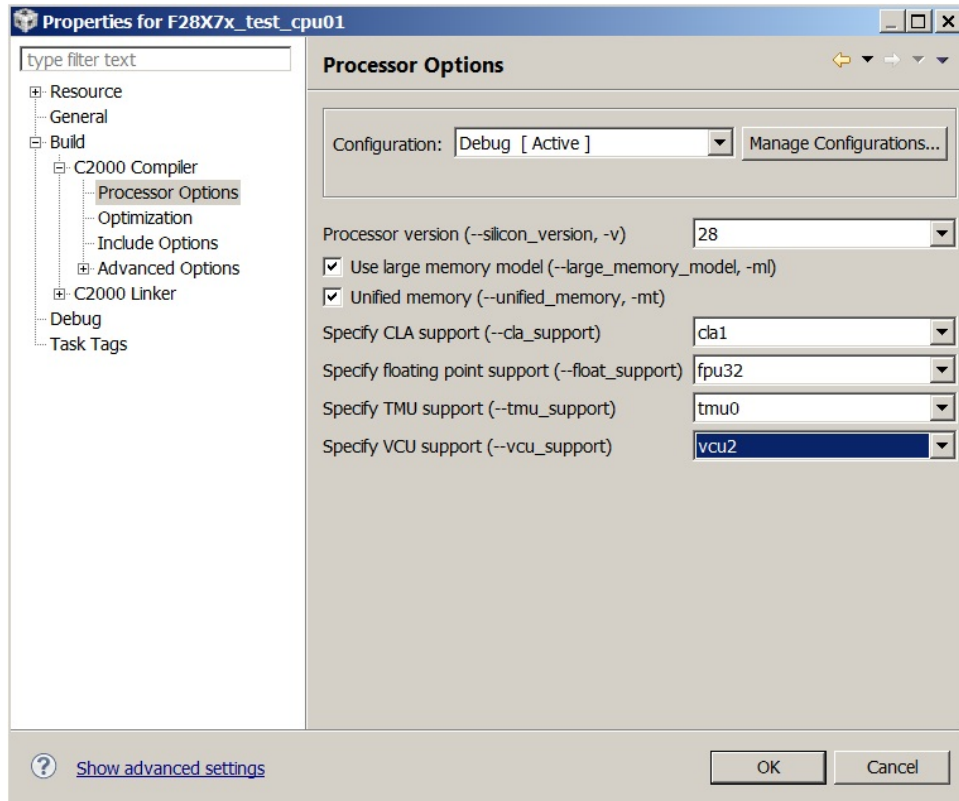


Figure 2.2: Project configuration dialog box

3. In the C2000 Compiler entry look for and select the Include Options. Click on the add directory icon to add a directory to the search path. Click the File System button to browse to the F2837xD\_common\include folder of your controlSUITE installation (typically C:\TI\controlSUITE\device\_support\F2837xD\VERSION\F2837xD\_common\include). Click ok to add this path, and repeat this same process to add the F2837xD\_headers\include directory.

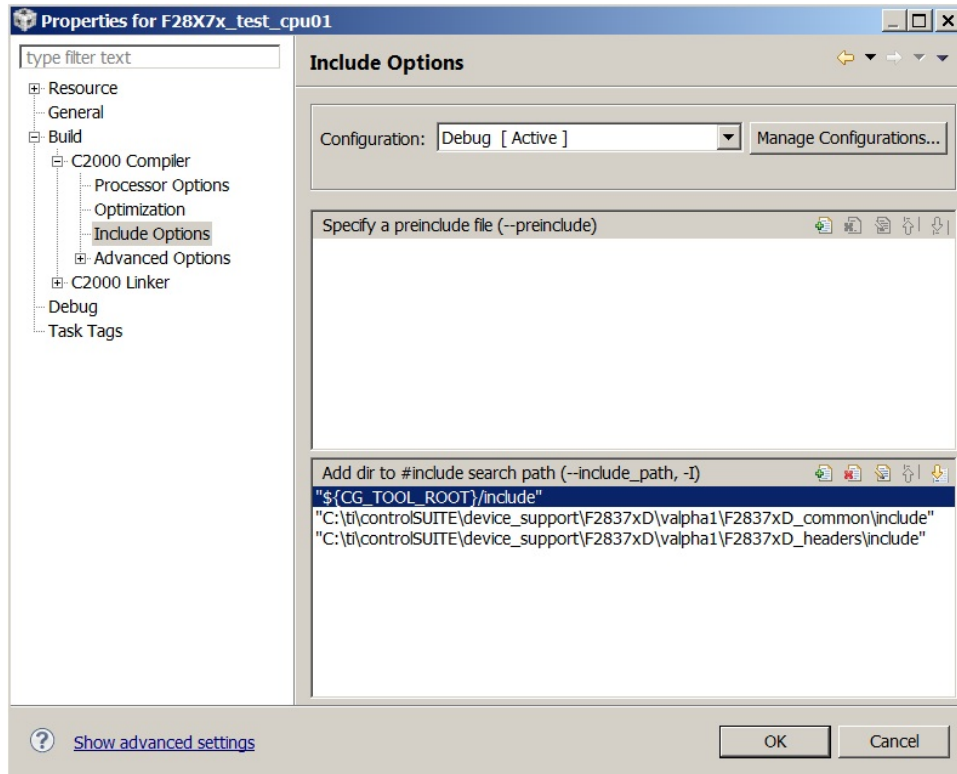


Figure 2.3: Project configuration dialog box



4. Expand the Advanced Options and look for the Predefined Symbol entry. Add a Pre-define NAME called "CPU1". This ensures that the header files build correct for this CPU.

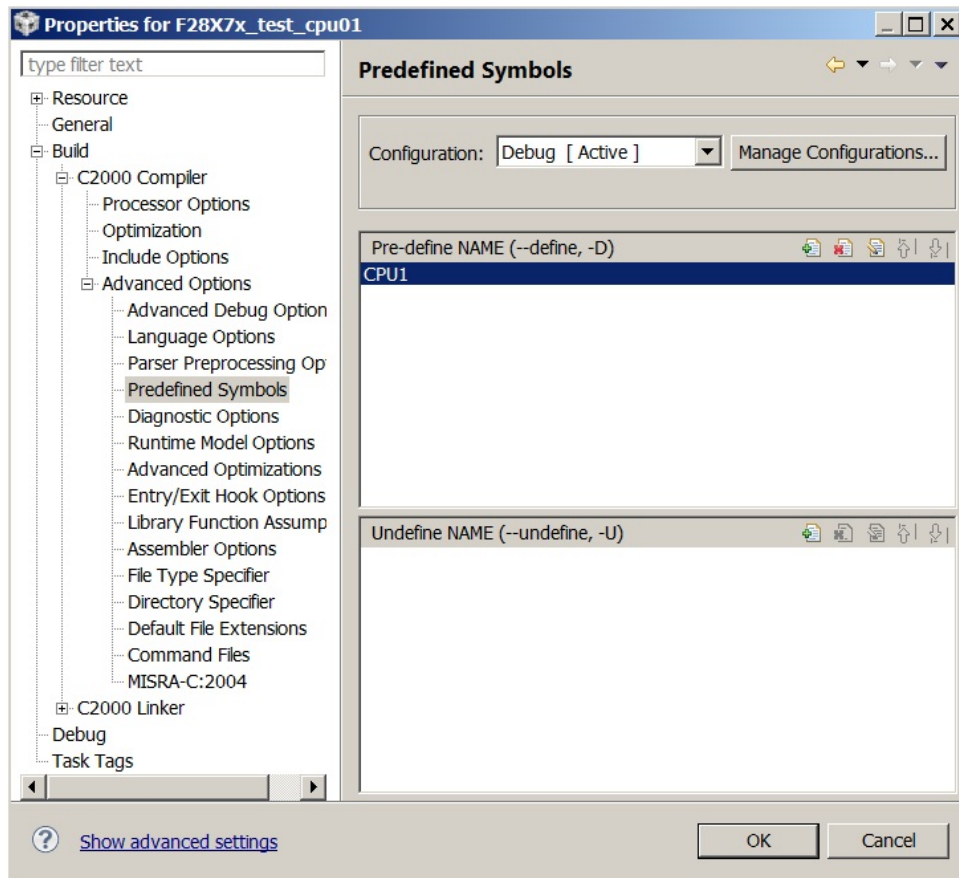


Figure 2.4: Project configuration dialog box

5. Click on the Linker File Search Path. Add these directories to the search path: F2837xD\_common\cmd and F2837xD\_headers\cmd. Then you'll also want to add the following files: rts2800\_fpu32.lib, 2837x\_RAM\_lnk\_cpu1.cmd, and F2837x-Headers\_nonBIOS\_cpu1.cmd. Finally, delete libc.a, we will use rts2800\_fpu32.lib as our run time support library instead.

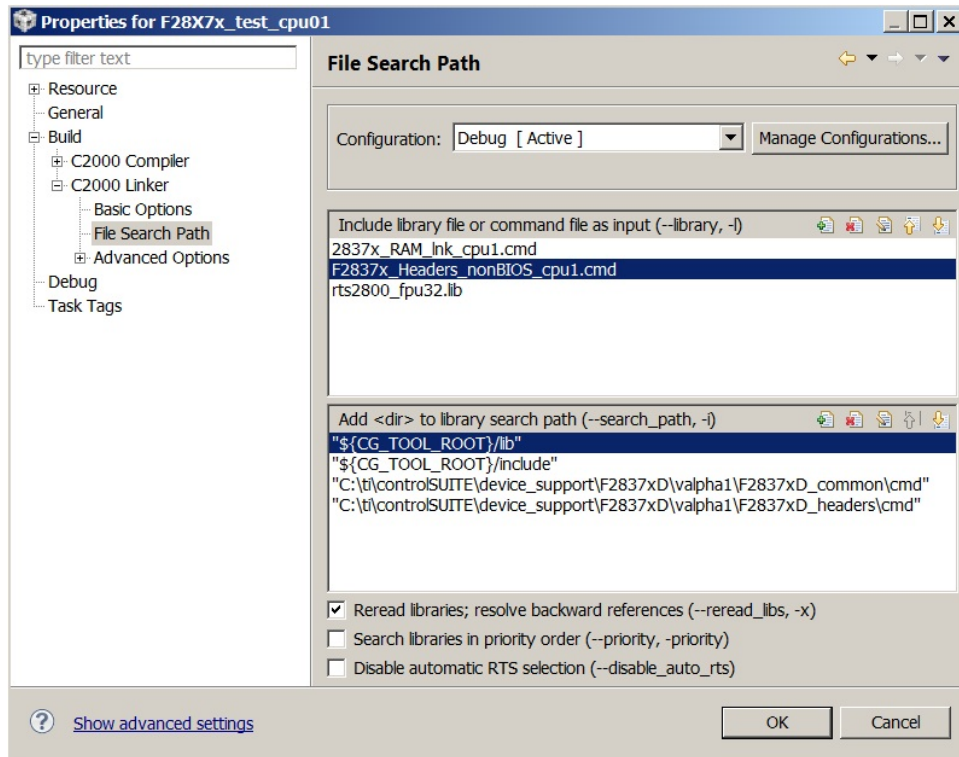


Figure 2.5: Project configuration dialog box

6. While you have this window open select the Symbol Management options under C2000 Linker Advanced Options. Specify the program entry point to be `code_start`. Select ok to close out of the Build Properties.

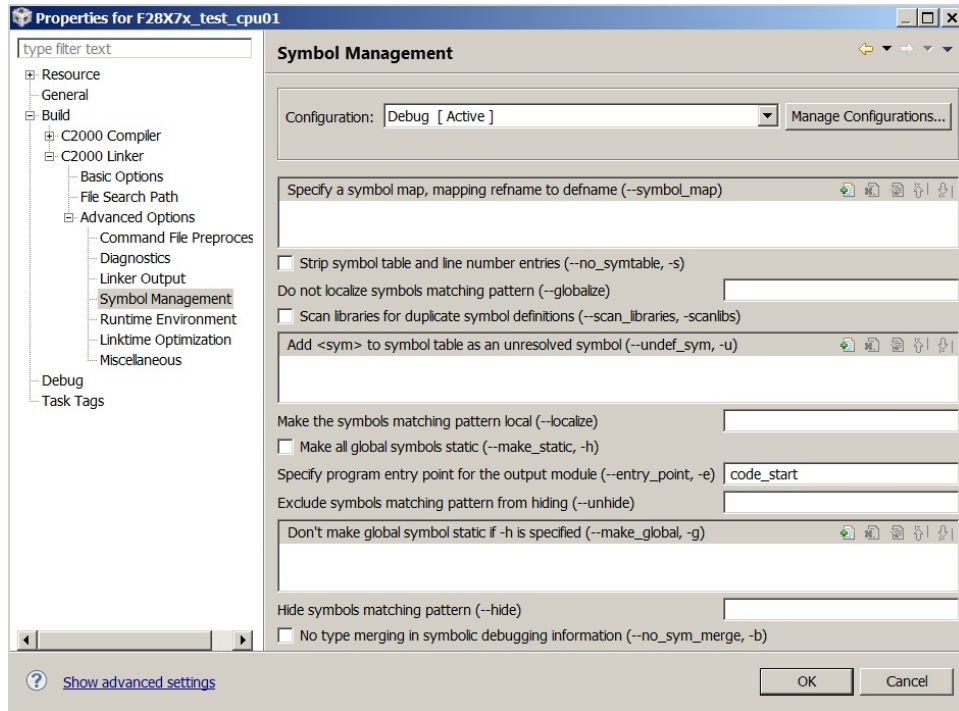


Figure 2.6: Include path setup

7. Next we need to link in a few files which are used by the header files. To do this right click on your project in the workspace and select Add Files... Navigate to the F2837xD\_headers\source directory, and select F2837xD\_GlobalVariableDefs.c. After you select the file you'll have the option to copy the file into the project or link it. We recommend you link files like this to the project as you will probably not modify these files. Link in the following files as well:

- F2837xD\_common\source\F2837xD\_CodeStartBranch.asm
- F2837xD\_common\source\F2837xD\_usDelay.asm
- F2837xD\_common\source\F2837xD\_SysCtrl.c
- F2837xD\_common\source\F2837xD\_Gpio.c
- F2837xD\_common\source\F2837xD\_Ipc.c

At this point your project workspace should look like the following:

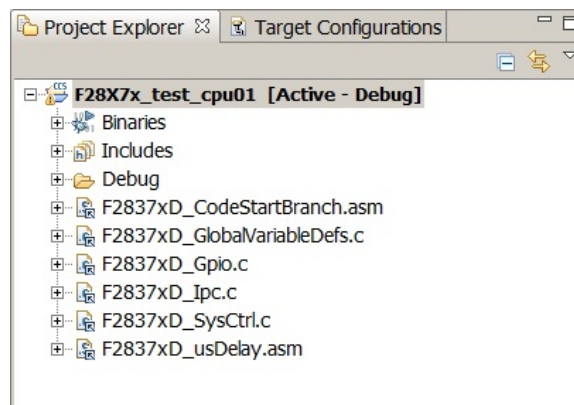


Figure 2.7: Linking files to project

8. Create a new file by right clicking on the project and selecting New -> File. Name this file main.c and copy the following code into it:

```
#include "F28x_Project.h"

void main(void)
{
    uint32_t delay;

    InitSysCtrl();

    // Set pin direction
    EALLOW;
    GpioCtrlRegs.GPDIR.bit.GPIO10 = 1;
    EDIS;

    GPIO_SetupPinOptions(14, GPIO_OUTPUT, GPIO_PUSHPULL);
    GPIO_SetupPinMux(14, GPIO_MUX_CPU2, 0);

    // turn off LED
    GpioDataRegs.GPADAT.bit.GPIO10 = 1;

    while(1)
    {

        // Turn on LED
        GpioDataRegs.GPADAT.bit.GPIO10 = 0;

        // Delay for a bit.
        for(delay = 0; delay < 2000000; delay++)
        {

        }

        // Turn off LED
        GpioDataRegs.GPADAT.bit.GPIO10 = 1;

        // Delay for a bit.
        for(delay = 0; delay < 2000000; delay++)
        {

        }

    }
}
```

9. Save main.c and then attempt to build the project by right click on it and selecting Build Project. Assuming the project builds try debugging this project on a F2837xD device. When the code runs you should see GPIO 10 toggle.

## CPU 2 Subsystem Project Creation

1. From the main CCS window select File -> New -> CCS Project. Name your project and choose a location for it to reside. Click Finish and your project will be created.

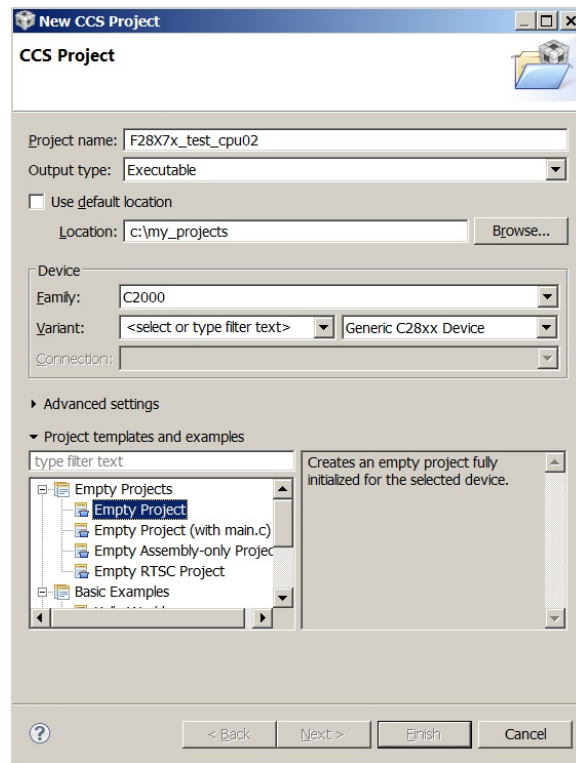


Figure 2.8: Creating a new C28 project

2. Before we can successfully build a project we need to setup some build specific settings. Right click on your project and select Properties. Look at the Processor Options and ensure they match the below image:

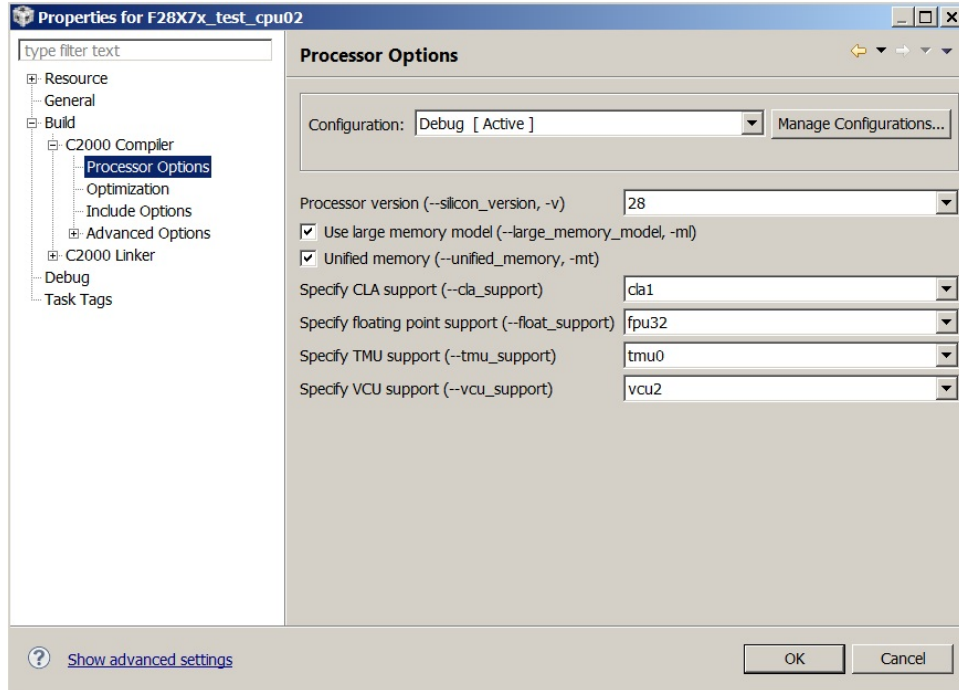


Figure 2.9: Project configuration dialog box

3. In the C2000 Compiler entry look for and select the Include Options. Click on the add directory icon to add a directory to the search path. Click the File System button to browse to the F2837xD\_common\include folder of your controlSUITE installation (typically C:\TI\controlSUITE\device\_support\F2837xD\VERSION\F2837xD\_common\include). Click ok to add this path, and repeat this same process to add the F2837xD\_headers\include directory.

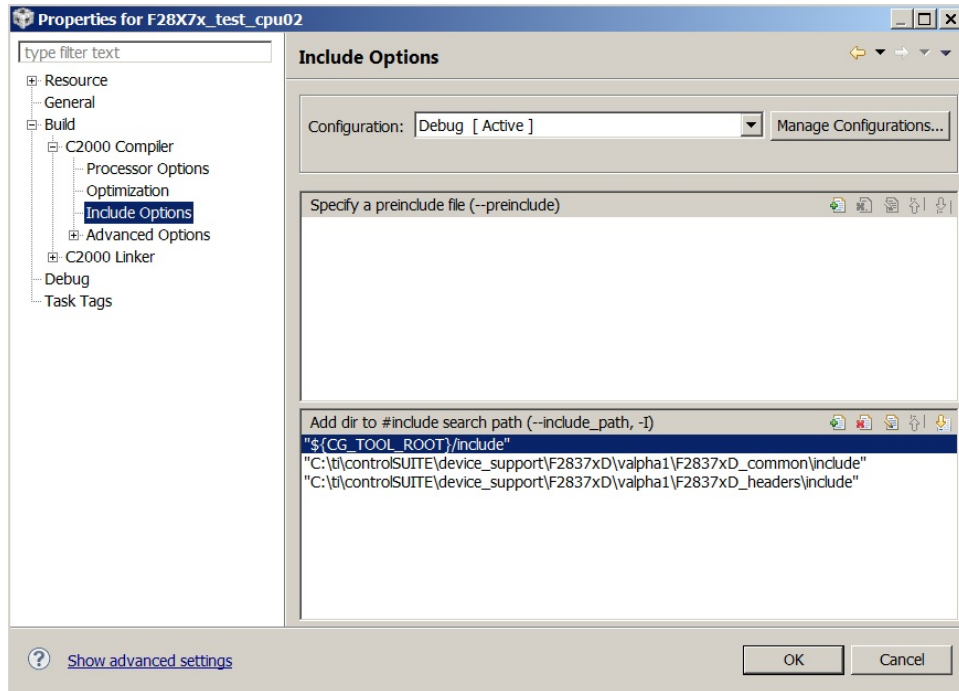


Figure 2.10: Project configuration dialog box



4. Expand the Advanced Options and look for the Predefined Symbol entry. Add a Pre-define NAME called "CPU2". This ensures that the header files build correct for this CPU.

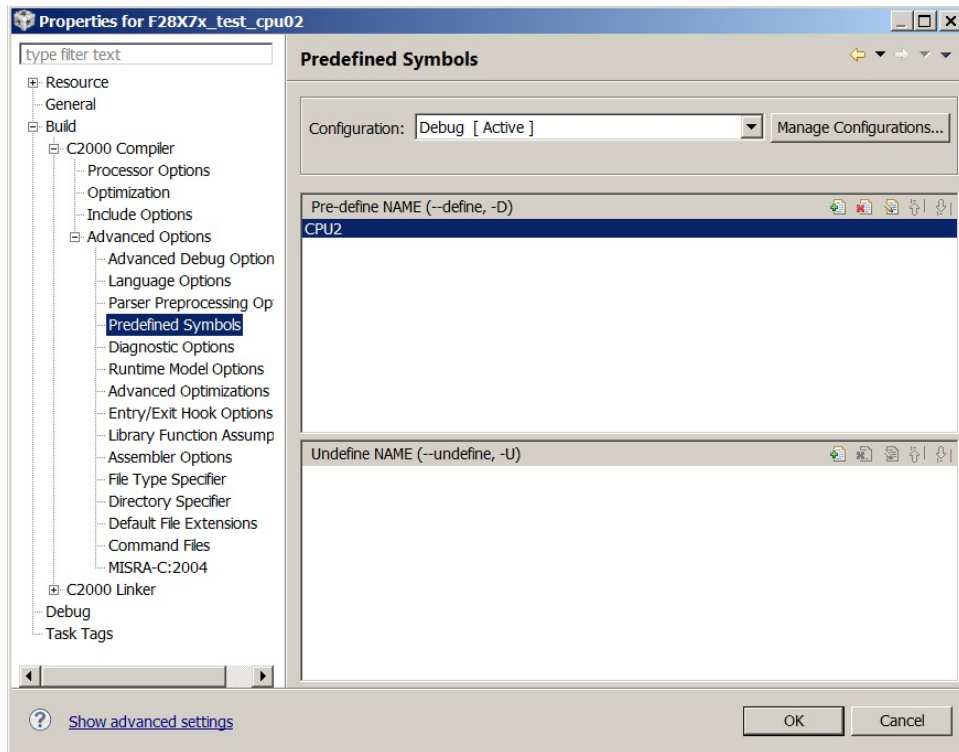


Figure 2.11: Project configuration dialog box

- Click on the Linker File Search Path. Add these directories to the search path: F2837xD\_common\cmd and F2837xD\_headers\cmd. Then you'll also want to add the following files: rts2800\_fpu.lib, 2837x\_RAM\_lnk\_cpu2.cmd, and F2837x-Headers\_nonBIOS\_cpu2.cmd. Finally, delete libc.a, we will use rts2800\_fpu.lib as our run time support library instead.

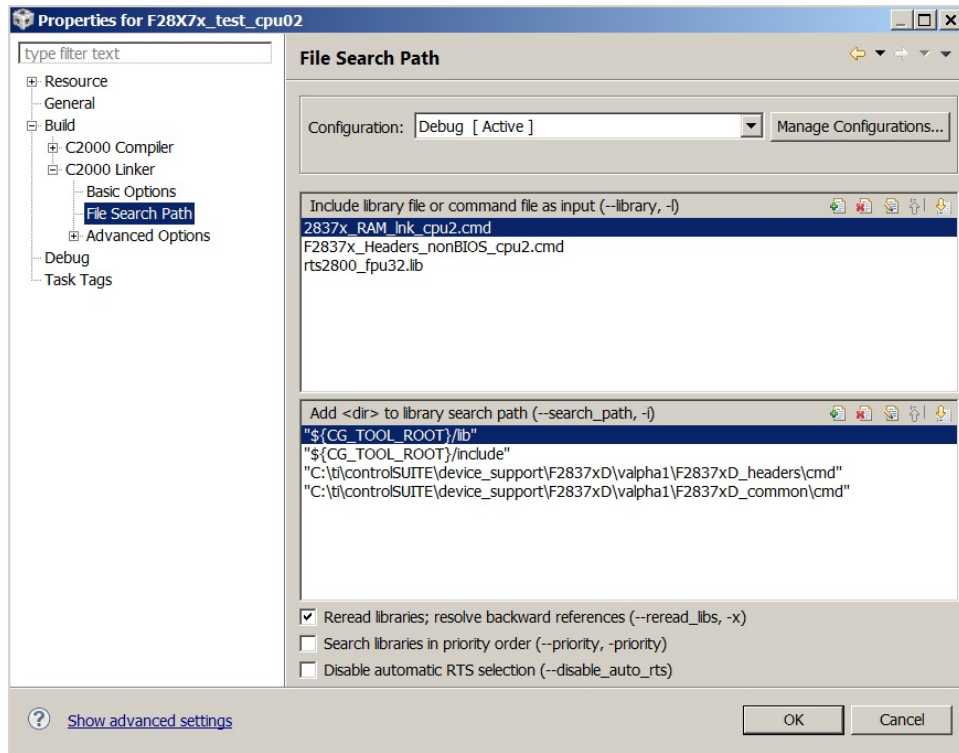


Figure 2.12: Project configuration dialog box

6. While you have this window open select the Symbol Management options under C2000 Linker Advanced Options. Specify the program entry point to be `code_start`. Select ok to close out of the Build Properties.

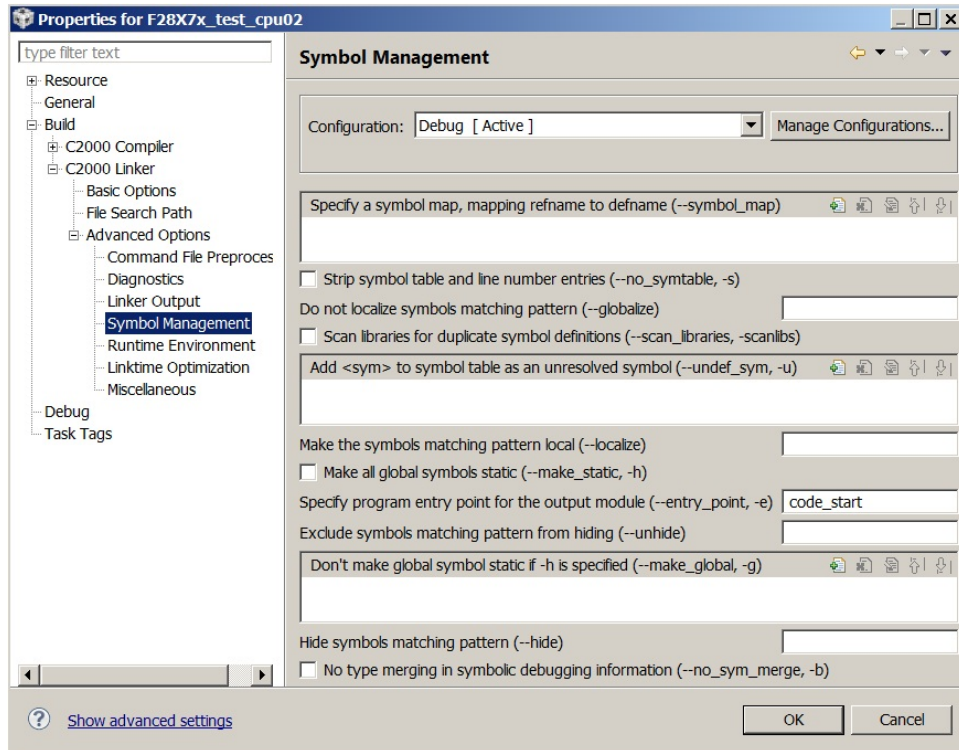


Figure 2.13: Include path setup

7. Next we need to link in a few files which are used by the header files. To do this right click on your project in the workspace and select Add Files... Navigate to the F2837xD\_headers\source directory, and select F2837xD\_GlobalVariableDefs.c. After you select the file you'll have the option to copy the file into the project or link it. We recommend you link files like this to the project as you will probably not modify these files. Link in the following files as well:

- F2837xD\_common\source\F2837xD\_CodeStartBranch.asm
- F2837xD\_common\source\F2837xD\_usDelay.asm
- F2837xD\_common\source\F2837xD\_SysCtrl.c
- F2837xD\_common\source\F2837xD\_Gpio.c
- F2837xD\_common\source\F2837xD\_Ipc.c

At this point your project workspace should look like the following:

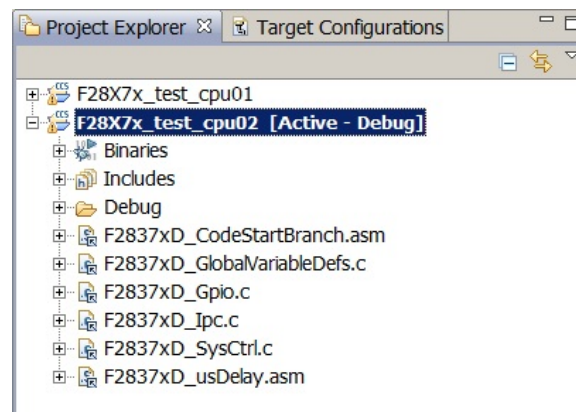


Figure 2.14: Linking files to project

8. Create a new file by right clicking on the project and selecting New -> File. Name this file main.c and copy the following code into it:

```
#include "F28x_Project.h"

void main(void)
{
    uint32_t delay;

    // turn off LED
    GpioDataRegs.GPADAT.bit.GPIO14 = 1;

    while(1)
    {

        // Turn on LED
        GpioDataRegs.GPADAT.bit.GPIO14 = 0;

        // Delay for a bit.
        for(delay = 0; delay < 2000000; delay++)
        {
        }

        // Turn off LED
        GpioDataRegs.GPADAT.bit.GPIO14 = 1;

        // Delay for a bit.
        for(delay = 0; delay < 2000000; delay++)
        {
        }

    }
}
```

9. Save main.c and then attempt to build the project by right click on it and selecting Build Project. Assuming the project builds try debugging both these projects simultaneously on a F2837xD device, otherwise carefully examine the error and the above steps to determine what could have gone wrong.

## 2.3 Debugging Dual Core Applications

1. Ensure CCS version 5 is installed and up to date. You should have C2000 Code Generation Tools version 6.2.0 or later.
2. Connect a USB Mini cable from the computer to the USB port on the left hand side of the controlCARD. Windows will enumerate and try to install drivers. As long as CCS is installed, Windows should automatically find and install drivers for the emulator.
3. Apply power either via USB or the 5V DC in jack on the docking station. While the emulator on the board is powered from the host computer's USB port, the rest of the board is not.

The reason for this is that the JTAG connection on the F2837xD controlCARDs is completely electrically isolated. Because of the typical applications these devices will be used in, it is necessary to isolate the JTAG connection. However, for bench debug and evaluation (with low voltages), both halves of the board can be powered from the same supply (i.e. USB). Each power domain has an associated power LED which can be used to ensure that each domain has power.

4. Launch CCS and pick the workspace you would like to debug in.
5. Create a new target configuration. Click File -> New -> Target Configuration File and name the file appropriately (i.e. F2837xD\_xds100.ccxml). Select the emulator you intend to use (XDS100v2) from the drop down list, and then select the device variant present on your board (F2837xD controlCARDs have a F2837xD). Save the target configuration and close the window.

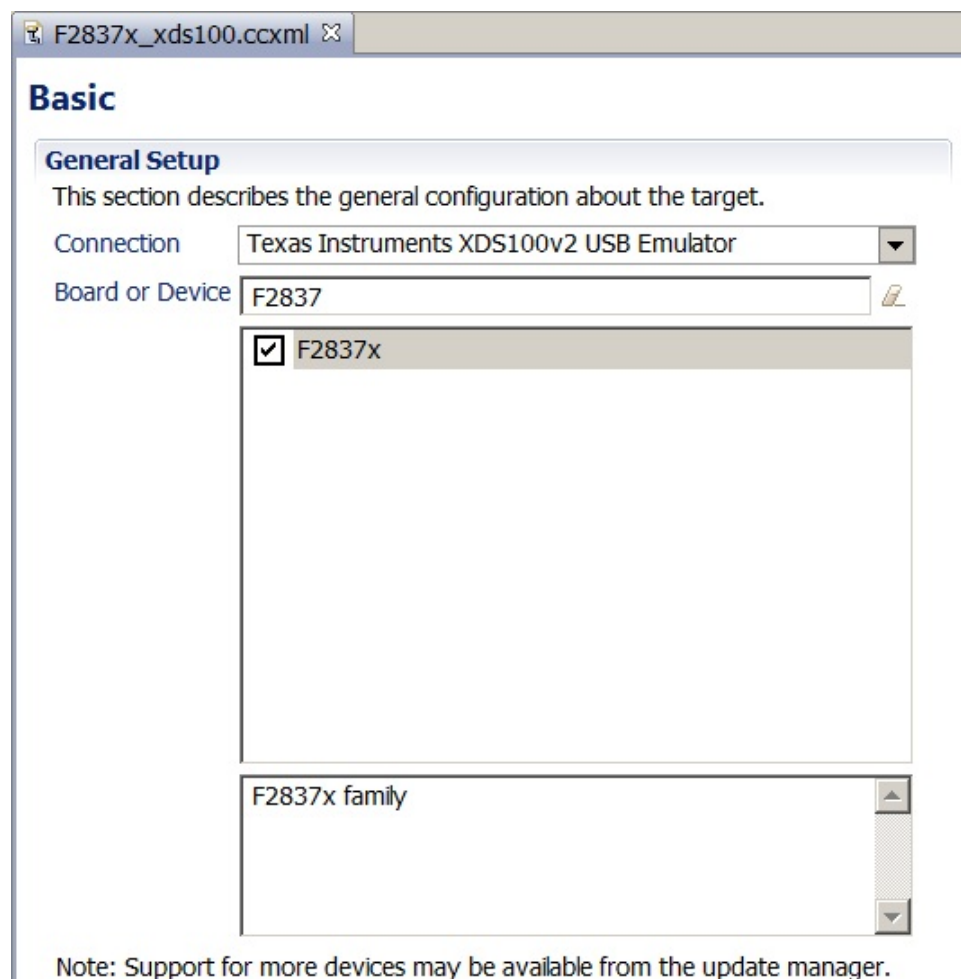


Figure 2.15: F2837xD Card Target Configuration Setup

6. Import the desired example projects (or skip this step if you are using projects you created in the Project Creation section). Click File -> Import, and in the CCS folder select Existing CCS/CCE Eclipse Projects before clicking Next. With the "Select search-directory" radio button checked, browse to the root of your controlSUITE installation. Device specific software as well as examples are stored in the `device_support/device_variant` folders. Navigate

to the F2837xD directory, and then to the F2837xD\_examples\_Dual directory. Click OK and CCS will parse all of the projects in this directory. Import any projects you wish to run into the workspace. **Do not select "Copy projects into workspace"**. These projects link to external resources relatively, so taking them out of controlSUITE will break the project.

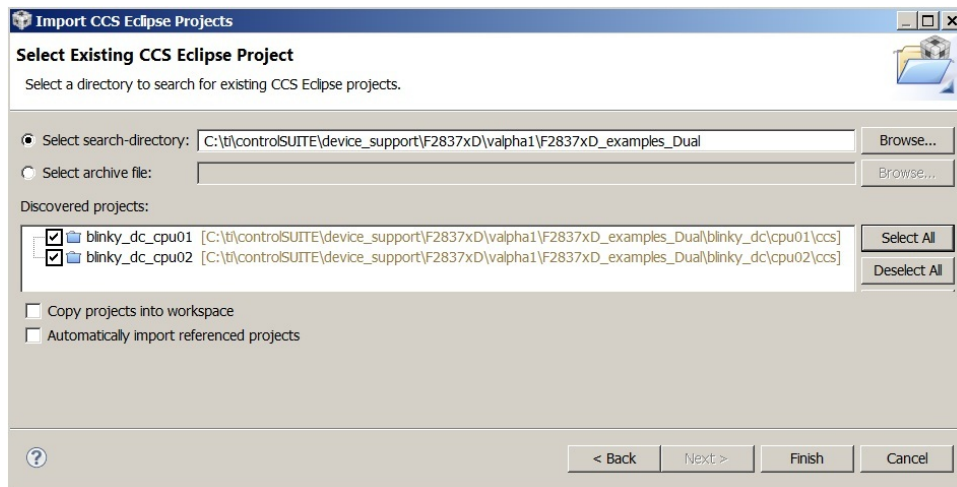


Figure 2.16: Importing F2837xD Projects

- Build each of the example projects. Right click on each project title and select build project.

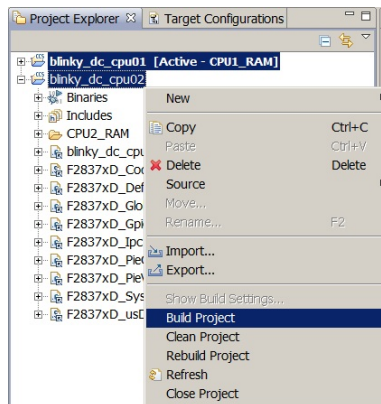


Figure 2.17: Building F2837xD Projects

- Launch the previously created target configuration. Click View -> Target Configurations. In the window that opens, find the target configuration you created previously, right click on it and select "Launch Target Configuration".

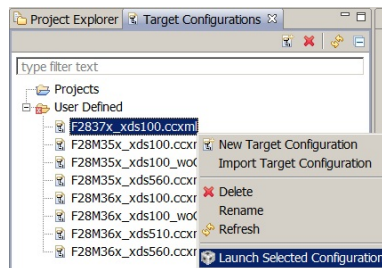


Figure 2.18: Launching a CCS Target Configuration

9. Connect to the device. Right click on each core in the debug window and select "Connect Target". This will connect CCS to the device and will allow you to load code and debug applications.

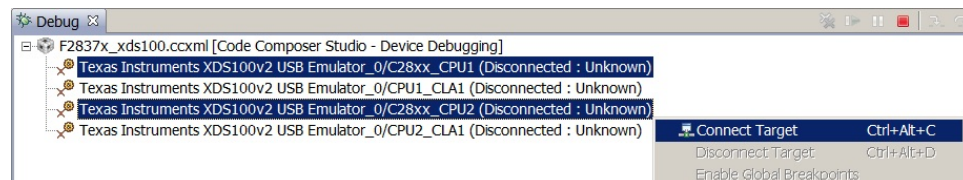


Figure 2.19: Connecting to a Target

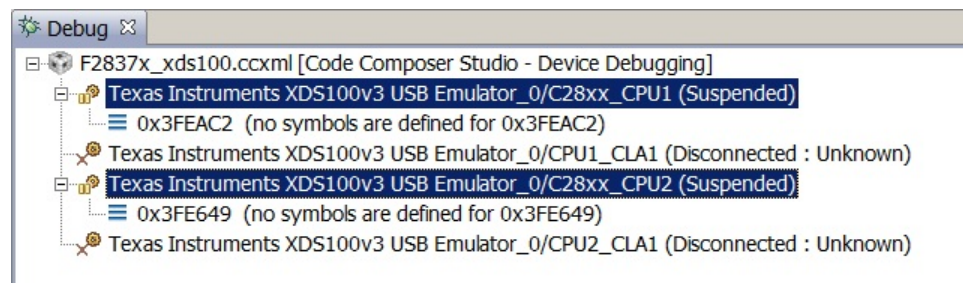


Figure 2.20: After connection to both cores

10. Load code on each of the cores. Select one of the cores in the debug window and then click Target -> Load Program. A dialog box is display which will allow you to select a program to load. Be careful to ensure that you load the appropriate out file on the appropriate core. Repeat this process for the other core by selecting it and following these same steps.
11. At this point both cores should have code loaded and be halted at main. From this point, users should be able to debug code just as they are used to with CCS. Please keep in mind that any action you take in CCS only has an effect on the core you currently have selected in the debug window. For instance if CPU 1 is selected, the memory window will display the memory map of of the system as seen by CPU 1. The opposite would be true if CPU 2 were selected.



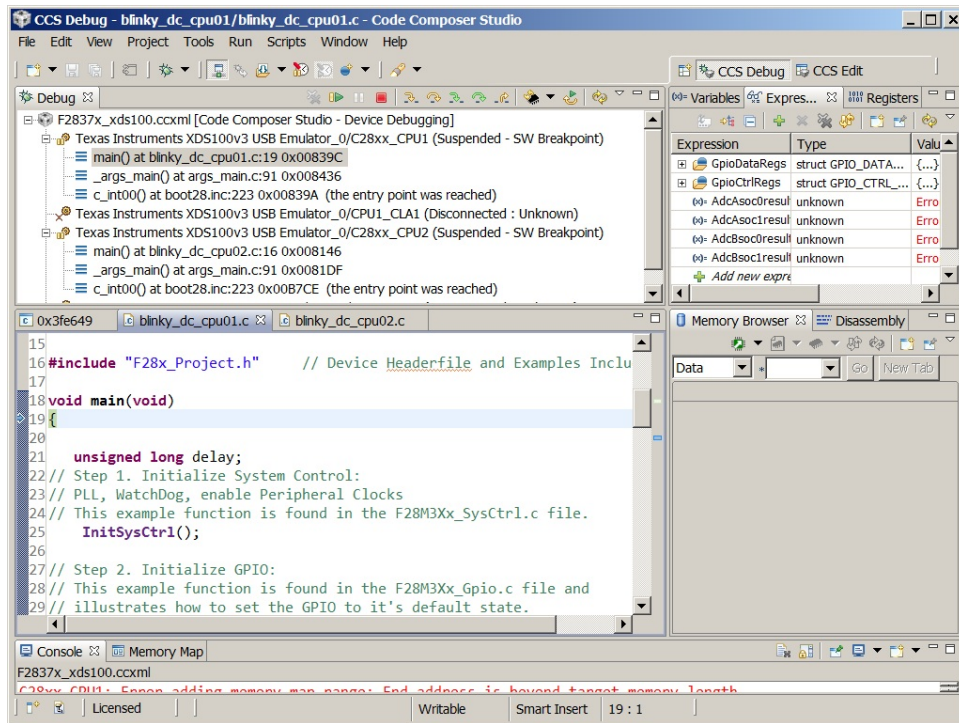


Figure 2.21: Projects loaded on each core

## 2.4 Troubleshooting

There are a number of things that can cause the user trouble while bringing up a debug session the first time. This section will try to provide solutions to the most common problems encountered with the Delfino devices.

### "I get a managed make error when I import the example projects"

This occurs when one imports a project for which he or she doesn't have the code generation tools for. Please ensure that you have at least version 6.2.0 of the C2000 Code Generation Tools.

### "I cannot build the example projects"

This is caused by linked resources not being where the project expects them to be. For instance, if you imported the projects and selected "Copy projects to workspace", the projects would no longer build because the files they reference aren't a part of your workspace. Always build and run the examples directly in the controlSUITE tree.

### "My F2837xD device isn't in the target configuration selection list"

The list of available device for debug is determined based on a number of factors, including drivers and tools chains available on the host system. If you system has previously been used only for development on previous C2000 devices, you may not have the required CCS device files. In CCS click on "Help, Check for updates" and follow the dialog boxes to update your CCS installation.

### "I cannot connect to the target"

This is most often times caused by either a bad target configuration, or simply the emulator being physically disconnected. If you are unable to connect to a target check the following things:

1. Ensure the target configuration is correct for the device you have.
2. Ensure the emulator is plugged in to both the computer and the device to be debugged.
3. Ensure that the target device is powered.

#### **"I cannot load code"**

This is typically caused by an error in the GEL script or improperly linked code. GEL files shipped in controlSUITE are tested and should work without modification with F2837xD devices, but advanced users may potentially alter GEL files depending on their overall system configuration. If you are having trouble loading code, check the linker command files and maps to ensure that they match the device memory map. If these appear correct, there is a chance there is something wrong in one of your GEL scripts.

#### **"When a core gets an interrupt, it faults"**

Ensure that the interrupt vector table is where the interrupt controller thinks it is. On both cores the interrupt vector table may be mapped to either RAM or flash. Please ensure that your vector table is where the interrupt controller thinks it is.

#### **"When the CPU1 comes up, it is not fresh out of reset"**

F2837xD devices support several boot modes, several of which allow program code to be loaded into and executed out of RAM via one of the device many serial peripherals. If the boot mode pins are in the wrong state at power up, one of these peripheral boot modes may be entered accidentally before the debugger is connected. This leaves the chip in an unclear state with potentially several of the peripherals configured as well as the interrupt vector table setup. If you are seeing strange behavior check to ensure that the "Boot to Flash" or "Boot to RAM" boot mode is selected.

## 3 Interrupt Service Routine Priorities

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### 3.1 Interrupt Hardware Priority Overview

With the PIE block enabled, the interrupts are prioritized in hardware by default as follows:

**Global Priority (CPU Interrupt level):**

CPU Interrupt	Hardware Priority
Reset	1(Highest)
INT1	5
INT2	6
INT3	7
INT4	8
INT5	9
INT6	10
INT7	11
...	...
INT12	16
INT13	17
INT14	18
DLOGINT	19(Lowest)
RTOSINT	20
reserved	2
NMI	3
ILLEGAL	-
USER1	-(Software Interrupts)
USER2	-
...	...

CPU Interrupts INT1 - INT14, DLOGINT and RTOSINT are maskable interrupts. These interrupts can be enabled or disabled by the CPU Interrupt enable register (IER).

**Group Priority (PIE Level):**

If the Peripheral Interrupt Expansion (PIE) block is enabled, then CPU interrupts INT1 to INT12 are connected to the PIE. This peripheral expands each of these 12 CPU interrupt into 8 interrupts. Thus the total possible number of available interrupts in the PIE is 96. Note, not all of the 96 are used on a 2803x device.

Each of the PIE groups has its own interrupt enable register (PIEIERx) to control which of the 8 interrupts (INTx.1 - INTx.8) are enabled and permitted to issue an interrupt.

CPU Interrupt	PIE Group	PIE Interrupts							
		Highest ————— Hardware Priority Within the Group ————— Lowest							
INT1	1	INT1.1	INT1.2	INT1.3	INT1.4	INT1.5	INT1.6	INT1.7	INT1.8
INT2	2	INT2.1	INT2.2	INT2.3	INT2.4	INT2.5	INT2.6	INT2.7	INT2.8
INT3	3	INT3.1	INT3.2	INT3.3	INT3.4	INT3.5	INT3.6	INT3.7	INT3.8
... etc ...									
... etc ...									
INT12	12	INT12.1	INT12.2	INT12.3	INT12.4	INT12.5	INT12.6	INT12.7	INT4.8

Table 3.1: PIE Group Hardware Priority

## 3.2 PIE Interrupt Priorities

The PIE block is organized such that the interrupts are in a logical order. Interrupts that typically require higher priority, are organized higher up in the table and will thus be serviced with a higher priority by default.

The interrupts in a control subsystem can be categorized as follows (ordered highest to lowest priority):

### 1. Non-Periodic, Fast Response

These are interrupts that can happen at any time and when they occur, they must be serviced as quickly as possible. Typically these interrupts monitor an external event.

On the F2837xD devices, such interrupts are allocated to the first few interrupts within PIE Group 1 and PIE Group 2. This position gives them the highest priority within the PIE group. In addition, Group 1 is multiplexed into the CPU interrupt INT1. CPU INT1 has the highest hardware priority. PIE Group 2 is multiplexed into the CPU INT2 which is the 2nd highest hardware priority.

### 2. Periodic, Fast Response

These interrupts occur at a known period, and when they do occur, they must be serviced as quickly as possible to minimize latency. The A/D converter is one good example of this. The A/D sample must be processed with minimum latency.

On the F2837xD devices, such interrupts are allocated to the group 1 in the PIE table. Group 1 is multiplexed into the CPU INT1. CPU INT1 has the highest hardware priority

### 3. Periodic

These interrupts occur at a known period and must be serviced before the next interrupt. Some of the PWM interrupts are an example of this. Many of the registers are shadowed, so the user has the full period to update the register values.

In the F2837xD device's PIE modules, such interrupts are mapped to group 2 - group 5. These groups are multiplexed into CPU INT3 to INT5 (the ePWM and eCAP), which are the next lowest hardware priority.

### 4. Periodic, Buffered

These interrupts occur at periodic events, but are buffered and hence the processor need

only service such interrupts when the buffers are ready to filled/emptied. All of the serial ports (SCI / SPI / I2C / CAN) either have FIFOs or multiple mailboxes such that the CPU has plenty of time to respond to the events without fear of losing data.

In the F2837xD device, such interrupts are mapped to INT6, INT8, and INT9, which are the next lowest hardware priority.

## 3.3 Software Prioritization of Interrupts

The user will probably find that the PIE interrupts are organized where they should be for most applications. However, some software prioritization may still be required for some applications.

Recall that the basic software priority scheme on the C28x works as follows:

- **Global Priority**

This priority can be managed by manipulating the CPU IER register. This register controls the 16 maskable CPU interrupts (INT1 - INT16).

- **Group Priority**

This can be managed by manipulating the PIE block interrupt enable registers (PIEIERx). There is one PIEIERx per group and each control the 8-interrupts multiplexed within that group.

The F28 software prioritization of interrupt example demonstrates how to configure the Global priority (via IER) and group priority (via PIEIERx) within an ISR in order to change the interrupt service priority based on user assigned levels. The steps required to do this are:

1. **Set the global priority**

Modify the IER register to allow CPU interrupts with a higher user priority to be serviced.

2. **Set the Group priority**

Modify the appropriate PIEIERx register to allow group interrupts with a higher user set priority to be serviced.

3. **Enable interrupts**

The software prioritized interrupts example provides a method using mask values that are configured during compile time to allow you to manage this easily.

To setup software prioritization for the example, the user must first assign the desired global priority levels and group priority levels.

This is done in the F2837xD\_common/include/F2837xD\_SWPrioritizedIsrLevels.h file as follows:

1. *User assigns global priority levels*

INT1PL - INT16PL

These values are used to assign a priority level to each of the 16 interrupts controlled by the CPU IER register. A value of 1 is the highest priority while a value of 16 is the lowest. More than one interrupt can be assigned the same priority level. In this case the default hardware priority would determine which would be serviced first. A priority of 0 is used to indicate that the interrupt is not used.

2. *User assigns PIE group priority levels*

GxyPL (where x = PIE group number 1 - 12 and y = interrupt number 1 - 8)

These values are used to assign a priority level to each of the 8 interrupts within a PIE group. A value of 1 is the highest priority while a value of 8 is the lowest. More than one interrupt can be assigned the same priority level. In this case the default hardware priority would determine which would be serviced first. A priority of 0 is used to indicate that the interrupt is not used.

Once the user has defined the global and group priority levels, the compiler will generate mask values that can be used to change the IER and PIEIERx registers within each ISR. In this manner the interrupt software prioritization will be changed. The masks that are generated at compile time are:

■ **IER mask values**

MINT1 - MINT16

The user assigned INT1PL - INT16PL values are used at compile time to calculate an IER mask for each CPU interrupt. This mask value will be used within an ISR to allow CPU interrupts with a higher priority to interrupt the current ISR and thus be serviced at a higher priority level.

■ **PIEIERxy mask values**

MGxy (where x = PIE group number 1 - 12 and y = interrupt number 1 - 8)

The assigned group priority levels (GxyPL) are used at compile time to calculate PIEIERx masks for each PIE group. This mask value will be used within an ISR to allow interrupts within the same group that have a higher assigned priority to interrupt the current ISR and thus be serviced at a higher priority level.

### 3.3.1 Using the IER/PIEIER Mask Values

Within an interrupt service routine, the global and group priority can be changed by software to allow other interrupts to be serviced. The procedure for setting an interrupt priority using the mask values created in the F28\_SWPrioritizedIsrLevels.h is the following:

1. **Set the global priority**

- Modify IER to allow CPU interrupts from the same PIE group as the current ISR.
- Modify IER to allow CPU interrupts with a higher user defined priority to be serviced.

2. **Set the group priority**

- Save the current PIEIERx value to a temporary register.
- The PIEIER register is then set to allow interrupts with a higher priority within a PIE group to be serviced.

3. **Enable interrupts**

- Enable all PIE interrupt groups by writing all 1's to the PIEACK register
- Enable global interrupts by clearing INTM

4. **Execute ISR.** Interrupts that were enabled in steps 1-3 (those with a higher software priority) will be allowed to interrupt the current ISR and thus be serviced first.

5. **Restore the PIEIERx register**

6. **Exit**

### 3.3.2 Example Code

The sample C code below shows an EV-A Comparator 1 Interrupt service routine software prioritization written in C. This interrupt is connected to PIE group 2 interrupt 1.

```
// Connected to PIEIER2_1 (use MINT2 and MG21 masks):
#if (G21PL != 0)
interrupt void EPWM1_TZINT_ISR(void)    // EPWM1 Trip Zone
{
    // Set interrupt priority:
    volatile Uint16 TempPIEIER = PieCtrlRegs.PIEIER2.all;
    IER |= M_INT2;
    IER &= MINT2;                    // Set "global" priority
    PieCtrlRegs.PIEIER2.all &= MG21; // Set "group" priority
    PieCtrlRegs.PIEACK.all = 0xFFFF; // Enable PIE interrupts
    asm(" NOP");
    EINT;

    // Insert ISR Code here.....
    // for now just insert a delay
    for(i = 1; i <= 10; i++) {}

    // Restore registers saved:
    DINT;
    PieCtrlRegs.PIEIER2.all = TempPIEIER;

    // Add ISR to Trace
    ISRTrace[ISRTraceIndex] = 0x0021;
    ISRTraceIndex++;
}
#endif

CMP1INT_ISR:
    ASP
    ADDB     SP,#1
    CLRC     OVM,PAGE0
    MOVW     DP,#0x0033
    MOV      AL,@36
    MOV      *-SP[1],AL
    OR        IER,#0x0002
    AND       IER,#0x0002
    AND       @36,#0x000E
    MOV      @33,#0xFFFF
    CLRC     INTM

    User code goes here...

    SETC     INTM
    MOV      AL,*-SP[1]
    MOV      @36,AL
    SUBB     SP,#1
```

NASP  
IRET

The interrupt latency is approx 22 cycles.

/\*!



## 4 CLA C Compiler

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### 4.1 Introduction

The goal of the CLA compiler is to implement enough of the C programming environment to make it easier to access the capabilities of the CLA architecture and integrate CLA task code and data into a C28x application.

The compiler is available as part of the codegen tools (v6.0.1 and later). All bugs, performance issues should be reported to Compiler Support at the forum [Compiler Forum](#).

### 4.2 Overview

The README.txt file included in the compiler download package contains the latest details on the CLA compiler's C language implementation and it is highly recommended that you go over this document before you begin coding.

#### 4.2.1 How to Invoke the CLA Compiler

The CLA compiler is invoked using the same command used for compiling C28x code (cl2000[.exe]).

Files that have a .cla extension will be recognized by the compiler as CLA C files. The shell will invoke separate CLA versions of the compiler passes to generate CLA-specific code. The object files generated by the compiler can then be linked with C28x objects files to create a C28x/CLA program.

Usage:

```
cl2000 -v28 -cla_support=cla0 [other options] file.cla
                                     or
cl2000 -v28 -cla_support=cla1 [other options] file.cla
```

**NOTE: THE COMPILER DOES NOT SUPPORT COMPILING BOTH CLA AND C28X C FILES IN ONE INVOCATION.**

## 4.2.2 C Language Implementation

### 4.2.2.1 Characteristics

#### Language

Supports C only. No C++ or GCC extension support.

#### Data Types

(NOTE THE DIFFERENCES FROM C28X DATA TYPES!!)

- char, short - 16 bits
- int, long - 32 bits ('long long' data type is not supported)
- float, double, long double - 32 bits
- pointers - 16 bits

IMPORTANT NOTES:
The CLA and C28x CPU have different type sizes. <ul style="list-style-type: none"><li>• When declaring data that will be shared by both C28x and CLA use type declarations that will result in objects of the same size</li><li>• To avoid ambiguity use typedefs for basic types that include size information (eg. int32, uint16, etc)</li></ul>
The CLA architecture is oriented for 32-bit data types. <ul style="list-style-type: none"><li>• 16-bit data types incur sign extension overhead and should primarily be used for load/store operations such as reading/writing 16-bit peripherals.</li></ul>
Pointers are <b>INTERPRETED</b> differently <ul style="list-style-type: none"><li>• Pointers on the C28 are 22-bits wide and require at minimum 2 contiguous 16-bit locations for storage. As such they are treated as 32-bit data types(since we cannot allocate 22 bit memory locations)</li><li>• The CLA treats pointers as 16-bit data types. Any pointer shared between the C28 and CLA will be interpreted as a 16-bit location by the CLA compiler and this could cause undesired or bad data accesses by the CLA.</li></ul>
<b>NOTE: THE CLA COMPILER DOES NOT PROVIDE 64-BIT DATA TYPE SUPPORT. THE CLA_TYPEDEFS HEADER FILE DOES HOWEVER DEFINE A 64 BIT INTEGER AS THE UNION OF TWO 32-BIT INTEGERS; THIS WAS DONE IN ORDER TO PREVENT ERRORS IN THE COMPILATION PROCESS OF OTHER PERIPHERAL HEADERS THAT USE 64-BIT TYPES, E.G. USB</b>

#### Pragmas

The compiler accepts C28x pragmas except for the FAST\_FUNC\_CALL

## C Standard Library

In general, the C standard library is not supported. `abs()` and `fabs()` are supported as intrinsics. An inline fast floating-point divide is supported.

## Keywords

The keywords `'__register'`, `'far'`, and `'ioport'` are not recognized

## Intrinsics

The following intrinsics are supported:

- `float __meisqrtf32(float)`
- `float __meinvf32(float)`
- `float __mminf32(float, float)`
- `float __mmaxf32(float, float)`
- `void __mswapf(float, float)`
- `short __mf32toi16r(float)`
- `unsigned short __mf32toui16r(float)`
- `float __mfracf32(float)`
- `__mdebugstop()`
- `__meallow()`
- `__medis()`
- `__msetflg(unsigned short, unsigned short)`
- `__mnop()`

## 4.2.3 Language Restrictions

### Global Initialization

Defining and initializing global data is not supported.

Since the CLA code is executed in an interrupt driven environment there is no C system boot sequence. As a result, definitions of the form 'int global\_var = 5;' are not allowed for variables that are defined globally (outside the scope of a function). Initialization of global data must either be done by the C28x driver code or within a function.

Variables defined as 'const' can be initialized globally. The compiler will create initialized data sections named **.const\_cla** to hold these variables. The same restriction applies to variables declared as 'static'. Even if the variable is defined within a function.

### Stack

Local variables and compiler temps are placed into a scratchpad memory area. On older CGT (before 6.4.0) these variables were accessed directly using the symbols '**\_\_cla\_scratchpad\_start**' and '**\_\_cla\_scratchpad\_end**' and it was expected that the user would manage this area and define these symbols using a linker command file. In CGT 6.4.0 (and above) these variables are placed in a ".scratchpad" memory section, which the compiler will then partition into local frames, one for the all eight tasks, and one for each leaf function. These local frames will have unique symbols that the compiler will use to access variables.

#### IMPORTANT NOTES:

Local variables and compiler temps are expected to be placed into a scratchpad memory area and accessed directly using the symbols '**\_\_cla\_scratchpad\_start**' and '**\_\_cla\_scratchpad\_end**' (for CGT 6.2.x and older), while they are placed in ".scratchpad" for CGT 6.4.0 (and above) and the compiler access them relative to the local frame symbol

- For the legacy memory convention (CGT 6.2.x and older) the user is expected to manage the size of the area and define start/end symbols using a linker command file. For the newer convention (CGT 6.4.0+), this is handled by the compiler
- This scratchpad serves as a CLA stack.

To allow debug of local variables, the linker .cmd file has been updated from that originally distributed

- Please ensure the changes to the .cmd file shown below are made before proceeding.
- The linker file should look like the code shown below.
- This also required a compiler released after July 21, 2011.

## Linker Command File (CGT 6.2.x and older)

The following is an example of what needs to be added to a linker command file to define the CLA compiler scratchpad memory (legacy convention):

- Define the scratchpad size - **CLA\_SCRATCHPAD\_SIZE** is a linker defined symbol that can be added to the application's linker command file to designate the size of the scratchpad memory.
- A SECTION's directive can reference this symbol to allocate the scratchpad area. This directive reserves a 0x100 word memory hole to be used as the compiler scratchpad area.
- The scratchpad area is named **CLAscratch** and is allotted to CLA Data RAM 1 (CLARAM1)
- The value of CLA\_SCRATCHPAD\_SIZE can be changed based on the application.

```
// Define a size for the CLA scratchpad area that will be used
// by the CLA compiler for local symbols and temps
// Also force references to the special symbols that mark the
// scratchpad area.

// If using --define CLA_SCRATCHPAD_SIZE=0x100, remove next line
CLA_SCRATCHPAD_SIZE = 0x100;
--undef_sym=__cla_scratchpad_end
--undef_sym=__cla_scratchpad_start

.....
MEMORY
{
    .....
}
SECTIONS
{
    //
    // Must be allocated to memory the CLA has write access to
    //
    CLAscratch :
    { *.obj(CLAscratch)
      . += CLA_SCRATCHPAD_SIZE;
      *.obj(CLAscratch_end) } > CLARAM1, PAGE = 1
    }
```

The scratchpad size can alternatively be defined and altered in the linker options of a project as shown below

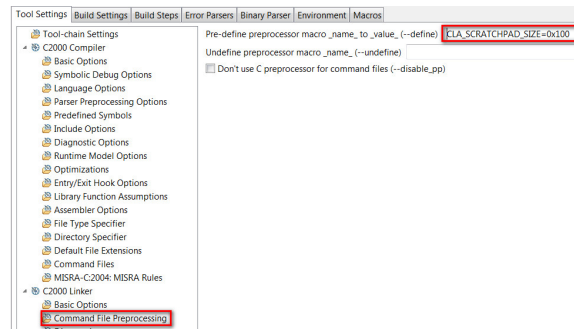


Figure 4.1: Adjusting scratchpad size through the linker options

## Linker Command File (CGT 6.4.0 and newer)

The following is an example of the linker command file with the new memory convention (CGT 6.4.0+):

- The old convention for CLAScratch will still be supported by the new compiler, albeit, inefficiently from a memory allocation standpoint.
- The new compiler creates a common local frame for the 8 tasks, i.e. each task's local frame is overlayed on top of each other - they use the same memory locations; this is possible since there is no nesting of tasks, so one task cannot corrupt the scratch area of another.
- By having the CLAScratch memory section, the compiler cannot take advantage of the overlaying strategy and is, instead, forced to allocate each task's locals in separate locations within the scratchpad.

```

.....
MEMORY
{
.....
}
SECTIONS
{
    //
    // Must be allocated to memory the CLA has write access to
    //
    .scratchpad : > CLARAM1, PAGE = 1
}

```

## Function Nesting

Only 2 levels of call stack depth is supported. See Section [4.2.5](#) for details on the calling conventions.

## Recursion

Recursive function calls are not supported.

## Function Pointers

Function pointers are not supported.

## Other Operations

The following operations are currently not supported due to lack of instruction set support making them expensive to implement. It is not clear that these operations are critical for typical CLA algorithms.

- Integer divide, modulus
- Integer unsigned compares

## 4.2.4 Memory Model - Sections

### CLA Program

The CLA compiler will place CLA code into section “**Cla1Prog**” as per the current convention used for CLA assembly.

### Global Data

Uninitialized global data will be placed in the section “**.bss\_cla**”

### Constants

Initialized constant data will be placed in section “**.const\_cla**”

### Heap

There is no support for operations such as malloc(). Therefore there is no C system heap for CLA.

## 4.2.5 Function Structure and Calling Conventions (CGT 6.2.x and older)

### Function Nesting

The compiler supports 2 level of function calls. Functions declared as interrupts may call leaf functions only. Leaf function may not call other functions. Functions not declared as interrupt

will be considered leaf functions. **NOTE: THE CLA TASKS ARE PREFIXED WITH THE KEYWORD '`__interrupt`' TO SET THEM APART FROM LEAF FUNCTIONS. THEY ARE NOT TO BE CONFUSED WITH C28X INTERRUPT SERVICE ROUTINES**

## Register Calling Convention

The CLA compiler supports calling functions with up to 2 arguments.

- Pointer arguments are passed in MAR0/MAR1.
- Integer/float arguments are passed in MR0,MR1.
- Integer and float return values from functions are passed in MR0.
- Pointer or return by reference value from functions are passed in MAR0.

## Register Save/Restore

All registers except for MR3 are saved on call. MR3 is saved on entry. **NOTE: IF YOU ARE WRITING AN ASM ROUTINE TO BE CALLED IN THE C CONTEXT IT IS YOUR RESPONSIBILITY TO SAVE/RESTORE MR3 UPON ENTRY AND EXIT RESPECTIVELY**

## Local Variables

A static scratchpad area is used as a stack for locals and compiler temporary variables. **NOTE:THE USER IS RESPONSIBLE FOR ENSURING THE SCRATCHPAD AREA IS ALLOCATED INTO THE MEMORY MAP AND IS LARGE ENOUGH. THIS IS DONE USING THE EITHER THE LINKER COMMAND FILE OR THROUGH THE PROJECT'S LINKER OPTIONS (SEE ABOVE).**

## Mixing CLA C and Assembly

When interfacing with CLA assembly language modules use the calling conventions defined above to interface with compiled CLA code.

## 4.2.6 Function Structure and Calling Conventions (CGT 6.4.0 and newer)

### Function Nesting

The compiler supports an infinite call depth subject to memory constraints. **NOTE: THE CLA TASKS ARE PREFIXED WITH THE KEYWORD '`__interrupt`' TO SET THEM APART FROM LEAF FUNCTIONS. THEY ARE NOT TO BE CONFUSED WITH C28X INTERRUPT SERVICE ROUTINES**

### Register Calling Convention

The CLA compiler supports calling functions with up to 2 arguments.

- Pointer arguments are passed in MAR0/MAR1.



- Integer/float arguments are passed in MR0,MR1, MR2.
- Additional arguments are passed on the scratchpad
- Integer and float return values from functions are passed in MR0.
- Pointer or return by reference value from functions are passed in MAR0.

## Register Save/Restore

All registers except for MR3 are saved on call. MR3 is saved on entry. **NOTE: IF YOU ARE WRITING AN ASM ROUTINE TO BE CALLED IN THE C CONTEXT IT IS YOUR RESPONSIBILITY TO SAVE/RESTORE MR3 UPON ENTRY AND EXIT RESPECTIVELY**

## Local Variables

A scratchpad area is used as a stack for locals, compiler temporary variables and passed arguments. A call graph is computed in the linker to determine which function frames can be overlayed in placement to save memory - these are usually the tasks since they can't be nested. All generated function frames are part of the .scratchpad section and are named in the form ".scratchpad:[function section name]". For example:

- `.scratchpad:Cl1Prog:_Cl1Task2`
- `.scratchpad:Cl1Prog:_Cl1Func1`

Therefore, the only section that needs to be placed in the linker command file is the .scratchpad section. All function frames that are part of that section will be placed automatically within the .scratchpad placement. It is not necessary to specify a size for the .scratchpad section. Additionally, CLA object files compiled with previous tool versions will be fully compatible with newly generated object files as long as the user supports both scratchpad naming conventions in the linker command file. However, the scratchpad section used for old object files cannot be overlayed with the new .scratchpad section and the user must ensure enough memory is available for both.

## Mixing CLA C and Assembly

When interfacing with CLA assembly language modules use the calling conventions defined above to interface with compiled CLA code.

## 4.3 Framework

The CLA examples are in the folder "*F2837xD\_examples\_Cpu1*". Each CLA example within this folder share a similar structure as shown in the figure below (Fig. 4.2)

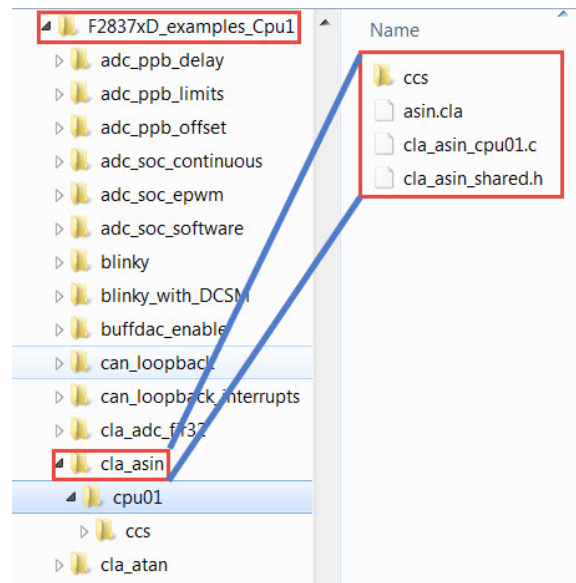


Figure 4.2: Structure of a CLA example

For any given *example* there are 3 specific files associated with it as described in Table. 4.1.

Source File	Description
<example>_cpu01.c	implements the main() routine which runs the tests; this often involves triggering a CLA task once or several times, running an algorithm within that task, returning and storing the result of that algorithm and then finally checking against a reference output. The main() also performs the system, peripheral, and CLA initialization. Variables declared in <example>_shared.h are defined here and allocated to memory (using #pragma DATA_SECTION). <b>NOTE: CLA VARIABLES MUST BE ALLOCATED TO A MEMORY SPACE THAT THE CLA HAS ACCESS TO, NAMELY THE CLA&lt;-&gt;CPU MESSAGE RAMS OR THE CLA DATA RAMS.</b>
<example>.cla	The C implementation of all the CLA tasks. File level data global to the CLA only(not shared with the C28x) should also be defined in this file.
<example>_shared.h	External declarations for the global data defined in the C28x code and referenced by the CLA task code.

Table 4.1: Example specific files

## 4.4 Getting Started with the CLA Compiler

The C code for the CLA is saved to a file with the .cla extension. If running an older version of CCSv5 (v5.2 or older) that does not recognize the extension, you can follow these steps:

**NOTE: FOR EACH NEW WORKSPACE THE USER MUST CONFIGURE CCS IN THE MANNER DESCRIBED BELOW**

1. Go to Windows->Preferences->C/C++->File Types.
2. Select "New"
3. Type in \*.cla in the top text box
4. In the drop down menu select C source file(see Fig. 4.3).
5. Select "ok"

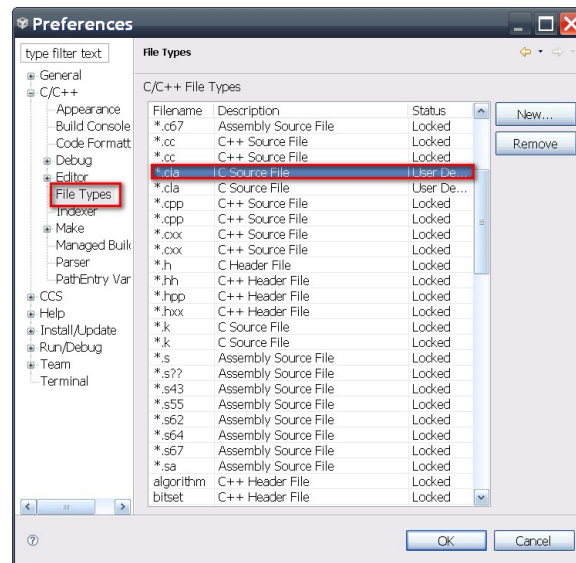


Figure 4.3: Configuring CCS5 to recognize the .cla extension

The IDE will now recognize the .cla extension as code to be compiled.

#### 4.4.1 Creating Your Own Project

The simplest way to start writing code is to copy over an existing project (from the examples folder) and to edit it. Lets take an example: I would like to create a new project, **exp2**, from an existing project, **atan**.

1. Copy a Project:
  - Make a copy of the **atan** folder in the example directory and rename it to **exp2**
2. Rename Files:
  - Rename all files `atan*.*` to `exp2*.*`. (Notice the naming convention. All files have the test folder name as a prefix, see Fig. 4.4 below)

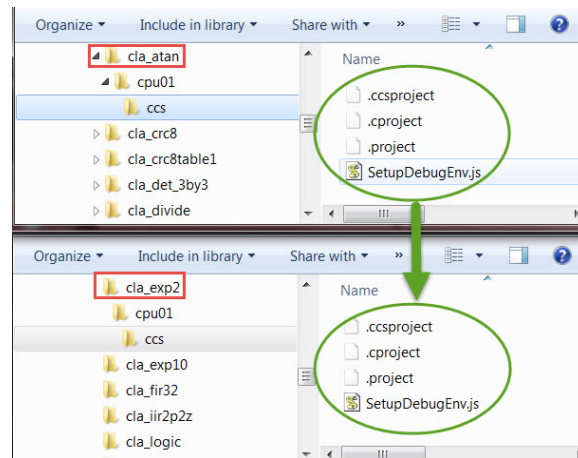


Figure 4.4: Creating a new project from existing examples

3. Edit the Project Files:

- Open the .cproject and .project files in any text editor and replace all instances of the word atan with exp2.
- This will ensure all the object files come out with the correct name and any directory dependencies are taken care of.
- If the project uses a predefined symbol, TEST\_NAME=<test\_name>. For e.g. the atan project might have a predefined symbol, TEST\_NAME=atan. By altering the .cproject files in the manner described you wont have to change the build settings for each new project .
- If the project does not use predefined symbols, go into the .c file and include the correct shared header file. For e.g. in our example, change *cla\_atan\_shared.h* to *cla\_exp2\_shared.h*

4. Import the Project:

- Import the exp2 project into your workspace (see Fig. 4.5).
- The files highlighted in the red box are common to all the CLA examples and are linked in by the .project file. The rest of the source files are specific to each test case

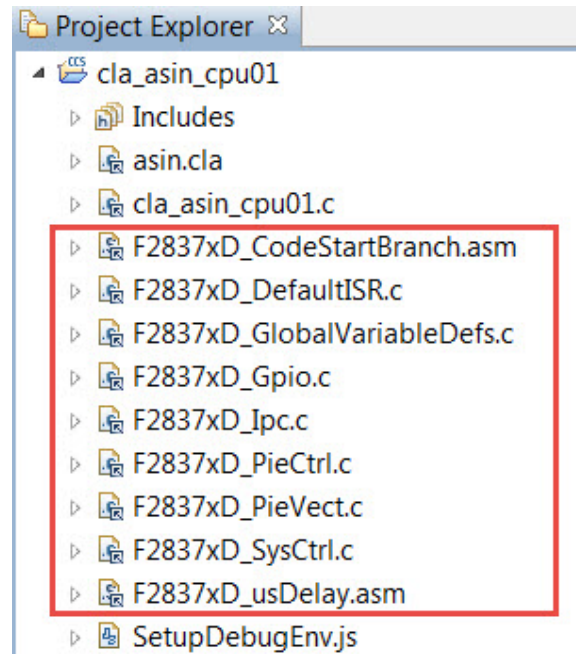


Figure 4.5: Common source files for each CLA example

5. Modify the Source:

- Edit the test specific source files.

## 4.4.2 Suggested Build Options

The following table lists build options that are useful for CLA C code. You can setup build properties that apply only to \*.cla file by right clicking the file and selecting Properties->C/C++ Build.

Option	Notes
<i>Debugging Model-&gt;Full Symoblic debug (-g)</i>	If you would like to access watch variables etc while debugging(default setting).
<i>Debugging Model-&gt;Suppress symbolic debug information</i>	View compiler generated assembly code without all the debug information.
<i>Optimization-&gt;Optimization Level = none - O2</i>	<b>DUE TO THE SMALL NUMBER OF REGISTERS AVAILABLE LESS AGGRESSIVE OPTIMIZATION MAY YIELD BETTER RESULTS (EG. -O1 vs -O2).</b>
<i>Assembler Options -&gt; Keep generated assembly files (-k)</i>	Useful if you want to compare compiler generated code with hand coded assembly.

Table 4.2: Suggested Build Options

## 4.5 Debugging

The user can follow these steps to start debugging their code on the CLA (The project *exp2* is used as an example here)

1. Add `__mdebugstop()`
  - Place an `__mdebugstop()` at the beginning of the CLA task you wish to debug. For example, task 1 of *exp2.cla*.
2. Set build options:
  - You can setup individual build properties for the \*.cla file seperately from the rest of the application.
  - Right click the .cla file and select **Properties->C/C++ Build**.
3. Connect to the CLA:
  - Once you have built your project and launched the debug session CCS, by default, will connect to only the C28 core.
  - To be able to debug CLA code you will need to connect to the CLA core. The action of connecting to the CLA core enables all software breakpoints and single-stepping abilities.
  - **IF YOU WISH TO STEP THROUGH C CODE BUILD THE PROJECT WITH -G (FULL SYMBOLIC DEBUG) TO GENERATE THE SYMBOLS THAT WILL BE LOADED TO THE DEBUGGER.**
    - (a) Click on the CLA debug session (highlighted in Fig. 4.6)
    - (b) Select *Target->Connect to Target* or hit Alt-C.
    - (c) Once the CLA core is connected proceed to load the project symbols by clicking on *Target->Load Symbols-><example>.out* (e.g. *exp2.out*).

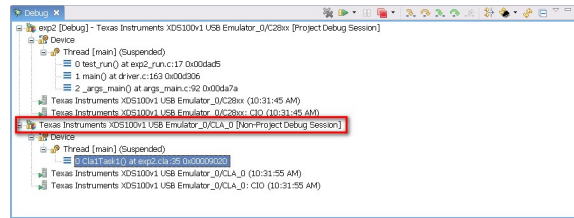


Figure 4.6: CLA Debug Session

#### 4. Run the C28x:

- In the exp2 example we have enabled task 1 of the CLA and we trigger it in software on the C28 side. When we run the code on the C28 debug session it seems to stall at the Cla1ForceTask1andWait() routine. It is waiting for the CLA task 1 to run to completion. When we switch over to the CLA session we see that execution has stopped at the \_\_mdebustop() intrinsic

#### 5. Debug the Code:

- At this point we can proceed to single step through the code or continue till completion.
- There are some restrictions to debugging the CLA and they are discussed next.

## 4.6 Known Debugging Issues

1. The CLA pipeline is not flushed on a single step and so results may not be visible until a few instructions later. Please refer to the CLA user guide or the device *Technical Reference Manual* for more details about the pipeline.  
**UNLIKE THE C28, SINGLE-STEPPING ON THE CLA DOES NOT FLUSH THE PIPELINE AND EXECUTE AN INSTRUCTION , IT MERELY MOVES THE PIPELINE FORWARD BY ONE STAGE)**
2. If you plan to debug (single step) code on the CLA it is necessary that MNOPs are placed prior to any MSTOP to ensure the instructions prior to the MSTOP proceed through the pipeline before the MSTOP executes. The compiler will insert these MNOPs if compiling with debug (-g). The MNOPs are unnecessary if you are not debugging the CLA code.
3. **YOU WILL NOT BE ABLE TO EXECUTE THE "RUN TO LINE" OR "STEP OVER" COMMANDS ON THE CLA. BE SURE TO PLACE \_\_MDEBUGSTOP() INTRINSICS AROUND FUNCTIONS YOU WISH TO STEP OVER AND HAVE THE CORE RUN TO THESE BREAKPOINTS DIRECTLY**

## 4.7 Tips and Tricks

### 4.7.1 Dealing with Pointers

Pointers are interpreted differently on the C28x and the CLA. The C28 treats them as 32-bit data types(address size is 22-bits) while the CLA can only use an address size of 16 bits. Assume the following structure is declared in a shared header file(i.e. common to the C28 and CLA) and defined and allocated to a memory section in a .c file

```
/*****
```

```
Shared Header File
*****/
typedef struct{
    float a;
    float *b;
    float *c;
}foo;

/*****
main.c
*****/
#pragma(X, "CpuToCla1MsgRam") //Assign X to section CpuToCla1MsgRam
foo X;

/*****
test.cla
*****/
__interrupt void Cla1Task1 ( void )
{
    float f1,f2;
    f1 = *(X.b);
    f2 = *(X.c); //Pointer incorrectly dereferenced
                  //Tries to access location 0x1503 instead
                  //of 0x1504
}
```

Assume that the C28 compiler will allocate space for X at the top of the section **CpuToCla1MsgRam** as follows:

Element	Address
X.a	0x1500
X.b	0x1502
X.c	0x1504

The CLA compiler will interpret this structure differently

Element	Address
X.a	0x1500
X.b	0x1502
<b>X.c</b>	<b>0x1503</b>

The CLA compiler treats pointers **b** and **c** as 16-bits wide and therefore incorrectly dereferences pointer **c**.

The solution to this is to declare a new pointer as follows:

```
*****
Shared Header File
*****/
typedef union{
    float *ptr; //Aligned to lower 16-bits
    Uint32 pad; //32-bits
```



```

}CLA_FPTR;

typedef struct{
    float a;
    CLA_FPTR b;
    CLA_FPTR c;
}foo;

/*****
main.c
*****/
#pragma(X, "CpuToClalMsgRam") //Assign X to section CpuToClalMsgRam
foo X;

/*****
test.cla
*****/
__interrupt void ClalTask1 ( void )
{
    float f1,f2;
    f1 = *(X.b.ptr);
    f2 = *(X.c.ptr); //Correct Access
}

```

The new pointer **CLA\_FPTR** is a union of a 32-bit integer and a pointer to a float. The CLA compiler recognizes the size of the larger of the two elements(the 32 bit integer) and therefore aligns the pointer to the lower 16-bits. Now both the pointers **b** and **c** will occupy 32-bit memory spaces and any instruction that tries to dereference pointer **c** will access the correct address 0x1504.

## 4.7.2 Benchmarking

The CLA does not support the clock function and therefore it is not possible to get a direct cycle count of a particular task. The user can configure the time base module on an ePWM to keep track of the execution time of a task

Setup the time base of ePWM1(or any ePWM) to run at SYSCLKOUT in the up-count mode as shown below:

```

void InitEPwm(void)
{
    // Setup TBCLK
    EPwm1Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP; // Count up
    EPwm1Regs.TBPRD = 0xFFFF; // Set timer period
    EPwm1Regs.TBCTL.bit.PHSEN = TB_DISABLE; // Disable phase loading
    EPwm1Regs.TBPHS.half.TBPHS = 0x0000; // Phase is 0
    EPwm1Regs.TBCTR = 0x0000; // Clear counter
    EPwm1Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1; // Clock ratio to SYSCLKOUT
    EPwm1Regs.TBCTL.bit.CLKDIV = TB_DIV1;
}

```

Proceed to define two macros **READ\_CLOCK** and **RESTART\_CLOCK**, the former to freeze the ePWM timer and copy the elapsed time to a variable, and the latter to restart the ePWM timer.

```
#define READ_CLOCK(X) __meallow();\
    EPwm1Regs.TBCTL.bit.CTRMODE = TB_FREEZE;\
    X = EPwm1Regs.TBCTR;\
    __medis();\
#define RESTART_CLOCK __meallow();\
    EPwm1Regs.TBCTL.bit.CTRMODE = TB_FREEZE;\
    EPwm1Regs.TBCTR = 0;\
    EPwm1Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP;\
    __medis();
```

Define a variable e.g. **ulCycleCount** to hold the cycle count

```
#pragma DATA_SECTION(ulCycleCount, "ClalToCpuMsgRAM");
unsigned long ulCycleCount;
```

Place the macro **RESTART\_CLOCK** at the beginning of a task to restart the ePWM timer and place **READ\_CLOCK** at the end of the task to read the value of the timer. The elapsed time will be give you the cycle count plus a minimal overhead from the two macros

```
__interrupt void ClalTask1 ( void )
{
    //Local Variables
    float a;

    __mdebugstop();
    RESTART_CLOCK;
    a = 10;
    ...
    ...
    ...
    READ_CLOCK(ulCycleCount);
}
```

## 5 CPU 1 Example Applications

These example applications show how to make use of various peripherals of a F2837xD device. These applications are intended for demonstration and as a starting point for new applications.

All these examples contain two build configurations which allow you to build each project to run from either RAM or Flash. To change how the project is built simply right click on the project and select "Build Configurations". Then, move over to set the active build configuration, either RAM or Flash.

Because CPU 1 is ultimately in control of the entire F2837xD device and these applications contain no CPU 2 dependencies, these examples may be run completely on their own without any associated CPU2 program. The only exception to this in the CPU1 examples is the `setup_cpu1` example. This example sets up all of the peripherals and GPIOs to be owned by CPU2. In addition, this example also has a special standalone flash build configuration which will send an IPC command to boot the second CPU and run the application in its flash memory.

All of these examples reside in the `device_support/F2837xD/<Version>/F2837xD_examples_Cpu1` subdirectory of the ControlSUITE package.

### 5.1 ADC PPB Delay Capture (`adc_ppb_delay`)

This example demonstrates delay capture using the post-processing block.

Two asynchronous ADC triggers are setup:

- ePWM1, with period 2048, triggering SOC0 to convert on pin A0
- ePWM1, with period 9999, triggering SOC1 to convert on pin A1

Each conversion generates an ISR at the end of the conversion. In the ISR for SOC0, a conversion counter is incremented and the PPB is checked to determine if the sample was delayed.

After the program runs, the memory will contain:

- **conversion** : the sequence of conversions using SOC0 that were delayed
- **delay** : the corresponding delay of each of the delayed conversions

### 5.2 ADC PPB Limits (`adc_ppb_limits`)

This example sets up the ePWM to periodically trigger the ADC. If the results are outside of the defined range, the post-processing block will generate an interrupt.

The default limits are 1000LSBs and 3000LSBs. With VREFHI set to 3.3V, the PPB will generate an interrupt if the input voltage goes above about 2.4V or below about 0.8V.

## 5.3 ADC PPB Offset (adc\_ppb\_offset)

This example software triggers the ADC. Some SOC's have automatic offset adjustment applied by the post-processing block.

After the program runs, the memory will contain:

- **AdcaResult** : a digital representation of the voltage on pin A0
- **AdcaResult\_offsetAdjusted** : a digital representation of the voltage on pin A0, plus 100 LSBs of automatically added offset
- **AdcbResult** : a digital representation of the voltage on pin B0
- **AdcbResult\_offsetAdjusted** : a digital representation of the voltage on pin B0 minus 100 LSBs of automatically added offset

## 5.4 ADC Continuous Triggering (adc\_soc\_continuous)

This example sets up the ADC to convert continuously, achieving maximum sampling rate.

After the program runs, the memory will contain:

- **AdcaResults** : A sequence of analog-to-digital conversion samples from pin A0. The time between samples is the minimum possible based on the ADC speed.

## 5.5 ADC ePWM Triggering (adc\_soc\_epwm)

This example sets up the ePWM to periodically trigger the ADC.

After the program runs, the memory will contain:

- **AdcaResults** : A sequence of analog-to-digital conversion samples from pin A0. The time between samples is determined based on the period of the ePWM timer.

## 5.6 ADC temperature sensor conversion (adc\_soc\_epwm\_tempsensor)

This example sets up the ePWM to periodically trigger the ADC. The ADC converts the internal connection to the temperature sensor, which is then interpreted as a temperature by calling the GetTemperatureC function.

After the program runs, the memory will contain:

- **sensorSample** : The raw reading from the temperature sensor.
- **sensorTemp** : The interpretation of the sensor sample as a temperature in degrees Celsius.

## 5.7 ADC SOC Software Force (adc\_soc\_software)

This example converts some voltages on ADCA and ADCB based on a software trigger.

After the program runs, the memory will contain:

- **AdcaResult0** : a digital representation of the voltage on pin A0
- **AdcaResult1** : a digital representation of the voltage on pin A1
- **AdcbResult0** : a digital representation of the voltage on pin B0
- **AdcbResult1** : a digital representation of the voltage on pin B1

Note: The software triggers for the two ADCs happen sequentially, so the two ADCs will run asynchronously.

## 5.8 ADC Synchronous SOC Software Force (adc\_soc\_software\_sync)

This example converts some voltages on ADCA and ADCB using input 5 of the input X-BAR as a software force. Input 5 is triggered by toggling GPIO0, but any spare GPIO could be used. This method will ensure that both ADCs start converting at exactly the same time.

After the program runs, the memory will contain:

- **AdcaResult0** : a digital representation of the voltage on pin A0
- **AdcaResult1** : a digital representation of the voltage on pin A1
- **AdcbResult0** : a digital representation of the voltage on pin B0
- **AdcbResult1** : a digital representation of the voltage on pin B1

## 5.9 Blinky

This example blinks LED X

## 5.10 Blinky with DCSM

This example blinks LED X

## 5.11 Buffered DAC Enable (buffdac\_enable)

This example generates a voltage on the buffered DAC output, DACOUTA/ADCINA0 (HSEC Pin 9) and uses the default DAC reference setting of VDAC.

When the DAC reference is set to VDAC, an external reference voltage must be applied to the VDAC pin. This can be accomplished by connecting a jumper wire from 3.3V to ADCINB0 (HSEC pin 12).

## 5.12 Buffered DAC Ramp (buffdac\_ramp)

This example generates a ramp wave on the buffered DAC output, DACOUTA/ADCINA0 (HSEC Pin 9) and uses the default DAC reference setting of VDAC.

When the DAC reference is set to VDAC, an external reference voltage must be applied to the VDAC pin. This can be accomplished by connecting a jumper wire from 3.3V to ADCINB0 (HSEC pin 12).

Run the included .js file to add the watch variables. This example uses the SGEN module. Documentation for the SGEN module can be found in controlSUITE/libs/dsp/SGEN/101/doc

The generated waveform can be adjusted with the following variables while running:

- **waveformGain** : Adjust the magnitude of the waveform. Range is from 0.0 to 1.0. The default value of 0.8003 centers the waveform within the linear range of the DAC
- **waveformOffset** : Adjust the offset of the waveform. Range is from -1.0 to 1.0. The default value of 0 centers the waveform
- **outputFreq\_hz** : Adjust the output frequency of the waveform. Range is from -maxOutputFreq\_hz to maxOutputFreq\_hz
- **maxOutputFreq\_hz** : Adjust the max output frequency of the waveform. Range - See SGEN module documentation for how this affects other parameters

The generated waveform can be adjusted with the following variables/macros but require recompile:

- **samplingFreq\_hz** : Adjust the rate at which the DAC is updated. Range - See SGEN module documentation for how this affects other parameters
- **REFERENCE** : The reference for the DAC. Range - REFERENCE\_VDAC, REFERENCE\_VREF
- **CPUFREQ\_MHZ** : The cpu frequency. This does not set the cpu frequency. Range - See device data manual
- **DAC\_NUM** : The DAC to use. Range - DACA, DACB, DACC

The following variables give additional information about the generated waveform: See SGEN module documentation for details

- **freqResolution\_hz**
- **maxOutput\_lsb** : Maximum value written to the DAC.
- **minOutput\_lsb** : Minimum value written to the DAC.
- **pk\_to\_pk\_lsb** : Magnitude of generated waveform.
- **cpuPeriod\_us** : Period of cpu.
- **samplingPeriod\_us** : The rate at which the DAC is updated. Note that samplingPeriod\_us has to be greater than the DAC settling time.
- **interruptCycles** : Interrupt duration in cycles.
- **interruptDuration\_us** : Interrupt duration in uS.

- **sgen** : The SGEN module instance.
- **DataLog** : Circular log of writes to the DAC.

## 5.13 Buffered DAC Random (buffdac\_random)

This example generates random voltages on the buffered DAC output, DACOUTA/ADCINA0 (HSEC Pin 9) and uses the default DAC reference setting of VDAC.

When the DAC reference is set to VDAC, an external reference voltage must be applied to the VDAC pin. This can be accomplished by connecting a jumper wire from 3.3V to ADCINB0 (HSEC pin 12).

## 5.14 Buffered DAC Sine (buffdac\_sine)

This example generates a sine wave on the buffered DAC output, DACOUTA/ADCINA0 (HSEC Pin 9) and uses the default DAC reference setting of VDAC.

When the DAC reference is set to VDAC, an external reference voltage must be applied to the VDAC pin. This can be accomplished by connecting a jumper wire from 3.3V to ADCINB0 (HSEC pin 12).

Run the included .js file to add the watch variables. This example uses the SGEN module. Documentation for the SGEN module can be found in controlSUITE/libs/dsp/SGEN/101/doc

The generated waveform can be adjusted with the following variables while running:

- **waveformGain** : Adjust the magnitude of the waveform. Range is from 0.0 to 1.0. The default value of 0.8003 centers the waveform within the linear range of the DAC
- **waveformOffset** : Adjust the offset of the waveform. Range is from -1.0 to 1.0. The default value of 0 centers the waveform
- **outputFreq\_hz** : Adjust the output frequency of the waveform. Range is from 0 to maxOutputFreq\_hz
- **maxOutputFreq\_hz** : Adjust the max output frequency of the waveform. Range - See SGEN module documentation for how this affects other parameters

The generated waveform can be adjusted with the following variables/macros but require recompile:

- **samplingFreq\_hz** : Adjust the rate at which the DAC is updated. Range - See SGEN module documentation for how this affects other parameters
- **SINEWAVE\_TYPE** : The type of sine generated. Range - LOW\_THD\_SINE, HIGH\_PRECISION\_SINE
- **REFERENCE** : The reference for the DAC. Range - REFERENCE\_VDAC, REFERENCE\_VREF
- **CPUFREQ\_MHZ** : The cpu frequency. This does not set the cpu frequency. Range - See device data manual
- **DAC\_NUM** : The DAC to use. Range - DACA, DACB, DACC

The following variables give additional information about the generated waveform: See SGEN module documentation for details

- **freqResolution\_hz**
- **maxOutput\_Isb** : Maximum value written to the DAC.
- **minOutput\_Isb** : Minimum value written to the DAC.
- **pk\_to\_pk\_Isb** : Magnitude of generated waveform.
- **cpuPeriod\_us** : Period of cpu.
- **samplingPeriod\_us** : The rate at which the DAC is updated. Note that samplingPeriod\_us has to be greater than the DAC settling time.
- **interruptCycles** : Interrupt duration in cycles.
- **interruptDuration\_us** : Interrupt duration in uS.
- **sgen** : The SGEN module instance.
- **DataLog** : Circular log of writes to the DAC.

## 5.15 Buffered DAC Square (buffdac\_square)

This example generates a square wave on the buffered DAC output, DACOUTA/ADCINA0 (HSEC Pin 9) and uses the default DAC reference setting of VDAC.

When the DAC reference is set to VDAC, an external reference voltage must be applied to the VDAC pin. This can be accomplished by connecting a jumper wire from 3.3V to ADCINB0 (HSEC pin 12).

Run the included .js file to add the watch variables. This example uses the SGEN module. Documentation for the SGEN module can be found in controlSUITE/libs/dsp/SGEN/101/doc

The generated waveform can be adjusted with the following variables while running:

- **waveformGain** : Adjust the magnitude of the waveform. Range is from 0.0 to 1.0. The default value of 0.8003 centers the waveform within the linear range of the DAC
- **waveformOffset** : Adjust the offset of the waveform. Range is from -1.0 to 1.0. The default value of 0 centers the waveform
- **outputFreq\_hz** : Adjust the output frequency of the waveform. Range is from 0 to maxOutputFreq\_hz
- **maxOutputFreq\_hz** : Adjust the max output frequency of the waveform. Range - See SGEN module documentation for how this affects other parameters

The generated waveform can be adjusted with the following variables/macros but require recompile:

- **samplingFreq\_hz** : Adjust the rate at which the DAC is updated. Range - See SGEN module documentation for how this affects other parameters
- **REFERENCE** : The reference for the DAC. Range - REFERENCE\_VDAC, REFERENCE\_VREF
- **CPUFREQ\_MHZ** : The cpu frequency. This does not set the cpu frequency. Range - See device data manual
- **DAC\_NUM** : The DAC to use. Range - DACA, DACB, DACC

The following variables give additional information about the generated waveform: See SGEN module documentation for details



- **freqResolution\_hz**
- **maxOutput\_Isb** : Maximum value written to the DAC.
- **minOutput\_Isb** : Minimum value written to the DAC.
- **pk\_to\_pk\_Isb** : Magnitude of generated waveform.
- **cpuPeriod\_us** : Period of cpu.
- **samplingPeriod\_us** : The rate at which the DAC is updated. Note that samplingPeriod\_us has to be greater than the DAC settling time.
- **interruptCycles** : Interrupt duration in cycles.
- **interruptDuration\_us** : Interrupt duration in uS.
- **sgen** : The SGEN module instance.
- **DataLog** : Circular log of writes to the DAC.

## 5.16 CAN-A to CAN-B External Transmit (can\_external\_transmit)

This example initializes CAN module A and CAN module B for external communication. CAN-A module is setup to transmit incrementing data for "n" number of times to the CAN-B module, where "n" is the value of TXCOUNT. CAN-B module is setup to trigger an interrupt service routine (ISR) when data is received. An error flag will be set if the transmitted data doesn't match the received data.

### Note:

Both CAN modules on the device need to be connected to each other via CAN transceivers.

### External Connections

- CANA is on GPIO31 (CANTXA) and GPIO30 (CANRXA)
- CANB is on GPIO8 (CANTXB) and GPIO10 (CANRXB)

### Watch Variables

- TXCOUNT - Adjust to set the number of messages to be transmitted
- txMsgCount - A counter for the number of messages sent
- rxMsgCount - A counter for the number of messages received
- txMsgData - An array with the data being sent
- rxMsgData - An array with the data that was received
- errorFlag - A flag that indicates an error has occurred

## 5.17 CAN External Loopback (can\_loopback)

This example shows the basic setup of CAN in order to transmit and receive messages on the CAN bus. The CAN peripheral is configured to transmit messages with a specific CAN ID. A message is then transmitted once per second, using a simple delay loop for timing. The message that is

sent is a 4 byte message that contains an incrementing pattern. A CAN interrupt handler is used to confirm message transmission and count the number of messages that have been sent.

This example sets up the CAN controller in External Loopback test mode. Data transmitted is visible on the CAN0TX pin and can be received with an appropriate mailbox configuration.

## 5.18 CAN External Loopback with Interrupts (can\_loopback\_interrupts)

This example shows the basic setup of CAN in order to transmit and receive messages on the CAN bus. The CAN peripheral is configured to transmit messages with a specific CAN ID. A message is then transmitted once per second, using a simple delay loop for timing. The message that is sent is a 4 byte message that contains an incrementing pattern. A CAN interrupt handler is used to confirm message transmission and count the number of messages that have been sent.

This example sets up the CAN controller in External Loopback test mode. Data transmitted is visible on the CAN0TX pin and can be received with an appropriate mailbox configuration.

This example uses the following interrupt handlers:

- INT\_CANA0 - CANIntHandler

## 5.19 CLA 5 Tap Finite Impulse Response Filter (cla\_adc\_fir32\_cpu01)

This example implements a 5 Tap FIR filter. It will setup EPWM1 to trigger ADCA at a frequency of 50KHz. Once the ADC completes sampling, it will trigger task 7 of the CLA which runs the filter on the ADC sample.

EPWM2 is setup to switch at 10KHz. Connect pin EPWM2A to ADCA0 on the board to see the filtering effect.

### Memory Allocation

- CPU to CLA1 Message RAM
  - A - Filter Coefficients
- CLA1 to CPU Message RAM
  - voltFilt - Filtered sample
  - X - filter sample delay line

### Watch Variables

- voltFilt - Filtered sample
- X - filter sample delay line

### External Connections

- EPWM2A (GPIO2) to ADCA0

## 5.20 CLA $\arcsine(x)$ using a lookup table (cla\_asin\_cpu01)

In this example, Task 1 of the CLA will calculate the arcsine of an input argument in the range (-1.0 to 1.0) using a lookup table.

### Memory Allocation

- CLA1 Math Tables (RAMLS0)
  - CLAasinTable - Lookup table
- CLA1 to CPU Message RAM
  - fResult - Result of the lookup algorithm
- CPU to CLA1 Message RAM
  - fVal - Sample input to the lookup algorithm

### Watch Variables

- fVal - Argument to task 1
- fResult - Result of  $\arcsin(fVal)$

## 5.21 CLA $\arctangent(x)$ using a lookup table (cla\_atan\_cpu01)

In this example, Task 1 of the CLA will calculate the arctangent of an input argument using a lookup table.

### Memory Allocation

- CLA1 Math Tables (RAMLS0)
  - CLAatan2Table - Lookup table
- CLA1 to CPU Message RAM
  - fResult - Result of the lookup algorithm
- CPU to CLA1 Message RAM
  - fNum - Numerator of sample input
  - fDen - Denominator of sample input

### Watch Variables

- fVal - Argument to task 1
- fResult - Result of  $\arctan(fVal)$

## 5.22 CLA CRC8 Table-Lookup Algorithm (cla\_crc8\_cpu01)

This example implements a table lookup method of determining the 8-bit CRC of a message sequence. The polynomial used is 0x07.

### Memory Allocation

- CLA1 Data RAM 0(RAMLS0)
  - table - CRC Lookup table
- CLA1 to CPU Message RAM
  - crc8\_msg1 - CRC of message 1
  - crc8\_msg2 - CRC of message 2
  - crc8\_msg3 - CRC of message 3
  - crc8\_msg4 - CRC of message 4
- CPU to CLA1 Message RAM
  - msg1 - Test message 1
  - msg2 - Test message 2
  - msg3 - Test message 3
  - msg4 - Test message 4

#### Watch Variables

- crc8\_msg1 - CRC of message 1
- crc8\_msg2 - CRC of message 2
- crc8\_msg3 - CRC of message 3
- crc8\_msg4 - CRC of message 4

## 5.23 CLA CRC8 Table-generation Algorithm (cla\_crc8table1\_cpu01)

This example will generate the lookup table for an 8bit CRC checker with the polynomial 0x07.

#### Memory Allocation

- CLA1 Data RAM 0(RAMLS0)
  - table - CRC Lookup table

#### Watch Variables

- table - Lookup table

## 5.24 CLA Determinant of 3X3 Matrix (cla\_det\_3by3\_cpu01)

In this example, Task 1 of the CLA will calculate the determinant of a 3x3 matrix.

#### Memory Allocation

- CLA1 to CPU Message RAM
  - fDet - Determinant of the 3x3 matrix
- CPU to CLA1 Message RAM

- x - 3x3 input matrix

**Watch Variables**

- fDet - Determinant of the 3x3 matrix

## 5.25 CLA Division: Newton Raphson Approximation (cla\_divide\_cpu01)

In this example, Task 1 of the CLA will divide two input numbers using multiple approximations in the Newton Raphson method.

**Memory Allocation**

- CLA1 to CPU Message RAM
  - Res - Result of the division operation
- CPU to CLA1 Message RAM
  - Num - Numerator of input
  - Den - Denominator of input

**Watch Variables**

- Num - Numerator of input
- Den - Denominator of input
- Res - Result of the division operation

## 5.26 CLA $10^X$ using a lookup table (cla\_exp2\_cpu01)

In this example, Task 1 of the CLA will calculate the Xth power of 10 using a table lookup method.

**Memory Allocation**

- CLA1 Math Tables (RAMLS0)
  - CLAexpTable - Lookup table
- CLA1 to CPU Message RAM
  - ExpRes - Result of the exponentiation operation
- CPU to CLA1 Message RAM
  - Val - The exponent

**Watch Variables**

- Val - Input
- ExpRes - Result of  $10^{Val}$

## 5.27 CLA $e^{\frac{A}{B}}$ using a lookup table (cla\_exp2\_cpu01)

In this example, Task 1 of the CLA will divide two input numbers using multiple approximations in the Newton Raphson method and then calculate the exponent of the result using a lookup table.

### Memory Allocation

- CLA1 Math Tables (RAMLS0)
  - CLAexpTable - Lookup table
- CLA1 to CPU Message RAM
  - ExpRes - Result of the exponentiation operation
- CPU to CLA1 Message RAM
  - Num - Numerator of input
  - Den - Denominator of input

### Watch Variables

- Num - Numerator of input
- Den - Denominator of input
- ExpRes - Result of  $e^{\frac{Num}{Den}}$

## 5.28 CLA 5 Tap Finite Impulse Response Filter (cla\_fir32\_cpu01)

This example implements a 5 Tap FIR filter. The input vector, stored in a lookup table, is filtered and then stored in an output buffer for storage.

### Memory Allocation

- CLA1 Data RAM 0 (RAMLS0)
  - fCoeffs - Filter Coefficients
  - fDelayLine - Delay line memory elements
- CLA1 to CPU Message RAM
  - xResult - Result of the FIR operation
- CPU to CLA1 Message RAM
  - xAdcInput - Simulated ADC input

### Watch Variables

- xResult - Result of the FIR operation
- xAdcInput - Simulated ADC input
- pass
- fail

## 5.29 CLA 2 Pole 2 Zero Infinite Impulse Response Filter (cla\_iir2p2z\_cpu01)

This example implements a Transposed Direct Form II IIR filter, commonly known as a Biquad. The input vector is a software simulated noisy signal that is fed to the biquad one sample at a time, filtered and then stored in an output buffer for storage.

### Memory Allocation

- CLA1 Data RAM 1 (RAML2)
  - S1\_A - Feedback coefficients
  - S1\_B - Feedforward coefficients
- CLA1 to CPU Message RAM
  - yn - Output of the Biquad
- CPU to CLA1 Message RAM
  - xn - Sample input to the filter

### Watch Variables

- fBiquadOutput
- pass
- fail

## 5.30 CLA Logic Test (cla\_logic\_cpu01)

In this example, Task 1 of the CLA implements a set of logic tests. More information about these logic statements can be found at:

<http://graphics.stanford.edu/~seander/bithacks.html#OperationCounting>

### Memory Allocation

- CLA1 to CPU Message RAM
  - cla\_pass\_count - Logic test pass count
  - cla\_fail\_count - Logic test fail count

### Watch Variables

- cla\_pass\_count - Logic test pass count
- cla\_fail\_count - Logic test fail count

## 5.31 CLA Matrix Multiplication (cla\_matrix\_mpy\_cpu01)

In this example, Task 1 of the CLA multiplies two 3x3 matrices.

### Memory Allocation

- CLA1 to CPU Message RAM
  - z - Result of the matrix multiplication
- CPU to CLA1 Message RAM
  - x - 3X3 Input Matrix
  - y - 3X3 Input Matrix

**Watch Variables**

- x - 3X3 Input Matrix
- y - 3X3 Input Matrix
- z - Result of the matrix multiplication

## 5.32 CLA Matrix Transpose (cla\_matrix\_transpose\_cpu01)

In this example, Task 1 of the CLA calculates the transpose of a 3x3 matrix.

**Memory Allocation**

- CLA1 to CPU Message RAM
  - z - Transposed Matrix
- CPU to CLA1 Message RAM
  - x - 3X3 Input Matrix

**Watch Variables**

- x - 3X3 Input Matrix
- z - Transposed Matrix

## 5.33 CLA Mixed C and Assembly Code (cla\_mixed\_c\_asm\_cpu01)

This example shows the use of both C and assembly code on the CLA. The arc-cosine function uses a table lookup method and polynomial interpolation to determine the angle corresponding to the argument. The tables are stored in the CLA data ROM.

The tables needed by the acos routine are located in the CLA data ROM. A symbol table library is included with this example:

```
c1bootROM_CLADDataROMSymbols(_fpu32).lib
```

The user must add this to the inclusion list in the upper window of the "File Search Path" options which can be found under "properties → c2000 linker → File Search Path"

Since this library is present in the source directory, the user must also add the search path to the bottom window "\${PROJECT\_ROOT}/../"

**Watch Variables**



- y1 - Accumulated results (angles in radians) from C routine
- y2 - Accumulated results (angles in radians) from asm routine

## 5.34 CLA Primes (cla\_prime\_cpu01)

In this example, Task 1 of the CLA calculates the set of prime numbers up to a length defined by the user.

### Memory Allocation

- CLA1 Data RAM 0 (RAMLS0)
  - out - Set of primes

### Watch Variables

- out - Set of primes

## 5.35 CLA Shell Sort (cla\_shellsort\_cpu01)

In this example, Task 1 will perform the shell sort iteratively. Task 2 will do the same with mswapf intrinsic and Task 3 will also implement an in-place sort on an integer vector

### Memory Allocation

- CLA1 Data RAM 1 (RAML2)
  - vector3 - Input/Output to task 3(in-place sorting)
- CLA1 to CPU Message RAM
  - vector1\_sorted - Sorted output Task 1
  - vector2\_sorted - Sorted output Task 2
- CPU to CLA1 Message RAM
  - vector1 - Input vector to task 1
  - vector2 - Input vector to task 2

### Watch Variables

- vector3 - Input/Output to task 3(in-place sorting)
- vector1\_sorted - Sorted output Task 1
- vector2\_sorted - Sorted output Task 2
- vector1 - Input vector to task 1
- vector2 - Input vector to task 2

## 5.36 CLA Square Root (cla\_sqrt\_cpu01)

In this example, Task 1 calculates the square root of a number using multiple iterations of the Newton-Raphson approximation

### Memory Allocation

- CLA1 to CPU Message RAM
  - fResult -  $\sqrt{fVal}$
- CPU to CLA1 Message RAM
  - fVal - Input value

### Watch Variables

- fVal - Input value
- fResult -  $\sqrt{fVal}$

## 5.37 CLA Vector Inverse (cla\_inverse\_cpu01)

In this example, Task 1 calculates the element-wise inverse of a vector while Task 2 calculates the element-wise inverse of a vector and saves the result in the same vector

### Memory Allocation

- CLA1 Data RAM 1 (RAML2)
  - vector2 - Input/Output vector for task 2
- CLA1 to CPU Message RAM
  - vector1\_inverse - Inverse of input vector1
- CPU to CLA1 Message RAM
  - vector1 - Input vector to task 1

### Watch Variables

- vector1 - Input vector to task 1
- vector1\_inverse - Inverse of input vector1
- vector2 - Input/Output vector for task 2

## 5.38 CLA Vector Maximum (cla\_vmaxfloat\_cpu01)

Task 1 calculates the vector max moving backward through the array.

Task 2 calculates the vector max moving forward through the array.

Task 3 calculates the vector max using the ternary operator.

Task 4 calculates the vector max using min/max intrinsics.

### Memory Allocation

- CLA1 to CPU Message RAM
  - max1 - Maximum value in vector 1
  - index1 - Index of the maximum value in vector 1
  - max2 - Maximum value in vector 2
  - index2 - Index of the maximum value in vector 2
  - max3 - Maximum value in vector 3
  - index3 - Index of the maximum value in vector 3
  - max4 - Maximum value in vector 4
  - min4 - Minimum value in vector 4
- CPU to CLA1 Message RAM
  - vector1 - Input vector to task 1
  - vector2 - Input vector to task 2
  - vector3 - Input vector to task 3
  - vector4 - Input vector to task 4
  - length1 - Length of vector 1
  - length2 - Length of vector 2

#### **Watch Variables**

- vector1 - Input vector to task 1
- vector2 - Input vector to task 2
- vector3 - Input vector to task 3
- vector4 - Input vector to task 4
- max1 - Maximum value in vector 1
- index1 - Index of the maximum value in vector 1
- max2 - Maximum value in vector 2
- index2 - Index of the maximum value in vector 2
- max3 - Maximum value in vector 3
- index3 - Index of the maximum value in vector 3
- max4 - Maximum value in vector 4
- min4 - Minimum value in vector 4

## **5.39 CLA Vector Minimum (cla\_vminfloat\_cpu01)**

Task 1 calculates the vector min moving backward through the array.

Task 2 calculates the vector min moving forward through the array.

Task 3 calculates the vector min using the ternary operator.

#### **Memory Allocation**

- CLA1 to CPU Message RAM
  - min1 - Minimum value in vector 1
  - index1 - Index of the minimum value in vector 1

- min2 - Minimum value in vector 2
- index2 - Index of the minimum value in vector 2
- min3 - Minimum value in vector 3
- index3 - Index of the minimum value in vector 3
- CPU to CLA1 Message RAM
  - vector1 - Input vector to task 1
  - vector2 - Input vector to task 2
  - vector3 - Input vector to task 3
  - length1 - Length of vector 1
  - length2 - Length of vector 2
  - length3 - Length of vector 3

#### Watch Variables

- vector1 - Input vector to task 1
- vector2 - Input vector to task 2
- vector3 - Input vector to task 3
- min - Minimum value in vector 1
- index1 - Index of the minimum value in vector 1
- min2 - Minimum value in vector 2
- index2 - Index of the minimum value in vector 2
- min3 - Minimum value in vector 3
- index3 - Index of the minimum value in vector 3

## 5.40 CMPSS Asynchronous Trip

This example enables the CMPSS1 COMPH comparator and feeds the asynch CTRIPOUTH to GPIO14/OUTPUTXBAR3 pin and CTRIPH to GPIO15/EPWM8B

The COMPH inputs are:

- POS signal from CMPIN1P pin
- NEG signal from internal DACH

## 5.41 CMPSS Digital Filter

This example enables the CMPSS1 COMPH comparator and feeds the output through the digital filter to the GPIO14/OUTPUTXBAR3 pin.

The COMPH inputs are:

- POS signal from CMPIN1P pin
- NEG signal from internal DACH

## 5.42 CPU Timers

This example configures CPU Timer0, 1, and 2 and increments a counter each time the timer asserts an interrupt.

### Watch Variables

- CpuTimer0.InterruptCount
- CpuTimer1.InterruptCount
- CpuTimer2.InterruptCount

## 5.43 SafeCopyCode Reset (dcsm\_scc\_reset\_cpu01)

This example shows how to issue a reset using the SafeCopyCode (SCC) function. In the case of a vector fetch while the PC points to the SCC function, an SCCRESETn gets generated. In this example, a CPU Timer interrupt is enabled to cause this vector fetch.

### Note:

The CPU Timer used can be switched based on the value passed to IssueSCCReset(). Valid values include **CPUTIMER0**, **CPUTIMER1**, and **CPUTIMER2**.

## 5.44 DMA GSRAM Transfer (dma\_gsram\_transfer)

This example uses one DMA channel to transfer data from a buffer in RAMGS0 to a buffer in RAMGS1. The example sets the DMA channel PERINTFRC bit repeatedly until the transfer of 16 bursts (where each burst is 8 16-bit words) has been completed. When the whole transfer is complete, it will trigger the DMA interrupt.

### Watch Variables

- **sdata** - Data to send
- **rdata** - Received data

## 5.45 ECAP APWM Example

This program sets up the eCAP pins in the APWM mode. This program runs at 200 MHz SYSCLK assuming a 20 MHz OSCCLK.

eCAP1 will come out on the GPIO5 pin. This pin is configured to vary between frequencies using the shadow registers to load the next period/compare values.

## 5.46 ECAP Capture PWM Example

This example configures ePWM3A for:

- Up count
- Period starts at 2 and goes up to 1000
- Toggle output on PRD

eCAP1 is configured to capture the time between rising and falling edge of the ePWM3A output.

#### External Connections

- eCAP1 is on GPIO19
- ePWM3A is on GPIO4
- Connect GPIO4 to GPIO19.

#### Watch Variables

- **ECap1PassCount** - Successful captures
- **ECap1IntCount** - Interrupt counts

## 5.47 EMIF ASYNC module (emif1\_16bit\_asram)

This example configures EMIF1 in 16bit ASYNC mode This example uses CS2 as chip enable.

#### Watch Variables:

- **TEST\_STATUS** - Equivalent to **TEST\_PASS** if test finished correctly, else the value is set to **TEST\_FAIL**
- **ErrCount** - Error counter

## 5.48 EMIF1 SDRAM Module (emif1\_16bit\_sdram\_dma)

This example configures EMIF1 in 16bit SDRAM mode and uses CS0 (SDRAM) as chip enable. It will first write to an array in the SDRAM and then read it back using the DMA for both operations. The buffer in SDRAM will be placed in the .farbss memory on account of the fact that its assigned the attribute "far" indicating it lies beyond the 22-bit program address space. The compiler will take care to avoid using instructions such as PREAD, which uses the Program Read Bus, or addressing modes restricted to the lower 22-bit space when accessing data with the attribute "far"

#### Note:

The memory space beyond 22-bits must be treated as data space for load/store operations only. The user is cautioned against using this space for either instructions or working memory.

Example has been tested using Micron 48LC32M16A2 "P -75 C" part.

#### Watch Variables:

- **TEST\_STATUS** - Equivalent to **TEST\_PASS** if test finished correctly, else the value is set to **TEST\_FAIL**
- **ErrCount** - Error counter

## 5.49 EMIF1 SDRAM Module (emif1\_16bit\_sdram\_far)

This example configures EMIF1 in 16bit SDRAM mode and uses CS0 (SDRAM) as chip enable. It will first write to an array in the SDRAM and then read it back using the FPU function, `memcpy_fast_far()`, for both operations. The buffer in SDRAM will be placed in the `.farbss` memory on account of the fact that its assigned the attribute "far" indicating it lies beyond the 22-bit program address space. The compiler will take care to avoid using instructions such as `PREAD`, which uses the Program Read Bus, or addressing modes restricted to the lower 22-bit space when accessing data with the attribute "far"

**Note:**

The memory space beyond 22-bits must be treated as data space for load/store operations only. The user is cautioned against using this space for either instructions or working memory.

**Watch Variables:**

- **TEST\_STATUS** - Equivalent to **TEST\_PASS** if test finished correctly, else the value is set to **TEST\_FAIL**
- **ErrCount** - Error counter

## 5.50 EMIF1 SDRAM Module (emif1\_32bit\_sdram)

This example configures EMIF1 in 32bit SDRAM mode. This example uses CS0 (SDRAM) as chip enable.

**Watch Variables:**

- **TEST\_STATUS** - Equivalent to **TEST\_PASS** if test finished correctly, else the value is set to **TEST\_FAIL**
- **ErrCount** - Error counter

## 5.51 EPWM dead band control (epwm\_deadband)

During the test, monitor ePWM1, ePWM2, and/or ePWM3 outputs on a scope.

- ePWM1A is on GPIO0
- ePWM1B is on GPIO1
- ePWM2A is on GPIO2
- ePWM2B is on GPIO3
- ePWM3A is on GPIO4
- ePWM3B is on GPIO5

This example configures ePWM1, ePWM2 and ePWM3 for:

- Count up/down
- Deadband

3 Examples are included:

- ePWM1: Active low PWMs
- ePWM2: Active low complementary PWMs
- ePWM3: Active high complementary PWMs

Each ePWM is configured to interrupt on the 3rd zero event. When this happens the deadband is modified such that  $0 \leq DB \leq DB\_MAX$ . That is, the deadband will move up and down between 0 and the maximum value.

View the EPWM1A/B, EPWM2A/B and EPWM3A/B waveforms via an oscilloscope

## 5.52 EPWM Trip Zone Module (epwm\_trip\_zone)

This example configures ePWM1 and ePWM2 as follows

- ePWM1 has TZ1 as one shot trip source
- ePWM2 has TZ1 as cycle by cycle trip source

Initially tie TZ1 high. During the test, monitor ePWM1 or ePWM2 outputs on a scope. Pull TZ1 low to see the effect.

### External Connections

- EPWM1A is on GPIO0
- EPWM2A is on GPIO2
- TZ1 is on GPIO12

This example also makes use of the Input X-BAR. GPIO12 (the external trigger) is routed to the input X\_BAR, from which it is routed to TZ1.

The TZ-Event is defined such that EPWM1A will undergo a One-Shot Trip and EPWM2A will undergo a Cycle-By-Cycle Trip.

## 5.53 EPWM Action Qualifier (epwm\_up\_aq)

This example configures ePWM1, ePWM2, ePWM3 to produce an waveform with independent modulation on EPWMxA and EPWMxB.

The compare values CMPA and CMPB are modified within the ePWM's ISR.

The TB counter is in up count mode for this example.

View the EPWM1A/B(PA0\_GPIO0 & PA1\_GPIO1), EPWM2A/B(PA2\_GPIO2 & PA3\_GPIO3) and EPWM3A/B(PA4\_GPIO4 & PA5\_GPIO5) waveforms via an oscilloscope.



## 5.54 EPWM Action Qualifier (epwm\_updown\_aq)

This example configures ePWM1, ePWM2, ePWM3 to produce an waveform with independent modulation on EPWMxA and EPWMxB.

The compare values CMPA and CMPB are modified within the ePWM's ISR.

The TB counter is in up/down count mode for this example.

View the EPWM1A/B(PA0\_GPIO0 & PA1\_GPIO1), EPWM2A/B(PA2\_GPIO2 & PA3\_GPIO3) and EPWM3A/B(PA4\_GPIO4 & PA5\_GPIO5) waveforms via an oscilloscope.

## 5.55 Frequency measurement using EQEP peripheral (Eqep\_freqcal)

This test will calculate the frequency and period of an input signal using eQEP module.

EPWM1A is configured to generate a frequency of 5 kHz.

### See also:

Section on Frequency Calculation for more details on the frequency calculation performed in this example.

In addition to the main example file, the following files must be included in this project:

- **Example\_freqcal.c** - includes all eQEP functions
- **Example\_EPwmSetup.c** - sets up EPWM1A for use with this example
- **Example\_freqcal.h** - includes initialization values for frequency structure.

The configuration for this example is as follows

- Maximum frequency is configured to 10KHz (BaseFreq)
- Minimum frequency is assumed at 50Hz for capture pre-scalar selection

**SPEED\_FR:** High Frequency Measurement is obtained by counting the external input pulses for 10ms (unit timer set to 100Hz).

$$SPEED\_FR = \frac{Count\ Delta}{10ms}$$

**SPEED\_PR:** Low Frequency Measurement is obtained by measuring time period of input edges. Time measurement is averaged over 64 edges for better results and capture unit performs the time measurement using pre-scaled SYSCLK.

Note that pre-scaler for capture unit clock is selected such that capture timer does not overflow at the required minimum frequency. This example runs forever until the user stops it.

### External Connections

- Connect GPIO20/EQEP1A to GPIO0/EPWM1A

### Watch Variables

- **freq.freqhz\_fr** - Frequency measurement using position counter/unit time out
- **freq.freqhz\_pr** - Frequency measurement using capture unit

## 5.56 EQEP Speed and Position Measurement (Eqep\_pos\_speed)

This example provides position measurement, speed measurement using the capture unit, and speed measurement using unit time out. This example uses the IQMath library. It is used merely to simplify high-precision calculations. The example requires the following hardware connections from EPWM1 and GPIO pins (simulating QEP sensor) to QEP peripheral.

- GPIO20/eQEP1A <- GPIO0/ePWM1A (simulates eQEP Phase A signal)
- GPIO21/eQEP1B <- GPIO1/ePWM1B (simulates eQEP Phase B signal)
- GPIO23/eQEP1I <- GPIO4 (simulates eQEP Index Signal)

See DESCRIPTION in Example\_posspeed.c for more details on the calculations performed in this example. In addition to this file, the following files must be included in this project:

- Example\_posspeed.c - includes all eQEP functions
- Example\_EPwmSetup.c - sets up ePWM1A and ePWM1B as simulated QA and QB encoder signals
- Example\_posspeed.h - includes initialization values for pos and speed structure

Note:

- Maximum speed is configured to 6000rpm(BaseRpm)
- Minimum speed is assumed at 10rpm for capture pre-scalar selection
- Pole pair is configured to 2 (pole\_pairs)
- QEP Encoder resolution is configured to 4000counts/revolution (mech\_scaler)
- Which means:  $4000/4 = 1000$  line/revolution quadrature encoder (simulated by EPWM1)
- EPWM1 (simulating QEP encoder signals) is configured for 5kHz frequency or 300 rpm ( $= 4 * 5000 \text{ cnts/sec} * 60 \text{ sec/min} / 4000 \text{ cnts/rev}$ )
- SPEEDRPM\_FR: High Speed Measurement is obtained by counting the QEP input pulses for 10ms (unit timer set to 100Hz).
- $\text{SPEEDRPM\_FR} = (\text{Position Delta}/10\text{ms}) * 60 \text{ rpm}$
- SPEEDRPM\_PR: Low Speed Measurement is obtained by measuring time period of QEP edges. Time measurement is averaged over 64edges for better results and capture unit performs the time measurement using pre-scaled SYSCLK
- Pre-scalar for capture unit clock is selected such that capture timer does not overflow at the required minimum RPM speed.

### External Connections

- Connect eQEP1A(GPIO20) to ePWM1A(GPIO0)(simulates eQEP Phase A signal)
- Connect eQEP1B(GPIO21) to ePWM1B(GPIO1)(simulates eQEP Phase B signal)

- Connect eQEP1I(GPIO23) to GPIO4 (simulates eQEP Index Signal)

**Watch Variables**

- qep\_posspeed.SpeedRpm\_fr - Speed meas. in rpm using QEP position counter
- qep\_posspeed.SpeedRpm\_pr - Speed meas. in rpm using capture unit
- qep\_posspeed.theta\_mech - Motor mechanical angle (Q15)
- qep\_posspeed.theta\_elec - Motor electrical angle (Q15)

## 5.57 External Interrupts (ExternalInterrupt)

This program sets up GPIO0 as XINT1 and GPIO1 as XINT2. Two other GPIO signals are used to trigger the interrupt (GPIO30 triggers XINT1 and GPIO31 triggers XINT2). The user is required to externally connect these signals for the program to work properly.

XINT1 input is synced to SYSCLKOUT.

XINT2 has a long qualification - 6 samples at  $510 \times \text{SYSCLKOUT}$  each.

GPIO34 will go high outside of the interrupts and low within the interrupts. This signal can be monitored on a scope.

Each interrupt is fired in sequence - XINT1 first and then XINT2

**External Connections**

- Connect GPIO30 to GPIO0. GPIO0 will be assigned to XINT1
- Connect GPIO31 to GPIO1. GPIO1 will be assigned to XINT2

Monitor GPIO34 with an oscilloscope. GPIO34 will be high outside of the ISRs and low within each ISR.

**Watch Variables**

- Xint1Count for the number of times through XINT1 interrupt
- Xint2Count for the number of times through XINT2 interrupt
- LoopCount for the number of times through the idle loop

## 5.58 Device GPIO Setup (GpioSetup)

Configures the F2837xD GPIO into two different configurations. This code is verbose to illustrate how the GPIO could be setup. In a real application, lines of code can be combined for improved code size and efficiency.

This example only sets-up the GPIO. Nothing is actually done with the pins after setup.

**In general:**

- All pullup resistors are enabled. For ePWMs this may not be desired.
- Input qual for communication ports (eCAN, SPI, SCI, I2C) is asynchronous

- Input qual for Trip pins (TZ) is asynchronous
- Input qual for eCAP and eQEP signals is synch to SYSCLKOUT
- Input qual for some I/O's and \_\_interrupts may have a sampling window

## 5.59 GPIO toggle test program (GpioToggle)

Three different examples are included. Select the example (data, set/clear or toggle) to execute before compiling using the define statements found at the top of the code.

Toggle all of the GPIO PORT pins

The pins can be observed using Oscilloscope.

## 5.60 HRPWM SFO Test (hrpwm\_duty\_sfo\_v8)

This program requires the F2837xD header files, which include the following files required for this example: SFO\_V8.h and SFO\_TI\_Build\_V8\_FPU.lib

Monitor ePWM1-ePWM8 A/B pins on an oscilloscope. DESCRIPTION:

This example modifies the MEP control registers to show edge displacement for high-resolution period with ePWM in Up-Down count mode due to the HRPWM control extension of the respective ePWM module.

This example calls the following TI's MEP Scale Factor Optimizer (SFO) software library V8 functions:

**int SFO();**

updates MEP\_ScaleFactor dynamically when HRPWM is in use updates HRMSTEP register (exists only in EPwm1Regs register space) with MEP\_ScaleFactor value

- returns 2 if error: MEP\_ScaleFactor is greater than maximum value of 255 (Auto-conversion may not function properly under this condition)
- returns 1 when complete for the specified channel
- returns 0 if not complete for the specified channel

This example is intended to explain the HRPWM capabilities. The code can be optimized for code efficiency. Refer to TI's Digital power application examples and TI Digital Power Supply software libraries for details.

All ePWM1 -7 all channels will have fine edge movement due to the HRPWM logic

=====

NOTE: For more information on using the SFO software library, see the F2837xD High-Resolution Pulse Width Modulator (HRPWM) Reference Guide

=====

To load and run this example:

1. **\*\*\*!!IMPORTANT!!\*\*** - in SFO\_V8.h, set PWM\_CH to the max number of HRPWM channels plus one. For example, for the F2837xD, the maximum number of HRPWM channels is 8. 8+1=9, so set define PWM\_CH 9 in SFO\_V8.h. (Default is 8)

2. Run this example at maximum SYSCLKOUT
3. Activate Real time mode
4. Run the code
5. Watch ePWM A / B channel waveforms on a Oscilloscope
6. In the watch window: Set the variable UpdateFine = 1 to observe the ePWMxA & ePWMxB output with HRPWM capabilities (default) Observe the period/frequency of the waveform changes in fine MEP steps
7. In the watch window: Change the variable UpdateFine to 0, to observe the ePWMxA & ePWMxB output without HRPWM capabilities Observe the period/frequency of the waveform changes in coarse SYSCLKOUT cycle steps.

## 5.61 HRPWM SFO Test (hrpwm\_prdupdown\_sfo\_v8)

This program requires the F2837xD header files, which include the following files required for this example: SFO\_V8.h and SFO\_TI\_Build\_V8\_FPU.lib

Monitor ePWM1-ePWM8 A/B pins on an oscilloscope. DESCRIPTION:

This example modifies the MEP control registers to show edge displacement for high-resolution period with ePWM in Up-Down count mode due to the HRPWM control extension of the respective ePWM module.

This example calls the following TI's MEP Scale Factor Optimizer (SFO) software library V8 functions:

**int SFO();**

updates MEP\_ScaleFactor dynamically when HRPWM is in use updates HRMSTEP register (exists only in EPwm1Regs register space) with MEP\_ScaleFactor value

- returns 2 if error: MEP\_ScaleFactor is greater than maximum value of 255 (Auto-conversion may not function properly under this condition)
- returns 1 when complete for the specified channel
- returns 0 if not complete for the specified channel

This example is intended to explain the HRPWM capabilities. The code can be optimized for code efficiency. Refer to TI's Digital power application examples and TI Digital Power Supply software libraries for details.

All ePWM1-8 A/B channels will have fine edge movement due to the HRPWM logic

=====

NOTE: For more information on using the SFO software library, see the F2837xD High-Resolution Pulse Width Modulator (HRPWM) Reference Guide

=====

To load and run this example:

1. **\*\*\*!!IMPORTANT!!\*\*** - in SFO\_V8.h, set PWM\_CH to the max number of HRPWM channels plus one. For example, for the F2837xD, the maximum number of HRPWM channels is 8. 8+1=9, so set define PWM\_CH 9 in SFO\_V8.h. (Default is 8)
2. Run this example at maximum SYSCLKOUT

3. Activate Real time mode
4. Run the code
5. Watch ePWM A / B channel waveforms on an Oscilloscope
6. In the watch window: Set the variable UpdateFine = 1 to observe the ePWMxA & ePWMxB output with HRPWM capabilities (default) Observe the period/frequency of the waveform changes in fine MEP steps
7. In the watch window: Change the variable UpdateFine to 0, to observe the ePWMxA & ePWMxB output without HRPWM capabilities Observe the period/frequency of the waveform changes in coarse SYSCLKOUT cycle steps.

## 5.62 HRPWM Slider Test (hrpwm\_slider)

This example modifies the MEP control registers to show edge displacement due to HRPWM control blocks of the respective EPwm module channel A and B will have fine edge movement due to HRPWM logic. Load the F2837xD\_HRPWM\_slider.gel file. Select the HRPWM\_eval from the GEL menu. A FineDuty slider graphics will show up in CCS. Load the program and run. Use the Slider to and observe the EPwm edge displacement for each slider step change. This explains the MEP control on the EPwmxA channels.

Monitor ePWM1-ePWM8 A/B pins on an oscilloscope.

## 5.63 I2C EEPROM Example (i2c\_eeprom)

This program will write 1-14 words to EEPROM and read them back. The data written and the EEPROM address written to are contained in the message structure, I2cMsgOut1. The data read back will be contained in the message structure I2cMsgIn1.

### External Connections

- This program requires an external I2C EEPROM connected to the I2C bus at address 0x50.

## 5.64 Low Power Modes: Halt Mode and Wakeup (lpm\_haltwake)

This example puts the device into HALT mode. If the lowest possible current consumption in HALT mode is desired, the JTAG connector must be removed from the device board while the device is in HALT mode.

The example then wakes up the device from HALT using GPIO10. GPIO10 wakes the device from HALT mode when a high-to-low signal is detected on the pin. This pin must be pulsed by an external agent for wakeup.

The wakeup process begins as soon as GPIO10 is held low for the time indicated in the device datasheet. After the device wakes up, GPIO11 can be observed to go low.

GPIO10 is configured as the LPM wakeup pin to trigger a WAKEINT interrupt upon detection of a low pulse. Initially, pull GPIO10 high externally.

To observe when device wakes from HALT mode, monitor GPIO11 with an oscilloscope (Cleared to 0 in WAKEINT ISR)

## 5.65 Low Power Modes: HIB Mode and Wakeup (lpm\_hibwake)

This example puts the device into HIB mode. This is the lowest possible power configuration of the device. To realize the lowest possible current consumption in HIB mode, The JTAG connector should be removed from the device board while the device is in HIB mode.

This example will configure the IoRestore Address, Memory Retention, and then enter HIB mode. After wake-up, the example will reconfigure the GPIOs, disable IO isolation and then re-enter main.

GPIOHIBWAKEn(GPIO41) wakes the device from HIB mode when a high->low->high signal is detected on the pin. This pin must be pulsed by an external agent for wakeup.

GPIO10 and GPIO11 are configured as outputs for status indicators to the outside world. Connect GPIO10 to an external agent to notify that the device has entered HIB mode. View both GPIO10 and GPIO11 on an oscilloscope to view the device status.

GPIO10 = 1, GPIO11 = 1: Device is in HIB mode

GPIO10 = 1, GPIO11 = 0: Code execution is in IoRestore, IO isolation has been disabled

GPIO10 = 0, GPIO11 = 0: Code execution is in main.

The wakeup process begins after GPIOHIBWAKEn is held low for the time indicated in the device datasheet and then brought high again. After the device wakes up, GPIO11 can be observed to go low in IoRestore and GPIO10 will go low when the program has re-entered main.

If M0M1 memory retention is not desired, set RETAINM0M1 to 0.

## 5.66 Low Power Modes: Device Idle Mode and Wakeup(lpm\_idlewake)

This example puts the device into IDLE mode then wakes up the device from IDLE using XINT1 which triggers on a falling edge from GPIO0.

This pin must be pulled from high to low by an external agent for wakeup. GPIO0 is configured as an XINT1 pin to trigger an XINT1 interrupt upon detection of a falling edge.

Initially, pull GPIO0 high externally. To wake device from idle mode by triggering an XINT1 interrupt, pull GPIO0 low (falling edge)

### External Connections

- To observe the device wakeup from IDLE mode, monitor GPIO1 with an oscilloscope, which goes high in the XINT\_1\_ISR.

## 5.67 Low Power Modes: Device Standby Mode and Wakeup(lpm\_standbywake)

This example puts the device into STANDBY mode. If the lowest possible current consumption in STANDBY mode is desired, the JTAG connector must be removed from the device board while the device is in STANDBY mode.

GPIO0 is configured as the LPM wakeup pin to trigger a WAKEINT interrupt upon detection of a low pulse. Initially, pull GPIO0 high externally. To wake device from standby mode, pull GPIO0 low for at least (2+QUALSTDBY) OSCCLKS, then pull it high again.

The example then wakes up the device from STANDBY using GPIO0. GPIO0 wakes the device from STANDBY mode when a low pulse (signal goes high->low->high) is detected on the pin. This pin must be pulsed by an external agent for wakeup.

As soon as GPIO0 goes high again after the pulse, the device should wake up, and GPIO1 can be observed to toggle.

### External Connections

- To observe when device wakes from STANDBY mode, monitor GPIO1 with an oscilloscope (set to 1 in WAKEINT ISR)

## 5.68 McBSP Loopback (mcbbsp\_loopback)

Three different serial word sizes can be tested. Before compiling this project, select the serial word size of 8, 16 or 32 by using the #define statements at the beginning of the code.

This example does not use interrupts. Instead, a polling method is used to check the receive data. The incoming data is checked for accuracy. If an error is found the error() function is called and execution stops.

This program will execute until terminated by the user.

### 8-bit word example:

The sent data looks like this:

00 01 02 03 04 05 06 07 .... FE FF

### 16-bit word example:

The sent data looks like this:

0000 0001 0002 0003 0004 0005 0006 0007 .... FFFE FFFF

### 32-bit word example:

The sent data looks like this:

FFFF0000 FFFE0001 FFFD0002 .... 0000FFFF

### Watch Variables:

- sdata1 - Sent data word: 8 or 16-bit or low half of 32-bit
- sdata2 - Sent data word: upper half of 32-bit



- rdata1 - Received data word: 8 or 16-bit or low half of 32-bit
- rdata2 - Received data word: upper half of 32-bit
- rdata1\_point - Tracks last position in receive stream 1 for error checking
- rdata2\_point - Tracks last position in receive stream 2 for error checking

**Note:**

sdata2 and rdata2 are not used for 8-bit or 16-bit word size

## 5.69 McBSP Loopback with DMA (mcbasp\_loopback\_dma)

This program is a McBSP example that uses the internal loopback of the peripheral and utilizes the DMA to transfer data from one buffer to the McBSP, and then from the McBSP to another buffer.

Initially, sdata[] is filled with values from 0x0000- 0x007F. The DMA moves the values in sdata[] one by one to the DXRx registers of the McBSP. These values are transmitted and subsequently received by the McBSP. Then, the DMA moves each data value to rdata[] as it is received by the McBSP.

The sent data buffer will alternate between:

0000 0001 0002 0003 0004 0005 .... 007F

and

FFFF FFFE FFFD FFFC FFFB FFFA ....

Three different McBSP serial word sizes can be tested. Before compiling this project, select the serial word size of 8, 16 or 32 by using the #define statements at the beginning of the code.

This example uses DMA channel 1 and 2 interrupts. The incoming data is checked for accuracy. If an error is found the error() function is called and execution stops.

By default for the McBSP examples, the McBSP sample rate generator (SRG) input clock frequency is LSPCLK (80E6/4) assuming SYSCLKOUT = 80 MHz.

This example will execute until terminated by the user.

**Watch Variables:**

- sdata - Sent data buffer
- rdata - Received data buffer

## 5.70 McBSP Loopback with Interrupts (mcbasp\_loopback\_interrupts)

This program is a McBSP example that uses the internal loopback of the peripheral. Both Rx and Tx interrupts are enabled.

Incrementing values from 0x0000 to 0x00FF are being sent and received.

This pattern is repeated forever.

By default for the McBSP examples, the McBSP sample rate generator (SRG) input clock frequency is LSPCLK 80E6/4.

**Watch Variables:**

- sdata - Sent data word
- rdata - Received data word
- rdata\_point - Tracks last position in receive stream for error checking

## 5.71 McBSP Loopback using SPI mode (mcbbsp\_spi\_loopback)

This program will execute and transmit words until terminated by the user. SPI master mode transfer of 32-bit word size with digital loopback enabled.

**McBSP Signals - SPI equivalent**

- MCLKX - SPICLK (master)
- MFSX - SPISTE (master)
- MDX - SPISIMO
- MCLKR - SPICLK (slave - not used for this example)
- MFSR - SPISTE (slave - not used for this example)
- MDR - SPISOMI (not used for this example)

By default for the McBSP examples, the McBSP sample rate generator (SRG) input clock frequency is LSPCLK 80E6/4.

**Watch Variables:**

- sdata1 - Sent data word(1)
- sdata2 - Sent data word(2)
- rdata1 - Received data word(1)
- rdata2 - Received data word(2)

## 5.72 SCI Echoback (sci\_echoback)

This test receives and echo-backs data through the SCI-A port.

The PC application 'hyperterminal' or another terminal such as 'putty' can be used to view the data from the SCI and to send information to the SCI. Characters received by the SCI port are sent back to the host.

**Running the Application**

1. Configure hyperterminal or another terminal such as putty:

For hyperterminal you can use the included hyperterminal configuration file SCI\_96.ht. To load this configuration in hyperterminal

1. Open hyperterminal
2. Go to file->open
3. Browse to the location of the project and select the SCI\_96.ht file.

Check the COM port. The configuration file is currently setup for COM1. If this is not correct, disconnect (Call->Disconnect) Open the File-Properties dialogue and select the correct COM port.

1. Connect hyperterminal Call->Call and then start the 2837xD SCI echoback program execution.
2. The program will print out a greeting and then ask you to enter a character which it will echo back to hyperterminal.

**Note:**

If you are unable to open the .ht file, or you are using a different terminal, you can open a COM port with the following settings

- Find correct COM port
- Bits per second = 9600
- Data Bits = 8
- Parity = None
- Stop Bits = 1
- Hardware Control = None

**Watch Variables**

- LoopCount - the number of characters sent

**External Connections**

Connect the SCI-A port to a PC via a transceiver and cable.

- GPIO28 is SCI\_A-RXD (Connect to Pin3, PC-TX, of serial DB9 cable)
- GPIO29 is SCI\_A-TXD (Connect to Pin2, PC-RX, of serial DB9 cable)

## 5.73 SCI FIFO Digital Loop Back Test (sci\_looback)

This program uses the internal loop back test mode of the peripheral. Other than boot mode pin configuration, no other hardware configuration is required.

This test uses the loopback test mode of the SCI module to send characters starting with 0x00 through 0xFF. The test will send a character and then check the receive buffer for a correct match.

**Watch Variables**

- **LoopCount** - Number of characters sent
- **ErrorCount** - Number of errors detected
- **SendChar** - Character sent
- **ReceivedChar** - Character received

## 5.74 SCI Digital Loop Back with Interrupts (sci\_loopback\_interrupts)

This program uses the internal loop back test mode of the peripheral. Other than boot mode pin configuration, no other hardware configuration is required. Both interrupts and the SCI FIFOs are used.

A stream of data is sent and then compared to the received stream. The SCI-A sent data looks like this:

00 01

01 02

02 03

....

FE FF

FF 00

etc..

The pattern is repeated forever.

### Watch Variables

- **sdataA** - Data being sent
- **rdataA** - Data received
- **rdata\_pointA** - Keep track of where we are in the data stream. This is used to check the incoming data

## 5.75 SD card using FAT file system (sd\_card)

This example application demonstrates reading a file system from an SD card. It makes use of FatFs, a FAT file system driver.

For additional details about FatFs, see the following site: [http://elm-chan.org/fsw/ff/00index\\_e.html](http://elm-chan.org/fsw/ff/00index_e.html)

The application may be operated via a serial terminal attached to UART0. The RS232 communication parameters should be set to 115,200 bits per second, and 8-n-1 mode. When the program is started a message will be printed to the terminal. Type "help" for command help.

## 5.76 SDFM Filter Sync CLA

In this example, SDFM filter data is read by CLA in Cla1Task1. The SDFM configuration is shown below:

- SDFM1 used in this example
- MODE0 Input control mode selected

- Comparator settings
  - Sinc3 filter selected
  - OSR = 32
  - HLT = 0x7FFF (Higher threshold setting)
  - LLT = 0x0000(Lower threshold setting)
- Data filter settings
  - All the 4 filter modules enabled
  - Sinc3 filter selected
  - OSR = 256
  - All the 4 filters are synchronized by using MFE (Master Filter enable bit)
  - Filter output represented in 16 bit format
  - In order to convert 25 bit Data filter into 16 bit format user needs to right shift by 9 bits for Sinc3 filter with OSR = 256
- Interrupt module settings for SDFM filter
  - All the 4 higher threshold comparator interrupts disabled
  - All the 4 lower threshold comparator interrupts disabled
  - All the 4 modulator failure interrupts disabled
  - All the 4 filter will generate interrupt when a new filter data is available

#### External Connections

- SDFM\_PIN\_MUX\_OPTION1 Connect Sigma-Delta streams to (SD-D1, SD-C1 to SD-D8,SD-C8) on GPIO16-GPIO31
- SDFM\_PIN\_MUX\_OPTION2 Connect Sigma-Delta streams to (SD-D1, SD-C1 to SD-D8,SD-C8) on GPIO48-GPIO63
- SDFM\_PIN\_MUX\_OPTION3 Connect Sigma-Delta streams to (SD-D1, SD-C1 to SD-D8,SD-C8) on GPIO122-GPIO137

## 5.77 SDFM Filter Sync CPU

In this example, SDFM filter data is read by CPU in SDFM ISR routine. The SDFM configuration is shown below:

- SDFM used in this example - SDFM1
- Input control mode selected - MODE0
- Comparator settings
  - Sinc3 filter selected
  - OSR = 32
  - HLT = 0x7FFF (Higher threshold setting)
  - LLT = 0x0000(Lower threshold setting)
- Data filter settings
  - All the 4 filter modules enabled
  - Sinc3 filter selected
  - OSR = 256

- All the 4 filters are synchronized by using MFE (Master Filter enable bit)
- Filter output represented in 16 bit format
- In order to convert 25 bit Data filter into 16 bit format user needs to right shift by 9 bits for Sinc3 filter with OSR = 256

Interrupt module settings for SDFM filter

- All the 4 higher threshold comparator interrupts disabled
- All the 4 lower threshold comparator interrupts disabled
- All the 4 modulator failure interrupts disabled
- All the 4 filter will generate interrupt when a new filter data is available.

## 5.78 SDFM Filter Sync DMA

In this example, SDFM filter data is read by DMA. The SDFM configuration is shown below:

- SDFM1 used in this example
- MODE0 Input control mode selected
- Comparator settings
  - Sinc3 filter selected
  - OSR = 32
  - HLT = 0x7FFF (Higher threshold setting)
  - LLT = 0x0000 (Lower threshold setting)
- Data filter settings
  - All the 4 filter modules enabled
  - Sinc3 filter selected
  - OSR = 256
  - All the 4 filters are synchronized by using MFE (Master Filter enable bit)
  - Filter output represented in 16 bit format
  - In order to convert 25 bit Data filter into 16 bit format user needs to right shift by 9 bits for Sinc3 filter with OSR = 256
- Interrupt module settings for SDFM filter
  - All the 4 higher threshold comparator interrupts disabled
  - All the 4 lower threshold comparator interrupts disabled
  - All the 4 modulator failure interrupts disabled
  - All the 4 filter will generate interrupt when a new filter data is available

## 5.79 SDFM PWM Sync

In this example, SDFM filter data is read by CPU in SDFM ISR routine. The SDFM configuration is shown below:

- SDFM1 is used in this example

- MODE0 Input control mode selected
- Comparator settings
  - Sinc3 filter selected
  - OSR = 32
  - HLT = 0x7FFF (Higher threshold setting)
  - LLT = 0x0000 (Lower threshold setting)

Data filter settings

- All the 4 filter modules enabled
- Sinc3 filter selected
- OSR = 256
- All the 4 filters are synchronized by using PWM (Master Filter enable bit)
- Filter output represented in 16 bit format
- In order to convert 25 bit Data filter into 16 bit format user needs to right shift by 9 bits for Sinc3 filter with OSR = 256
- Interrupt module settings for SDFM filter
  - All the 4 higher threshold comparator interrupts disabled
  - All the 4 lower threshold comparator interrupts disabled
  - All the 4 modulator failure interrupts disabled
  - All the 4 filter will generate interrupt when a new filter data is available

## 5.80 Setup CPU01

This example gives control of all shared GPIOs and peripherals to CPU02

## 5.81 SPI Digital Loop Back (spi\_loopback)

This program uses the internal loop back test mode of the peripheral. Other than boot mode pin configuration, no other hardware configuration is required. Interrupts are not used.

A stream of data is sent and then compared to the received stream. The sent data looks like this:

0000 0001 0002 0003 0004 0005 0006 0007 .... FFFE FFFF

This pattern is repeated forever.

### Watch Variables

- **sdata** - sent data
- **rdata** - received data

## 5.82 SPI Digital Loop Back with DMA (spi\_loopback\_dma)

This program uses the internal loop back test mode of the peripheral. Other than boot mode pin configuration, no other hardware configuration is required. Both DMA Interrupts and the SPI FIFOs are used.

A stream of data is sent and then compared to the received stream. The sent data looks like this:

0000 0001

0001 0002

0002 0003

....

007E 007F

### Watch Variables

- **sdata** - Data to send
- **rdata** - Received data
- **rdata\_point** - Used to keep track of the last position in the receive stream for error checking

## 5.83 SPI Digital Loop Back with Interrupts (spi\_loopback\_interrupts)

This program uses the internal loop back test mode of the peripheral. Other than boot mode pin configuration, no other hardware configuration is required. Both interrupts and the SPI FIFOs are used.

A stream of data is sent and then compared to the received stream. The sent data looks like this:

0000 0001

0001 0002

0002 0003

....

FFFE FFFF

FFFF 0000

etc..

This pattern is repeated forever.

### Watch Variables

- **sdata** - Data to send
- **rdata** - Received data
- **rdata\_point** - Used to keep track of the last position in the receive stream for error checking



## 5.84 Software Prioritized Interrupts(`sw_prioritized_interrupts`)

For most applications, the hardware prioritizing of the the PIE module is sufficient. For applications that need custom prioritizing, this example illustrates how this can be done through software.

For more information on F2837xD interrupt priorities, refer to the "Example ISR Priorities" Appendix in the Firmware Development Users guide

This program simulates interrupt conflicts by writing to the PIEIFR registers. This will cause multiple interrupt requests to come into the PIE block at the same time.

The interrupt service routines are software prioritized as per the table found in the F2837xD\_SWPrioritizedIsrLevels.h file.

### Running the Application

1. Before compiling you must set the Global and Group interrupt priorities in the F2837xD\_SWPrioritizedIsrLevels.h file.
2. Select which test case you'd like to run with the `#define CASE` directive (1-9, default 1).
3. Compile the code, load, and run
4. At the end of each test there is a hard coded breakpoint (ESTOP0). When code stops at the breakpoint, examine the ISRTrace buffer to see the order in which the ISR's completed. All PIE interrupts will be added to the ISRTrace. The ISRTrace will consist of a list of hex values as shown:  
 0x00wx <- PIE Group w interrupt x finished first  
 0x00yz <- PIE Group y interrupt z finished next
5. If desired, set a new set of Global and Group interrupt priorities and repeat the test to see the change.

### Watch Variables

- **ISRTrace** - Trace of ISR's in the order they complete. After each test, examine this buffer to determine if the ISR's completed in the order desired.

## 5.85 LED Blink Getting Started Program (`timed_led_blink`)

This example configures CPU Timer0 for a 500 msec period, and toggles the GPIO34 LED once per interrupt. For testing purposes, this example also increments a counter each time the timer asserts an interrupt.

### Watch Variables

- `CpuTimer0.InterruptCount`

Monitor the GPIO34 LED blink on (for 500 msec) and off (for 500 msec) on the F2837xD control card.

## 5.86 Profiling $\sin(x)$ using the TMU (tmu\_sinegen)

In this example, we will use TMU intrinsics to calculate the sine for a series of per-unit arguments (the argument is not represented in radians, it is normalized to the range -1.0 to 1.0). We will profile the execution time of the TMU versus the conventional implementation in the run-time support library

$$\forall x \in [-2\pi, 2\pi], x_{pu} = \frac{x}{2\pi} \quad y = \sin(x_{pu} * 2\pi)$$

Instead of using intrinsics, the compiler can implement most of the RTS trigonometric functions through TMU instructions if the option *fp\_mode* is set to *relaxed*. In this example, this option is left untouched; it defaults to the *strict* mode.

### Watch Variables

- timeRTS - time to run RTS routine
- timeTMU - time to run TMU routine

## 5.87 UPP Single Data Rate Receive (upp\_sdr\_rx)

This example sets up the F2837xD board's UPP with the single-data-rate(SDR) interface as a receiver.

**Important:** In order to run this example, two F2837xD boards are required. All the UPP pins from one board to the other must be connected with common ground. One board must be loaded with this example code and the other board must be loaded with the "upp\_sdr\_tx" example.

**Instructions:** # Load the "upp\_sdr\_tx" on board 1 # Load the "upp\_sdr\_rx" on board 2 # Run the "upp\_sdr\_rx" code on board 2 (Needs to be run before the tx code) # Run the "upp\_sdr\_tx" code on board 1

### Watch Variables:

- **TEST\_STATUS** - Equivalent to **TEST\_PASS** if test finished correctly, else the value is set to **TEST\_FAIL**
- **ErrCount** - Error counter

## 5.88 UPP Single Data Rate Transmit (upp\_sdr\_tx)

This example sets up the F2837xD board's UPP with the single-data-rate(SDR) interface as a transmitter.

**Important:** In order to run this example, two F2837xD boards are required. All the UPP pins from one board to the other must be connected with common ground. One board must be loaded with this example code and the other board must be loaded with the "upp\_sdr\_rx" example.

**Instructions:** # Load the "upp\_sdr\_tx" on board 1 # Load the "upp\_sdr\_rx" on board 2 # Run the "upp\_sdr\_rx" code on board 2 (Needs to be run before the tx code) # Run the "upp\_sdr\_tx" code on board 1

### Watch Variables:

- **TEST\_STATUS** - Equivalent to **TEST\_PASS** if test finished correctly, else the value is set to **TEST\_FAIL**
- **ErrCount** - Error counter

## 5.89 USB Generic Bulk Device (**usb\_dev\_bulk**)

This example provides a generic USB device offering simple bulk data transfer to and from the host. The device uses a vendor-specific class ID and supports a single bulk IN endpoint and a single bulk OUT endpoint. Data received from the host is assumed to be ASCII text and it is echoed back with the case of all alphabetic characters swapped.

UART0, connected to the FTDI virtual COM port and running at 115,200, 8-N-1, is used to display messages from this application.

A Windows INF file for the device is provided in ControlSUITE. This INF contains information required to install the WinUSB subsystem on WindowsXP and Windows 7. WinUSB is a Windows subsystem allowing user mode applications to access the USB device without the need for a vendor-specific kernel mode driver.

A sample Windows command-line application, **usb\_bulk\_example**, illustrating how to connect to and communicate with the bulk device is also provided. Project files are included to allow the examples to be built using Microsoft VisualStudio. Source code for this application can be found in directory **F2837xD\_common/tools/usb\_bulk\_example/Release**.

## 5.90 USB HID Keyboard Device (**usb\_dev\_keyboard**)

This example application turns the evaluation board into a USB keyboard supporting the Human Interface Device class. When GPIO0 is pulled high, a sequence of key presses is simulated to type a string. Care should be taken to ensure that the active window can safely receive the text; enter is not pressed at any point so no actions are attempted by the host if a terminal window is used (for example). The LED2 is used to indicate the current Caps Lock state and is updated in response to any other keyboard attached to the same USB host system.

The device implemented by this application also supports USB remote wakeup allowing it to request the host to reactivate a suspended bus. If the bus is suspended (as indicated on the application display), toggling GPIO0 will request a remote wakeup assuming the host has not specifically disabled such requests.

To run the example compile the project, load to the target, and run the example. After the example is running, connect a USB cable from the PC to the microUSB port on the controlCARD. Then toggle GPIO0 while the PC's window focus is in a window that can receive keyboard input (i.e. Notepad).

## 5.91 USB HID Mouse Device (**usb\_dev\_mouse**)

This example application turns the evaluation board into a USB mouse supporting the Human Interface Device class. After loading and running the example simply connect the PC to the controlCARDs microUSB port using a USB cable, and the mouse pointer will move in a square pattern for the duration of the time it is plugged in.

UART0, connected to the FTDI virtual COM port and running at 115,200, 8-N-1, is used to display messages from this application.

## 5.92 USB Serial Device (usb\_dev\_serial)

This example application turns the evaluation kit into a virtual serial port when connected to the USB host system. The application supports the USB Communication Device Class, Abstract Control Model to redirect UART0 traffic to and from the USB host system.

Connect USB cables from your PC to both the mini and microUSB connectors on the controlCARD. Figure out what COM ports your controlCARD is enumerating (typically done using Device Manager in Windows) and open a serial terminal to each of with the settings 115200 Baud 8-N-1. Characters typed in one terminal should be echoed in the other and vice versa.

Assuming you installed controlSUITE in the default directory, a driver information (INF) file for use with Windows XP and Windows 7 can be found in C:/ti/controlSUITE/F2837xD/VERSION/F2837xD\_common/windows\_drivers.

## 5.93 USB Dual Detect (usb\_dual\_detect)

This program uses a GPIO to do ID detection. If a host is connected to the device's USB port, the stack will switch to device mode and enumerate as mouse. If a mouse device is connected to the device's USB port, the stack will switch to host mode and display the mouse's movement and button press information in a serial terminal.

## 5.94 USB HID Keyboard Host (usb\_host\_keyboard)

This example application demonstrates how to support a USB keyboard attached to the evaluation kit board. The display will show if a keyboard is currently connected and the current state of the Caps Lock key on the keyboard that is connected on the bottom status area of the screen. Pressing any keys on the keyboard will cause them to be sent out the UART at 115200 baud with no parity, 8 bits and 1 stop bit. Any keyboard that supports the USB HID BIOS protocol should work with this demo application.

To run the example you should connect a HID compliant keyboard to the microUSB port on the top of the controlCARD and open up a serial terminal with the above settings to view the characters typed on the keyboard.

## 5.95 USB HID Mouse Host (usb\_host\_mouse)

This application demonstrates the handling of a USB mouse attached to the evaluation kit. Once attached, the position of the mouse pointer and the state of the mouse buttons are output to the display.

The first UART, which is connected to the FTDI virtual serial port on the controlCARD board, is configured for 115,200 bits per second, and 8-N-1 mode. When a HID compliant mouse is connected to the microUSB port on the top of the controlCARD, position and button information will be displayed to the console.

## 5.96 USB Mass Storage Class Host (usb\_host\_msc)

This example application demonstrates reading a file system from a USB mass storage class device. It makes use of FatFs, a FAT file system driver. It provides a simple command console via the UART for issuing commands to view and navigate the file system on the mass storage device.

The first UART, which is connected to the FTDI virtual serial port on the controlCARD board, is configured for 115,200 bits per second, and 8-N-1 mode. When the program is started a message will be printed to the terminal. Type "help" for command help.

After loading and running the example, open a serial terminal with the above settings to open the command prompt. Then connect a USB MSC device to the microUSB port on the top of the controlCARD.

For additional details about FatFs, see the following site: [http://elm-chan.org/fsw/ff/00index\\_e.html](http://elm-chan.org/fsw/ff/00index_e.html)

## 5.97 Watchdog

This example shows how to service the watchdog or generate a wakeup interrupt using the watchdog. By default the example will generate a Wake interrupt. To service the watchdog and not generate the interrupt uncomment the ServiceDog() line the the main for loop.



## 6 Dual Core Example Applications

These example applications show how to make use of F2837xD device functions which span both the CPU 1 and CPU 2. All of these examples contain two example projects: one for CPU 1 and one for CPU 2.

Like the CPU1 only projects, these projects also contain different build configurations for RAM and Flash builds. All of the CPU1 projects contain RAM and Flash build configurations with debugger support, as well as a standalone flash build configuration which sends an IPC command to boot the second core and begin executing the application in its flash. The CPU2 projects all only contain a flash and RAM build configuration as there are no dependencies in the code regarding whether the application is running with or without a debugger.

To run one of these examples after compiling it, load the appropriate programs on each of the two cores. Then, for more example specific instructions please refer to the documentation regarding the example you wish to run on the following pages or in the comments of the example sources.

All of these examples can be found in the

`device_support/F2837xD/<Version>/F2837xD_examples_Dual` subdirectory of the ControlSUITE package.

### 6.1 ADC & EPWM on CPU2

This example demonstrates how to make use of the ADC and EPWM peripherals from CPU2. Device clocking (PLL) and GPIO setup are done using CPU1, while all other configuration of the peripherals is done using CPU2.

CPU2 configures EPWM1 in up count mode in a similar fashion to what is done in the `epwm_up_aq` example. The ADC is configured in continuous conversion mode similar to the `adc_soc_continuous` example. GPIO0 can be connected to ADCINA0 and the results buffer `AdcaResults` graphed in CCS to view the duty cycle of the generated waveform.

### 6.2 Blinky

Dual Core Blinky Example. This example demonstrates how to implement and run a standalone application on both cores.

### 6.3 CLA $\arcsine(x)$ using a lookup table (`cla_asin_cpu01`)

In this example, `cpu1` will be used to initialize the clocks for `cpu2.cla1`. Task 1 of the CLA on `cpu2` will calculate the arcsine of an input argument in the range (-1.0 to 1.0) using a lookup table.

#### Memory Allocation

- CLA1 Math Tables (RAMLS0)
  - CLAasinTable - Lookup table

- CLA1 to CPU Message RAM
  - fResult - Result of the lookup algorithm
- CPU to CLA1 Message RAM
  - fVal - Sample input to the lookup algorithm

#### Watch Variables

- fVal - Argument to task 1
- fResult - Result of  $\arcsin(fVal)$

#### Note:

CPU2 must turn on the CLA clock by writing a 1 to CpuSysRegs.PCLKCR0.bit.CLA1.

## 6.4 CLA 2 Pole 2 Zero Infinite Impulse Response Filter (cla\_iir2p2z\_cpu01)

This example implements a Transposed Direct Form II IIR filter, commonly known as a Biquad. The input vector is a software simulated noisy signal that is fed to the biquad one sample at a time, filtered and then stored in an output buffer for storage.

#### Memory Allocation

- CLA1 Data RAM 1 (RAML2)
  - S1\_A - Feedback coefficients
  - S1\_B - Feedforward coefficients
- CLA1 to CPU Message RAM
  - yn - Output of the Biquad
- CPU to CLA1 Message RAM
  - xn - Sample input to the filter

#### Watch Variables

- fBiquadOutput
- pass
- fail

#### Note:

CPU2 must turn on the CLA clock by writing a 1 to CpuSysRegs.PCLKCR0.bit.CLA1.

## 6.5 CPU01 to CPU02 IPC Driver

This example tests all of the basic read/write CPU01 to CPU02 IPC Driver functions available in F2837xD\_ipc\_Driver.c. The CPU01 project sends commands to the CPU02 project, which then processes the commands. The CPU02 project responds to the commands sent from the CPU01 project. Note that IPC INT0 and IPC INT1 are used for this example to process IPC commands.

#### Watch Variables for CPU01 :



- ErrorCount - Counts # of errors
- pusCPU01BufferPt - Stores 256 16-bit words block to write to CPU02
- pusCPU02BufferPt - Points to beginning of 256 word block received back from CPU02
- usWWord16 - 16-bit word to write to CPU02
- ulWWord32 - 32-bit word to write to CPU02
- usRWord16 - 16-bit word to read from CPU02
- ulRWord32 - 32-bit word to read from CPU02

**Watch Variables for CPU02 :**

- ErrorFlag - Indicates an unrecognized command was sent from CPU01 to CPU02.

## 6.6 CPU01 to CPU02 IPC Lite Drivers (cpu01\_to\_cpu2\_ipcdrivers\_lite)

This example application demonstrates the use of the CPU01 to CPU02 IPC Lite Driver Functions which allow the CPU01 to read/write to addresses on the CPU02. CPU02 to CPU01 MSG RAM is used to pass the addresses of local variables between the processors.

**Watch Variables on CPU01:**

- ErrorCount - Counts # of errors
- usWWord16 - 16-bit word to write to CPU02
- ulWWord32 - 32-bit word to write to CPU02
- usRWord16 - 16-bit word to read from CPU02
- ulRWord32 - 32-bit word to read from CPU02

**Watch Variables on CPU02:**

- ErrorFlag - Indicates an unrecognized command was sent from CPU01 to CPU02.

## 6.7 CPU01 to CPU02 IPC Write Protect Driver

This example tests all of the basic read/write CPU01 to CPU02 IPC Write Protect Driver functions available in F2837xD\_Ipc\_Driver.c. The CPU01 project sends commands to the CPU02 project, which then processes the commands. The CPU02 project responds to the commands sent from the CPU01 project. Note that IPC INT0 and IPC INT1 are used for this example to process IPC commands.

**Watch Variables for CPU01 :**

- ErrorCount - Counts # of errors
- ulCPU01Buffer - Stores 4 32-bit words block to write to CPU02
- pulCPU01BufferPt - Points to beginning of 256 word block received back from CPU02

- usWWord16 - 16-bit word to write to CPU02
- ulWWord32 - 32-bit word to write to CPU02
- usRWord16 - 16-bit word to read from CPU02
- ulRWord32 - 32-bit word to read from CPU02

**Watch Variables for CPU02 :**

- ErrorFlag - Indicates an unrecognized command was sent from CPU01 to CPU02.

## 6.8 CPU02 to CPU01 IPC Driver

This example tests all of the basic read/write CPU02 to CPU01 IPC Driver functions available in F2837xD\_ipc\_Driver.c. The CPU02 project sends commands to the CPU01 project, which then processes the commands. The CPU01 project responds to the commands sent from the CPU02 project. Note that IPC INT0 and IPC INT1 are used for this example to process IPC commands.

**Watch Variables for CPU02 :**

- ErrorCount - Counts # of errors
- usCPU02Buffer - Stores 256 16-bit words block to write to CPU01
- pusCPU01BufferPt - Points to beginning of 256 word block received back from CPU01
- usWWord16 - 16-bit word to write to CPU01
- ulWWord32 - 32-bit word to write to CPU01
- usRWord16 - 16-bit word to read from CPU01
- ulRWord32 - 32-bit word to read from CPU01

**Watch Variables for CPU01 :**

- ErrorFlag - Indicates an unrecognized command was sent from CPU02 to CPU01.

## 6.9 CPU02 to CPU01 IPC Lite Drivers (cpu02\_to\_cpu1\_ipcdrivers\_lite)

This example application demonstrates the use of CPU02 to CPU01 IPC Lite Driver Functions which allow the CPU02 to read/write to addresses on the CPU01. CPU01toCPU02 MSG RAM is used to pass the addresses of local variables between the processors.

**Watch Variables for CPU02:**

- ErrorCount - Counts # of errors
- usWWord16 - 16-bit word to write to CPU01
- ulWWord32 - 32-bit word to write to CPU01
- usRWord16 - 16-bit word to read from CPU01
- ulRWord32 - 32-bit word to read from CPU01

**Watch Variables for CPU01 :**

- ErrorFlag - Indicates an unrecognized command was sent from CPU02 to CPU01.

## 6.10 CPU02 to CPU01 IPC Write Protect Driver

This example tests all of the basic read/write CPU02 to CPU01 IPC Write Protect Driver functions available in F2837xD\_Ipc\_Driver.c. The CPU02 project sends commands to the CPU01 project, which then processes the commands.

The CPU01 project responds to the commands sent from the CPU02 project. Note that IPC INT0 and IPC INT1 are used for this example to process IPC commands.

**Watch Variables for CPU02 :**

- ErrorCount - Counts # of errors
- ulCPU02Buffer - Stores 4 32-bit words block to write to CPU01
- pulCPU01BufferPt - Points to beginning of 256 word block received back from CPU01
- usWWord16 - 16-bit word to write to CPU01
- ulWWord32 - 32-bit word to write to CPU01
- usRWord16 - 16-bit word to read from CPU01
- ulRWord32 - 32-bit word to read from CPU01

**Watch Variables for CPU01 :**

- ErrorFlag - Indicates an unrecognized command was sent from CPU01 to CPU02.

## 6.11 DMA Transfer Shared Peripheral

This example shows how to initiate a DMA transfer on CPU1 from a shared peripheral which is owned by CPU2. In this specific example, a timer ISR is used on CPU2 to initiate a SPI transfer which will trigger the CPU1 DMA. CPU1's DMA will then in turn update the EPWM1 CMPA value for the PWM which it owns. The PWM output can be observed on the GPIO pins configured in the InitEPwm1Gpio() function.

**Watch Pins**

- GPIO0 and GPIO1 - ePWM output can be viewed with oscilloscope

## 6.12 Flash Programming Solution SCI for Single or Dual Core

In this example, we set up a UART connection with a host using SCI, receive commands for CPU1 to perform which then sends ACK, NAK, and status packets back to the host after receiving and

completing the tasks. This kernel has the ability to program, verify, unlock, reset, run, and boot CPU2 to SCI boot loader. Each command either expects no data from the command packet or specific data relative to the command.

In this example, we set up a UART connection with a host using SCI, receive an application for CPU01 in -sci8 ascii format to run on the device and program it into Flash.

## 6.13 Firmware Upgrade Kernels using USB for Single or Dual Upgrade

### Build Configuration: DUAL

In this example, we set up a USB connection with a host, receive a binary application for CPU01 in sci8 format to run on the device and program it into Flash. Then CPU01 receives a CPU02 kernel and loads that into Shared RAM. This kernel should be linked to run from RAMGS2 and RAMGS3. CPU01 then boots CPU02 with an IPC message and tells it to branch to address \$0x0000E000\$. CPU01 continues to receive another binary application to be run in CPU02 Flash and it transmits the binary application to CPU02 through IPC. CPU02 reads the application from IPC and programs it into Flash. After CPU01 and CPU02 complete, they both branch to their respective applications programmed in their respective Flash Banks.

### Build Configuration: CPU01\_RAM

In this example, we set up a USB connection with a host, receive a binary application for CPU01 in hex boot format to run on the device and program it into Flash.

## 6.14 Flash Programming

This example demonstrates F021 Flash API usage.

## 6.15 IPC GPIO toggle

This example shows GPIO input on the local CPU triggering an output on the remote CPU. A GPIO input change on CPU01 causes an output change on CPU02 and vice versa.

CPU1 has control of GPIO31, GPIO15 and GPIO14.

CPU2 has control of GPIO34, GPIO12 and GPIO11.

### Hardware Connections

- connect GPIO15 to GPIO11
- connect GPIO14 to GPIO12

### Watch Pins

- GPIO31 - output on CPU2 (LED blinking if using control card)
- GPIO11 - input on CPU2

- GPIO34 - output on CPU1 (LED blinking if using control card)
- GPIO14 - input on CPU1
- GPIO12 - square wave output on CPU02
- GPIO15 - square wave output on CPU01

## 6.16 Shared RAM management (RAM\_management)

This example shows how to assign shared RAM for use by both the CPU02 and CPU01 core. Shared RAM regions are defined in both the CPU02 and CPU01 linker files. In this example GS0 and GS14 are assigned to/owned by CPU02. The remaining shared RAM regions are owned by CPU01. In this example:

A pattern is written to c1\_r\_w\_array and then IPC flag is sent to notify CPU02 that data is ready to be read. CPU02 then reads the data from c2\_r\_array and writes a modified pattern to c2\_r\_w\_array. Once CPU02 acknowledges the IPC flag to , CPU01 reads the data from c1\_r\_array and compares with expected result.

A Timed ISR is also serviced in both CPUs. The ISRs are copied into the shared RAM region owned by the respective CPUs. Each ISR toggles a GPIO. Watch GPIO31 and GPIO34 on oscilloscope. If using the control card watch LED1 and LED2 blink at different rates.

- c1\_r\_w\_array[] is mapped to shared RAM GS1
- c1\_r\_array[] is mapped to shared RAM GS0
- c2\_r\_array[] is mapped to shared RAM GS1
- c2\_r\_w\_array[] is mapped to shared RAM GS0
- cpu\_timer0\_isr in CPU02 is copied to shared RAM GS14 , toggles GPIO31
- cpu\_timer0\_isr in CPU01 is copied to shared RAM GS15 , toggles GPIO34

### Watch Variables

- error Indicates that the data written is not correctly received by the other CPU.

## 6.17 SDFM Filter Sync CLA

In this example, SDFM filter data is read by CPU-1 CLA in Cla1Task1. The CPU-2 CLA is also initialized for demonstration purposes and can be setup to interface with SDFM.

The SDFM configuration is shown below:

- SDFM1 used in this example
- MODE0 Input control mode selected
- Comparator settings
  - Sinc3 filter selected
  - OSR = 32
  - HLT = 0x7FFF (Higher threshold setting)
  - LLT = 0x0000(Lower threshold setting)

- Data filter settings
  - All the 4 filter modules enabled
  - Sinc3 filter selected
  - OSR = 256
  - All the 4 filters are synchronized by using MFE (Master Filter enable bit)
  - Filter output represented in 16 bit format
  - In order to convert 25 bit Data filter into 16 bit format user needs to right shift by 9 bits for Sinc3 filter with OSR = 256
- Interrupt module settings for SDFM filter
  - All the 4 higher threshold comparator interrupts disabled
  - All the 4 lower threshold comparator interrupts disabled
  - All the 4 modulator failure interrupts disabled
  - All the 4 filter will generate interrupt when a new filter data is available

### External Connections

- SDFM\_PIN\_MUX\_OPTION1 Connect Sigma-Delta streams to (SD-D1, SD-C1 to SD-D8,SD-C8) on GPIO16-GPIO31
- SDFM\_PIN\_MUX\_OPTION2 Connect Sigma-Delta streams to (SD-D1, SD-C1 to SD-D8,SD-C8) on GPIO48-GPIO63
- SDFM\_PIN\_MUX\_OPTION3 Connect Sigma-Delta streams to (SD-D1, SD-C1 to SD-D8,SD-C8) on GPIO122-GPIO137



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