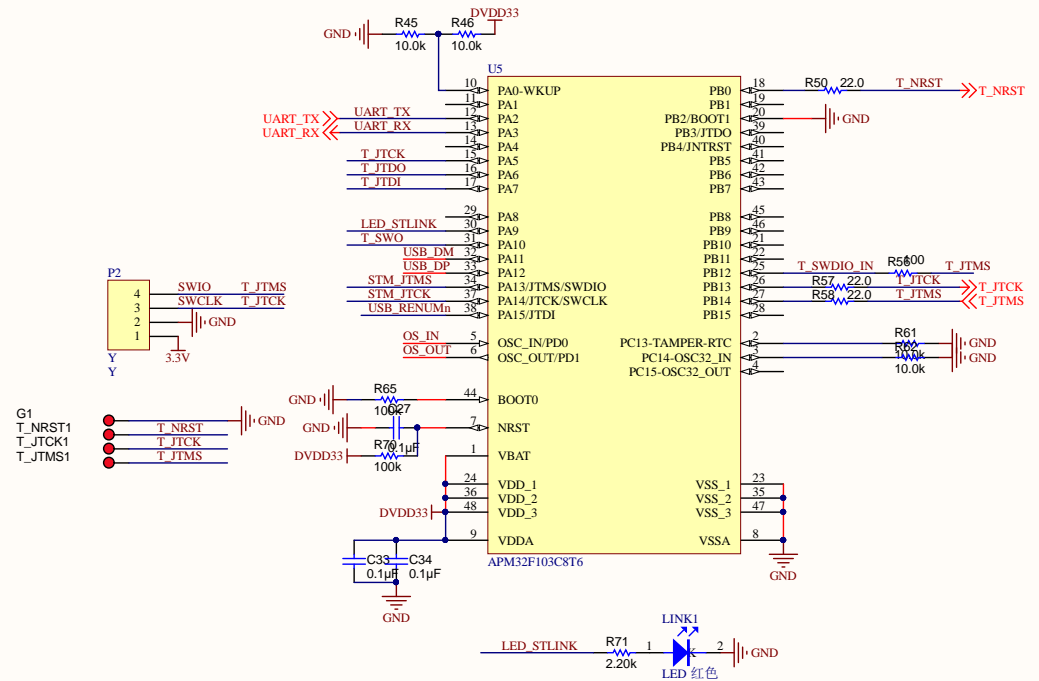
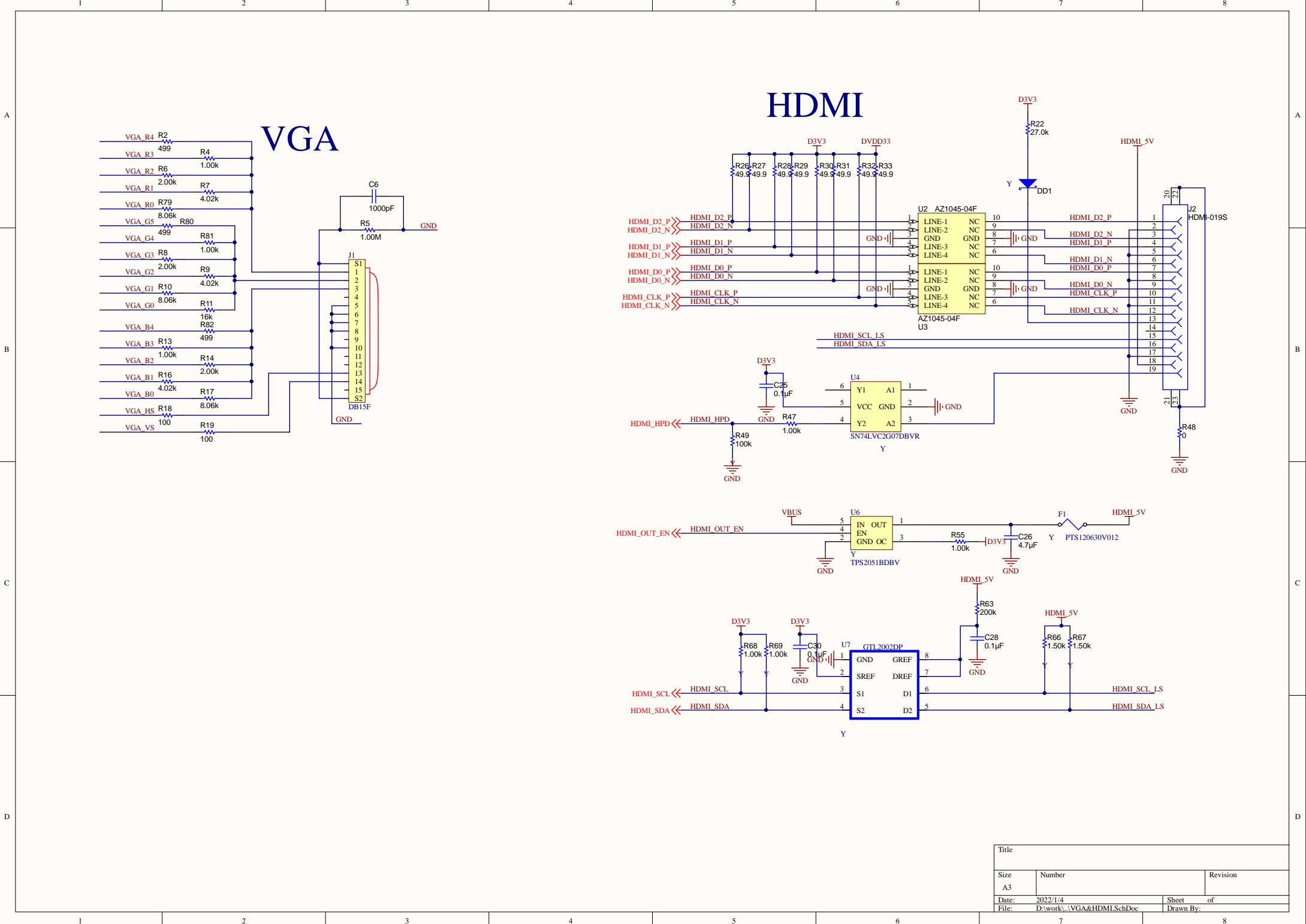
[illegible]

Title			
Size A3	Number		Revision
Date:	2022/1/4	Sheet	of
File:	D:\work\...SD&DAP.SchDoc	Drawn By:	



Title		
Size	Number	Revision
A3		
Date:	2022/1/4	Sheet of
File:	D:\work\...\VGA&HDMI.SchDoc	Drawn By:

A

B

C

D

A

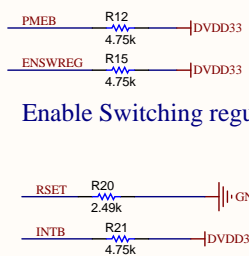
B

C

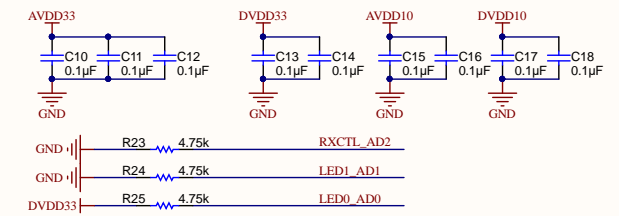
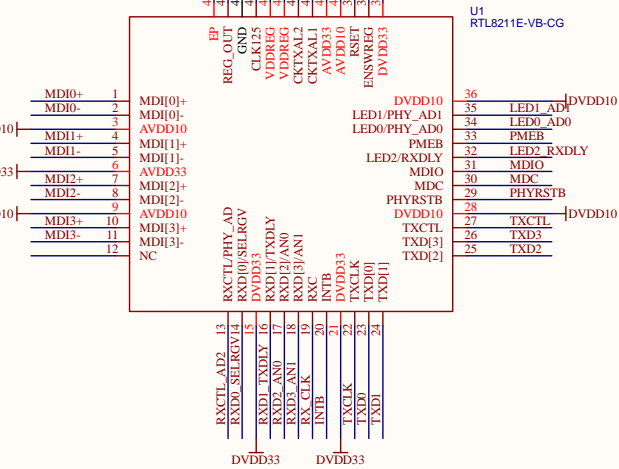
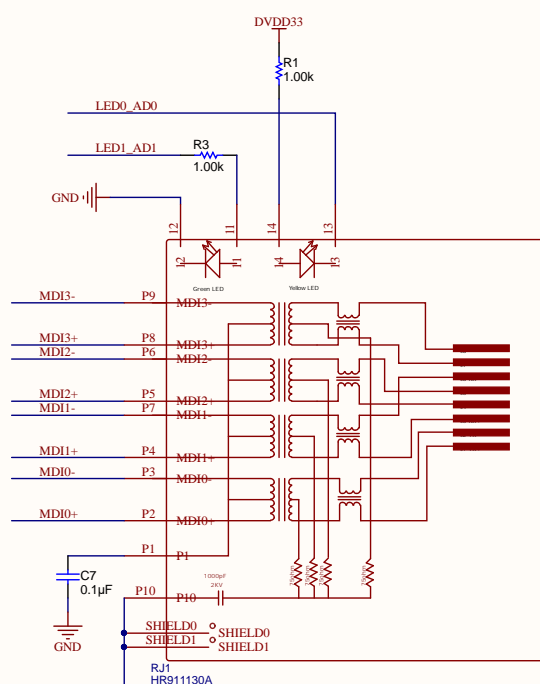
D



网口



Enable Switching regulator

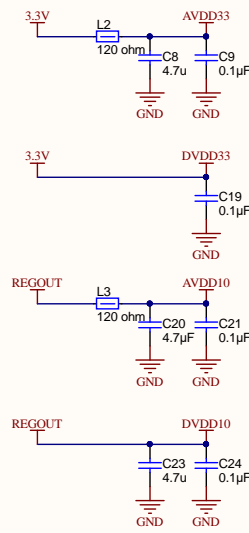
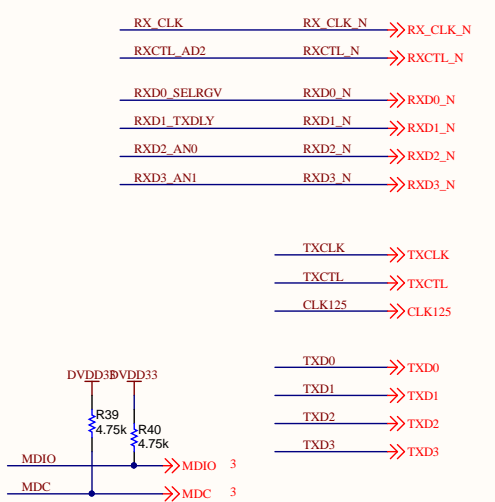


PHY Address=001

RGMII

config for all capability

with TX/RX delay



Title		
Size	Number	Revision
A3		
Date:	2022/1/4	Sheet 1 of 1
File:	D:\work\2021\安路-IO扩展板(fpga)\展IO板\IO板Doc	