Zeren (George) Li

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Education

Purdue University

Master of Science in Electrical and Computer Engineering — August 2022 – May 2025

- Thesis: Cache side channel attacks on ARM-based mobile device

Bachelor of Science in Computer Engineering — August 2018 – May 2022

- Major: Computer Engineering

Project

Multicore Processor Design and Prototyping

- Designed and implemented a single-cycle CPU that supports the MIPS instruction set and operates at a frequency of 35 MHz on a FPGA board.
- Designed and implemented a 60 MHz dual-core MIPS CPU with a five-stage pipeline on an FPGA board. This CPU handles common data and structural hazards, features L1 cache support for both instructions and data, utilizes MSI-based cache coherence, supports LL/SC instructions for data synchronization between the two cores, and incorporates a 2-bit predictor and a branch target buffer to mitigate control hazards by 15%.

ASIC Design

- Designed RTL diagrams for UART Receiver module and APB-Slave interface module. Implemented and integrated APB-Slave interface module and UART Receiver module.
- Designed RTL diagrams for USB receiver, transmitter, and AHB-Lite module. Implemented USB receiver with the AHB-Lite module using System Verilog
- Developed verification test benches for all aforementioned modules.

Gimbal Vehicle

- Utilized STM32F091 and STM32F446 to design and construct a wireless controller and a gimbal-mounted vehicle. The controller manages both the vehicle and the gimbal.
- Extracted data from four Mecanum wheel's hall sensors to devise algorithms facilitating omnidirectional movement.
- Harnessed data from the MPU6050 Accelerometer Gyroscope Module in conjunction with the Kalman filter algorithm, ensuring the gimbal's horizontal and vertical stability irrespective of the chassis's orientation, with a margin of error for angles of less than 3 degrees.

Z-cache Replication

- Utilized the Gem5 simulator to implement and evaluate Z-cache, with a specific focus on analyzing L2 cache misses across the SPEC2017 benchmark. Conducted a comparative analysis of three cache management techniques: 4-way associative cache, skewed-associative cache, and Z-cache. All techniques were implemented on the TimingSimple CPU model to minimize complexities typically introduced by more advanced CPU models.

Experience

Embedded System Course Graduate Teaching Assistance — January 2023 - Current

- Oversaw two lab sessions for an Embedded Systems class, assisting 50+ students. Supervised a team of eight undergraduate teaching assistants. Fielded student inquiries on topics including ARM assembly language, STM32F091 microcontroller programming, and embedded systems protocols.

Computer Vision for Forest Inventory Analysis (CVFIA) — August 2020 – August 2021

- Utilized C++ to create user-friendly maps from point clouds and standard maps within an experimental forest. Integrated GPS coordinates from the experimental forest into stereo cameras to improve the precision of trees placements on stand maps.

Leadership

ECE 47700 Senior Design - Team leader

- Managed progress reports of the project, maintained the project webpage, and organized team meetings. Assisted teammates with technical challenges related to STM32, peripheral components, and system algorithms.

Skills & Abilities

Programming and Development Tool

- C/C++, Java, Python, MATLAB, ARM Assembly, SystemVerilog, Pawn (scripting language for GoldSrc), Cuda(C++)
- Git, Makefile, Shell Script, Android Studio, QuestaSim, STM32Cube IDE, Gem5, GPGPU-Sim, Ghidra, Clang
- I2C, SPI, UART/USART, TCP/IP, MSI, PWM

Languages

- Chinese (Native), English (Proficient)

Courses

Purdue university

Microprocessor Systems and Interfacing, Data Structures, Object-Oriented Programming with Java, Introduction to Artificial Intelligence, Operating Systems Engineering, Compilers And Translator Writing Systems, Computer and Network security, Discrete Math, ASIC Design, Advanced Software Engineering, Computer Design and Prototyping, Computer Network System, Computer Architecture, Programmable Accelerator Architectures.