Optoelectronic Memristor Model for Optical Synaptic Circuit of Spiking Neural Networks

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***Abstract*—Optoelectronic memristors are suitable candidates for hardware implementation of optical synapses in spiking neural networks (SNNs), thanks to their electrical and optical characteristics. To study the feasibility of memristor-based optical synapses in SNNs, a behavior model for optoelectronic memristors is proposed in this paper, including electrical programming modeling and photocurrent read modeling. Based on the model, the behavior of a molecular ferroelectric (MF)/semiconductor interfacial memristor is simulated. This paper also proposes an optical synaptic circuit for trace-based spike-timing-dependent plasticity (STDP) learning rule. The electrical characteristics of the memristor are explored and exploited to emulate the trace in the pairwise nearest-neighbor STDP, while the optical characteristics are utilized for non-destructive readout and weight calculation. Synaptic-level simulation results show a 99.96% correlation coefficient (CC) and a 1.91% relative root mean square error (RRMSE) in the weight approximate computation. Extending the simulation to the network level, the optoelectronic memristor-based unsupervised STDP learning system can achieve a 92.07±0.64% accuracy on the MNIST benchmark.**

***Index Terms*—Optoelectric memristor, memristor model, optical synapse, trace dynamics, STDP learning rule**

I. Introduction

Unlike purely electronic memristors, optoelectronic memristive devices have both electrical and optical synaptic characteristics. Responding to electric and light pulses, optoelectronic memristors are equipped with photocurrent readout or even optical resistive switching modulation functionalities [1]. Mimicking the human brain and visual system, the optoelectronic memristors-based neuromorphic computing paradigm provides a promising path for the high-speed and low-power implementation of spiking neural networks (SNNs).

Inspired by the information processing mechanism in biology, SNN exhibits great potential not only in brain-like cognitive functions such as working memory [2], but also in real-world applications including target tracking [3], optical flow estimation [4] and ECG classification [5]. Spike-timing-dependent plasticity (STDP) is one of the most widely-used unsupervised learning methods in SNNs. Among all the variants of unsupervised STDP learning rules, the trace-based approach captures the pre- and post-synaptic spatiotemporal dynamics, which is biologically plausible and can achieve better performance in classification tasks compared to non-exponential counterparts [6]–[9].

A lot of progress has been made in the memristor-based implementation of the trace-based STDP learning system to reduce the high data movement cost and high computational intensity of the key trace computation [10], [11]. However, in the electrical memristor-based implementations, the frequent readout operations in the trace-based STDP learning system introduce unwanted variations [12], [13] and may harm the stability and performance of the system. The unique electronic and optical characteristics of some optoelectronic memristors [14] make them a promising solution to achieve non-destructive readout operations.

Advances have been achieved in optoelectronic memristors and their application in artificial neural networks (ANNs) [14]–[17]. However, optoelectronic memristor-based implementations are more limited in scale compared to their electronic counterparts, as the largest optoelectronic memristor crossbar currently implemented is a 32×32 array [17]. In addition, there are few behavioral models available to carry out large-scale optoelectronic memristor-based SNN learning system simulations.

This work focuses on the modeling of optoelectronic memristors, and proposes a non-destructive optical synaptic circuit to facilitate large-scale neuromorphic implementation of trace-based STDP learning system. The main contributions can be concluded as follows:

- An optoelectronic memristor model is proposed to simulate the electrical and optical characteristics of a bipolar ferroelectric synaptic device using a molecular ferroelectric (MF)/semiconductor interfacial memristor.
- An optical synaptic circuit for the trace-based STDP learning rule is proposed and simulated based on the model.
- The simulation is extended to the network level for digit classification. The feasibility of the optoelectronic memristor-based learning system is validated with 0.10% accuracy degradation on the MNIST benchmark.

* Jiawei Xu and Yi Zheng contributed equally to this work.

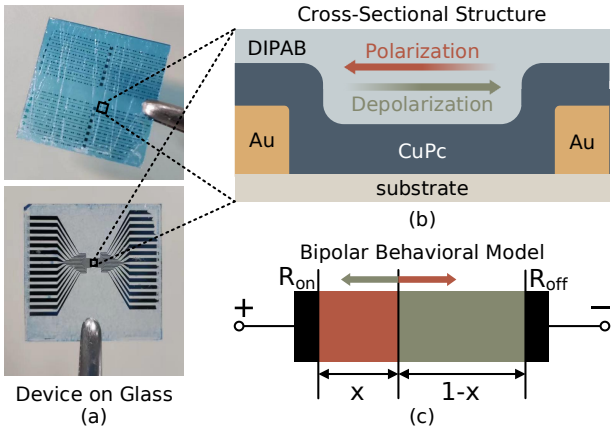


Fig. 1. The MF/semiconductor interfacial memristor. Photographs of the MF/CuPc devices on silicon oxide and PI substrates (a). The cross-sectional structure of the interfacial device (b). The conceptual diagram of the behavioral model for the device (c).

II. Optoelectronic Memristor

A. MF/Semiconductor Interfacial Memristor

Combining the high density of the electronic domain with the high speed and low energy consumption of the optical domain, optoelectronic memristors can play a leading role in future SNN circuitry. Some works fabricated optically-controlled optoelectronic memristors with optical programming and electrical readout [15]–[17]. This work focuses on electrical-programmed optoelectronic memristors with photocurrent readout functionalities.

The memristor used in this work is a MF/semiconductor interfacial memristor [14] with tunable depolarization fields and light sensitivity. As shown in Fig. 1, fabricated on multiple substrates including SiO_2/Si, the memristive device employs copper phthalocyanine (CuPc) films as the semiconductor layer, which is sandwiched between the electrodes and the MF layers consisting of diisopropylammonium bromide (DIPAB) films. The MF/CuPc interfaces present memristive behavior with a tunable horizontal conductive path. In addition, the introduction of semiconductor CuPc layers provides light sensitivity for optical signal input.

B. Electrical and Optical Characteristics

For electrical characteristics, the conductance/resistance of the MF/semiconductor interfacial memristor depends on the history of charge flux through the interface. Due to the ohmic and tunneling effect caused by the MF layer's field amplification effect, free charges are captured by the MF/semiconductor interface as compensation charges, which can contribute to the conductivity of the interface and exhibit resistive memory function at the same time [14].

For optical characteristics, photoresponse can be observed by applying a laser pulse to the CuPc layer after electrical poling. The photocurrent is generated in a self-powered way, presumably as the result of the stray fields at MF/CuPc interfaces caused by incomplete compensation of polarization. The photoresponsivity can be modulated by electrical stimuli in a nonlinear way, as shown in Fig. 2. The long retention time of the photoresposivity after poling is observed and will not be affected by the optical stimuli.

III. Optoelectronic Memristor Model

To facilitate the feasibility analysis of optoelectronic memristor-based synaptic circuits for the SNN learning system, a model is proposed to emulate the memristor behavior. The model consists of two key parts, including electrical programming modeling and photocurrent readout modeling.

A. Electrical Programming Modeling

Inspired by the widely-used VTEAM model for electronic memristors [18], the proposed optoelectronic memristor model is based on an expression of the derivative of an internal state variable. Here in the proposed model, the internal state variable $x(t)$ in the range [0, 1] reflects the polarization during the electrical stimulation phase, and is linearly mapped to the photoresponsivity of the optoelectronic memristor. Behaviorally, the electrical programming phase is represented by:

$$\frac{dx(t)}{dt} = \begin{cases} k_{\text{off}} \cdot (\frac{v(t)}{v_{\text{off}}} - 1)^{\alpha_{\text{off}}} \cdot f_{\text{off}}(x), & 0 < v_{\text{off}} < v \\ 0, & v_{\text{on}} < v < v_{\text{off}} \\ k_{\text{on}} \cdot (\frac{v(t)}{v_{\text{on}}} - 1)^{\alpha_{\text{on}}} \cdot f_{\text{on}}(x)), & v < v_{\text{on}} < 0 \end{cases} \tag{1}$$

where $v(t)$ is the device voltage of the optoelectronic memristor, v_{on} and v_{off} are threshold voltages, and t is the time. Parameters α_{on} and α_{off} are constants, k_{on} is a negative constant, whereas k_{off} is a positive constant. Functions $f_{\text{on}}(x)$ and $f_{\text{off}}(x)$ are window functions [19] that mimic the nonlinear internal state switching during electrical programming:

$$f_{\text{off}}(x) = j \cdot (1 - x)^{p_{\text{off}}} \qquad f_{\text{on}}(x) = j \cdot x^{p_{\text{on}}} \tag{2}$$

Here, j, p_{on} and p_{off} are positive constants. The parameter j controls the magnitude. Parameters p_{on} and p_{off} indicate the nonlinearity degree, as the nonlinearity of an optoelectronic memristor is gradually weakened when p_{on} and p_{off} are approaching 0.

B. Photocurrent Readout Modeling

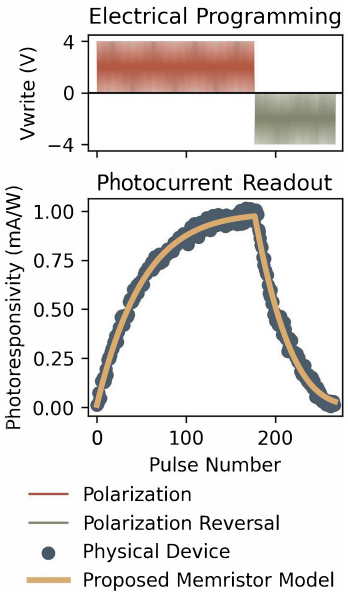
In the photocurrent readout phase, light stimuli are used as input to induce photocurrent as the output. When the memristor receives a light stimulus, the photocurrent I_p will be generated as:

$$I_p = R_\lambda \times P \tag{3}$$

where R_λ is the photoresponsivity of the device after electrical programming, and P is the received illumination power. The minimum and maximum photoresponsivities are represented by R_{on} and R_{off}, respectively. The internal state variable x is linearly mapped to R as:

$$R_\lambda = R_{\text{on}} + (R_{\text{off}} - R_{\text{on}}) \cdot x \tag{4}$$

If $x = 0$, the photoresponsivity of the optoelectronic memristor is at the minimum value R_{on}, while the photoresponsivity of the device is at the maximum value R_{off} when $x = 1$.



Param	Value
α_{off}	5
α_{on}	5
v_{off}	2 V
v_{on}	-2 V
R_{off}	0.99 mA/W
R_{on}	0.01 mA/W
j	1
λ	633 nm
P	0.2 μW
dt	30 ms
p_{off}	0.9
p_{on}	0.7
k_{off}	0.64 s^{-1}
k_{on}	-0.84 s^{-1}
CC	99.70%
RRMSE	2.53%

Fig. 2. Parameter settings and optoelectronic memristor model fitting results.

C. Model Fitting Performance

In this work, the MF/semiconductor interfacial memristor is fitted with the proposed model. During the electrical programming phase, the memristor is poled using electrical pulses of +4/-4 V with a 30 ms duration and a 200 ms period; while in the photocurrent readout phase, the photoresponse of the memristor is collected under a 633-nm laser of 25.68 mW/cm^2. At every readout operation, the received illumination power of the memristor is 0.2 μW. Given the photoresponsivity-polarization characteristics in Fig. 2, a set of parameters is chosen to fit the model to the reference behavior of the physical device. Similar to that in [11], the fitting parameters, including α_{on}, α_{off}, v_{on}, v_{off}, R_{on}, R_{off} and j, are manually chosen according to the properties of the physical device reported in [14]. The fitting procedure is iterated on p_{on}, p_{off}, k_{on} and k_{off}, where the relative root mean square error (RRMSE) is minimized using gradient descent and simulated annealing algorithms.

The graphical and numerical fitting results are demonstrated in Fig. 2. For the electrically-poled and optically-stimulated MF/semiconductor interfacial memristor, the proposed model can achieve a decent fit, with 99.70% in the correlation coefficient (CC) and 2.53% in the RRMSE.

IV. Optoelectronic STDP-based Learning System

The optoelectronic memristor-based STDP learning system is explored in this work. Based on the optoelectronic memristor, the electrical characteristics are utilized to perform approximate computing of trace dynamics, while the optical characteristics are exploited to implement readout and weight calculation. An optical synaptic trace circuit is designed and illustrated in Fig. 3(a).

A. Trace Dynamics

In a trace-based STDP learning system, the synapse strength is modulated by the timing of spike trains through key traces

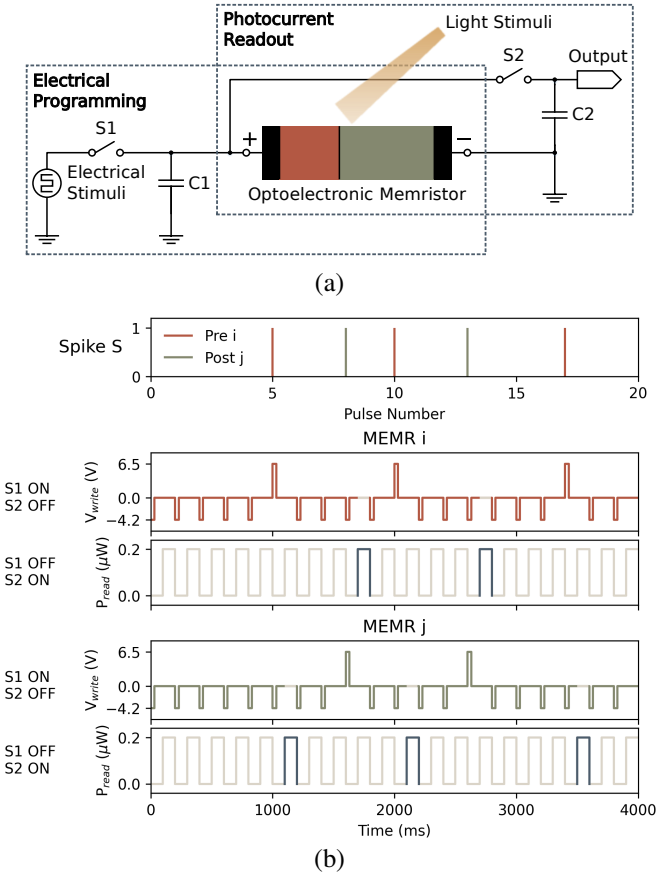


Fig. 3. The diagram of the proposed optical synaptic trace circuit (a). The pre- and post-synaptic trace circuitry is controlled by the post- and pre-synaptic spikes (b).

[6]–[8]. The pairwise nearest-neighbor STDP learning rule is one of the most widely-used learning rules in an unsupervised SNN learning system. The spatiotemporal dynamics of a trace X is defined as:

$$\begin{cases} \tau \cdot \frac{dX}{dt} = -X & S = 0 \\ X = \delta & S = 1 \end{cases} \tag{5}$$

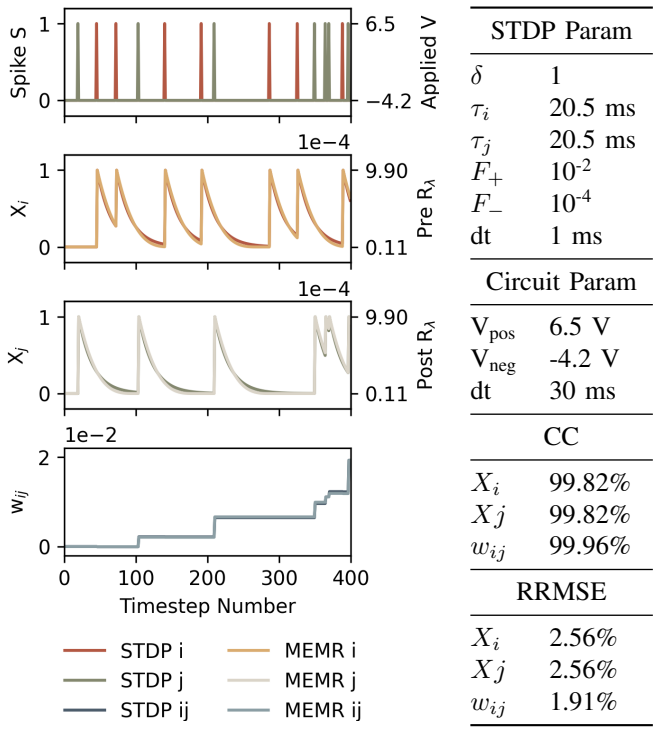
where t is the time, the parameter τ is the time constant, δ is a constant, and S is the incoming spike.

There are two key traces, including the pre-synaptic trace X_i and the post-synaptic trace X_j, in the weight w_{ij} computation of the pairwise nearest-neighbor STDP learning rule:

$$\begin{cases} \tau_i \cdot \frac{dX_i}{dt} = -X_i & S_i = 0 \\ X_i = \delta & S_i = 1 \end{cases} \quad \begin{cases} \tau_j \cdot \frac{dX_j}{dt} = -X_j & S_j = 0 \\ X_j = \delta & S_j = 1 \end{cases} \tag{6}$$

$$\frac{dw_{ij}}{dt} = F_+ \cdot X_i \cdot S_j - F_- \cdot X_j \cdot S_i \tag{7}$$

Here, F_+ and F_- are all constants and denote the learning rate for a post- and pre-synaptic spike, respectively. The graphical trace and weight computation process of the pairwise nearest-neighbor STDP learning rule are illustrated in Fig. 4.



STDP Param	
δ	1
τ_i	20.5 ms
τ_j	20.5 ms
F_+	10^{-2}
F_-	10^{-4}
dt	1 ms
Circuit Param	
V_{pos}	6.5 V
V_{neg}	-4.2 V
dt	30 ms
CC	
X_i	99.82%
Xj	99.82%
w_{ij}	99.96%
RRMSE	
X_i	2.56%
Xj	2.56%
w_{ij}	1.91%

Fig. 4. Trace simulation and weight approximate computation results.

B. Optical Synaptic Trace Circuit

The nonlinear photoresponsivity change of the optoelectronic memristor during electrical programming exhibits great similarity with the trace dynamics. Therefore, the memristor is utilized to perform approximate computing of the trace. According to equation (7), to carry out weight calculation, the pre-synaptic trace X_i is needed when a post-synaptic spike occurs ($S_j = 1$), while the post-synaptic trace X_j is needed when a pre-synaptic spike comes ($S_i = 1$). To realize non-destructive readout of the pre- and post-synaptic traces, the photocurrent readout functionality of the memristor is exploited, since the photoresponsivity after poling can retain a long retention time and the memristor cannot be poled by optical stimuli. Based on the electrical and optical characteristics, an optical synaptic circuit is designed as shown in Fig. 3(a).

The proposed optical synaptic circuit has two operating modes, the electrical programming mode and the photocurrent readout mode, as shown in Fig. 3(b). In the electrical programming mode, the +6.5/-4.2 V electrical stimuli (duration: 30 ms, period: 200 ms) are applied to the memristor to perform approximate computing of the trace. In the photocurrent readout mode, the memristor receives 0.2 μW light stimuli (duration: 100 ms, period: 200 ms) to generate photocurrent for weight calculation. The synaptic circuit is switched between the two operating modes according to the pre- or post-synaptic spike S.

The optoelectronic memristor-based optical synaptic circuit is simulated using the proposed model to evaluate the approximate computing results. The parameters of the pairwise nearest-neighbor STDP learning rule and graphical simulation results of the trace dynamics and weight computation are presented in Fig. 4. The CC and RRMSE are adopted as the simulation metrics. The synaptic-level simulation results show 99.96% CC and 1.91% RRMSE in the weight computation of pairwise nearest-neighbor STDP.

TABLE I
EXPERIMENTAL SETTINGS AND NETWORK-LEVEL SIMULATION RESULTS

Network and Experimental Settings	
Input Size	28×28
Excitatory Neuron	625
Inhibitory Neuron	625
Training Example	60,000
Test Example	10,000
Trial Number	100

Original Network	
Mean Accuracy	92.17%
Accuracy STD	0.57%
Memristor-Based Network	
Mean Accuracy	92.07%
Accuracy STD	0.64%

C. Network-level Simulation

To validate the feasibility of the optical synaptic circuit, the simulation is extended to the network level. The experiment tested the network performance on the MNIST benchmark of the optoelectronic memristor-based unsupervised SNN learning system. The original network combines the trace-based pairwise nearest-neighbor STDP learning rule with the self-organizing map algorithm [7]. The trace-based learning rule is approximately computed through the optoelectronic memristor model. The network parameters and experimental settings are listed in Table I. Test results reported in Table I are measured over 100 independent trials and compared with the original network performance. The simulation results show that the optoelectronic memristor-based unsupervised STDP learning system can achieve a 92.07±0.64% accuracy on the MNIST benchmark, with a 0.10% loss in the mean accuracy and a 0.07% increase in the standard deviation (STD).

V. Conclusion

This work focuses on the modeling of optoelectronic memristors with the functionalities of electrical programming and photocurrent readout. The proposed behavioral optoelectronic memristor model can achieve a decent fit of a MF/semiconductor interfacial memristor with 99.70% in the CC and 2.53% in the RRMSE. An optical synaptic circuit for trace-based STDP learning rules is proposed and simulated based on the model. The feasibility of the optoelectronic memristor-based learning system is validated on both the synaptic and network levels. The experimental results on the MNIST benchmark show only a 0.10% loss in the mean accuracy and a 0.07% increase in the standard deviation.

VI. Acknowledgement

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