Modeling Cycle-to-Cycle Variation in Memristors for In-Situ Unsupervised Trace-STDP Learning

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***Abstract*—Evaluating the computational accuracy of Spiking Neural Network (SNN) implemented as in-situ learning on large-scale memristor crossbars remains a challenge due to the lack of a versatile model for the variations in non-ideal memristors. This brief proposes a novel behavioral variation model along with a four-stage pipeline for physical memristors. The proposed variation model combines both absolute and relative variations. Therefore, it can better characterize different memristor cycle-to-cycle (C2C) variations in practice. The proposed variation model has been used to simulate the behavior of two physical memristors. Adopting the non-ideal memristor model, the trace-based spiking-timing dependent plasticity (STDP) unsupervised in-memristor learning system is simulated. Although the synaptic-level weight simulation shows a performance degradation of 7.99% and 4.07% increase in the relative root mean square error (RRMSE), the network-level simulation results show no accuracy loss on the MNIST benchmark. Furthermore, the impacts of absolute and relative C2C variations on network performance are simulated and analyzed through two sets of univariate experiments.**

***Index Terms*—Memristor, non-ideality, variation model, trace-based STDP, in-situ unsupervised learning.**

I. Introduction

MEMRISTORS provide an ideal computing paradigm for brain-inspired neural networks (NNs), given their ability to fuse computation and memory and to mimic synapses. This property has been exploited for efficient in-situ learning of emerging spiking neural networks (SNNs) [1], [2], [3]. Furthermore, the non-volatility and non-linearity of memristors have prompted researchers to use them to implement biologically plausible synaptic learning rules, especially the trace-based spike-timing dependent plasticity (STDP) [4], [5], [6].

Despite recent advances in memristor technologies, the non-idealities of physical memristors [7] have impeded the implementation of large-scale memristor-based neuromorphic systems. Among all the non-idealities, the cycle-to-cycle (C2C) variation in memristors is one of the major challenges to the performance of the memristor-based in-situ computation [8], [9], [10]. Although there has been some work on studying and analyzing C2C variations, a systematic study of C2C variations and their impact on large-scale SNN implementation are lacking. There are two major challenges: 1) the largest crossbar that has been implemented is a 128×64 array [11], and as a consequence, existing memristor crossbars are not large enough to perform the variation study for large-scale ($>$10k synapses) SNN implementations; 2) lack of a model that is versatile enough to model C2C variations in memristors.

Due to the memristor non-idealities, the experimental implementation of large-scale memristor arrays is still in its infancy, not to mention the memristor variation study for large-scale SNN implementations. Therefore, various designer-friendly memristor models have been proposed to facilitate large-scale simulations [12]. In terms of the memristor C2C variation, a common modeling approach is to simulate the C2C variation through simple Gaussian noise [13], [14], [15], [16], [17], [18]. However, existing models are insufficient for characterizing the varying C2C variations in different memristors. C2C variations in certain memristors exhibit a significant positive correlation with conductance, whereas in others, the correlation is weak. What is needed is a versatile model that can capture the above-mentioned varying correlation and emulate memristor C2C variations at the behavioral level to allow efficient simulation of large-scale memristor-based SNNs.

This brief presents a versatile C2C variation model for large-scale memristor-based SNN learning systems. The contributions of this brief can be summarized as follows:

- A novel behavioral model of memristor C2C variations is proposed, which is the first to capture the varying correlation between variation and conductance in memristors.
- A four-stage pipeline is proposed to overcome the challenge of fitting the variation model. The pipeline extracts statistical features from the distribution of C2C variations to enable accurate fitting of raw data.

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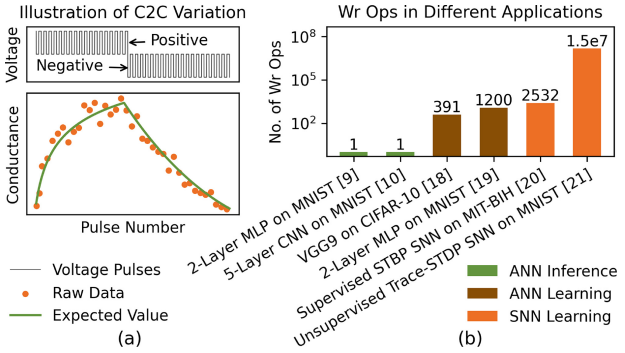

Fig. 1. (a) Impact of C2C variation on memristor conductance during write (Wr) operations. (b) The number of Wr operations (Ops) required for different NN applications.

- This model has been validated for two typical memristors, and has been used to study the network-level impact of C2C variations on the in-situ learning of the biologically-plausible SNN that relies on the trace-STDP learning rule.

II. Memristor C2C Variation

A. C2C Variation in NN Learning

Memristors commonly exhibit multiple non-ideal properties, such as limited analog states, non-linear and asymmetric programming, low yield, aging effect, retention loss, device-to-device (D2D) variation, and C2C variation [7]. The C2C variation refers to the inconsistency observed in the response of a memristor to the same pulse over time, even with the same initial state. It is caused by the inherent randomness in internal atomic configurations at each write operation [8].

The negative effects of C2C variation are highly application-dependent. Fig. 1 illustrates the C2C variation during memristor write operations, and compares the number of write operations required for different NN applications. Here, the numbers reported for NN learning tasks are measured over one training epoch. In the case of inference tasks, only one write operation is necessary to program the memristors based on the pre-determined weights [9], [10]. However, for learning tasks, a greater number of write operations are typically required as the weights are adjusted during the learning process [18], [19], [20], [21].

In memristor-based systems for NN inference and learning, C2C variations often limit their ability to achieve high accuracies. For ANNs, previous studies have identified that C2C variations can harm the accuracies in both inference and learning tasks [9], [10], [18]. In supervised SNN learning tasks adopting a spatio-temporal backpropagation (STBP) learning rule [20], memristors can serve as weights in a similar manner to memristor-based ANN implementations. For the more biologically-plausible trace-STDP learning rules in unsupervised SNN learning [21], the sophisticated exponential trace dynamics pose a challenge to memristor-based implementations. Recent research proposes a memristor-based synaptic circuit [6] as an energy-efficient solution. The similarity between the trace dynamics and the memristor non-linearity is explored, where memristors are utilized as traces instead of weights. This design reduces the scale of the memristor crossbar, but the number of write operations in one training epoch is 4 orders of magnitude higher. However, there is still no network-level feasibility analysis of the memristor-enabled implementation of trace-STDP learning rules, nor studies of the C2C variation on the network performance.

Targeting trace-STDP SNN in-situ learning, this brief focuses on the C2C variation and aims to fill these gaps through network-level simulations using the proposed variation model.

B. Memristor Behavioral Model

To study the variations of physical memristor devices, a memristor behavioral model is necessary to minimize the unwanted variations introduced by unsatisfactory model fitting results. In this brief, a conductance-based variant of the VTEAM model [12] is adopted along with a window function [22] to emulate the non-linearity of memristors:

$$G(t) = G_{\text{on}} + (G_{\text{off}} - G_{\text{on}}) \cdot x(t) \tag{1}$$

$$\frac{dx(t)}{dt} = \begin{cases} k_{\text{off}} \cdot (\frac{v(t)}{v_{\text{off}}} - 1)^{\alpha_{\text{off}}} \cdot f(x(t)), & 0 < v_{\text{off}} < v(t) \\ 0, & v_{\text{on}} < v(t) < v_{\text{off}} \\ k_{\text{on}} \cdot (\frac{v(t)}{v_{\text{on}}} - 1)^{\alpha_{\text{on}}} \cdot f(x(t)), & v(t) < v_{\text{on}} < 0 \end{cases} \tag{2}$$

$$f(x(t)) = j[\text{sgn}(-i(t)) \cdot (x(t) - 1) + \text{stp}(-i(t))]^{p(i(t))} \tag{3}$$

$$i(t) = G(t) \cdot v(t) \qquad p(x) = \begin{cases} p_{\text{off}}, & x \geq 0 \\ p_{\text{on}}, & x < 0 \end{cases} \tag{4}$$

$$\text{sgn}(x) = \begin{cases} 1, & x \geq 0 \\ -1, & x < 0 \end{cases} \qquad \text{stp}(x) = \begin{cases} 1, & x \geq 0 \\ 0, & x < 0 \end{cases} \tag{5}$$

Here, t is the time, $x(t)$ is an internal state variable ranging [0, 1], $v(t)$ is the voltage applied to the memristor, $i(t)$ is the current passing through the memristor, and $G(t)$ is the conductance of the memristor. The parameters v_{on} and v_{off} are threshold voltages, G_{on} and G_{off} are the minimum and maximum conductances of the memristor, respectively. The parameters k_{on}, k_{off}, α_{on}, and α_{off} are constants. In the window function, j controls the magnitude, and the function $p(x)$ determines the degree of linearity. The parameters p_{on} and p_{off} are positive constants, and the closer p to 0, the weaker the non-linearity of the memristor. The $i(t)$ is considered positive when the internal state $x(t)$ moves towards 1.

C. Relative Variation and Absolute Variation

Relative variation and absolute variation are the two components that contribute to the overall C2C variation. Relative variation is defined as the portion of variations that is proportional to the current state of the memristor. Absolute variation is defined as the inherent variations in the system that are independent of the current state of the memristor.

Existing works on variation modeling adopt either relative or absolute variation models, utilizing random errors of a Gaussian distribution with mean zero [13], [14], [15], [16], [17], [18]. For example, in the works [13], [14], [15], a relative variation model is employed, while [16], [17], [18] adopt an absolute variation model. Relative variation models emphasize the correlation between the variation to memristor conductance, while absolute variation models ignore that correlation. However, in practical scenarios, the variations in memristors always exist as a combination of both relative and absolute variations. Furthermore, the correlation between variation and conductance can vary across different memristors, exhibiting either a significant positive correlation [23] or a weak correlation [24] as shown in Fig. 2. The existing variation models are insufficient for accurately characterizing the varying variations in different memristors.

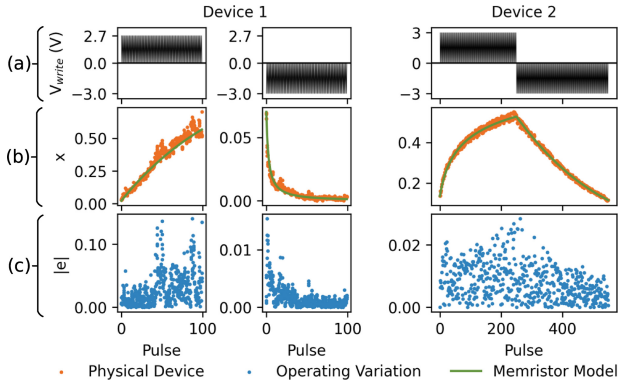

Fig. 2. (a) Voltage pulses applied to memristors. (b) Memristor internal state variable $x(t)$ responding to pulses and memristor model fitting results. (c) C2C variations in the two devices.

III. Memristor Variation Modeling

A. Modeling of C2C Variations

This brief proposes a versatile behavioral variation model that combine the relative variation e_{re} and the absolute variation e_{ab} into one model $e(x)$. For every $x(t)$, the disturbed x' can be mathematically expressed as:

$$x'(t) = x(t) + e(x) \qquad e(x) = e_{\text{re}} \cdot x(t) + e_{\text{ab}} \tag{6}$$

$$e_{\text{re}} \sim N\left(0, \sigma_{\text{re}}^2\right) \qquad e_{\text{ab}} \sim N\left(0, \sigma_{\text{ab}}^2\right) \tag{7}$$

In terms of C2C variation, the internal state x in the equation (1) is studied instead of the conductance. This choice is motivated by two key reasons: 1) analyzing the relative variation reveals that for the same conductance variation, the variation percentage in the case of G_{on} is much higher than that in the case of G_{off} [16]; 2) it is difficult to compare the device variation when the conductance values of different memristors vary by orders of magnitude. The utilization of x is beneficial for achieving normalization.

The proposed variation model is validated on two typical bipolar memristors: a ferroelectric memristor [23] (device 1) and a molecular ferroelectric/semiconductor interfacial memristor [24] (device 2). The fitting of the combined model poses a challenge, considering: 1) there is limited raw data available; 2) combing both relative and absolute variation, it is impossible to directly fit the model to raw data through a distribution fitter. To address this challenge, a four-step fitting pipeline is proposed based on an important assumption: the random variables e_{re} and e_{ab} follow a Gaussian distribution. As a result, the combined variation $e(x)$, for each $x(t)$, also follows a Gaussian distribution with mean zero and variance $\sigma_{\text{re}}^2 \cdot x(t)^2 + \sigma_{\text{ab}}^2$. The four-step pipeline aims to extract statistical features from the distribution of C2C variations to enable accurate fitting:

- *Rearranging:* The $|e(t)|$ in Fig. 2(c) are rearranged into $|e(x)|$ by the corresponding x value, as shown in Fig. 3.
- *Clustering:* The rearranged $|e(x)|$ are divided into n clusters, with m variation data points in each cluster, as illustrated by the different colored fills in Fig. 3. For the device 1 in Fig. 3(a), the n and m are set to 10 and 55, while for the C2C variation data of device 2 in Fig. 3(b), $n = 10$ and $m = 100$. The mean value of $|e(x)|$ in each cluster is statistically analyzed as $\overline{|e|}$, and the squares of $\overline{|e|}$ are illustrated as the orange dots in Fig. 3.

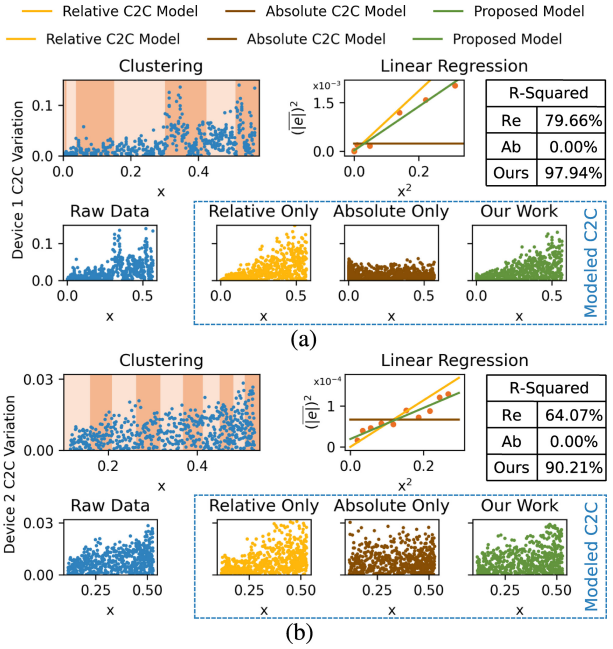

Fig. 3. Fitting results and simulation examples of the proposed variation model on device 1 (a) and device 2 (b). The blue dots represent the raw C2C variation data, while the yellow, brown and green dots illustrate examples of the C2C variation modeled by relative C2C model, absolute C2C model, and the proposed model, respectively.

- *Linear Regression:* Setting x^2 as the independent variable and $(\overline{|e|})^2$ as the dependent variable, linear regression is performed to obtain $(\overline{|e|})^2 = \beta_1 \cdot x^2 + \beta_0$. Here, the square is adopted to match the variance of the combined variation $e(x)$.
- *Calculation:* To calculate σ_{re} and σ_{ab}, the correlation between the variance σ^2 and the expected absolute value $E(|X|)$ of a Gaussian distributed variable serves as the key enabler. Let X follow an ordinary normal distribution $N(0, \sigma^2)$, then $|X|$ follows a half-normal distribution with $E(|X|) = \sigma\sqrt{2/\pi}$. Therefore, σ_{re} and σ_{ab} can be calculated as:

$$\sigma_{\text{re}}^2 = \beta_1 \cdot \pi/2 \qquad \sigma_{\text{ab}}^2 = \beta_0 \cdot \pi/2 \tag{8}$$

B. Evaluation of the Variation Model

To obtain the parameters of the conductance-based memristor model, the fitting procedure follows that of the VTEAM model [12], where k_{off} and k_{on} are iterated to minimize the relative root mean square error (RRMSE) [6]. The remaining parameters are manually chosen according to the reported physical characteristics of memristors. The parameters and the fitting results are depicted in Table I and Fig. 2. Both device 1 and 2 exhibit non-linear behavior. As shown in Fig. 2(b), device 1 demonstrates a higher degree of non-linearity during the conductance declining phase in response to negative pulses, while device 2 exhibits a higher degree of non-linearity during the conductance rising phase in response to positive pulses.

The modeling of the C2C variations in devices 1 and 2 is performed by the proposed four-stage pipeline, and the obtained σ_{re} and σ_{ab} are listed in Table I. The absolute variations in device 1 and 2 are at a similar level, while the relative variation in device 1 surpasses that in device 2 by one order of magnitude, indicating a stronger correlation between the C2C

TABLE I
FITTING CHARACTERISTICS OF THE PROPOSED MODEL TO MEMRISTOR DEVICES

Memristor	Memristor Model													Variation Model	
	α_{off}	α_{on}	v_{off}[V]	v_{on}[V]	G_{off}[S]	G_{on}[S]	k_{off}[s^{-1}]	k_{on}[s^{-1}]	j	p_{off}	p_{on}	dt	RRMSE	$\sigma_{relative}$	$\sigma_{absolute}$
Device 1	5	5	1.4	-2.0	9.0×10^{-6}	7.0×10^{-8}	1.1×10^{5}	-7.4×10^{8}	1	0.9	1.8	100 ns	3.94%	1.03×10^{-1}	5.78×10^{-3}
Device 2	5	5	2.0	-2.0	1.9×10^{-9}	2.5×10^{-10}	19.5	-3.4	1	5.0	0.7	30 ms	2.20%	2.44×10^{-2}	5.49×10^{-3}
Ideal	1	1	1.0	-1.0	1.0×10^{-6}	1.0×10^{-8}	100.0	-100.0	1	1	1	1 ms	-	-	-

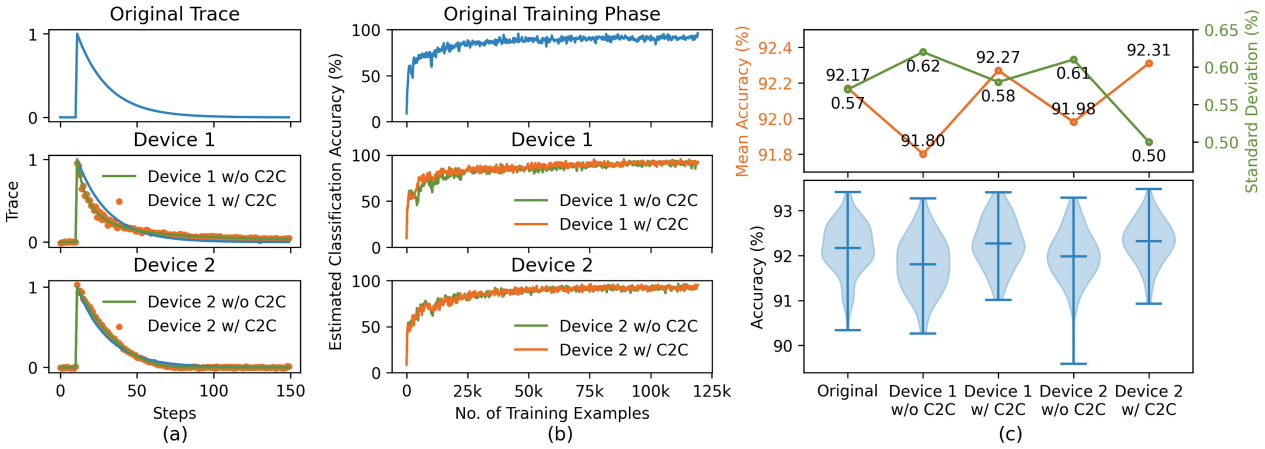

Fig. 4. Synaptic-level and network-level memristor-based simulation results. The synaptic-level impact of C2C variations on trace dynamics (a). The impact of C2C variations on the SNN training phase (b). The network-level impact of C2C variations on the in-situ SNN learning system (c).

variation and conductance in device 1. As shown in Fig. 3, compared to the other two widely-used models, the proposed variation model can better render the C2C variation of physical memristor devices, demonstrating goodness of fit exceeding 90% in terms of the R-squared value.

IV. NON-IDEAL MEMRISTOR-BASED STDP LEARNING

A memristor-based architecture is proposed to simulate the trace-STDP in-situ learning system, and the impact of memristor C2C variation is studied on the network-level simulation.

A. Memristor-Based Architecture

The proposed architecture is built on the SNN that combines the trace-STDP learning rules with the self-organizing map (SOM) algorithm [21]. As shown in Fig. 5, the network consists of a 28×28 input layer and a processing layer, containing a variable number of excitatory and inhibitory neurons. During the training phase, all synapses from input neurons to excitatory neurons are trained using trace-STDP through memristor-based approximate calculation. The synaptic weight change is calculated based on the pre- and post-synaptic traces, and these exponential time-dependent traces are approximated by non-linear conductance changes of memristors.

The C2C variations of memristors have a negative impact on the approximation of traces. Adopting the fitted variation model of the two typical physical memristor devices, the synaptic-level simulation results of 10,000 random spike trials show that the C2C variation increases the weight simulation metric RRMSE from 4.55% to 12.55% and from 0.11% to 4.18%, for device 1 and device 2 respectively. In this brief, the C2C variations of memristors are further studied on the network level. The effects of absolute and relative C2C variations on the unsupervised learning systems are also simulated and tested through experiments.

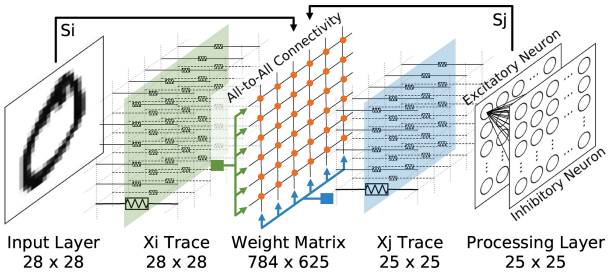

Fig. 5. Memristor-based architecture for trace-STDP in-situ learning system.

B. Simulation With Physical Devices

For the memristor-based training test, a network with 625 excitatory and inhibitory neurons is trained by presenting 60,000 examples of the MNIST training set twice, and evaluated on all 10,000 test examples. Besides the original trace-based STDP learning rule, the network is trained with the two memristors with (w/) and without (w/o) C2C variations. Test accuracy results and standard deviations are reported in Fig. 4(c), each averaged over 100 independent trials.

The original network can reach 92.17±0.57% on the MNIST benchmark. The inherent non-linearity of devices 1 and 2 only results in <0.4% accuracy penalty. Disturbing the memristor model with the modeled C2C variation, the synaptic-level trace simulation results in Fig. 4(a) show certain perturbation. However, on the network level, no significant change in the estimated classification accuracy is observed throughout the whole training phase. Furthermore, there is no loss of accuracy for the two memristor-based implementations (w/ C2C variations) compared to the original network.

C. Experiments of C2C Variation

To study the network-level impact of absolute and relative variation, the network is trained using the memristor-based

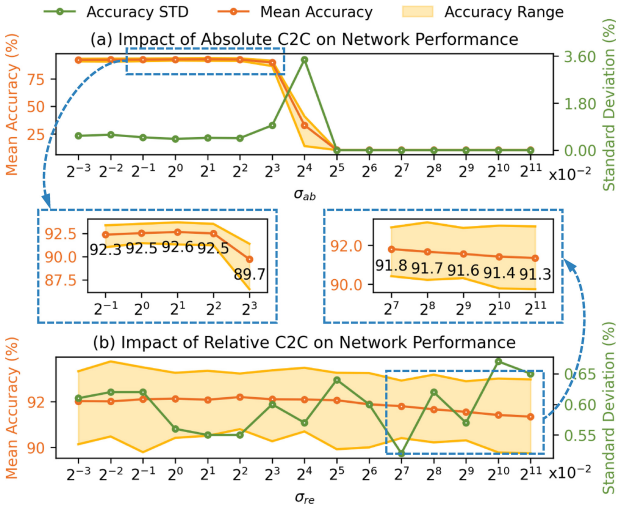

Fig. 6. Univariate experiments on network performance. (a) Impact of absolute C2C variations with $e_{\text{re}} = 0$. (b) Impact of relative C2C variations with $e_{\text{ab}} = 0$.

learning rule disturbed with absolute variation only and relative variation only, respectively. The experimental results are reported in Fig. 6, and each result is measured over 100 independent trials. For absolute variations, when σ_{ab} is increased to 0.16, the network suffers significant performance degradation. For relative variations, σ_{re} has a relatively smaller impact on the network performance, because relative variations have little impact on near-zero trace variables.

D. Experiments on Additional Applications

The variation models of the two devices are further utilized to study the impact of C2C variations on other NN applications, including the inference and training tasks of VGG16 on CIFAR-10 dataset [18] and the supervised learning task of STBP-SNN on MIT-BIH dataset [20]. In these experiments, memristors are employed to represent weights, and the write operations are conducted either for initial weight programming or for weight update at each batch. The accuracy losses of device 1 and device 2 for VGG16 inference are 1.14% and 0.65% respectively, while negligible accuracy losses are reported in the VGG16 training task and the supervised STBP-SNN learning task. Despite the higher frequency of write operations in the NN training tasks, they demonstrate better resilience to C2C variations compared to inference tasks.

Future work can build on the proposed memristor C2C variation model and explore its applications in various memristor-based applications. In addition, studying and integrating other memristor non-idealities into the behavioral model is a crucial aspect to advance the understanding and performance optimization of memristor-based systems.

V. Conclusion

We propose a novel behavioral variation model that can be integrated into a memristor model to characterize the device C2C variation. Through a four-stage pipeline, the versatility of the proposed model is validated with two published memristor devices. Adopting the non-ideal memristor model, this brief extends the previously proposed memristor-based synaptic circuit to the network level. For the two physical memristor-based learning systems, although the synaptic-level weight simulation shows a performance degradation by 7.99% and 4.07% increase in RRMSE, no accuracy losses are reported on the network-level MNIST benchmark.

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