P730 UNIVERSAL FANOUT BUFFER

Technical Manual

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1. Introduction

The P730 Universal Fanout Buffer is a high speed, multipurpose digital fanout, configurable as either a 1 to 8 or a dual 1 to 4 buffer capable of passing signals from DC up to 1 Gbps. The electrical inputs can be set to respond to digital thresholds representing anything from CMOS, 5V PECL and negative ECL logic levels; optional optical inputs can accept signals of up to 2 mW without need for external attenuators. Output voltage levels can be set to provide output levels from CMOS to double-terminated negative ECL.

The standard versions of the P730 are as follows:

Version	Electrical Inputs	Optical Inputs
P730-1	Two	Two (850 nm, ST Connector)
P730-3	Two	Two (1310 nm, ST Connector)
P730-5	Two	Two (1550 nm, ST Connector)

Features of the P730 include:

- DC coupled electrical inputs are usable up to 1 Gbps
- Input-to-output bank assignment is routable without moving cabling
- Programmable logic in thresholds (-4 V to +4 V) can be set independently per input
- Programmable logic out voltages (-3.6 V to +5 V, 50 Ω source) can be set independently per output bank
- Insertion delay is under 3 nanoseconds, with random jitter less than or equal to 12 picoseconds RMS
- Comes in sturdy anodized aluminum enclosure with optional mounting flanges for extra security
- Expanded input-to-output bank assignment architecture allows user-configurable routing of either electrical or optical input to either output bank
- Independent optical thresholds with front panel accessible test points
- Monitor outputs provide analog verification of optical signal integrity and power measurement

2. Specifications: P730 Universal Fanout Buffer

FUNCTION	1:8 or dual 1:4 universal fanout
INPUTS	Electrical input voltage range (E0, E1): +6 V to -4 V (50 Ω termination) Optional optical input range (F0, F1): 0 µW to 2 mW
INPUT THRESHOLDS	Electrical: ±4 V Optical: 500 µW to 2 mW, typical
PROPAGATION DELAY	3 ns, typical
OUTPUTS	Two independent banks of four outputs each (X0-X3, Y0-Y3) Unloaded output voltage: +5 V, maximum Unloaded output voltage: -3.6 V, minimum Unloaded output swing: 5 V peak to peak, maximum Source impedance: 50 Ω
MONITOR OUTPUT	Optical monitor scaling: 100 mV/mW ±10% into 50 Ω Source impedance: 50 Ω
BANDWIDTH	500 MHz analog, 1 Gb/s NRZ
RISETIME	≤ 500 ps
FALLTIME	≤ 500 ps
JITTER	≤ 12 ps RMS
OUTPUT SKEW	Within Bank: < 800 ps Bank X to Bank Y: < 1 ns
MINIMUM PULSE WIDTH	≥ 750 ps
OPERATING TEMPERATURE	0 to 60°C; extended MIL/COTS ranges available
CALIBRATION INTERVAL	One year
POWER	+15 V to +24 V, 26 Watts, typical Highland Technology J24 Universal AC adapter supplied
CONNECTORS	ST optical input receptacles Gold plated SMB electrical inputs, electrical outputs and optical monitor outputs 2.1 mm X 5.5 mm barrel power connector
INDICATORS	LEDS: Green power, blue channel triggers
PACKAGING	5.0” (L) x 7.0” (W) x 2.25” (H) anodized aluminum enclosure
CONFORMANCE	Designed to meet UL/FCC/CE requirements

3. Operation

3.1. Panel Layout

The standard P730 unit is packaged in an anodized aluminum enclosure. Input connectors and controls are generally located on the front panel of the device, while output connectors and controls, along with the power connector and power switch, are located on the back.

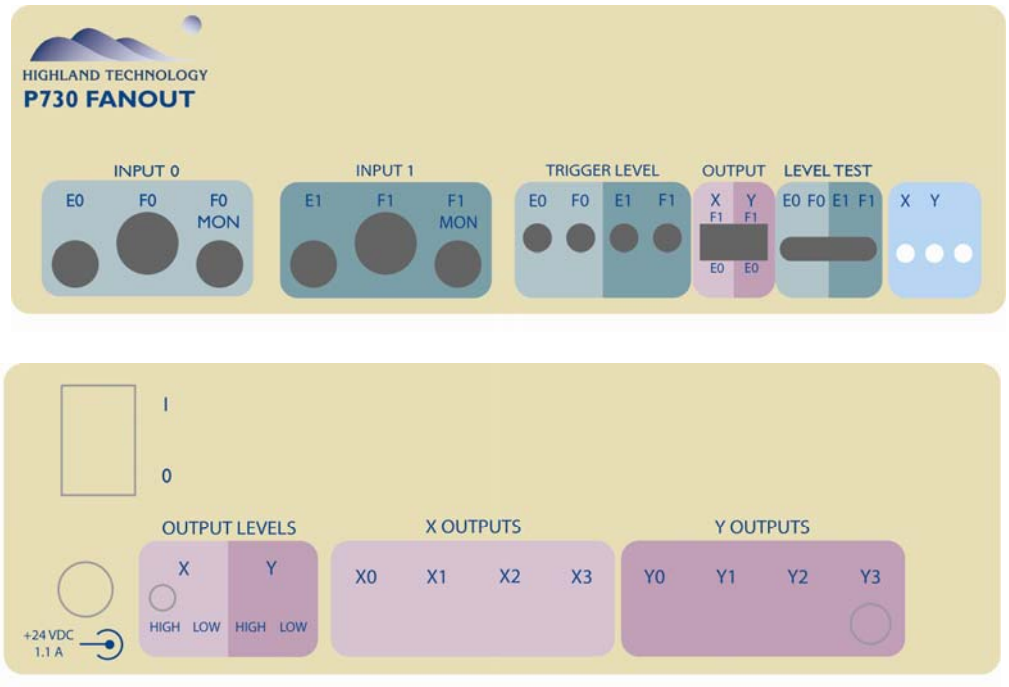


Figure 1: Front (top) and rear (bottom) panel overlays of P730 (P730-1 shown)

3.2. Overall Block Diagram

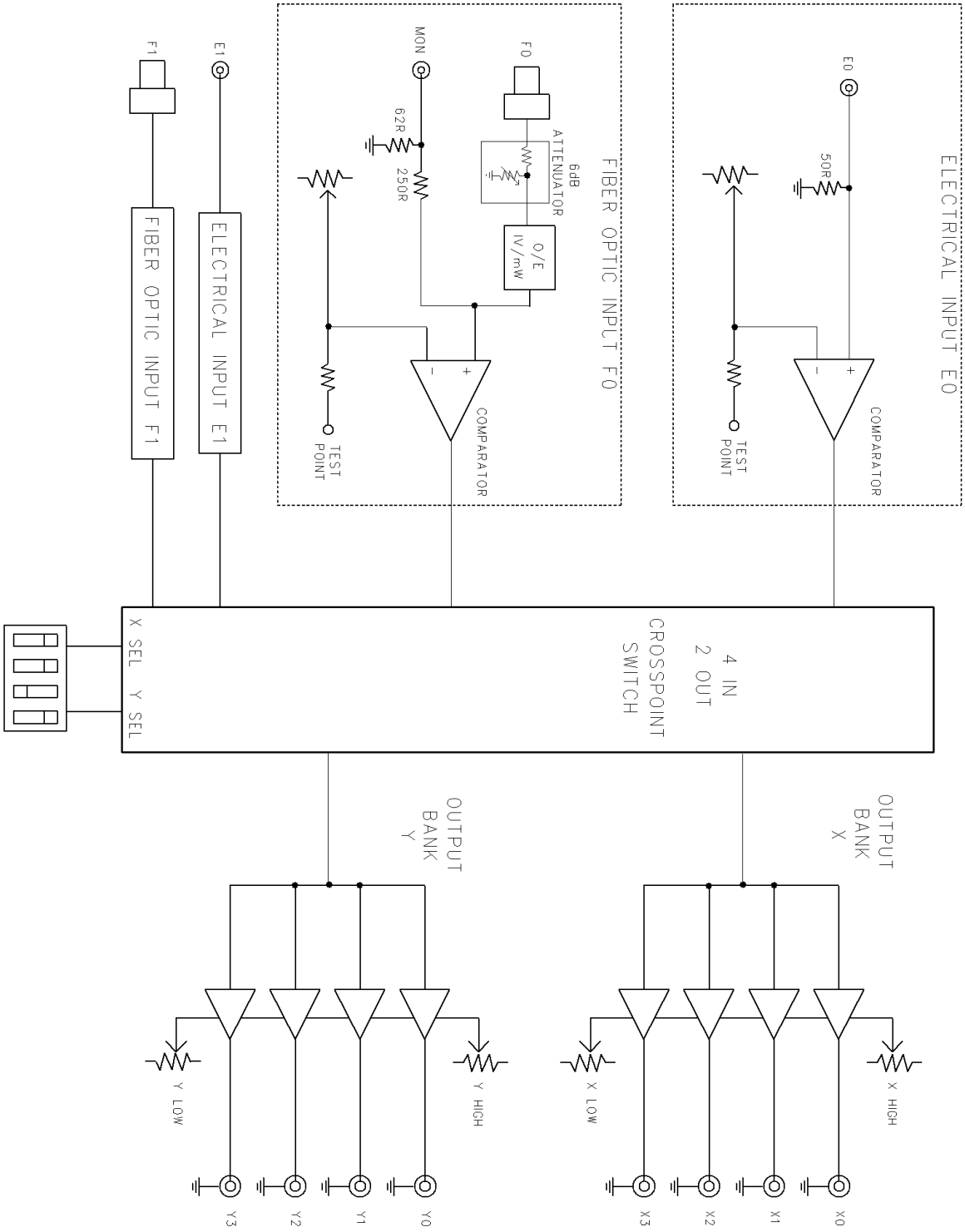


Figure 2: P730 Block Diagram

3.3. Input Signals

The P730 accepts two electrical inputs on SMB coaxial connectors, labeled as E0 and E1 on the front panel. These inputs are terminated with 50 Ω to ground, meaning that signals provided by a 50 Ω source will appear to the P730 with one half of the nominal amplitude.

The signal at each of these connectors will be compared to an adjustable threshold voltage and produce a logic high or logic low signal. The threshold level for E0 is set by turning the E0 trimpot, and can be read out by connecting a voltmeter between the E0 level test jack and any ground, including SMB connector shields and the front panel mounting screws. E1 works similarly. Recommended threshold voltages for some common logic inputs are:

TTL from 50 Ω	+0.5 V
5 V PECL from zero Ω	+3.7 V
5 V PECL from 50 Ω	+1.85 V
3.3 V PECL from zero Ω	+2.0 V
NECL from zero Ω	-1.3 V
NIM from current sink	-0.4 V
±1 V sine wave	0.0 V

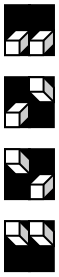
Optical inputs are labeled F0 and F1. They also include a monitor output on an SMB connector for each optical input, which allows the optical input to be read back out as an analog signal. The monitor signal is factory calibrated to 200 mV/mW of optical input signal when measured on a high-impedance oscilloscope (or 100 mV/mW into a 50 Ω scope). The F0 and F1 threshold trimpots and level test jacks use a 100 mV/mW scaling. Experimentally, the optimal threshold for optical signals is about 30% of the monitor reported peak optical power. Too high or too low a setting can result in excess jitter or unreliable operation.

As an example, if after connecting an optical fiber to F0 and starting a test signal from your optical source, you connect a high-speed, 50 Ω oscilloscope to the F0 monitor output, and measure a signal from 0 to 100 mV, this corresponds to an optical power of roughly 1 mW. A 500 μW threshold level would correspond to 50 mV, measured on the F0 level test jack. If you had been measuring the monitor signal on a conventional high-impedance scope instead you would have seen a signal from 0 to 100 mV; the threshold of 50 mV would remain unchanged.

3.4. Input-to-output Bank Assignment

The P730 features front panel user-configurable switches that allow routing any of the available inputs to either of the output banks. This allows:

- Routing any one input to the X output bank, and another to the Y output bank, creating a dual 1:4 fanout
- Routing the same input to both the X and Y output banks, creating a 1:8 fanout
- Dynamically switching a given output bank between different input sources.



Selection of the desired routing is made by the 4 switches on the front panel. The left two switches select the input for the X output bank, the right two select the input for the Y output bank. For each pair of switches, the left switch is down to select an electrical input, and up to select an optical input. The right switch of the pair is down to select a 0 numbered input, and up to select a 1 numbered input.

3.5. Signal Indicator Lights

There are two blue LEDs that serve as signal indicator lights, one for each output bank. These lights will flash brightly when a rising edge crosses the threshold on their respective banks' selected inputs. After the momentary flash, the light will remain dimly on while the signal is above the input threshold, and off while the signal is below the threshold.

3.6. Signal Polarity Inversion

The polarity of each output bank can be made inverted relative to the input. To access the signal inversion switches, remove the top cover by first removing the two upper screws on each side of the unit, then lifting the cover straight up. The signal inversion switches are towards mid-line of the unit, in front of the output buffers, and can be adjusted with a flat head screwdriver. The Y output bank polarity is controlled by S4 and the X output bank polarity is controlled by S5. Normally the polarity switches are rotated fully clockwise (CW). If signal inversion is desired, rotate the appropriate polarity switch fully counter-clockwise (CCW).

CAUTION: Switching the polarity while the P730 is on may cause damage to the unit. Make sure power is off and unit unplugged before switching the output signal polarity.

3.7. Output Signals

The output signals are known collectively as output banks X and Y, and individually as X0-X3, and Y0-Y3. A bank of outputs shares a common input source as selected by the front panel switches (see section 3.4 above), and outputs the same logic high and low voltage levels. If the same input signal is selected for both the X and Y output banks, the bank Y levels are set independently of the bank X levels.

Voltages are set by turning two trimpots per output bank. These trimpots are located on the back of the P730. Facing the rear panel, the two trimpots on the left correspond to output bank X, and the two on the right to output bank Y. For a given pair of trimpots, the left sets the logic high output voltage, and the right sets the logic low output voltage. Note that these settings cannot be used to invert the logic signal; the high voltage cannot be taken lower than the low voltage. To invert signals, see section 3.6 above. Additionally, there is a maximum output voltage swing of 5 V peak to peak. Attempting to create a wider swing than this will clamp the high voltage at slightly more than 5 V above the low voltage.

3.8. Power

The P730 ships with the Highland J24, a +24 V, 1.25 A wall-plug universal power supply. The input power connector accepts a standard 2.1 mm x 5.5 mm, center-positive barrel power connector, and can be run on power supplies from +15 V to +24 V. The P730 provides no electrical isolation from the power supply; the ring of the power connector must be at electrical ground if it is not floating. The J24 ships by default with only a US AC plug. International customers should also order international AC plug adapter kit J14.

There is a power switch on the rear panel of the P730. When looking at the front of the unit, it will be on the back, in the upper right-hand corner.

The P730 also incorporates an onboard self-resetting PPTC fuse. In the event of a fault, the PPTC fuse will limit current delivery to the P730.

4. Troubleshooting

Green power LED is not lit:

- Ensure +24 V adapter is plugged into both back of unit and AC power.
- Check that power switch is on.

Blue bank signal LED never lights:

- Make sure the input signal is connected correctly to both the source and the P730. Electrical inputs should go to the E0 or E1 connectors, NOT the F0 MON or F1 MON connectors. Optical inputs should go to the F0 or F1 connectors. Either should click firmly into place.
- Make sure you have routed the correct input to the output bank corresponding to the signal LED (see sections 3.4, 3.5 above).
- If the desired input is electrical, ensure that the logic high voltage level is more than the threshold level for that input (see section 0 above).
- If the desired input is optical, ensure that the monitor output signal shows an input signal being received, and that the threshold level is set to about 30% of the peak optical power (see section 0 above).

Blue bank signal LED always on dimly:

- Make sure you have routed the correct input to the output bank corresponding to the signal LED (see sections 3.4, 3.5 above).
- If the desired input is electrical, ensure that the logic low voltage level is less than the threshold level for that input (see section 0 above).
- If the desired input is optical, ensure that the monitor output signal shows an input signal with clear low periods, and that the threshold level is set above the baseline noise.

Blue bank signal LED always on brightly:

- This indicates a signal rate of greater than about 10 Hz, and is not an error.

Blue bank signal LED comes on, but there is no output:

- Ensure cables are properly connected.
- Check settings of output bank HIGH and LOW trimpots on back panel.

5. Dimensions and Mounting

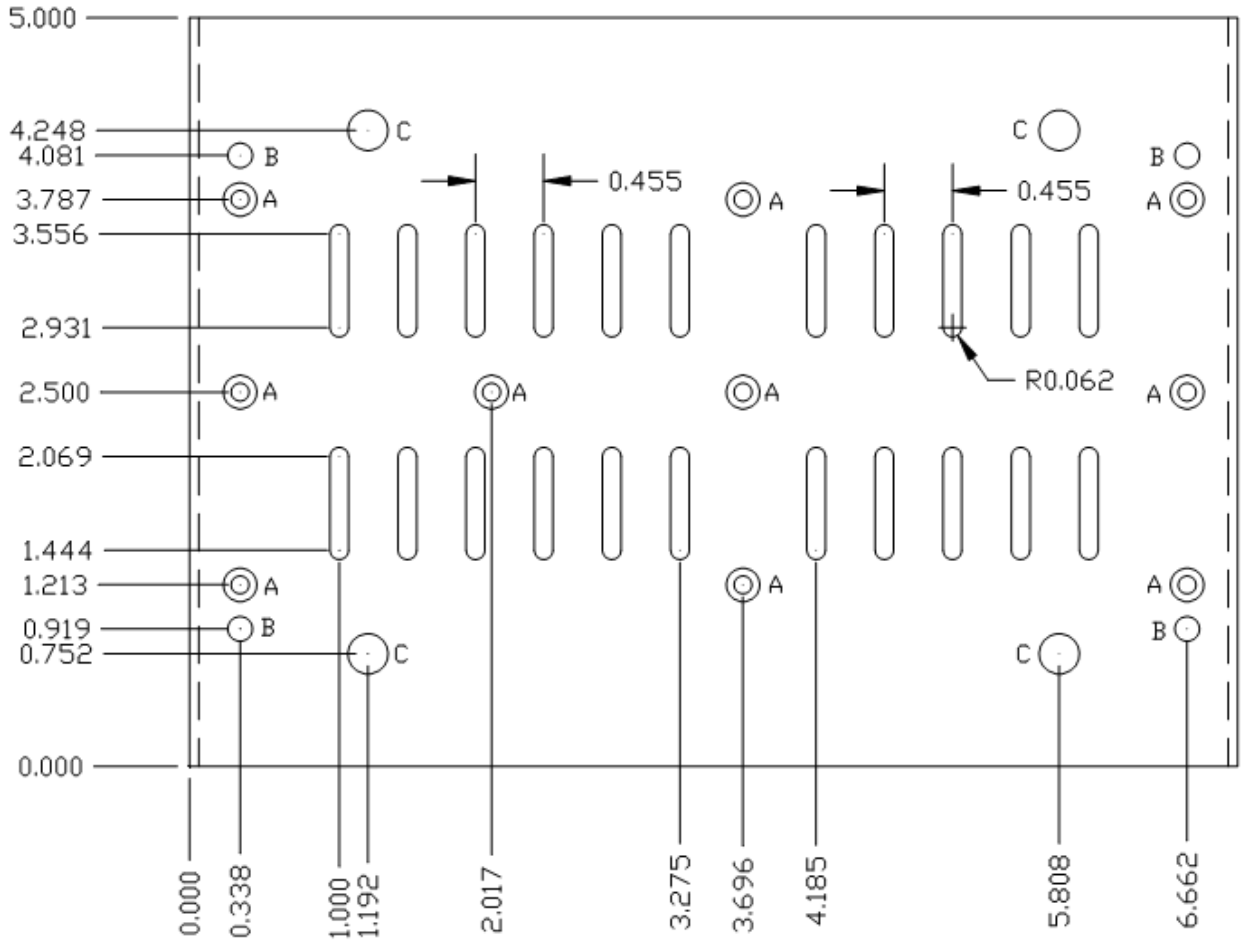


Figure 3: P730 Bottom Panel Mounting Dimensions

Mounting holes are reference B: 4-40 threads, 3/16” max plunge depth.

6. Versions

Standard versions of the P730 include:

P730-1 dual 850 nm 1:4 benchtop optical-to-electrical fanout buffer with ST connectorization

P730-3 dual 1310 nm 1:4 benchtop optical-to-electrical fanout buffer with ST connectorization

P730-5 dual 1550 nm 1:4 benchtop optical-to-electrical fanout buffer with ST connectorization

Discontinued versions of the P730 include:

P730-9 dual 1:4 benchtop electrical-to-electrical fanout buffer
Discontinued Dec 2015

P730-11 dual 850 nm 1:4 benchtop optical-to-electrical fanout buffer with FC connectorization
Discontinued Dec 2015

P730-13 dual 1310 nm 1:4 benchtop optical-to-electrical fanout buffer with FC connectorization
Discontinued Dec 2015

P730-15 dual 1550 nm 1:4 benchtop optical-to-electrical fanout buffer with FC connectorization
Discontinued Dec 2015

7. Customization

Consult factory for information about additional custom versions.

8. Hardware Revision History

Revision D	September 2014 Stability improvements, Output driver updates
Revision C	May 2009 Fully functional revision
Revision B	Aug 2008
Revision A	Feb 2008

9. Accessories

J24	24 volt power supply
J41	3' SMB to SMB cable
J41-2	6" SMB to SMB cable
J42	3' SMB to SMA cable
J53	3' SMB to BNC cable
J53-2	6" SMB to BNC cable
J720	single-channel compact electrical-to-fiberoptic converter
J724	single-channel compact buffered electrical-to-fiberoptic converter
P10	19" rack mount shelf (two p-boxes per rack)