



- 1. BLOCK DIAGRAM
- 2. TRIGGER
- 3. HIT + LC OSC
- 4. DPLL
- 5. CLOCKS
- 6. ZYNQ 1
- 7. ZYNQ 2
- 8. ZYNQ 3
- 9. VERNIER A
- 10. VERNIER B
- 11. VERNIER C
- 12. VERNIER D
- 13. OUTPUT A, B
- 14. OUTPUT C, D
- 15. GATE, CLOCK I/O
- 16. COMMUNICATIONS
- 17. DACS, BIST
- 18. MEMORIES
- 19. POWER SUPPLIES 1
- 20. POWER SUPPLIES 2
- 21. ANDOR OPTION

ENGINEER C.D/J.L/M.G.	DATE 1/23/2024	HIGHLAND TECHNOLOGY INC.	
DRAWN CD/SY	1/24/2024	SCHEMATIC, T662 EMBEDDED DDG MODULE	
CHECKED			
APPROVED J.LARKIN	1/21/2024		
RELEASED		DRAWING NO: 28S662	REV: D
		SHEET: 1 OF 21	FILE: 28S662D.sch

UNMARKED PARTS ARE 0603