



SHEETS

1	BLOCK DIAGRAM
2	BUS CONNECTOR
3	FPGA POWER CONFIG
4	FPGA IO NE
5	FPGA IO SW
6	BIST
7	POWER
8	LOCAL_BIST
9	POWER2
10	RELAYS
11	CHANNEL 0 LOAD
12	CHANNEL 0 PWR_ADC
13	CHANNEL 1 LOAD
14	CHANNEL 1 PWR_ADC
15	CHANNEL 2 LOAD
16	CHANNEL 2 PWR_ADC
17	CHANNEL 3 LOAD
18	CHANNEL 3 PWR_ADC
19	CHANNEL 4 LOAD
20	CHANNEL 4 PWR_ADC
21	CHANNEL 5 LOAD
22	CHANNEL 5 PWR_ADC
23	CHANNEL 6 LOAD
24	CHANNEL 6 PWR_ADC
25	CHANNEL 7 LOAD
26	CHANNEL 7 PWR_ADC
27	CPU COOLER

1_BLOCK_DIAGRAM

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ENGINEER J.L/R.G	DATE 10/2/2023	HIGHLAND TECHNOLOGY INC.	
DRAWN S.Y.	11/29/2023	SCHEMATIC, P945 LOAD MODULE	
CHECKED			
APPROVED			
RELEASED		DRAWING NO: 23S945	REV: B
SHEET: 1 OF 27 FILE: 23S945B.sch			