

## SHEETS

- 1 BLOCK DIAGRAM
- 2 CHANNELS 0-5
- 3 CHANNELS 6-11
- CHANNELS 12-17
- CHANNELS 12 17
- 5 CHANNELS 18-23
- CHANNELS 24-29
- 7 CHANNELS 30-35
- 8 CHANNELS 36-41
- 9 CHANNELS 42-47
- 10 BIST DRIVERS 0-11
- 11 BIST DRIVERS 12-23
- II DIST DINIVERS 12 20
- 12 BIST DRIVERS 24-35
- 13 BIST DRIVERS 36-47
- 14 CLAMPS 1
- 15 CLAMPS 2
- 16 FPGA 1
- 17 FPGA 2
- 18 VME BUS 1
- 19 VME BUS 2 & FLASH
- 20 VME P2
- 21 POWER & LEDs

BLOCK DIAGRAM

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ENGINEERING CHANGE ORDERS MAY APPLY

		ENGINEERING CHANGE ORDERS MAT AFFET		
ENGINEER	DATE	LUCIU AND TECHNOLOGY	, 1710	
J LARKIN	7/31/14	HIGHLAND TECHNOLOGY	INC.	
DRAWN L LARKIN	7/31/14	SCHEMATIC, V280		
CHECKED		l <u> </u>		
		ISOLATED DIGITAL INPUT M	ODULE	
APPROVED				
		drawing no: 22S280	PEV. B	
RELEASED		DRAWING NO: 225280   REV: B		
		SHEET: 1 OF 21 FILENAME:22	S280B.SCH	