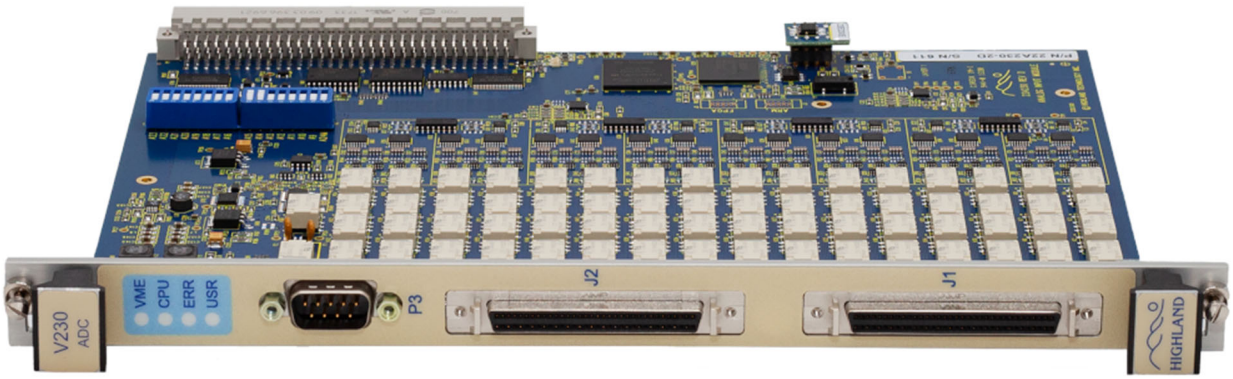
HIGHLAND TECHNOLOGY

V230

64-CHANNEL VME

ANALOG INPUT MODULE



Technical Manual

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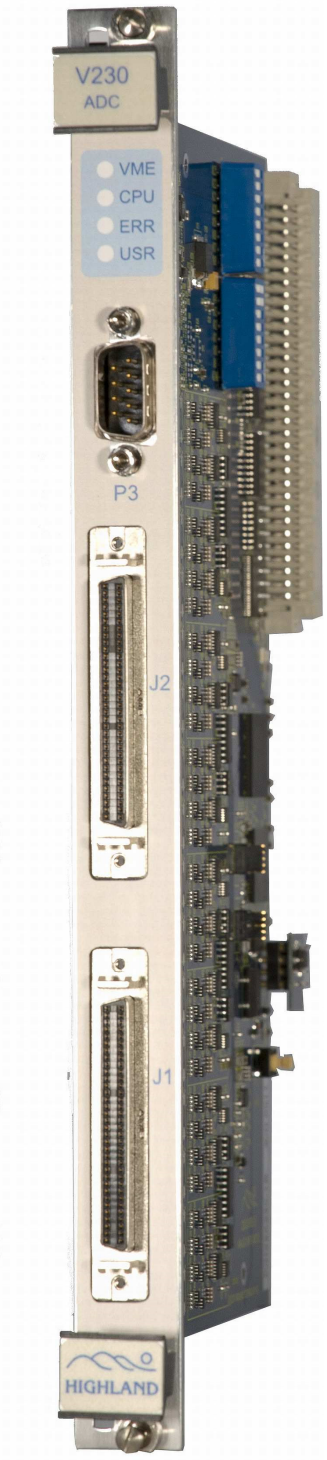


This is the manual for the V230, a 64 channel analog-to-digital converter VME module.

Features of the V230 include:

- Multiplexed, 64-channel differential A/D converter
- Each channel is independently programmable for input range and digital lowpass filtering
- Input ranges of ± 102.4 mV, ± 1.024 volts, and ± 10.24 volts with 16-bit resolution
- Common-mode rejection 80 dB typ, ± 12 volt common-mode range
- Overload protected to ± 30 volts on all ranges
- 15.625 KHz sample rate per channel, 1M s/s total
- Programmable 200 Hz and 17 Hz filters. The 17 Hz filter notches 50/60 Hz and all harmonics
- No realtime handshaking is required. Once channel parameters are set up, measurements appear in dual-port memory registers with VMEbus-speed access. Users can read digitized data at any time.
- Optional test connector supports in-crate calibration check
- Clearly labeled dipswitches set VME address; no jumpers, headers, or trimpots
- Optional built-in self-test (BIST)

2 Specifications: V230 Analog Input Module

FUNCTION	64-channel differential analog-to-digital converter
DEVICE TYPE	16-bit VME register-based slave: A24:A16:D16; Implements 256 16-bit registers at switch selectable addresses in the VME 16 or 24 bit addressing spaces
CHANNELS	64, fully differential
RANGES	Programmable per channel ±102.4 mV ± 1.024 V ± 10.24 V
RESOLUTION	16 bits, 3.125 µV on 102.4 mV range
SAMPLE RATE	Fast mode: 15.625 ksps/channel Slow mode: 976.56 sps/channel
INPUT IMPEDANCE	2 MΩ min, either input to ground
INPUT COMPLIANCE	±12V either input to ground
ACCURACY[1]	±10.24 V range: ± 5 mV ±1.024 V range: ± 0.5 mV ±102.4 mV range: ± 0.3 mV
CMRR	80 dB typical
FILTERING	Programmable per channel: none, 200 Hz Bessel lowpass filter, or 17 Hz sinc² filter with notches at 50/60 Hz and harmonics
PROTECTION	± 30 volts continuous, ±80 volts for 10 µs, any input to ground
OPERATING TEMPERATURE	0 to 60°C; extended MIL/COTS ranges available
CALIBRATION INTERVAL	Two years

[1] Accuracy specifications are guaranteed only when adjacent channels are not overloaded. See section 5.4 for more information.

POWER	VME supplies: + 5 volts, 0.8 amp max +12 volts, 200 mA max -12 volts, 200 mA max
CONNECTORS	Two 68-pin female SCSI connectors (MD68) for channels D9 male for test (not connected on -1 version)
INDICATORS	LEDs indicate VME access, CPU activity, error conditions; additional LED is user programmable
PACKAGING	6U single-wide VME module
CONFORMANCE	ANSI/VITA 1-1994 (R2002) VMEbus spec; does not support byte writes

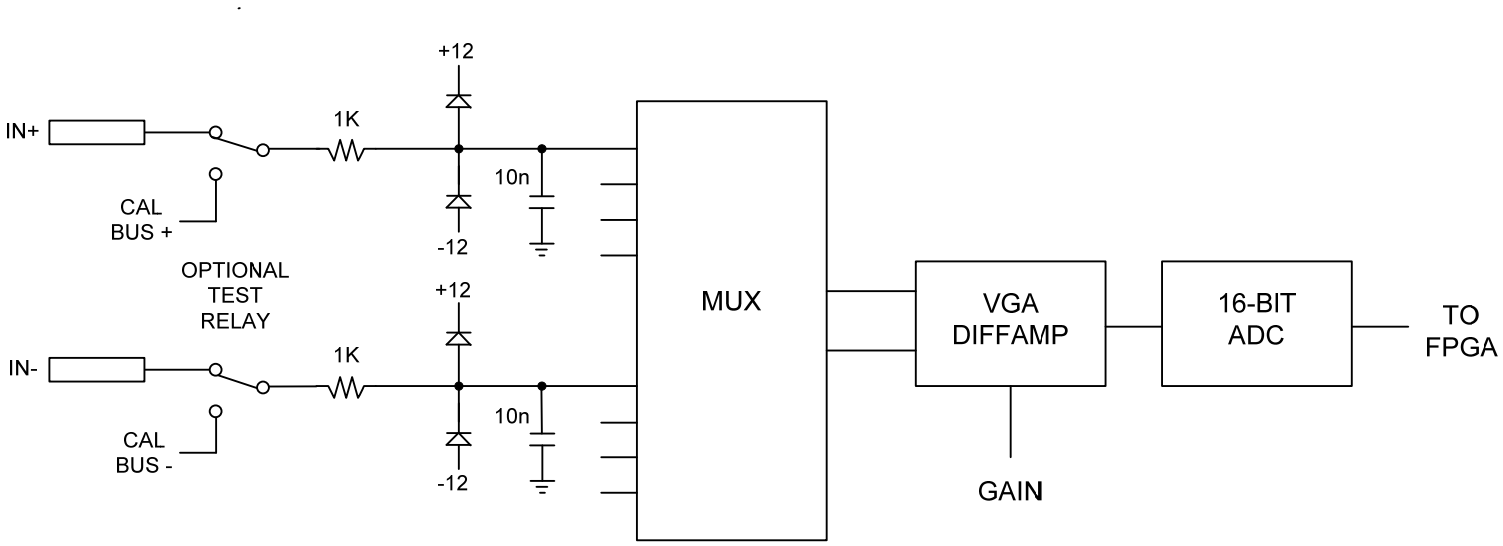
3 Overview

The V230 provides 64 independent differential analog inputs, multiplexed into 16-bit analog-to-digital converters. Each channel is digitized at a rate of 15.625 KHz.

Each channel includes

- Optional BIST/CAL relay
- Input protection
- Analog multiplexer
- Variable-gain differential amplifier
- 16-bit A/D converter
- Digital signal processing

The equivalent circuit of one channel is shown below:



CAUTION: V230 differential inputs have approximately 2 MΩ impedance to ground. If connected to floating sources, users should provide a DC path to ground to prevent leakage currents and hum from producing excess common-mode voltages.

4 Connectors and Installation

4.1 Address DIP Switches

The V230 appears as 256 16-bit registers in the VME 16 or 24-bit addressing spaces. The base address of the 256 registers is set by dip switches.

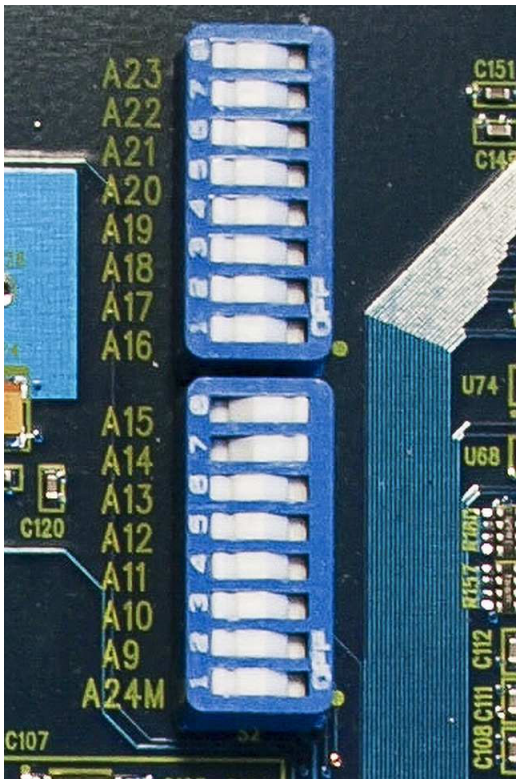
Two rocker-type dipswitches are provided near the top right corner of the board. They are labeled, top to bottom, "A23" through "A9" and finally "A24M".

To set a switch to the logical "1" or "ON" position, press the side of the switch nearest its "Axx" lettering. Use a toothpick or paper clip, not a pen or pencil.

The A24M switch, when set, allows the board to operate in the VME 24-bit (A24) address space; in this case, all address switches are active and the board responds to VME address modifier codes 0x39 and 0x3D.

If the A24M switch is off, the module resides in the A16 space and responds to address modifiers 0x29 and 0x2D. In this case, only address switches A15 through A9 are active.

Units are shipped with switches A15 and A14 on, all others off, locating the register base at 0xC000 in the A16 space, as shown below.



Address DIP Switch

4.2 Installation

The V230 may be installed in any standard 6U VME crate, including VME64 variants. It supports 16-bit data transfers using the P1 connector.

The V230 passes all interrupt and bus grant signals, and may be used with backplane grant jumpers installed or not installed.

CAUTION: Do not install or remove the V230 with crate power on. VME modules are not hot-pluggable. The V230 will be damaged if hot-plugged.

CAUTION: Fully seat the module and secure front-panel screws before applying power.

CAUTION: Handle the V230 with proper ESD precautions to avoid static damage.

CAUTION: V230 differential inputs are high impedance. If connected to floating sources, users should provide a DC path to ground to prevent leakage currents and hum from producing excess common-mode voltages.

4.3 Channel Input Connectors

4.3.1 SCSI

Two front-panel female 68-pin SCSI connectors are provided. Pinout is as follows:

Channel	Connector	V+ Pin	V- Pin
0	J1	1	35
1	J1	2	36
2	J1	3	37
3	J1	4	38
4	J1	5	39
5	J1	6	40
6	J1	7	41
7	J1	8	42
8	J1	9	43
9	J1	10	44
10	J1	11	45
11	J1	12	46
12	J1	13	47
13	J1	14	48
14	J1	15	49
15	J1	16	50
16	J1	19	53
17	J1	20	54
18	J1	21	55
19	J1	22	56
20	J1	23	57
21	J1	24	58
22	J1	25	59
23	J1	26	60
24	J1	27	61
25	J1	28	62
26	J1	29	63
27	J1	30	64
28	J1	31	65
29	J1	32	66
30	J1	33	67
31	J1	34	68
32	J2	1	35
33	J2	2	36
34	J2	3	37

Channel	Connector	V+ Pin	V- Pin
35	J2	4	38
36	J2	5	39
37	J2	6	40
38	J2	7	41
39	J2	8	42
40	J2	9	43
41	J2	10	44
42	J2	11	45
43	J2	12	46
44	J2	13	47
45	J2	14	48
46	J2	15	49
47	J2	16	50
48	J2	19	53
49	J2	20	54
50	J2	21	55
51	J2	22	56
52	J2	23	57
53	J2	24	58
54	J2	25	59
55	J2	26	60
56	J2	27	61
57	J2	28	62
58	J2	29	63
59	J2	30	64
60	J2	31	65
61	J2	32	66
62	J2	33	67
63	J2	34	68
GND	J1	17	51
GND	J1	18	52
GND	J2	17	51
GND	J2	18	52

The eight GND pins listed above are PCB/VME backplane grounds. Connector shells are bonded to the VME front panel, which connects to the crate frame through the module securing screws.

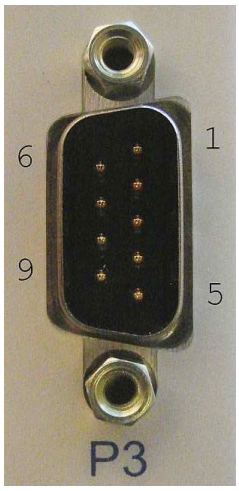
Highland can furnish SCSI cable assemblies and screw-type termination panels. See Chapter 8: Accessories.

4.4 Optional D9 Calibration Connector

A male D9 connector is provided on the V230-2 modules, which is supplied with the BIST option. It allows for connection to an external precision voltage source or DVM, allowing verification of module calibration without removing field-wiring connectors. Each input channel incorporates a relay which allows it to be switched, under software control, to this test connector.

Pinout of the D9 connector is:

P3-7	CalSig+
P3-6	CalSig-
P3-5	VME GROUND



An external voltage source may be connected to Pins 7 and 6, and one or more channel relays activated to allow channels to measure the test source instead of its normal input. If no other path exists from the test supply to ground, it is recommended that its low side be connected to P3-5 in order to establish a solid common-mode reference.

Modules equipped with BIST can also internally generate test voltages that can be applied simultaneously to the D9 test connector and to the internal cal bus. This allows channel calibration verification using an external voltmeter.

The RELAYS register is used to control the channel test relays and the MODE register controls access to the cal bus. For example, writing value 7 to RELAYS and 1 to MODE will connect the external test source to the input of channel 7.

See sections 6.2.2, 6.2.4, and 7.3 for details of channel test switching.

5 Operation

5.1 LEDs

There are four front-panel LED indicators.

The blue VME led flashes whenever the module is accessed from the VME bus.

The green CPU led flashes about once a second to indicate CPU activity

The red ERR led will flash to indicate errors:

One blink	Channel Configuration Error
Two blinks	Calibration table error; default calibrations are in use
Three blinks	Power supply or BIST error
Four blinks	FPGA error; module may not respond to the VME bus

The orange USR led displays a user-defined blink pattern. See section 6.2.3

There is an additional LED on the PCB surface which illuminates green when the FPGA is properly configured.

5.2 Powerup Defaults

At powerup or following a reboot macro, the module setup will be:

All channels on ± 10.24 volt ranges

All digital filters off; channels at full bandwidth

RELAYS, MODE, and BMUX registers clear

ULED led control register clear

The red ERR LED will be on at powerup, and will go off in about 5 seconds when the module is properly initialized.

Users can immediately read input voltages in the 64 RDAT0 through RDAT63 (signed, 16 bit) realtime data registers.

Powerup or reboot takes about 5 seconds.

The power supply self-test is run at powerup; see section 7.4.

5.3 Quick Start Procedure

Basic operation of the V230 can be demonstrated by the following steps:

A 6U VME crate and computer interface are required. The crate must be compliant with the IEEE 1014 VME specification, or the equivalent ANSI/VITA 1-1994 (R2002) VMEbus spec. Any crate with the standard power supplies (+12, +5, -12) and the 16-bit "P1" bus is adequate.

The computer interface must allow, as a minimum, reading and writing 16-bit registers in the A16 or A24 address spaces.

Pick an address space and module base address and set the V230 dip switches accordingly. See section 4.1. The as-shipped default is address 0xC000 in the 16-bit address space.

With crate power off, insert the V230 into any crate slot and firmly secure its mounting screws. **Do not hot-plug VME modules.**

Power up. After a few seconds, the V230 green "CPU" LED should flash, and the other LEDs should be off.

Now run software that can display the contents of VME registers.

Read the manufacturer ID register, the16-bit VME register at the module base address. The default address would be 0xC000. The blue "VME" LED should flash, and the register value should be 0xFEEE, identifying this as a Highland VME module.

Read the next register, offset address 2, default 0xC002. It should read 22230 decimal, 0x56D6, identifying the module as a V230.

The module powers up digitizing all analog inputs, all on their ± 10.24 volt ranges.

Read the RDAT0 register, register 128, offset address 0x100, default address 0xC100. This represents the differential voltage applied to channel 0 at J1 pins 1 and 35. If the register value is "N", and is interpreted as a signed 16-bit value from -32768 (0x8000) to +32767 (0x7FFF), the voltage is

```
V = N * 10.24 / 32768
```

The other channel voltages can be read in the RDAT1 through RDAT63 realtime data registers, as mapped in section 6.1.

Channel ranges and filter settings can be changed by writing to the channel control registers; see section 6.2.9.

5.4 Overloading Channels

Due to the multiplexed architecture of the V230, when one channel is badly overloaded it can cause measurement errors on other channels in the same multiplexing bank. For instance, a channel programmed to the ± 102.4 mV range with 10V applied to the input can cause up to 1 mV of error on the next channel acquired.

This issue affects other channels sharing the same multiplexing bank, each of which is 8 channels. The issue is of diminishing effect from the overloaded channel as banks are swept through in increasing sequence, modulo 8. So, channels 0-7 are one bank, 8-15 the next, etc. An overload on channel 5 will have most impact on channel 6, then roughly half as much on channel 7, less still on channel 0, less still on channel 1, etc.

Bleedthrough to adjacent channels begin at over twice the maximum readable value for the channel, and starts to become appreciable at about fivefold. No bleedthrough occurs inside a channel's range;

The first and most obvious solution is, of course, to not overload the channels. Should it be likely that a channel would be overloaded, it could instead be changed to use a higher voltage range on which it would not.

If this is not an option, the other solution is to slow the V230 scan rate. This allows the amplifiers to settle out and fully recover from the overload before proceeding on to sample the next channel.

In order to do this, set the SLOW bit (bit 8, 0x100) of the MODE register (offset 0x1A). This will reduce the scan rate by a factor of 16 across the entire module, to 976.6 Hz/channel, and reduce the maximum bleed to under 100 µV.

Use of the SLOW bit will not affect the frequency responses of the optional digital filters, which will continue to behave in the same manner regardless of the setting of the SLOW bit.

6 VME Registers

The V230 implements 256 16-bit VME registers. REG# below is the ordinal register number in decimal; OFFSET is the hex VMEbus offset from the module base address.

Registers identified as "RO" should be treated as read-only and should not be written from VME; these registers are periodically refreshed by the internal microprocessor.

Read-write (RW) registers are written and read back by VME and, after powerup initialization, are not altered by the internal microprocessor.

"Read-write + macro" registers (RWM) can be written and read by the user, but may also be changed by the V230 in response to a user executed MACRO command. A macro handshake protocol is defined in section 6.2.7.

Registers tagged **#** are serviced by FPGA logic at VMEbus speed.

Registers tagged **B** are provided on modules with the BIST option.

See section 6.3 for comments on realtime issues.

6.1 VME Register Map

Reg Name	REG#	Offset	R/W	Function	# B
VXI MFR	0	0x00	RO	Highland ID: reads 65262, xFEEE	
VXI TYPE	1	0x02	RO	V230 module ID, 22230, 0x56D6	
SERIAL	3	0x06	RO	unit serial number	
ROM ID	4	0x08	RO	firmware ID, typically 22230 decimal	
ROM REV	5	0x0A	RO	firmware revision, typically ASCII "A"	
MCOUNT	6	0x0C	RO	microprocessor IRQ update counter	
DASH	7	0x0E	RO	module version (dash) number	
SCAN	8	0x10	RO	ADC scan counter	#
RELAYS	11	0x16	RW	controls optional cal-bus relays	B
ULED	12	0x18	RW	user LED control	
MODE	13	0x1A	RW	module operating mode	B
CALID	14	0x1C	RO	calibration table status	
CHER	15	0x1E	RO	channel configuration error ID	
MACRO	16	0x20	RWM	macro command register	
PARAM0	17	0x22	RWM	macro parameter	
PARAM1	18	0x24	RWM	macro parameter	
PARAM2	19	0x26	RWM	macro parameter	
YCAL	20	0x28	RO	calibration date: year	
DCAL	21	0x2A	RO	calibration date: month/day	
BERN	22	0x2C	RO	optional BIST error count	B
BMUX	23	0x2e	RW	optional BIST mux control	B
CTL0	64	0x80	RW	channel 0 control	
CTL1	65	0x82		channel 1 control	
...					

Reg Name	REG#	Offset	R/W	Function	# B
CTLn	64+n				
...					
CTL62	126	0xFC		channel 62 control	
CTL63	127	0xFE		channel 63 control	
RDAT0	128	0x100	RO	channel 0 realtime data	#
RDAT1	129	0x102	RO	channel 1 realtime data	#
...					#
RDATn	128+n				#
...					#
RDAT62	190	0x17C	RO	channel 62 realtime data	#
RDAT63	191	0x17E	RO	channel 63 realtime data	#
BIST0	192	0x180		BIST reporting region	B
...	...				B
BIST31	223	0x1BE			B
PERR	240	0x1E0	RO	power supply error flags	B
EP1	241	0x1E2	RO	+1.2V power supply voltage	B
EP2	242	0x1E4	RO	+2.048	B
EP2.5	243	0x1E6	RO	+2.5	B
EP3	244	0x1E8	RO	+3.3	B
EP5	245	0x1EA	RO	+5	B
EP15	246	0x1EC	RO	+15	B
EM15	247	0x1EE	RO	-15	B
UTEST	254	0x1FC	RW	user read/write test register	
HTEST	255	0x1FE	RO	always reads 0xABCD	

6.2 Detailed Register Descriptions

6.2.1 Module Overhead Registers

A number of read-only overhead registers are provided.

Name	Offset	Description
VXI MFR	0x000	Always reads 0xFEEE, Highland's registered VXI module ID code.
VXITYPE	0x002	always reads 22230 decimal to identify a V230 module
SERIAL	0x006	module serial number.
ROM ID	0x008	firmware version, typically 22230 decimal
ROM REV	0x00A	ASCII code identifying the revision letter of the firmware, typically 0x0041, ascii "A"
MCOUNT	0x00C	a 16-bit counter that is incremented by the internal microprocessor at about 250 Hz.
DASH	0x00E	module version (dash) number.
SCAN	0x010	a 16-bit counter that is incremented each full channel scan, specifically when channel 63 is digitized. It counts at 15.625 KHz.

6.2.2 RELAYS Registers (Offset 0x016)

On V230-2 models, the RELAYS register controls actuation of the optional channel test relays.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0	C		K5	K4	K3	K2	K1	K0

If the MODE register is set nonzero, one channel test relay will be actuated, as selected by the K5...K0 bits. The analog input of the selected channel will then be disconnected from the front-panel SCSI connector and connected to the internal cal bus, which may in turn be driven from the internal BIST voltage generator or from the CALSIG+ and CALSIG- Pins (Pins 7 and 6) of the D9 test connector.

Additionally, each bit B0..B7 actuates a group of 8 channel relays as follows:

B0 Channels 0-7
B1 Channels 8-15
B2 Channels 16-23
B3 Channels 24-31
B4 Channels 32-39
B5 Channels 40-47
B6 Channels 48-55
B7 Channels 56-63

Setting these bits will turn on all of the associated channels at once, in addition to whatever channel is specified by the K bits.

The C bit overrides the K and B bits. If the C bit is nonzero, then all channels with the K bit set in their control registers will be selected simultaneously.

Upon altering the RELAYS register it may take up to 25 milliseconds before all relay contact changes have settled.

6.2.3 ULED - User LED Control (Offset 0x018)

An orange LED is provided on the front panel for user application. The ULED register allows user flash patterns to be loaded. An internal shift register is periodically loaded from the contents of the ULED register, and the MS bit of this register operates the orange LED. The shift register is left-shifted every 125 milliseconds, and the register is reloaded every 16 shifts, namely every 2 seconds.

ULED pattern 0x0000 turns the user LED off. Pattern 0xFFFF turns it steady on.

6.2.4 MODE – Module Control (Offset 0x01A)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							SLOW							C1	C0

If V230 channels may be subjected to

V230 modules furnished with the BIST option include an internal calibration bus and the BIST test voltage generator. The MODE register controls routing of signals between the front-panel D9 connector, the cal bus, and the BIST source.

The mapping of MODE values is...

```
0     Off             D9 and BIST are disconnected;
                      All channel test relays are off.

1     Channel Test    The D9 connector drives the cal bus
```

2	BIST drive	The BIST voltage generator drives the cal bus, with voltage set by the BMUX register
3	Both	Both the D9 connector and the BIST source are connected to the cal bus.

In mode 1, users may apply an external voltage to the D9 connector pins 7 and 6, and those signals are connected to cal bus lines CAL+ and CAL- respectively. Now any channel whose test relay is activated will digitize the test voltage.

Mode 2 will apply an internally-generated test voltage to the cal bus, as selected by the BMUX register. See section 7.3.

In mode 3, the BIST voltage is applied to the cal bus and the D9 path is enabled. This outputs the BIST test voltage to the D9, so that an external, traceable DVM may be used to verify channel calibrations without the need for an external voltage source. See section 7.3.

A mode change may take up to 25 milliseconds.

6.2.5 CALID, YCAL, DCAL - Calibration Status Registers

The CALID register (offset 0x01C) displays a value which reflects the currently installed calibration table. The normal value is 22230 decimal, 0x56D6. If the factory calibration table is corrupted, the firmware will install the default calibration table, the CALID register will display value 0xDEFC and the red LED will flash three times every few seconds..

YCAL (offset 0x028) and DCAL (offset 0x02A) display the last date of module calibration. YCAL is the year, as an integer, such as 2011 decimal. The high byte of DCAL (bits 15..8) is month 1-12, and the low byte (bits 7..0) is day 1-31. The recommended factory recalibration interval for the V230 is one year.

6.2.6 BIST Registers

See section 7 for description of the various BIST registers.

6.2.7 MACRO, PARAMx - Macro Controls (Offsets 0x020-0x026)

The macro control register allows the execution of microprocessor routines which perform calibration and test tasks. Some macros also take a parameter in the PARAM0 register. PARAM1 and PARAM2 are currently unused.

To execute a macro, verify that the MS bit (bit 15) of the MACRO register is clear, then write any required parameter into PARAM0 and then write a macro code to the MACRO register. Wait until the MS bit of MACRO self-clears.

The MACRO codes are...

```
0x8400    no-op dummy macro

0x8401    run full BIST; see section 7.1

0x8407    Reboot. The module will disappear from
          the VME bus for about 5 seconds.

0x8408    self-test one channel. PARAM0 is channel
          number. See section 7.2.

0x8409    power supply test. See section 7.4.
```

The power supply test, macro 0x8409, is available on all versions of the V230.

6.2.8 CHER - Channel Setup Error ID (Offset 0x01E)

The CHER register displays the channel number of any channel which has a setup error, namely a channel whose channel control register is programmed incorrectly. If multiple channels are in error, only the first channel number will appear. If no channel setup errors exist, the value of this register will be -1, 0xFFFF.

If one or more channels have setup errors, the red ERR front-panel LED will flash twice every few seconds.

6.2.9 Channel Control Registers (Offset 0x080, 0x082 … 0x0FE)

Each of the 64 input channels has a channel control register, CTL0 through CTL63.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							K			F1	F0			RN1	RN0

If the K bit is set, and the RELAYS register has its C bit set, the corresponding channel test relay will be actuated.

The RN bits select the input range for this channel, with the two RN bits encoded 0 through 3. Ranges are:

RN Code	Range	Approx LSB Resolution
0	reserved	
1	± 102.4 mV	3.125 µV
2	± 1.024 V	31.25 µV
3	± 10.24 V	312.5 µV

The power-up default is 3, selecting the ± 10.24 volt range.

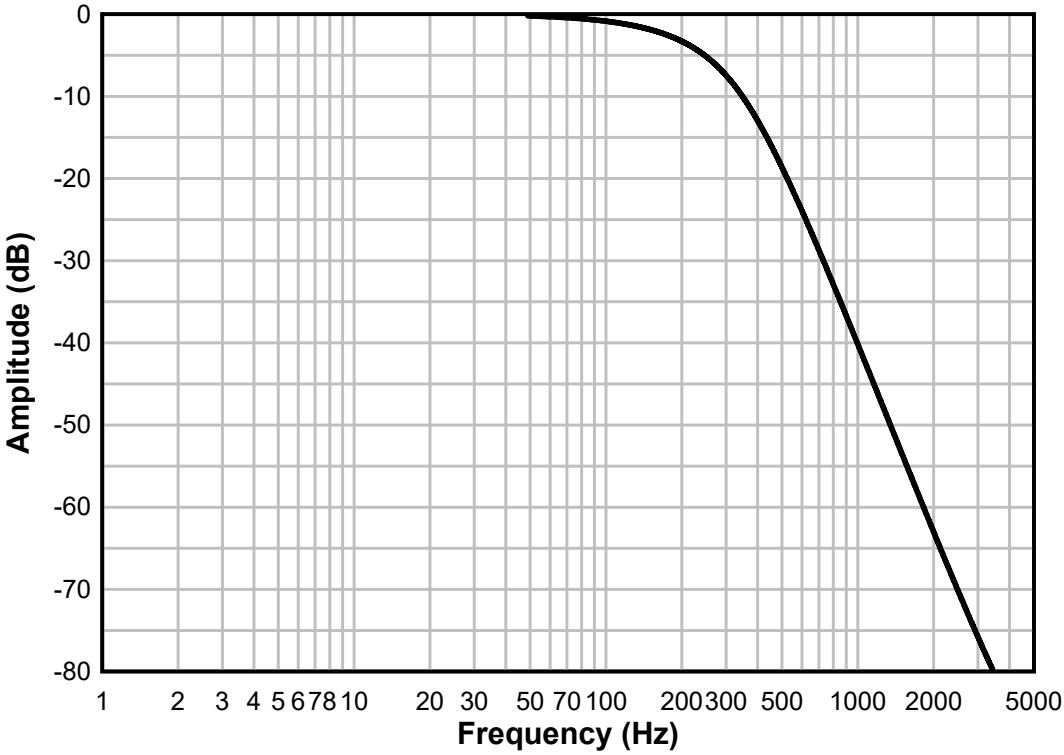
The F bits select the filtering for this channel, with the bits encoded 0 to 3. Filter choices are:

RN Code	Filter Selection
0	No filtering
1	200 Hz Bessel filter
2	17 Hz sinc² filter
3	reserved

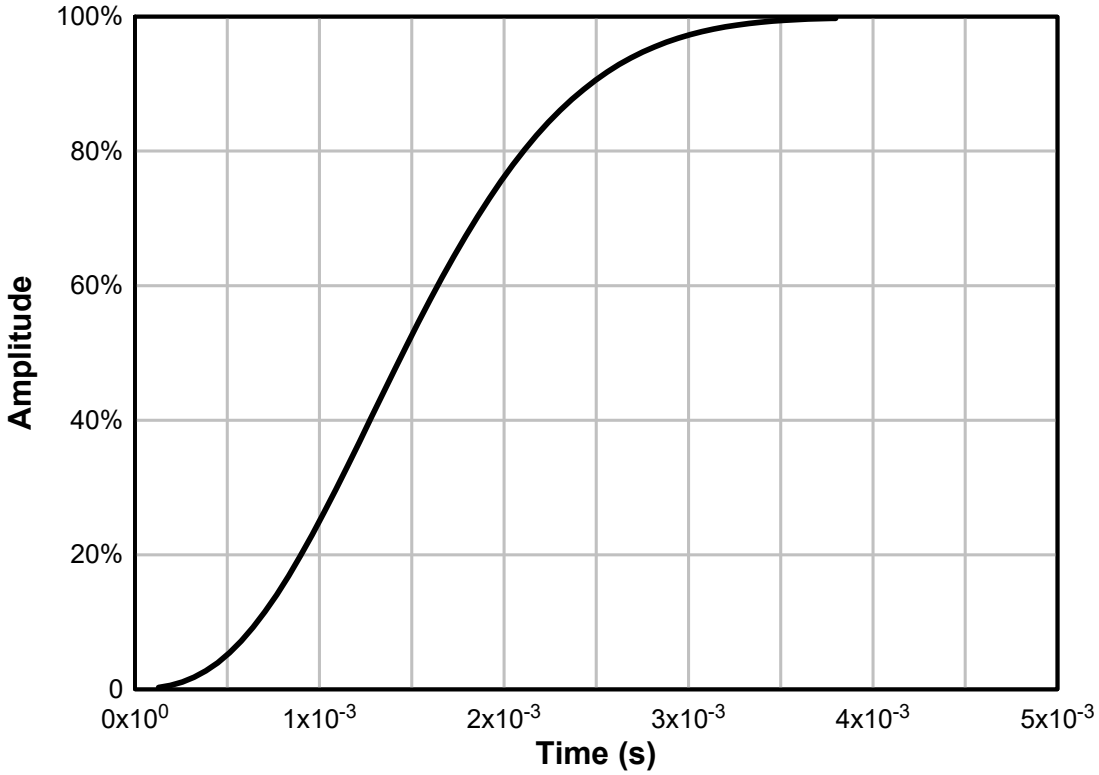
Both filter selections have linear phase and no overshoot. The Bessel filter provides some smoothing for data that may have fast transients. The sinc² filter is applied on top of the Bessel filter, and provides substantially more aggressive filtering, with excellent noise rejection at all power line harmonic frequencies.

Frequency and step responses for both filters follow.

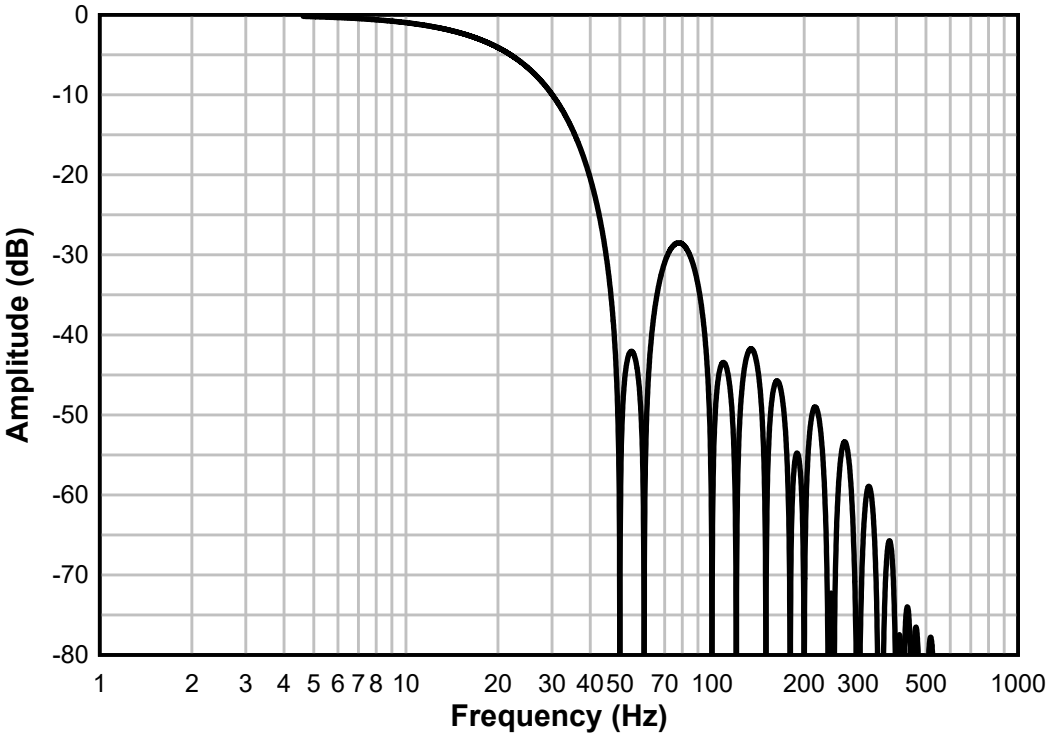
200 Hz Bessel Filter



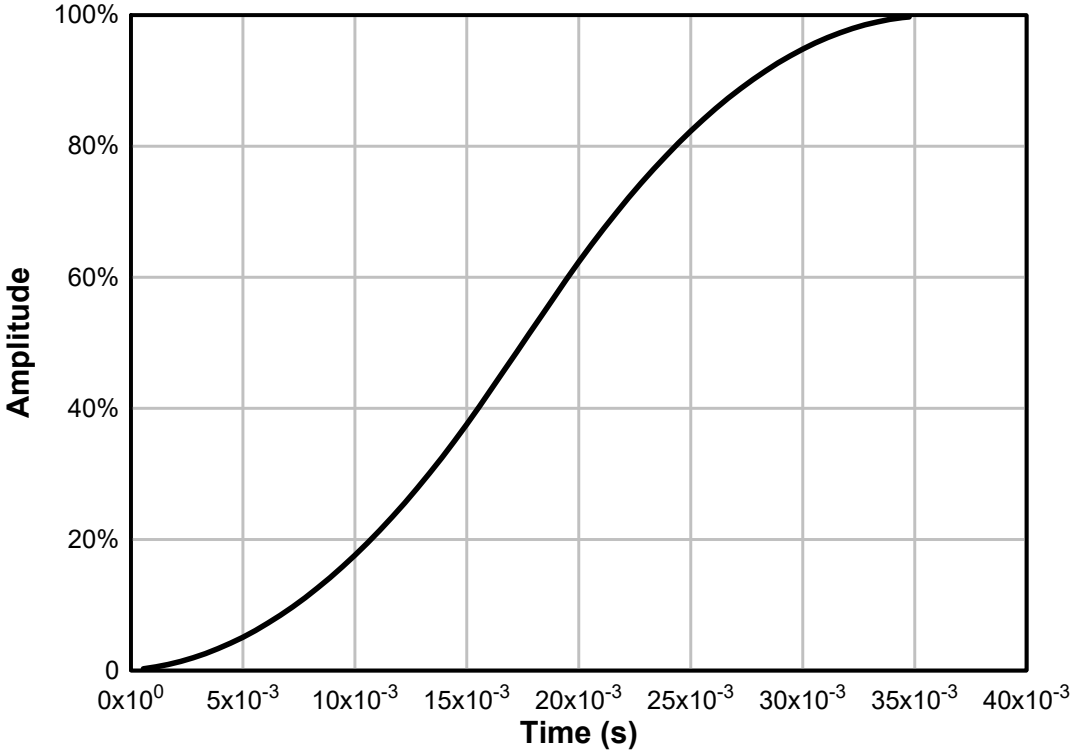
200 Hz Bessel Filter



17 Hz sinc^2 Filter



17 Hz sinc^2 Filter



6.2.10 Channel Realtime Data (Offset 0x100, 0x102 … 0x17E)

Each of the 64 input channels has a realtime data register RDATn. This register is loaded with ADC data, optionally lowpass-filtered, sampled at the 15.625 KHz channel sample rate. An RDAT register may be read at any time and returns the latest analog sample. The value is interpreted as a signed 16-bit integer which spans the full bipolar range of the current ADC range. If one reads signed 16-bit integer N from this register, the actual voltage is

```
V = Range * N / 32768
```

where Range is 10.24, 1.024, or 0.1024 volts

For example, on the ±10.24 volt range,

```
 32767     0x7FFF    is   +10.239688  volts
     1     0x0001    is    +0.0003125 volts
     0     0x0000    is     0         volts
    -1     0xFFFF    is    -0.0003125 volts
-32767     0x8001    is   -10.239688  volts
-32768     0x8000    is   -10.2400    volts
```

6.3 Realtime Considerations

When programming the V230, some VME register writes are serviced in FPGA hardware and some are processed by the on-board microprocessor. Registers tagged # in the register listing are hardware processed and their functions take place immediately when a register is written. Other VME registers are dual-port memory serviced by the uP. The microprocessor normally services these registers about every 2.5 milliseconds.

Changes in channel control registers or the RELAYS or MODE registers may take up to 25 milliseconds to settle.

Channel realtime data registers are updated as the multiplexed channels are digitized.

VMEbus response time (DS0* to DTACK*) averages about 125 ns.

7 BIST

The V230-2 version is equipped with the optional BIST facility. This includes the D9 test connector, internal calibration bus, BIST voltage generator, and 64 channel test relays.

Such V230 units are capable of connecting one or multiple channel inputs at a time to the internal calibration bus. The CAL bus may in turn be connected to the D9 test connector, the internal BIST voltage generator, or both. This allows users to apply known voltages to the channels and verify calibration, or to use an external DVM to verify channel calibration. This facility is controlled by the MODE and RELAYS registers, as noted in sections 6.2.2 and 6.2.4.

Internal self-test verifies reasonable channel performance for all ranges of all channels. Tests measure offset at zero input, gain near positive full scale and negative full scale, and verify common-mode rejection.

Formal calibration verification requires that an external, NIST-traceable precision voltage source be connected to the D9 test connector and then to individual channel inputs. The MODE register also allows the internal BIST voltage generator to drive the internal cal bus and, if desired, also drive the D9 test connector. This allows the V230 to internally generate channel test voltages which can be measured with an NIST-traceable digital voltmeter.

7.1 Full BIST

To invoke the full automated BIST sequence, verify that the MS bit of the MACRO register is clear, then write 0x8401 to MACRO. Wait until the MS bit of MACRO clears, then read the BIST error counter register BERN. Execution time will be about 20 seconds.

If any errors are reported in the BERN register, read the channel BIST status bytes beginning at address BFLAG0, corresponding to channels 0 through 63. A zero value indicates no channel errors. Note that even-numbered channel BIST bytes are located in bits 15..0 of a VME word, and odd=channel bytes are in 7..0.

The BFLAGn byte register format is....

7	6	5	4	3	2	1	0
CER	NER	PER	ZER		RA2	RA1	RA0

The RA0 through RA2 bits flag errors detected on gain ranges 0 through 2 respectively.

ZER is set if there was excessive zero offset on any range.

PER flags a gain error on any range with the input near positive full-scale.

NER flags a gain error on any range with the input near negative full-scale.

CER indicates insufficient common-mode rejection on any range, or an input impedance error.

Full BIST also runs the power supply self-test, reporting supply voltages, updating the VPERR error flags register, and counting any supply errors in BERN. See 7.4.

7.2 Single-channel Self-Test

To test a single channel, verify that the MS bit of the MACRO register is clear, then write the channel number (0..63) to the PARAM0 register, then write 0x8408 to the MACRO register. Wait until the MS bit of MACRO clears, then read the BIST error counter register BERN. Execution time will be about 0.2 second.

The results of the test will be reported in the BIST area of the register map.

The first word, at BIST0, will summarize the results. The LS byte, bits 7..0, are in the same format as the all-channel tests, namely

7	6	5	4	3	2	1	0
CER	NER	PER	ZER		RA2	RA1	RA0

The following 17 words will report actual measurements for the various tests that were run. They are...

REGISTER	RANGE	MEASUREMENT	EXPECTED VALUE
BIST1	0	ZERO	0 ± 326
BIST2	0	+83.1 mV	+26592 ± 326
BIST3	0	-90.5 mV	-28960 ± 326
BIST4	0	+10V CMRR	0 ± 1377
BIST5	0	-10V CMRR	0 ± 1377
BIST6	1	ZERO	0 ± 326
BIST7	1	+911 mV	+29152 ± 326
BIST8	1	-911 mV	-29152 ± 326
BIST9	1	+10V CMRR	0 ± 427
BIST10	1	-10V CMRR	0 ± 427
BIST11	2	ZERO	0 ± 326
BIST12	2	+10.00 V	+32000 ± 326
BIST13	2	-10.00 V	-32000 ± 326

BIST14	2	+10V CMRR	0	± 336
BIST15	2	-10V CMRR	0	± 336

7.3 Background BIST MUX function

On V230-2 modules, when a BIST macro operation is not active, users may control the BIST voltage generator, which allows a selection of signals to be applied to the internal calibration bus. The MODE register controls signal routing when an automatic BIST sequence is not active; see section 6.2.4.

To route the BIST voltage generator test signal to a channel, set the MODE register to 2 or 3 and use the RELAYS register to select the channel whose test relay will connect it to the CAL bus. Mode 2 connects the BIST voltage generator to the internal cal bus. In mode 3, the BIST source drives both the cal bus and the front-panel D9 test connector.

The BMUX register controls the signal applied to the cal bus. The register layout is...

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									H2	H1	H0		L2	L1	L0

where the "H" nibble selects the voltage to be applied to the CAL+ bus, and the "L" nibble selects the voltage to be applied to the CAL- bus. The encoding of both nibbles is...

CODE	VOLTAGE
0	+10.00 V
1	+911 mV
2	+83.1 mV
3	+8.25 mV
4	-10.00 V
5	-90.5 mV
6	+10.00 V through 1 M ohms
7	GND

Example: Set MODE to 3

Set RELAYS to 12

Write 0x0017 to the BMUX register

Now CAL+ will be +911 mV and CAL- will be zero volts. Channel 12 will consequently be disconnected from its normal input and will digitize the +911 mV test voltage. The test voltage can be verified, using an external DVM, at pins 7 and 6 of the front-panel D9 connector.

Note that channels are provided with protective devices which limit input current in over-range conditions. Overdriving channels beyond their programmed voltage range regions can cause current to be drawn from the calibration bus and external cal sources or BIST multiplexers, which could cause unexpected readings.

7.4 Power Supply BIST

The V230 has provision for monitoring its internal power supply voltages. The power supplies are checked when the full BIST test (macro 0x8401) is executed. These tests can also be invoked with the 0x8409 macro. All versions of the V230 can execute the power supply tests.

The PERR register flags power supply voltage errors, and the EP1...EM15 registers report actual supply voltages. BERN counts any errors.

The PERR register layout is...

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									M15	P15	P5	P3	P2.5	P2	P1

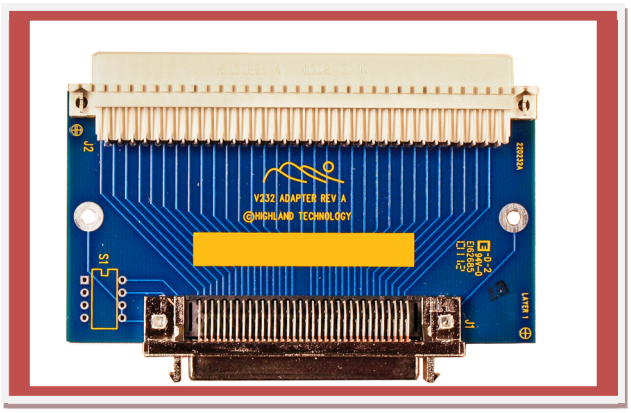
Each bit has a corresponding voltage reporting register. The LSB value is 1 millivolt.

BIT	VOLTAGE	REGISTER
P1	+1.25	EP1
P2	+2.048	EP2
P2.5	+2.5	EP2.5
P3	+3.3	EP3
P5	+5	EP5
P15	+15	EP15
M15	-15	EM15

8 Accessories

8.1 V232 SCSI-DIN Adapter

The V232 SCSI-DIN adapter board can be used by customers looking to migrate legacy DIN connected installations to SCSI connected boards, either to allow the use of the D9 test bus or because SCSI cables are considered more manageable than the ribbon cable associated with the DIN connectors. Used in this capacity, the following two systems would be equivalent as seen from the female DIN connector:



V230-1 or V230-2

↓

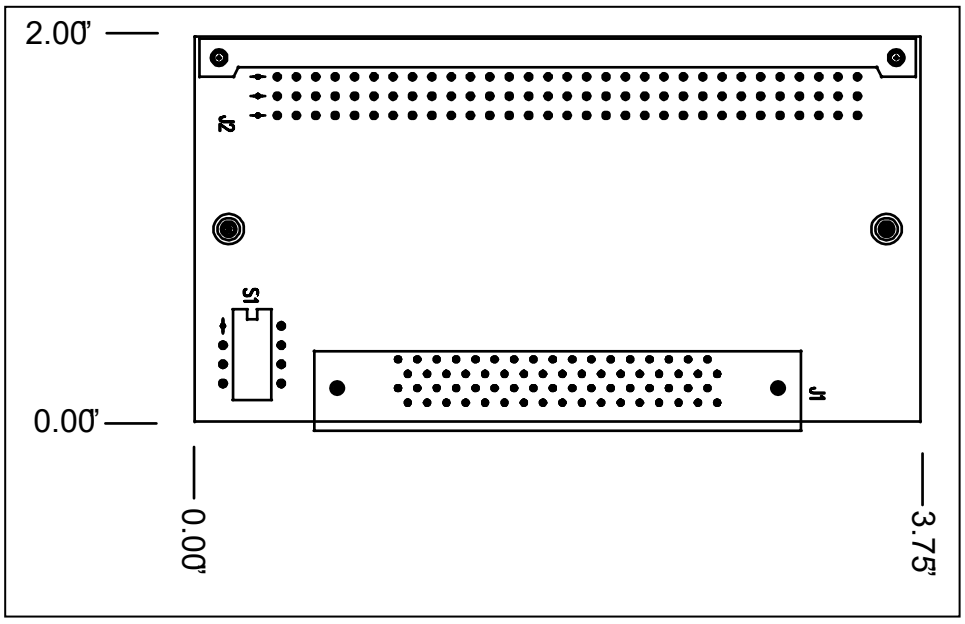
SCSI cable

↓

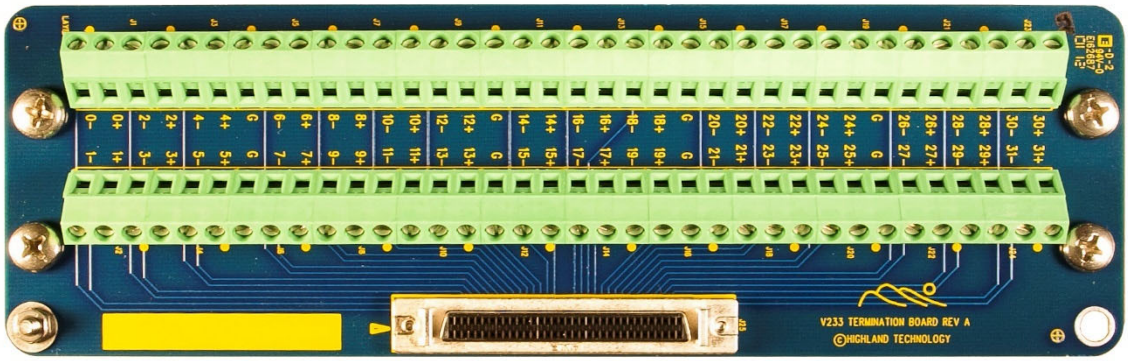
V232

↓

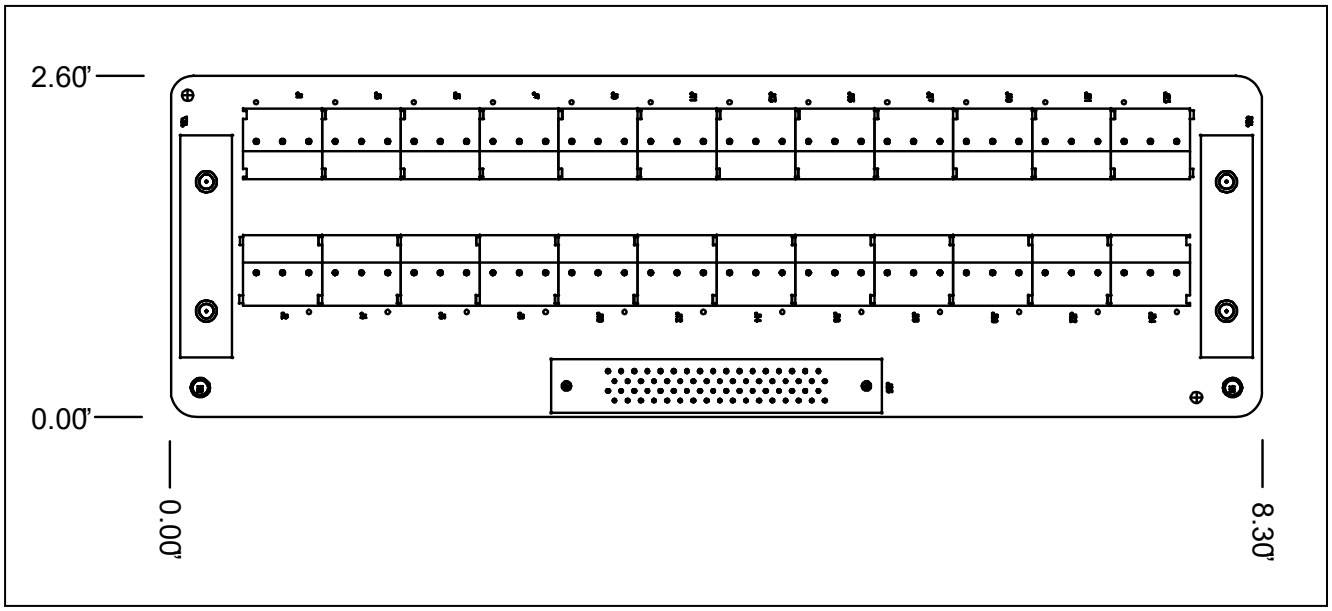
Female DIN on V232



8.2 V233 SCSI Termination Panel



The V233 transitions the 32 differential channels on one V230 SCSI connector to screw terminals. One or two may be connected to a V230. DIN rail clips are provided to allow the panel to be easily mounted.



9 Versions

Standard V230 versions include:

V230-1:	64-channel VME analog input module with two 68-pin female SCSI connectors
V230-2:	64-channel VME analog input module with two 68-pin female SCSI connectors with BIST
V230-11:	64-channel VME analog input module with two 68-pin female SCSI connectors with conformal coating
V230-21:	64-channel VME analog input module with two 68-pin female SCSI connectors with BIST and conformal coating

10 Hardware and Firmware Revision History

10.1 Hardware Revision History

Revision D	October 2017 Fixed a ground loop observed in some VME crates due to connecting the front panel to PCB ground.
Revision C	February 2012
Revision B	October 2011
Revision A	April 2011 Initial PCB release

10.2 Firmware Revision History

The firmware is provided as a plug-in EPROM chip which can be field upgraded. This chip is labeled "230-B". It includes both the microprocessor firmware and the FPGA configuration.

22E230-E	November 2014 Added C bit to RELAYS register and K bit to channel control registers.
22E230-D	May 2014 Fixed bounding errors in filters. Added SLOW bit to the MODE register.
22E230-C	January 2014 Improved BIST testing.
22E230-B	January 2014 Provided BIST functionality.

11 Accessories

J58-1:	3′ 68 pin male SCSI to 68 pin male SCSI
V232-1:	68-pin female SCSI connector to 96-pin female DIN connector adapter cable
V233-1:	32-channel SCSI termination panel