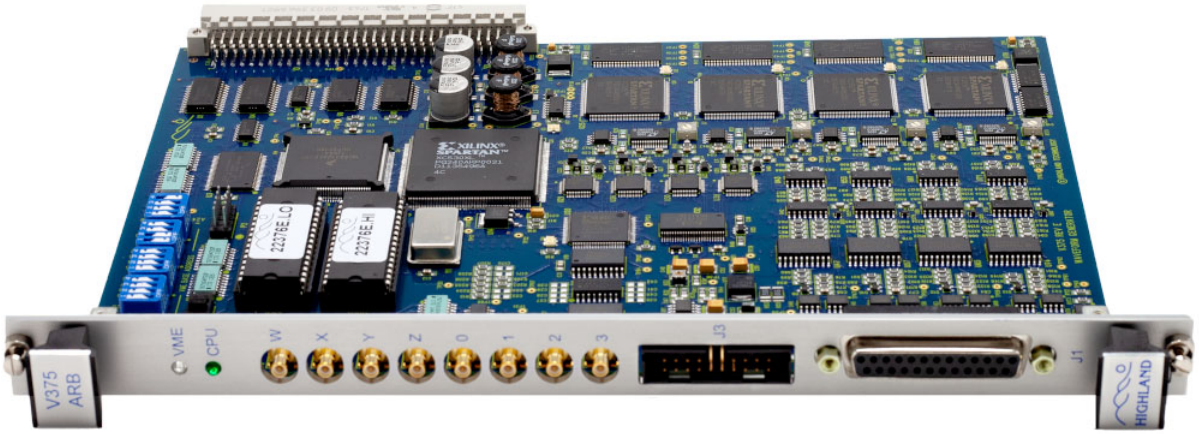
HIGHLAND TECHNOLOGY

V375

4-CHANNEL VME

WAVEFORM GENERATOR



Technical Manual

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1. Introduction

The V375 is a four-channel VME-module programmable arbitrary waveform generator. It is intended for use in the generation of relatively low-frequency waveshapes, as might be used in vibration testing, polyphase AC waveform generation, and simulation or excitation of rotating machinery.

The V375 generates waveforms by scanning sequential data points stored in user-loadable memory, with outputs processed by digital-to-analog converters, smoothing filters, and output amplifiers. The module provides full and smooth realtime control of waveform, frequency, amplitude, DC offset, and phase.

Principal features of the V375 include the following:

- Four independent direct digital synthesizer (DDS) frequency sources allow smooth variation of waveform scan rates without requiring waveform table reloads
- Four versatile, memory-table-driven waveform generators scan up to 65,536 discrete points per waveform at up to 15 MHz point step rate
- Versatile wave memory partitioning allows waveform read/write operations concurrent with wave generation, so multiple waveforms can be loaded and selected in real time
- 32-bit frequency resolution and 16-bit amplitude resolution
- Per-channel divisors allow simulation of fractional 'gear-ratio' waveshapes
- Continuous-play (non-repetitive waveform) modes available
- Output frequency, amplitude, phase, and DC offset are smoothly alterable in real time
- Channels may operate independently or may be synchronized within a module or across multiple modules, up to 16 modules, 64 channels, in a single VME crate
- Output stage analog summing allows mixing of up to four generated waveforms, plus one user-supplied waveform/external analog input
- Onboard microprocessor performs macro commands: complex waveshape building, Fourier synthesis, pulse train generation, sweeping, and test functions
- Programmable waveform sweep, jump and triggered burst mechanisms allow realtime waveform control
- Programmable lowpass filters are provided to smooth discrete sample points

This manual refers to V375 hardware revisions B, C and D. The V375 revision A did not support the JUMP or BURST operations. See Section 13 for a summary of hardware and firmware revisions.

2. Specifications

FUNCTION	4-channel waveform synthesis VME module
DEVICE TYPE	16-bit VME register-based slave: A24:A16:D16 Implements 256 16-bit registers at switch-selectable addresses in the VME 16- or 24-bit addressing spaces
OUTPUTS	Four channels of arbitrary waveform output, ±10 volts max, 50 Ω output impedance, 100 mA max Bandwidth 175 KHz full power, 300 KHz at 5 volts p-p; slew rate 6 volts/µs typical Amplitude accuracy ± 2% Four TTL-level sync/logic output pulses
RESOLUTION	16 bits amplitude, 32 bits frequency
INPUTS	Four TTL-level auxiliary logic inputs Four analog summing inputs
WAVE MEMORY	64k x 16 bits per channel
FREQUENCY SYNTHESIZERS	Four direct-digital frequency synthesizers step through waveform memory; 15 MHz max, 0.0093 Hz resolution, ±0.005% accuracy
OPERATING TEMPERATURE	0 to 60° C; extended MIL/COTS ranges available
CALIBRATION INTERVAL	One year
POWER	Standard VME supplies : +5 volts, 900 mA nominal +12 volts, 100 mA nominal plus load current -12 volts, 150 mA nominal plus load current
CONNECTORS	D25 female connector for signal outputs SMB test connectors for outputs and syncs

INDICATORS	LEDs indicate processor heartbeat and VME access
PACKAGING	Single-wide 6U VME module
CONFORMANCE	ANSI/VITA 1-1994 (R2002) VMEbus spec; does not support byte writes

3. Theory of Operation

3.1 General Architecture

Figure 1 is the overall block diagram of the V375 Synthesizer module, and Figure 2 is the block diagram of a typical output channel.

The V375 module includes the following:

1. MICROPROCESSOR. A 32-bit Motorola MC68332 embedded CPU supervises module operations. Embedded processor code is stored on a pair of replaceable EPROM chips; these same chips hold the FPGA (gate array) logic chip configuration data, allowing hardware and software upgrades in the field.
2. VME INTERFACE. An FPGA-based interface is used, implementing a bank of 16-bit VME memory locations accessible both from the VME bus and from the internal processor. The module does not use interrupts, and passes all bus grant signals.
3. SYNTHESIZERS. Four direct-digital synthesizers, A...D, each capable of creating a periodic clock signal from millihertz to 15 MHz with millihertz resolution. Frequency synthesizers may be reprogrammed smoothly on the fly.
4. WAVEFORM GENERATORS. Four waveform generator Channels 0...3 are provided. Each consists of the following:
    a. A programmable divider, capable of division by integer values from 1 to 256. Each divider may be programmed to accept the clock generated by any of the four synthesizers.
    b. A waveform scan counter capable of counting to a programmable modulus from 64 to 65,536 in 2:1 steps; scan counter modulus determines the current waveform block size.
    c. A 3-port waveform memory holding 65,536 16-bit words of stored waveform points. The entire memory is accessible from VME, from the internal microprocessor, and from the waveform generator. At any instant, one block of this memory can be selected as the live waveform source, while other blocks are available for loading alternate waveforms. The wave memory may also be used in continuous-play modes; see Section 5.7.
    d. A 16-bit-resolution multiplying digital-to-analog converter which receives arbitrary waveform points from the waveform memory and constructs the analog waveforms. The fullscale range of the DAC is dynamically programmable to adjust waveform amplitude.
    e. A multipole, programmable-bandwidth active lowpass filter which smoothes the stepped DAC output into a continuous waveform.
    f. BURST and JUMP control logic.

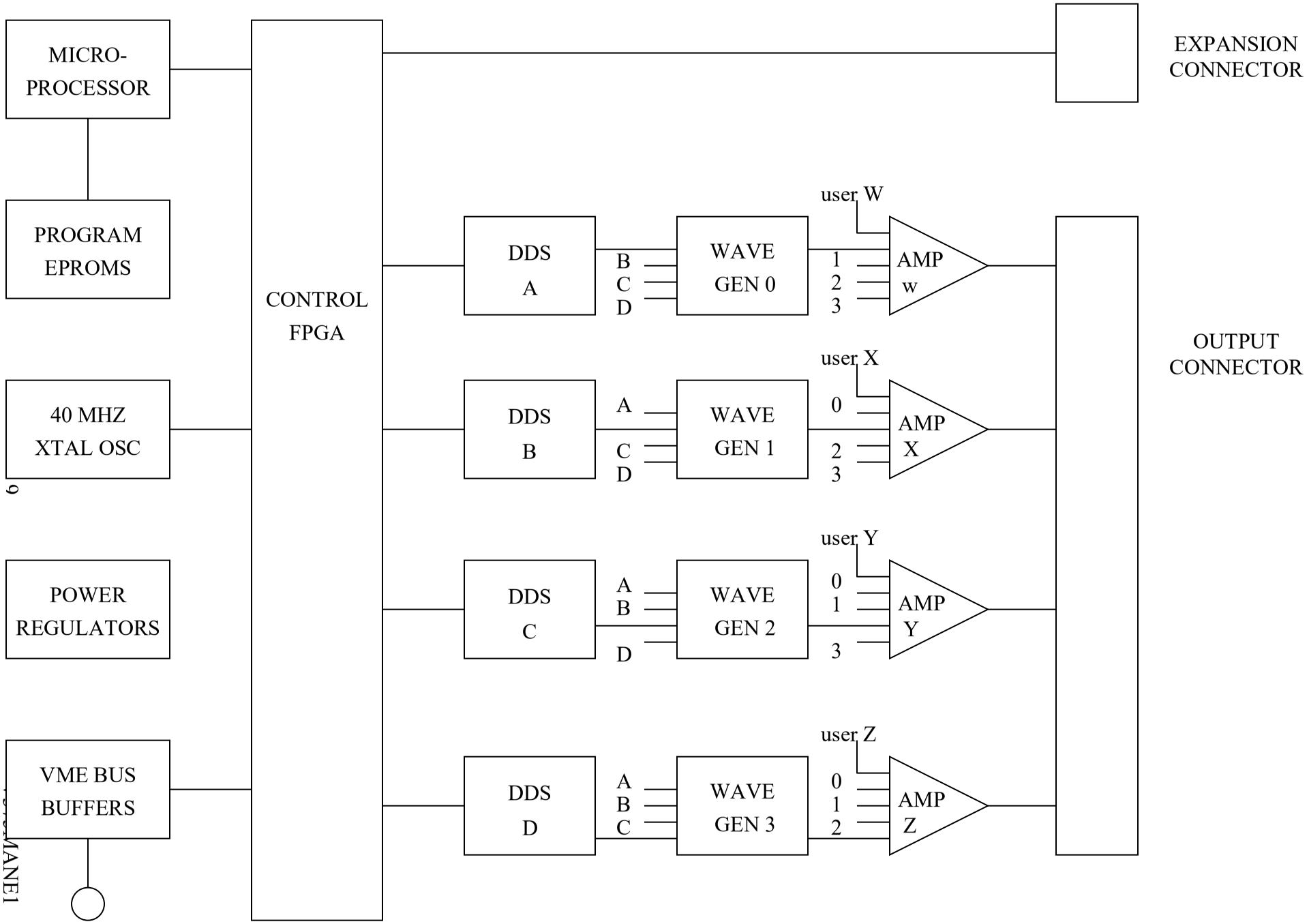

FIG 1
OVERALL V375 BLOCK DIAGRAM

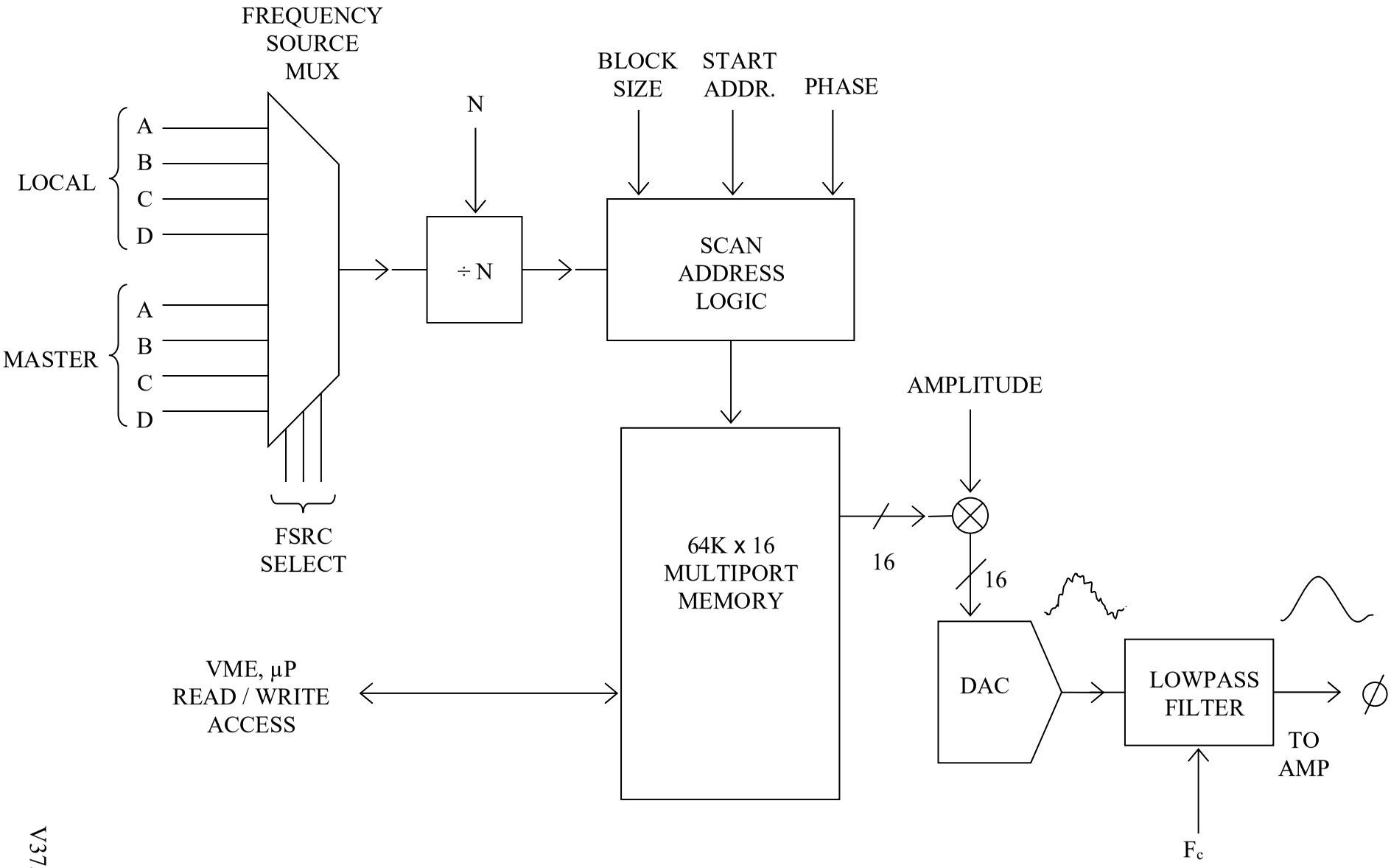

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FIG 2
CHANNEL BLOCK DIAGRAM

5. OUTPUT AMPLIFIERS. Four output amplifiers W...Z are provided.

   Each amplifier has an analog summing matrix, allowing any output to be any desired sum of the signals generated by any of the four waveform generators, plus a user-supplied analog signal. Each amplifier can provide up to ±10 volts peak output. Each amplifier includes a programmable ±10 volt, 16-bit resolution DC-offset DAC.
6. SUPPORT CIRCUITS. The module includes a 40-MHz master clock, all required power regulators, VME and processor activity indicators, and appropriate test points.
7. OUTPUT CONNECTOR. A single female 25-pin D-sub connector is provided for all output signals. The analog outputs (W, X, Y, Z) and SYNC signals (0, 1, 2, 3) are also available on front-panel SMB connectors.
8. EXPANSION CONNECTOR. A connector is provided to permit multiple modules to be used in master-slave mode, allowing up to 64 waveforms to be synchronized.

3.2 Nomenclature and Defaults

The four DDS frequency synthesizers are labeled A, B, C, and D, referred to generically as 'DDSa'.

The four waveform generators are 0, 1, 2, and 3, generically referred to as 'wave generator n'.

The four output amplifiers are W, X, Y, and Z, generically 'amp z'.

As the powerup default, the V375 is set up as four independent waveform generators, as follows:

- Synthesizer A drives waveform generator 0, which drives output amp W.
- Synthesizer B drives waveform generator 1, which drives output amp X.
- Synthesizer C drives waveform generator 2, which drives output amp Y.
- Synthesizer D drives waveform generator 3, which drives output amp Z.

Users may select any one DDS as the clock of any waveform generator, and any combination of generator outputs may be summed into any output amplifier.

When two's complementary binary numbers are associated with voltage outputs, scaling is theoretically +32767 (0x7FFF) for +9.99969 volts (+10 volts less 1 LSB) and -32768 (0x8000) for -10.000 volts. The endpoints are casually referred to as +10 and -10 volts.

A waveform analog output is determined by the product of a 16-bit waveform memory value and the setting of a 16-bit amplitude DAC. By convention, waveform points are considered to range from -1.0 to +1.0 over a numerical range of -32768 to +32767, and amplitude DACs are considered to span -10 to +10 volts over the same numerical range.

3.3 Frequency Synthesizers

There are four DDS (direct digital synthesizer) frequency sources, A, B, C, and D. Each is programmable to generate a clock at up to 15 MHz in steps of about 0.009 Hz. Each DDS may be held in a stopped state by

asserting the appropriate bit in the RESETS register, and will begin running when the bit is dropped. New frequencies may be loaded into multiple DDS channels on one module and installed coherently.

3.4 Waveform Generators

There are four waveform generators, 0, 1, 2, and 3.

A waveform is created by writing up to 65,536 discrete analog output points into each channel waveform memory, with the memory points being scanned and converted sequentially. The memory output points are processed at a rate determined by the selected DDS clock, divided by the individual channel divisor.

Each wave channel may use any of the four onboard DDS frequency synthesizers, or an expansion input, allowing channel groups to be synchronized. Because each channel has its own programmable divisor, channels which share a common synthesizer may be run at integer-fractional speed ratios, and will track in phase and frequency as synthesizer frequencies are altered.

Depending on the chosen scan-block size (equivalent to the scan counter modulus), each memory can hold from one (counter mod = 65,536) to 1024 (counter mod = 64) different waveforms, one of which may be selected to be the 'live' waveform. Users can switch freely among the many stored waveshapes, and may read or write any memory location at any time. The JUMP mechanism allows changes of phase or waveshape to be made at controlled times relative to actual waveform timing.

Provision is made for synchronizing the start of one or more channels, either on a single module or across multiple modules used in a master/slave configuration. A wave generator channel is reset when its selected DDS clock source is held reset.

Each waveform generator has an associated AMPn register which scales the amplitude of the waveform. A wave memory point of +32767 with an AMPn value of +32767 results in positive full-scale (+10 volt) output. The AMPn value is signed, two's complement so it can scale, or invert, waveforms in real time.

Unfiltered arbitrary waveform generators produce inherently jagged outputs, and require very large numbers of steps (i.e., very small incremental changes) to simulate a smooth waveshape. A suitable lowpass filter can be inserted into the signal path to smooth out the steps and allow correspondingly larger stepsizes to be used while still creating smooth waveforms. In general, a suitable lowpass filter has a cutoff frequency well above the highest signal frequency needed, but well below the waveform generator step rate (that is, the selected DDS frequency divided by any selected divisor).

The V375 has a programmable lowpass filter assigned to each waveform generator. Seven selectable cutoff frequencies are available, beginning at 3 KHz and increasing in steps to 300 KHz. Since a filter is down 3 dB (0.707 amplitude) at its cutoff frequency, a good filter selection will typically be a cutoff frequency of several times that of the highest waveform frequency component of interest.

Note that the output filters add phase lag as the signal frequency approaches the filter cutoff (-3 dB) point. For a sine wave signal, phase shift is typically about 10 degrees at 0.1 times filter cutoff, 55 degrees at 0.5 cutoff, and about 90 degrees at the cutoff frequency. If different wave generator channels have identical filter settings, channel-to-channel relative phase shifts will be small.

Users may also select 'filter OFF' for use in pulse-generating applications; pulse slew rate will be about 6 volts/microsecond.

Effective firmware revision 22376E, the count modulus of the waveform counter may be set to any value from 1 to 65536, the counter may be programmed to count up or down, and the counter may be read in real time. Additionally, the TTL-level SYNC outputs may be selected to output the DDS clock, the LSB of DAC data, or the MSB of the waveform counter.

3.5 Output Amplifiers

There are four output amplifiers, denoted W, X, Y, and Z.

Each amplifier may be programmed to sum one to four waveform sources (wave generators 0, 1, 2, and 3) into a common output signal. There is an additional signal that may be supplied by the user (one per channel) to be summed into the output as well. The user-supplied signals may only go to the channel they are associated with and cannot be combined with other channels' outputs.

Each output amplifier has its own DC-offset DAC which is summed into the final signal out. Output slew rate is about 6 V/µs, so undistorted 20-volt peak-to-peak outputs are limited to 175 KHz. Up to 5 volts p-p can be output at 300 KHz.

3.6 Register Access

Two kinds of registers are accessible from the VME bus: hard (realtime) and soft (microprocessor) registers. Most simple waveform control functions are 'hard', meaning that VMEbus actions directly and immediately alter the contents of the addressed register. Hard registers include the basic frequency, divisor, amplitude, phase, summing, offset, and reset functions. Soft registers are actually dual-port memory locations which are shared between the VME bus and the internal microprocessor. Data loaded into these soft registers will be processed by the µP with various associated execution delays. Examples of soft functions include loading the waveform memories with complex shapes (sines, harmonics, pulse trains) and executing diagnostics.

3.7 Waveform Address Processing

On any given channel, the user specifies the following parameters:

1. The waveform block size, from 64 to 65,536 points, in binary steps.
2. The starting point in waveform memory for extraction of the 'live' waveform. This ranges from 0 to 65,472 and must be at an integral block boundary.
3. The selected DDS synthesizer A-D, its frequency, and an optional divisor.
4. A phase rotator, expressed in unit memory locations; angle in degrees equals 360 * rotator / blocksize.

Figure 3 shows how these factors are combined to sequentially access waveform memory locations. The divided DDS clock steps a 16-bit binary counter which is the basic waveform scanner. The contents of the 16-bit binary phase rotator are added to the counter output to form the basic scan address sequence. The user-entered memory start point is combined with the phase-shifted scan address in the bit blender; if the waveform block size is 'N' bits (example: N = 9 for a block size of 512 points) the blender selects the low N bits of the scan address and the high [16-N] bits of the start address and combines them into a single 16-bit memory pointer. The final memory address is used to read a waveform memory location and grab the next sequential wave point to feed to the D/A converter.

See section 7 for additional operating modes.

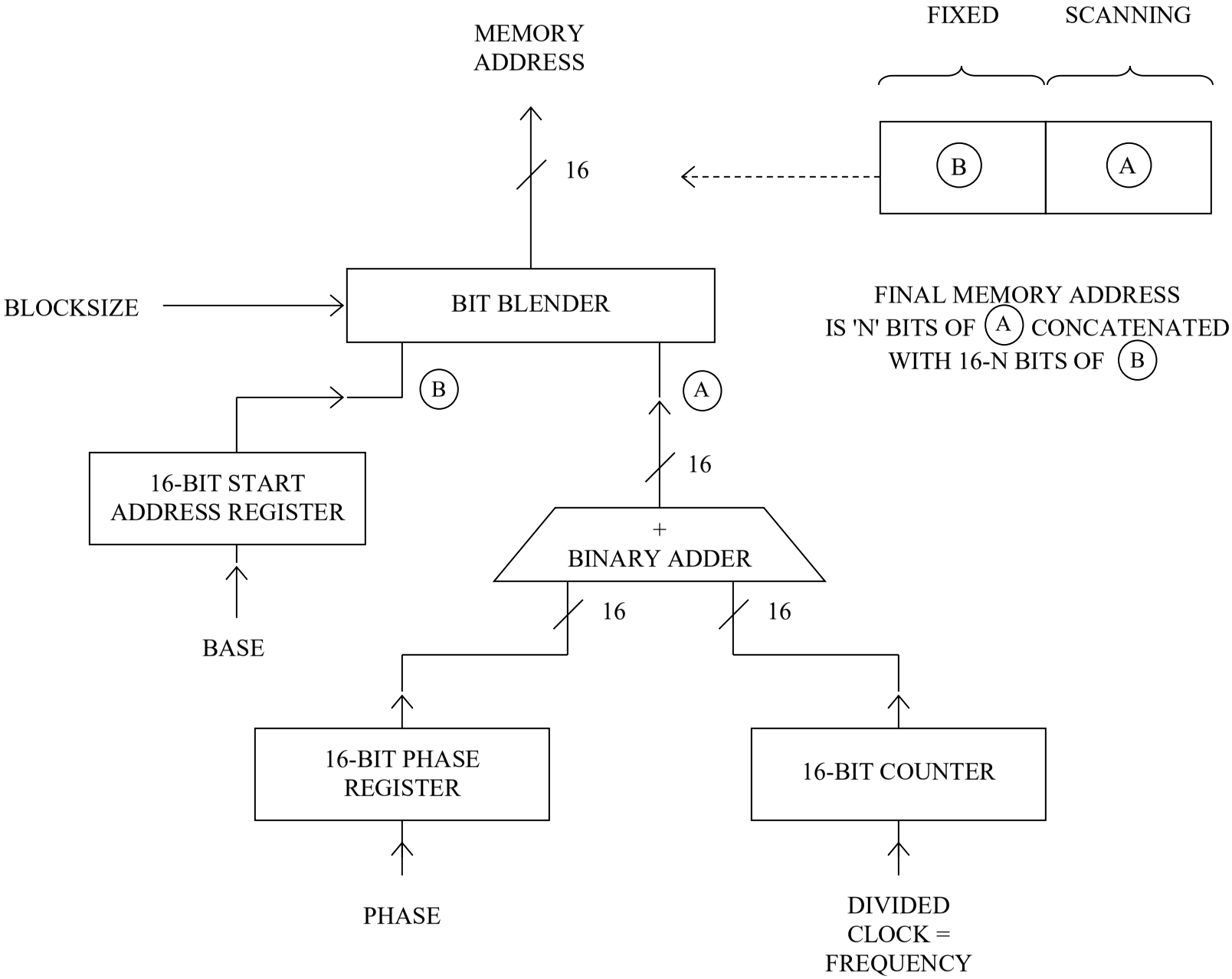

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FIG 3
WAVEFORM MEMORY
ADDRESS CALCULATION

4. Front-Panel Connectors and LEDs

4.1 Output Connector

The main output connector is a female DB-25 located on the front panel. The pinout is as follows:

Pin #	**Signal Name**	
1	Ground	
2	Output W	also SMB "W"
3	Ground	
4	Output X	also SMB "X"
5	Ground	
6	Output Y	also SMB "Y"
7	Ground	
8	Output Z	also SMB "Z"
9	Ground	
10	Sync 0	also SMB "0"
11	Ground	
12	Sync 1	also SMB "1"
13	Ground	
14	Sync 2	also SMB "2"
15	Ground	
16	Sync 3	also SMB "3"
17	External Input We	
18	External Input Xe	
19	External Input Ye	
20	External Input Ze	
21	Aux TTL input 0	
22	Aux TTL input 1	
23	Aux TTL input 2	
24	Aux TTL input 3	
25	Ground	

Outputs W, X, Y, and Z are the final, summed analog waveforms. Each has a 50-ohm source impedance and ±10 volts open-circuit full-scale range. These outputs can drive any load of 50 ohms or more; peak output is ±5 volts into an external 50-ohm load. Amplitude accuracy is best into a high-impedance load.

The SYNC pulses are +5 volt logic-level signals, one for each of the waveform generators 0...3. The signal is a square wave whose rising edge corresponds to the 'top dead center' (first waveform point) of each synthesized waveform, namely the MSB of the current block address. Altering a channel PHASE register does not affect the SYNC signal. Note that a SYNC may not be an unambiguous trigger when multiple

waveform generators are summed into amplifier outputs. See section 7 for additional SYNC options.

We, Xe, Ye, and Ze are optional user-supplied inputs summed into the outputs W, X, Y or Z. Each input can only be summed into the corresponding output. These inputs should be grounded when not in use, as there is no facility for disabling the external inputs.

It is recommended that user cabling incorporate individually shielded signal lines to prevent crosstalk between waveforms or between sync signals and waveforms. Users may elect to not use the D25 connector and take analog outputs and SYNC pulses from the front-panel SMB connectors.

'Ground' connections are to VMEbus common. Aux pins are reserved for future use.

See Section 8 for details regarding the four Aux TTL inputs.

4.2 Test Connectors

Eight front-panel SMB coaxial connectors are provided for signal monitoring. Four are connected to the DB-25 connector SYNC outputs, and four are connected to the waveform signal outputs.

4.3 Master/Slave Daisychain

The V375 includes a front-panel 20-pin ribbon-cable connector which supports the master/slave mechanism of synchronizing channels across multiple modules. Up to 16 modules may be interconnected, with one module designated the master. Ribbon cables are Highland part number V372-n, where 'n' is the number of modules to be interconnected, from n=2 to n=16.

4.4 LED Indicators

The module is equipped with two LED indicators.

The green 'CPU' LED flashes briefly once per second to indicate that the onboard microprocessor program is executing. If the module is configured as the master, each blink will be a brief double-flash. While the µP is processing MACRO commands, it will illuminate brightly.

The green LED will glow steadily during diagnostic self-tests so long as no errors have been detected.

The blue 'VME' LED flashes whenever the module is addressed from the VME bus.

5. VME Register Map and Programming

The following is a summary of the VME-accessible registers on the V375 module. A total of 256 16-bit registers are implemented. Switches on the module set the base address, anywhere in the 24-bit or 16-bit VME address spaces.

REG # below is the ordinal register number in decimal; OFFSET is the hex VMEbus offset from the module base address. The H/S column indicates whether the register is 'hard' (immediate action) or 'soft' (microprocessor serviced).

REG NAME	REG #	OFFSET	H/S	Function
VXI MFR	0	0x00	S	VXI manufacturer ID: always 65262, FEEE hex
VXITYPE	1	0x02	S	module type, always 22375, 5767 hex
VXI STS	2	0x04	S	VXI status register
ROM ID	4	0x08	S	firmware ROM ID, typically 22376 decimal
ROM REV	5	0x0A	S	firmware ROM revision, typically ASCII ‘A’
MCOUNT	6	0x0C	S	microprocessor update counter
MASTER	8	0x10	H	master/slave control register + SYNC bits
RESETS	9	0x12	H	channel resets register
STROBE	10	0x14	H	DDS data strobes register
VRUN	15	0x1E	S	macro command execution timer
MACRO	16	0x20	S	macro command register
CP0	17	0x22	S	command parameters
.	.	.	S	“
.	.	.	S	“
.	.	.	S	“
CP110	127	0xFE	S	“
FAHI	128	0x100	H	DDS synthesizer A frequency, MS 16 bits
FALO	129	0x102	H	DDS synthesizer A frequency, LS 16 bits
FBHI	136	0x110	H	DDS synthesizer B frequency, MS 16 bits
FBLO	137	0x112	H	DDS synthesizer B frequency, MS 16 bits
FCHI	144	0x120	H	DDS synthesizer C frequency, MS 16 bits

REG NAME	REG #	OFFSET	H/S	Function
FCLO	145	0x122	H	DDS synthesizer C frequency, MS 16 bits
FDHI	152	0x130	H	DDS synthesizer D frequency, MS 16 bits
FDLO	153	0x132	H	DDS synthesizer D frequency, MS 16 bits
AMP0	160	0x140	H	waveform generator 0 amplitude
AMP1	161	0x142	H	waveform generator 1 amplitude
AMP2	162	0x144	H	waveform generator 2 amplitude
AMP3	163	0x146	H	waveform generator 3 amplitude
OFSW	164	0x148	H	output W DC offset
OFSX	165	0x14A	H	output X DC offset
OFSY	166	0x14C	H	output Y DC offset
OFSZ	167	0x14E	H	output Z DC offset
SRC0	176	0x160	H	Channel 0 synthesizer/reset source
DIV0	177	0x162	H	Channel 0 divisor
PTR0	178	0x164	H	Channel 0 waveform memory pointer
WAV0	179	0x166	H	Channel 0 waveform memory data
SIZ0	180	0x168	H	Channel 0 waveform block size
BAS0	181	0x16A	H	Channel 0 waveform start location
PHA0	182	0x16C	H	Channel 0 phase rotation
FLT0	183	0x16E	H	Channel 0 filter control
JMP0	184	0x170	H	Channel 0 jump control
TRG0	185	0x172	H	Channel 0 jump target
JPH0	186	0x174	H	Channel 0 jump phase
JBA0	187	0x176	H	Channel 0 jump base
SNP0	188	0x178	H	Channel 0 phase snapshot (J1-21)
BCC0	189	0x17A	H	Channel 0 burst control
BCX0	190	0x17C	H	Channel 0 burst count
SUMW	191	0x17E	H	amplifier W analog summing control
SRC1	192	0x180	H	Channel 1 synthesizer/reset source
DIV1	193	0x182	H	Channel 1 divisor
PTR1	194	0x184	H	Channel 1 waveform memory pointer
WAV1	195	0x186	H	Channel 1 waveform memory data

REG NAME	REG #	OFFSET	H/S	Function
SIZ1	196	0x188	H	Channel 1 waveform block size
BAS1	197	0x18A	H	Channel 1 waveform start location
PHA1	198	0x18C	H	Channel 1 phase rotation
FLT1	199	0x18E	H	Channel 1 filter control
JMP1	200	0x190	H	Channel 1 jump control
TRG1	201	0x192	H	Channel 1 jump target
JPH1	202	0x194	H	Channel 1 jump phase
JBA1	203	0x196	H	Channel 1 jump base
SNP1	204	0x198	H	Channel 1 phase snapshot (J1-22)
BCC1	205	0x19A	H	Channel 1 burst control
BCX1	206	0x19C	H	Channel 1 burst count
SUMX	207	0x19E	H	amplifier X analog summing control
SRC2	208	0x1A0	H	Channel 2 synthesizer/reset source
DIV2	209	0x1A2	H	Channel 2 divisor
PTR2	210	0x1A4	H	Channel 2 waveform memory pointer
WAV2	211	0x1A6	H	Channel 2 waveform memory data
SIZ2	212	0x1A8	H	Channel 2 waveform block size
BAS2	213	0x1AA	H	Channel 2 waveform start location
PHA2	214	0x1AC	H	Channel 2 phase rotation
FLT2	215	0x1AE	H	Channel 2 filter control
JMP2	216	0x1B0	H	Channel 2 jump control
TRG2	217	0x1B2	H	Channel 2 jump target
JPH2	218	0x1B4	H	Channel 2 jump phase
JBA2	219	0x1B6	H	Channel 2 jump base
SNP2	220	0X1B8	H	Channel 2 phase snapshot (J1-23)
BCC2	221	0x1BA	H	Channel 2 burst control
BCX2	222	0x1BC	H	Channel 2 burst count
SUMY	223	0x1BE	H	amplifier Y analog summing control
SRC3	224	0x1C0	H	Channel 3 synthesizer/reset source
DIV3	225	0x1C2	H	Channel 3 divisor
PTR3	226	0x1C4	H	Channel 3 waveform memory pointer
WAV3	227	0x1C6	H	Channel 3 waveform memory data
SIZ3	228	0x1C8	H	Channel 3 waveform block size

REG NAME	REG #	OFFSET	H/S	Function
BAS3	229	0x1CA	H	Channel 3 waveform start location
PHA3	230	0x1CC	H	Channel 3 phase rotation
FLT3	231	0x1CE	H	Channel 3 filter control
JMP3	232	0x1D0	H	Channel 3 jump control
TRG3	233	0x1D2	H	Channel 3 jump target
JPH3	234	0x1D4	H	Channel 3 jump phase
JBA3	235	0x1D6	H	Channel 3 jump base
SNP3	236	0x1D8	H	Channel 3 phase snapshot (J1-24)
BCC3	237	0x1DA	H	Channel 3 burst control
BCX3	238	0x1DC	H	Channel 3 burst count
SUMZ	239	0x1DE	H	amplifier Z analog summing control
TPASS	251	0x1F6	S	diagnostic pass counter, longword 251:252
TERROR	253	0x1FA	S	diagnostic error count, longword 253:254
TSTOP`	255	0x1FE	S	diagnostic control word

Unassigned registers in the 0-255 range are reserved and should not be written to.

VME Registers are described in detail below. Within each register, bits are numbered 15 (MSB) through 0 (LSB). Bits 7...0 are the LS byte, and bits 15...8 are the MS byte. The V375 allows only 16-bit data writes.

5.1 VXIMFR: VXI Manufacturer's ID

This register displays Highland's VXI-registered manufacturer's ID code. It always reads as 0xFEEE.

5.2 VXITYPE: Module Type

This register displays the module type. It normally reads as 22375 decimal, 0x5767.

5.3 VXISTS: VXI Status Register

This register implements the VXI-standard status reporting function. Active bits are 2 (PASSED), 3 (READY), and 14 (MODID).

Shortly after powerup, these bits will be set and all other status bits will be zeroes. Note that the module does NOT support the MODID mechanism.

5.4 ROMID: Firmware Version

The microprocessor software version ID is read here, with a typical value of 22376 decimal (0x5768). Other code versions, having different functionality, may have different ID codes.

5.5 ROMREV: Firmware Revision

The revision letter of the firmware may be read at this location, as an ASCII character, 'E' (0x45) for the current firmware release.

5.6 MCOUNT: CPU Activity Counter

The MCOUNT register appears as a 16-bit binary counter which is incremented by the microprocessor at a 1-KHz rate.

5.7 MASTER: Master/Slave Control

If the LSB of this register is set, the module will be the master, and will put its four synthesizer frequencies and reset pulses onto the external daisy-chain bus. Only one module on the bus may be the master.

Bits 11...8 of this register are read-only SYNC bits for waveform generators 3...0 respectively. These bits are driven by a realtime square wave which rises at the start of the wave block currently being scanned.

It is possible to use V375 channels in an infinite-length synthesis mode, as might be required to output non-repetitive waveforms. For example, one could select a waveform blocksize of 65,536 points, load the entire wave buffer, and start the outputs. When the appropriate SYNC bit falls, the first half of the wave buffer has been played, and may then be reloaded. Similarly, when SYNC rises, the top half of the buffer has just been finished, and that block of 32,768 words may be reloaded.

5.8 RESETS: Reset Control

Bits 3...0, when set, hold DDS sources D...A respectively in the reset state. In this state, the synthesizer is stopped, and any wave generators that use this DDS are also reset: their divisor counter is initialized, and the waveform scan counter is held clear. During reset, wave generators statically deliver their first waveform point, which is wave point '0' if the phase shift register is zero; when reset is dropped, waveform generation begins from that point.

If several wave generators are assigned to use a common DDS clock, and their phase relationship is important, assign those wave channels to the selected DDS, then briefly reset that DDS to reset and phase-synchronize the wave channels.

5.9 STROBE: DDS Frequency Strobe

When a new 32-bit integer is loaded to specify a new DDS clock frequency, the user must load the 32-bit frequency control value as two 16-bit words. The actual 32-bit frequency value is not installed until the

appropriate STROBE bit is written. Bits 3...0 of STROBE install the new frequency values of DDS Channels D...A respectively. One can load new values into multiple DDS frequency-control registers and then assert multiple STROBE bits in a single VME write, updating one to four DDS frequencies coherently. See Section 5.11 for details.

The MS and LS frequency control registers may be written in any order and with any delays, but it is mandatory that BOTH the high and low frequency registers be written before asserting the corresponding STROBE bit.

5.10 MACRO: Macro Command Register

The MACRO register conveys command codes to the microprocessor. Refer to Section 6 for details.

5.11 FaHI: DDS Frequency

Each of the DDS frequency synthesizers A...D has a pair of frequency-control registers, FaHI and FaLO. If the HI:LO pair is treated as a 32-bit unsigned integer F, then the DDS frequency will be as follows:

40,000,000 * F / 2^32 Hertz,

about 0.009313 Hz per LSB. The maximum allowable frequency is 15 MHz. The 40-MHz reference source is accurate to ±0.005%, with all four synthesizers on any board sharing a common reference oscillator.

As noted in Section 5.9, to install a new frequency it is required to write BOTH the FaHI and FaLO registers with new data, then to write a '1' to the appropriate STROBE bit.

5.12 SRCn: Waveform Generator Clock Source

Each wave generator 0...3 has a SRCn register, which selects one of eight DDS frequency sources to be used to drive this channel. Register contents 0...3 will select local synthesizers A through D, and 4...7 will respectively select synthesizers MA...MD, the A...D synthesizers on the master module. The MA...MD selections are useful only when this module is operating as a slave that is connected via the front-panel ribbon cable to a master module. The powerup default is for each generator to use its 'own' local synthesizer (i.e., SRC0 = 0, SRC1 = 1, etc.).

5.13 DIVn: Channel Divisor

A frequency source divisor 'm' may be loaded into a DIVn register. The effective synthesis rate of waveform generator n will be divided by a factor of m+1, allowing division from 1 (m=0) to 256 (m=255). The powerup default is m=0, effectively 'no division'. If several waveform generators are programmed to use a common DDS clock source, and different divisors are used on the various generators, waveforms can be created which simulate gear-ratio couplings. To avoid phase ambiguity, divisors should be loaded while the associated DDS is held reset.

5.14 PTRn, WAVn : Waveform Memory Pointer and Data Registers

Each Channel 0...3 has a PTR register which points into the channel's 65,536-word waveform memory. The PTR registers are used for VME access to waveform memory.

Once PTRn is loaded, memory data may be read or written through the associated WAVn register at VMEbus speed. Each time a WAV register is used, its associated PTR register is post-incremented to point to the next memory location, allowing waveforms to be block transferred into or out of wave memory at high speed. Note that, on transitioning between read and write operations, the PTRn register should be reloaded.

5.15 AMPn: Channel Amplitude

Each channel 0...3 has a waveform amplitude register which scales waveform memory points into output voltage levels. Each memory point can be treated as a signed 16-bit integer which is scaled by the signed 16-bit value in AMPn such that the maximum waveform amplitude is ±10 volts. For example, a memory value of 0x4000 (equivalent to +0.5 of full scale) scaled by an AMPn value of 0x7000 (equivalent to +8.75 volts full scale) gives an output of +4.375 volts.

AMPn registers power up at zero, so must be loaded to enable outputs.

5.16 SIZn: Waveform Block Size

A waveform channel's SIZn register determines the size of the portion of its waveform memory that is scanned to generate a 'live' waveform.

SIZ contents	**blocksize**
0	64 words
1	128
2	256
3	512
4	1024
5	2048
6	4096
7	8192
8	16384
9	32768
10	65536

The powerup default value is 4 (1024 points). The advanced JUMP logic allows arbitrary block size; see section 7.

5.17 BASn: Waveform Start Address

Within each channel's 64K waveform memory, one sub-block may be chosen to be the live waveform region. The BASn register specifies this address. BASn is a 16-bit pointer into wave memory, not a block number. For example, if SIZ is 6, selecting 4096 (0x1000) points per waveform, then memory can be considered to hold up to 16 different waveforms; setting BASn to zero selects the 0'th block, and setting BAS to 0xF000 hex selects the last waveform, block 15. In this example, bits 0...11 of BAS are ignored, as these bits of the memory scan address are generated by the scan counter and phase rotation logic.

If BASn is reloaded, the output waveform will jump from the current shape to that defined in the newly selected block. One can be loading a new set of waveforms into unused blocks simultaneously with waveform generation from the selected active memory block.

5.18 PHAn: Phase Shift Register

The value in a channel's PHA register effectively rotates the sequence in which points are scanned from waveform block of memory. If this register contains integer value R, the wave block is rotated by

R * 360 / B degrees,

where B is the current blocksize, 64 to 65536 words.

For a blocksize of 4096 samples, a value R = 1024 corresponds to a 90-degree phase lead, since it advances the sample location 1024 addresses into the 4096-point programmed wavelist. In this example, only the low 12 bits of PHA are used, and the rotation is quantized to 360/4096 = 0.0879 degrees. The PHA register may be considered unsigned (phase lead only) or as being two's complement (allowing 180-degree lead or lag).

If the waveform in memory is a sine wave, R = 1024 would in this case result in a phase lead of 90 degrees, producing a cosine output relative to the SYNC signal. If the waveform is a pulse train, the train will appear to move left on an oscilloscope (i.e., occur earlier in time) as R is increased.

5.19 FLTn: Waveform Filter Control

Each waveform generator 0...3 has an associated lowpass filter and a corresponding filter select register. Users may write to each FLT register to select the filter cutoff frequency. Choices are...

FLT value	**cutoff, Hertz**
0	3 K
1	6 K
2	15 K
3	30 K
4	60 K
5	150 K
6	300 K
7	off (pulse mode)

The powerup default is selection 6, 300 KHz.

5.20 SUMz: Waveform Analog Summing Control

Each amplifier W...Z can be selected to sum up to four waveform signals into its output. An amplifier's SUM register controls this function. For amplifier 'z', SUMz register bits 0...3 respectively sum waveform generators 0...3 into the output. The powerup default values of the four SUM registers are such as to assign only the four waveform signals 0...3 to the amplifiers W...Z respectively. If a SUMz register is cleared, only the amplifier DC offset (with no waveform), plus any user-supplied external summing signal, appears at output 'z'.

5.21 OFFz: Amplifier DC Offset

Each amplifier has a DC offset register OFFz. This value declares a constant offset to be added to the output signal of that channel; this value does not affect other channel outputs, even if crossover summing is in use. Scaling of offset is +32767 for +10 volts, -32768 for -10 volts. An output will clip if its summed waveforms and offset peak at over ±10 volts, typically saturating at about ±11 volts. The powerup value is zero.

5.22 Jump Control Registers

The JMPn, TRGn, JPHn, and JBAn registers are used to manage the JUMP mechanism, and are discussed in Section 7.

5.23 Burst Control Registers

The BCCn (burst control) and BCXn (burst count) registers control the burst mechanism (see Section 8).

5.24 SNAn : Phase Snapshot Registers

Four phase-snapshot registers are implemented in the V375-3B version module. Each is associated with a TTL-level electrical input pin on the J1 connector; pin numbers are noted in the registers summary table.

For each of the four waveform generators, upon the receipt of a rising edge on the associated TTL input pin, the current value of the channel waveform counter is latched into the channel's SNP register. To convert this into a phase angle, mask the register value with the appropriate number of LSBs corresponding to the block size currently in effect, divide by block size, and multiply by 360 degrees. The TTL snapshot signals may be driven by external devices or by the SYNC output of other V375 channels on the same or other modules. This facility allows the relative phases of V375 channels to be determined in real time.

The snapped value is of the waveform counter before the phase offset of the PHAn register is added. The snapped value is generally about 1 LSB + 100 ns later (numerically larger) than a perfect phase snapshot.

On modules which implement the snapshot option, the function is always enabled and does not interfere with other uses of the input pins, specifically the BURST function.

The Snapshot registers may also be used to display the realtime waveform counter registers; see section 7.

5.25 Notes on Register Sharing

Registers in the waveform generators are accessible by both the VME bus and by the module's internal microprocessor. Potential conflicts are resolved by convention.

The microprocessor will access the waveform generators at powerup time to initialize the system. This will take a maximum of 3 seconds after powerup to complete. The VME user should not access the module during this interval. When the READY bit in the status register is set, and MCOUNT begins counting, initialization is over.

During the execution of any macro command, the microprocessor 'owns' any targeted VME registers, so users should refrain from any writes to those locations until the macro execution is complete. If a macro affects wave memory, the related PTRn and WAVn registers should not be read or written during macro execution. During a SWEEP operation, targeted parameters may be read but should not be overwritten.

6. Macro Commands

The onboard microprocessor can execute macro commands which assist in loading and managing the module. As with all other V375 registers, only 16-bit (word) accesses should be used when executing macro functions.

Use the following procedures to execute a command:

- Check that bits 7...0 of the MACRO register are clear, indicating that any previous commands have been executed.
- Write any required command parameters into the command parameter registers CP0...CP110 which immediately follow the MACRO register.
- Write a valid command code into MACRO; this must be a 16-bit write.
- Wait until bits 7...0 of MACRO clear. Do NOT access any related waveform channel registers during this busy period.
- Read returned parameters if any.

If a command results in an error, bit 15 of the MACRO register will be set and bits 7...0 will be cleared to indicate command completion. Bits 10...8 return specific error codes. If an undefined macro is invoked, MACRO will be returned as 0xFF00.

After a command has completed execution, the VRUN register will display the macro execution time in milliseconds. Command codes are as follows:

HEX CODE	**FUNCTION**
0x01	Build Fourier series.
0x02	Add Fourier series.
0x03	Build Gear Waveform.
0x05	Build pulse train.
0x06	Overlay pulse train.
0x09	Load constant.
0x0D	Measure frequency.
0x0F	Sweep.
0x20	Reinitialize module.
0x22	Test VME dual-port memory.
0x23	Test waveform memory.
0x24	Test watchdog timer.
0x25	Hibernate.

0x26 Test CPU static ram.

Commands 0x20 and up terminate with module reinitialization so deviate from the standard macro-ending sequence. All macros may take as long as one millisecond before execution begins.

CAUTION: When a macro is executed, the associated command parameters are not cleared; if left as written, executing another macro command will re-execute the old parameters. It is suggested that all appropriate command parameters be loaded or cleared before loading a new macro command.

6.1 Macro Command: Build Fourier Series

A waveform, defined as a Fourier series, can be loaded into a waveform buffer. Command parameters CP0 through CP103 define a waveform consisting of a DC term and up to 50 sine wave harmonics. A waveform of up to 65,536 points may be synthesized.

The command parameters are as follows:

```
CP0    channel number, 0...3
CP1    start location in wave memory
CP2    maximum (last) harmonic, 1...50

CP3    0th harmonic (DC term) amplitude
CP4    unused

CP5    1st harmonic (fundamental) amplitude
CP6    1st harmonic phase angle
CP103  50th harmonic amplitude
CP104  50th harmonic phase angle
```

Amplitudes are signed 16-bit integers, with -32768 to +32767 corresponding to the range -1.0 to +1.0 of fullscale amplitude; the channel AMPn register scales the actual analog output levels to ±10 volts max.

Phase shifts are unsigned integers, 0 to 65535 corresponding to 0 to 360 degrees of phase lead. Zero phase shift generates a sine wave starting at the beginning of the waveform block. Note that this phase shift specifier does not depend on the current block size. The phase integers may also be considered signed two's complement, range -180 to +180 degrees.

After the parameters are loaded and the command code is written into the MACRO register, the processor will synthesize the waveform and load it into waveform memory, in the selected channel, starting at the specified wave memory location. The CP1 start address should be, but is not constrained to be, located at a block boundary.

The number of points loaded into wave memory is equal to the currently-defined waveform block size for that channel. If the current block size is, say, 8192 points, the fundamental sine wave will complete one full cycle in 8192 points, and would make an actual output sine wave of frequency DDSa / (8192 * DIVn)

The synthesized waveform is computed to 32-bit precision, then clipped to the range -32768 to +32767 before being poked into waveform memory.

The execution time of this command is about

BLOCKSIZE * MAX_HARMONIC * 6 microseconds,

or somewhat less when some of the Fourier amplitudes are zero. For a blocksize of 4096 points, with 15 harmonics, execution time will be about 500 milliseconds.

Error codes, returned in bits 10...8 of MACRO, are as follows:

```
1   illegal number
2   illegal blocksize
3   illegal maximum harmonic
```

Parameters are not cleared after the macro is executed.

6.2 Macro Command: Add Fourier Series

This command is identical to the BUILD FOURIER SERIES command, except that the computed data points are added to those already in the target waveform region.

6.3 Macro Command: Build Gear Waveform

This command loads the selected waveform block with a waveshape typical of the output of a magnetic pickup sensing a rotating gear. The gear may have any number of teeth, from 1 to 512, and up to 16 teeth may be defined as 'short' teeth, exceptions having a pulse level different from the default value.

Command parameters are as follows:

```
CP0   channel number 0...3
CP1   start location in wave memory
CP2   total number of teeth 'n' 1...512
CP3   DC baseline
CP4   waveshape (currently unused)
CP5   pulse width
CP6   default top-of-pulse voltage

CP7   first short pulse index
CP8   first short pulse level
```

```
CP9    second short pulse index
CP10   second short pulse level


etc.   up to 16 short pulses
```

One can thus select a DC baseline, create a uniform train of positive or negative pulses, then have some number of the pulses be a different amplitude or polarity, including zero. The first pulse begins at 'top dead center', namely the very beginning of the waveform block. Pulses are assumed to be uniformly spaced around 360 degrees, and one can later use the channel PHASE register to twist the whole pulse train as desired.

Pulse width is scaled 0...65535 for 0...359.99 degrees, so a tooth width value of 500 would correspond to about 2.75 degrees, or 62 waveform points for a block size of 8192 points. One LSB of 'width' is about 0.0055 degrees.

A short pulse is defined by its index (i.e., the tooth number) and its top-of-pulse level. A 'short' pulse may in fact be larger or smaller that the default pulse height. To create a missing tooth, declare a short pulse having amplitude equal to the CP3 (baseline) value.

Up to 16 exception ('short') pulses may be listed in any order. A short pulse index value of 0 ends the exception list.

The 'waveshape' parameter is currently unused; future versions may allow simulation of analog signals as might be generated by variable-reluctance or other particular sensors.

If CP7 is set to zero, this macro becomes a simple square wave generator.

Error codes, returned in bits 10...8 of MACRO, are as follows:

```
1      illegal channel number
2      illegal blocksize
3      illegal tooth count 'n'
```

Command parameters are NOT cleared.

6.4 Macro Command: Build Pulse Train

This command allows creation of an arbitrary pulse train of up to 35 pulses. Macro parameters are as follows:

```
CP0    channel number 0...3
CP1    start location in wave memory
CP2    number of pulses n
CP3    DC baseline
CP4    waveshape (unused)
```

```
CP5   pulse 1 level (first pulse top-of-pulse voltage)
CP6   pulse 1 position (equivalent phase angle)
CP7   pulse 1 width



.
.
.
CPx   pulse n level
CPy   pulse n position
CPz   pulse n width
```

Positions and widths are expressed as 0...65535, corresponding to 0...360 degrees, where 360 degrees represents the full blocksize currently selected. One LSB of position or width is then about 0.0055 degrees.

Error codes, returned in bits 10...8 of MACRO, are as follows:

```
1     illegal channel number
2     illegal blocksize
3     illegal pulse count 'n'
```

Command parameters are NOT cleared.

6.5 Macro Command: Overlay Pulse Train

This command is identical to the BUILD PULSE TRAIN command, except that the DC baseline points are not written, and the computed pulse tops are written over the waveform already stored in the selected waveform memory block. This is equivalent to a continuation of the pulse parameter list of the BUILD PULSE TRAIN macro, allowing an unlimited number of pulse events to be described.

6.6 Macro Command: Load Constant

This command writes a constant value into a region of waveform memory. Parameters are as follows:

```
CP0   channel number 0...3
CP1   start pointer 0...65535  first location to load
CP2   end pointer 0...65535  last location to load
CP3   constant value
```

The constant will be written into the specified region of waveform memory. If 'end' is below 'start', the operation will wrap.

Error codes, returned in bits 10...8 of MACRO, are as follows:

```
1      illegal channel number
2      illegal blocksize
```

6.7 Macro Command: Sweep

This macro allows a number of waveform parameters to be smoothly slewed from their current value to a final target value. Items that may be swept include the following:

- DDS frequencies A, B, C, and D.
- Wave generator gains AMP0, AMP1, AMP2, AMP3.
- Wave phases PHA0, PHA1, PHA2, PHA3.
- Output DC offsets OFSW, OFSX, OFSY, OFSZ.

The sweeping process is begun by loading the MACRO parameter list and then executing the SWEEP macro code.

The command parameters are as follows:

```
CP0    sweep time, DDS frequency A
CP1    target frequency, MS word
CP2    target frequency, LS word

CP3    sweep time, DDS frequency B
CP4    target frequency, MS word
CP5    target frequency, LS word

CP6    sweep time, DDS frequency C
CP7    target frequency, MS word
CP8    target frequency, LS word

CP9    sweep time, DDS frequency D
CP10   target frequency, MS word
CP11   target frequency, LS word

CP12   sweep time, AMP0
CP13   wave gen 0 target amplitude
CP14   unused

CP15   sweep time, AMP1
```

```
CP16   wave gen 1 target amplitude
CP17   unused



CP18   sweep time, AMP2
CP19   wave gen 2 target amplitude
CP20   unused

CP21   sweep time, AMP3
CP22   wave gen 3 target amplitude
CP23   unused

CP24   sweep time, PHA0
CP25   wave gen 0 phase target
CP26   unused

CP27   sweep time, PHA1
CP28   wave gen 1 phase target
CP29   unused

CP30   sweep time, PHA2
CP31   wave gen 2 phase target
CP32   unused

CP33   sweep time, PHA3
CP34   wave gen 3 phase target
CP35   unused

CP36   sweep time, OFSW
CP37   output amp W offset target
CP38   unused

CP39   sweep time, OFSX
CP40   output amp X offset target
CP41   unused

CP42   sweep time, OFSY
```

```
CP43   output amp Y offset target
CP44   unused



CP45   sweep time, OFSZ
CP46   output amp Z offset target
CP47   unused
```

A sweep time, T, is associated with each variable. Values of T may be as follows:

- T = 0 to 3 ignore this sweep command
- T = 4 to 32767 begin sweeping, time to target = T milliseconds
- T = negative cancel sweeping, this item

To begin ramping a selected item, set its sweep time to 4 or more, set its target to the desired final value, and execute the SWEEP macro. On any given execution of the macro, a ramp time of 0 to 3 indicates that the associated variable should be ignored (i.e., no sweeping is begun, and any sweep already in progress continues without change). Sweep times may range from 4 milliseconds to 32.7 seconds.

To cancel sweeping on any variable, set its ramp time negative (i.e., set the MSB of 'T'). The parameter will then be frozen at its current value.

All targets are in the same form as is normally used to load the corresponding hardware registers. The MSB of a 32-bit DDS frequency value is always treated as zero, since DDS frequencies are limited to 15 MHz.

When the macro is executed, for all items with a value of T in the 'start sweeping' range, the microprocessor will, once a millisecond, reload the associated parameter with a suitable incremental value such as to reach the target in T milliseconds.

Any number of sweeping operations may be initiated at any time. If an 'in-progress' parameter sweep is overwritten, the variable will begin to ramp toward the new target at the new rate.

While sweeping is active on any register, users should not try to write to that register, as the ramp mechanism will overwrite the value every millisecond until the target is reached.

For sweeping purposes, DDS frequencies are treated as unsigned 32-bit values, and other variables are treated as 16-bit, two's complement numbers. Frequencies, waveform amplitudes, and DC offsets will ramp unambiguously from their present values toward the final targets in the obvious manner.

The sweeping of phases is inherently tricky, as phase repeats mod 360 degrees, and there are always two ways to get from one phase to another: by rolling K degrees in one direction, or 360-K in the other. The SWEEP logic treats the ENTIRE 16-bit PHAn register as a two's complement value, and ramps 'up' (i.e., ramps in the phase lead direction) if the target appears more positive than the start value, and ramps down (in the lag direction) if the target is below the start value. To ensure that a phase sweep proceeds in the 'lead' direction, the 16-bit target should be more positive than the start value, and vice versa. Keep in mind that, for all block sizes except 65536, one or more of the phase MSBs are unused by the hardware bit blender

logic, so are available to force the phase ramp to slew in the preferred direction. One can always change the unused MSBs of a PHASE register before beginning a sweep if this helps clarify the direction the phase ramp will take.

For smaller block sizes it is possible to sweep more than 360-degrees. For example, if blocksize is 2048 and the phase register is currently at 512, phase leads by 90 degrees. If a final target value of 5120 is declared, the waveform will ramp through an additional 810 degrees, to a final phase angle of "900" degrees (actually 900 mod 360 = 180 degrees) before stopping.

Like the amplitude and offset values, the 16-bit, two's complement phase value cannot sweep below -32768 or above +32767.

SWEEP returns no error codes. Command parameters are NOT cleared.

6.8 Macro Command: Frequency Measurement

The V375 has a provision for readback of the four output waveforms. Each of the four analog outputs is sampled at the output of the final amplifier, resistively divided by 2:1, and measured by the TPU (time processor unit) of the internal CPU. To use this facility, do the following:

1. Program each output to swing from 0 volts (or less) to +7.5 (or more).
2. Set up the channel to produce a stable sine or square waveform. Square waves will give more repeatable measurements.
3. Poke the command code into the MACRO register, and wait for bits 7...0 of MACRO to clear. Execution takes about 1 second.

The frequency of the W output will be presented in command parameter registers 0 and 1. The frequencies of the X, Y, and Z channels are reported in paired command parameter registers 2:3, 4:5, and 6:7.

Data is presented as 32-bit integers, high endian format. The system measures all signal transitions over a 1-second interval, so the reported value is actually twice the frequency in hertz. Practical considerations limit measurement to about 200 KHz max.

This facility is intended for general functional verification, not for quantitative error measurement. No errors are returned.

6.9 Macro Command: Reinitialize Module

This command is executed by writing 'password' 1029 hex into the first command parameter, then writing the command code into the MACRO register. This will cause all module registers to return to their powerup states and all waveform outputs to go to zero volts. Execution will take about 500 milliseconds. The actual sequence is as follows:

- Interrupts are disabled; MCOUNT stops counting.
- VME registers are cleared, from bottom (0) to top (255). This clears the VME status register before the MACRO register is cleared, and clears all AMP and OFS DACs and all summing registers.

- Internal CPU RAM is cleared, clearing all sweep control blocks.
- Waveform memories are cleared.
- Default channel setups are installed.
- The VME status register is loaded with MODID, READY, and PASSED bits.
- Interrupts are enabled and normal operation resumes.

If the password is incorrect, error code 3 will be returned.

6.10 Macro Command: Test VME Dual-Port Memory

This command makes the internal CPU test the VME register memory. Command parameters are as follows:

```
CP0   First word to test  range 0...249
CP1   Last word to test    1...250
```

The TSTOP register must be loaded with 0x137 before the macro is issued, and the test runs until TSTOP is cleared by the user. Longword TPASS will count test passes, and longword TERROR counts errors. The front-panel green CPU LED will stay on steady if no errors are detected. When TSTOP is cleared, the test will stop and the module will be reinitialized.

Registers which are not fully read-write (MASTER, WAVn, JMPn) are excluded from testing. Output waveforms are unpredictable during this test.

Error codes, returned in bits 10...8 of MACRO, are as follows:

```
3     illegal TSTOP value
4     illegal test limits
```

6.11 Macro Command: Test Waveform Memory

This command makes the internal CPU test the waveform memory. Command parameters are

```
CP0   Wave channel to test  0...3
CP1   First word to test  0...65534
CP2   Last word to test 1...65535
```

The TSTOP register must be loaded with 0x137 before the macro is issued, and the test runs until TSTOP is cleared by the user. Longword TPASS will count test passes, and longword TERROR counts errors. The front-panel green CPU LED will stay on steady if no errors are detected. When TSTOP is cleared, the test will stop and the module will be reinitialized.

Error codes, returned in bits 10...8 of MACRO, are as follows:

```
3      illegal TSTOP value
4      illegal test limits
```

6.12 Macro Command: Test Watchdog Timer

This test is initiated by loading password value 0x6666 into CP0, then loading the command code into the MACRO register. This will essentially hang the operating program and force a watchdog timer reset, equivalent to a full powerup start cycle. Watchdog delay is about 0.8 seconds, and restart time is about three seconds. The module will disappear from the VME bus briefly during the restart.

Error code 3 will be returned if the password is incorrect.

6.13 Macro Command: Hibernate

This command ceases all microprocessor services except the watchdog timer refresh. TSTOP must be set to 0x137 before the command is issued. The loop will exit, and the module will reinitialize, when TSTOP is cleared.

This is useful for running VME memory tests from the VME port. Error code 3 is returned if TSTOP is incorrect when the macro is issued.

6.14 Macro Command: Test CPU Static RAM

This command tests the internal CPU 128 Kbyte static RAM. No parameters are required.

The TSTOP register must be loaded with 0x137 before the macro is issued, and the test runs until TSTOP is cleared by the user. Longword TPASS will count test passes, and longword TERROR counts errors. The front-panel green CPU LED will stay on steady if no errors are detected. When TSTOP is cleared, the test will stop and the module will be reinitialized.

Error code 3 is returned if TSTOP is incorrect when the macro is issued.

7. Jump Mechanism

It is often desirable to change the phase or waveshape of a signal at a specific point in the realtime waveform. The V375 provides a means to synchronize changes in phase or waveshape to the realtime position of a waveform.

7.1 Overall Function

Each of the four V375 waveform generators has a mechanism for assigning the next values of waveform phase and base address, and for requesting that either of these values be changed at some selected point in the actual waveform. This is implemented on a per-channel basis, under the assumption that, if a group of channels are being used in some coherent manner (polyphase generation, complex pulse summing, etc.) they share a common DDS clock source and are running with synchronized waveform counters, so there is no need for a master/slave cross-channel jump mechanism.

Each waveform generator channel has four jump-related registers, as follows:

- JMPn: channel jump control register
- TRGn: jump target
- JPHn: jump phase
- JBAn: jump base address

Bits in the JMPn register request and report the status of jumps. The TRGn register determines the realtime jump point, and JPHn and JBAn hold the new (requested) values of waveform phase and base (live waveform) address respectively.

If the jump mechanism is not needed, these registers may be ignored.

7.2 Jump Control Registers

Each channel has a JMPn control register, with two active bits. Bit0 (the LSB) is the phase jump request bit, and bit1 is the base block jump request.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	BLjmp	PHjmp

To initiate a jump, do the following:

- Load the jump target register TRGn to select the time of jump.
- If a phase jump is desired, load JPHn with the new phase value.
- If a base block (waveshape) jump is desired, load JBAn with the new baseblock value; this should select the waveform block which contains the new waveform.

- Set the desired bit or bits in JMPn to request a phase jump, baseblock jump, or both.
- Wait for the jump to complete. After the jump, both active bits of JMPn will clear, and the realtime PHAn (phase) and BASn (baseblock) registers will reflect the new, actual values.
- If the user clears the request bits in the JMPn register before the actual jump occurs, the jump will be cancelled.

A channel's TRGn register determines when a jump happens. The low 'm' bits of TRGn are compared to the 16-bit waveform scan counter (see figure 3), with new values loaded into PHAn and/or BASn at the instant when these values are equal. The number of compared bits 'm' varies from 6 (when blocksize is 64 points) to 16 (blocksize of 65,536 points). The result is that the value of TRGn is scaled identically to the format of the phase-shift register PHAn. If TRGn is targeted at phase [blocksize-1], the last point of the current block is output and the jump happens at 'top dead center', namely when the active bits of the waveform scan counter pass through zero, coincident with the rising edge of the channel SYNC signal.

Note that the jump target timing comparison is independent of the value currently loaded into the PHAn phase register.

At the instant of comparison, when the waveform scan counter is equal to the programmed jump target, that waveform point is output to the channel ADC from the "old" waveform; the next point will be selected from wave memory as defined by the new, post-jump phase and block.

The JPHn register holds the new desired phase value. The contents of JPHn are loaded into the actual phase register PHAn at jump time.

The JBAn register holds the new desired base block (live waveform select) value. The contents of JBAn is loaded into the actual BASn register at jump time.

7.3. Advanced Jump Functions

Beginning with firmware version 22376E, several functions were added to the JUMP CONTROL registers.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	CTR	0	0	0	0	DOWN	0	S2	S1	S0	0	LOOP	BLjmp	PHjmp

The two lsb's continue to function as noted in section 7.2.

If the user sets the CTR bit, the channel snapshot register SNAn will display the realtime contents of the waveform counter, namely the 16-bit address in wave memory that is currently driving the D/A converter.

If the user sets the DOWN bit, the waveform counter will count down instead of the normal up direction. It is recommended that the DDS clock source which drives the channel be at zero frequency or held reset while the direction bit is changed, and especially while direction bits of coordinated channels are changed.

If the LOOP bit is set, the waveform counter will count up to the value that is loaded into the channel's jump target TRGn register. In this mode, channel blocksize should be set to maximum, 65536. For example, to

count mod 50,000, set the LOOP bit and load TRG0 with 49999. The waveform generator 0 address counter will then count 0,1,2...49998,49999,0... If the DOWN bit were then set, the count sequence would be 3,2,1,0,49999,49998...

When LOOP mode is enabled, it is strongly recommended that blocksize be set to maximum, 65536, and that the wave generator phase control (PHAn) and baseblock (BASn) registers be zeroed, and that the PHjmp and BLjmp functions not be used.

The three Sx bits select the electrical signal that drives the SYNC output of this channel, available on the D25 and SMB front-panel connectors. These three bits are encoded as...

0	inverted MSB of the waveform block address, "classic" SYNC
1	selected DDS clock
2	LSB of the waveform memory (DAC) data
3	MSB of the waveform counter
4	logic high
5..7	logic low

Note that the advanced JUMP features can be used with the normal analog waveform outputs, and that the DOWN (reverse count), CTR (waveform counter read), and sync output selection features can be used in regular non-LOOP modes.

7.4 Jump Examples

7.4.1 Torque Transducer

Consider a shaft that has two variable-reluctance speed sensors. Each sensor generates one pulse per shaft revolution, and the phase of the pulses varies as the shaft is twisted by torque. Suppose a pulse spacing of 90 degrees corresponds to zero torque, and that the lagging pulse may vary from 80 to 110 degrees at the expected torque extremes. One could program V375 Channels 0 and 1 to have identical pulse waveforms and to use the same DDS clock, with channels summed to simulate this signal, and the PHA1 register set to the nominal 90-degree phase shift (literally 270 degree lead = 90 lag) that represents torque. To make "safe" changes in the setting of the PHA1 register, post the desired phase value in JPH1 and set the LSB of JMP1 to request a jump. If blocksize were 2048 points, setting TRG1 to 2047 would make the jump occur at the TDC of Channel 0 (i.e., when both the Channel 0 and Channel 1 counters pass through zero) which is a safe time to alter the PHA1 register.

7.4.2 Polyphase AC

Suppose V375 wave generators 0, 1, and 2 are used to generate a 3-phase waveform set. They would share a common DDS clock, be reset and enabled together to synchronize their scan counters, and their active baseblocks would be loaded with identical sine waves, using the FOURIER macro.

Overall programming could be as follows:

- Program wave Channels 0, 1, and 2 to all use clock DDSA. Assume DDSA = 409.6 KHz for a 400 Hz system.

- Set channel blocksize as desired, with divisors disabled. Assume a blocksize of 1024 points for this example.

- Reset and un-reset DDSA to synchronize channel counters.

- Clear all BASn and PHAn registers
.
- Assign wave0 to output W, wave1 to X, wave2 to Y.

- Set amplitudes, filters, and offsets as desired.

- Use the Fourier macro to load an identical, fundamental sine wave into block 0 of all three wave memories.

- Set PHA0 to 0; this is phase A of the polyphase sine wave and is our overall 'zero phase angle' reference.

- Set PHA1 to 682 (0x2AA) for 240 degrees lead (120 lag), phase B.

- Set PHA2 to 341 (0x155) for 120 degrees lead (240 lag), phase C.

The V375 will now generate a 3-phase sine wave. Now suppose we want to add waveform distortion to phase B of the wave set. We could load a distorted sine wave into block 1 of Channel 1's wave memory (starting at wave memory address 1024) and schedule a coherent jump to change to this new waveform at the next zero crossing of the phase 'B' signal.

Since the phase B signal is generated by wave Channel 1 by means of a 240 degree lead, B will cross zero when the A phase (from wave gen 0) is at 120 degrees lag, which happens when the wave generator 0 counter is at 341, one third of 1024. So we'd like Channel 1 (which generates phase B) to jump when the Channel 0 counter is 341; but since all three wave generator counters are synchronized, we can jump when wave gen 1's counter is 341. So we set TRG1 to 341, JBA1 to 1024 (to aim at the 'new' waveform) and request a baseblock jump in JMP1. This would ensure a waveform change at the zero crossing of the phase B waveform.

7.4.3 Quadrature Encoder Simulation

Suppose we desire to simulate a rotary encoder which has digital outputs A, B, and R, where A and B are quadrature levels each of which makes 1000 cycles per revolution, and R is an index pulse that happens once per revolution. We will use a single clock synthesizer, DDSA, to clock waveform generators 0, 1, and 2, which will respectively generate the A, B, and R signals. The three TTL signals will appear on the SYNC outputs of the respective wave generator channels. The LSB of each waveform memory word will be used as the TTL data output.

The programming sequence might be...

Program wave generators 0, 1, and 2 to use clock DDSA by setting the SRC0, SRC1, and SRC2 registers to 0.

Set bit 0 of the RESETS register to hold reset DDSA and its three client channels.

Clear channel divisor registers DIV0, DIV1, and DIV2

Set DDSA frequency to zero by clearing FAHI and FALO and poking the LSB of the STROBE register.

Set waveform block sizes to maximum by writing 10 decimal into SIZ0, SIZ1, and SIZ2

Set waveform count modulus by writing 3999 into jump targets TRG0, TRG1, and TRG2.

Clear phase shift registers PHA0, PHA1, and PHA2.

Clear waveform base address registers BAS0, BAS1, and BAS2.

Load all three channel jump control registers JMP0, JMP1, and JMP2 with 0x2024, to select LOOP mode, readout of the wave counters, count up, and to select the LSB DAC data as the SYNC source.

Load waveform memories with the pattern...

address	wave 0	wave 1	wave 2
00000	00001	00000	00001
00001	00001	00001	00000
00002	00000	00001	00000
00003	00000	00000	00000
.			
.			
.			
03996	00001	00000	00000
03997	00001	00001	00000
03998	00000	00001	00000
03999	00000	00000	00000

which places 1000 quadrature cycles into the channel 0 and 1 memories, and a single index pulse into memory 2. Note that one can clear the PTR0, PTR1, and PTR2 wave pointers and then use their autoincrement modes to pour the 4000 waveform data points for each channel into WAV0, WAV1, and WAV2.

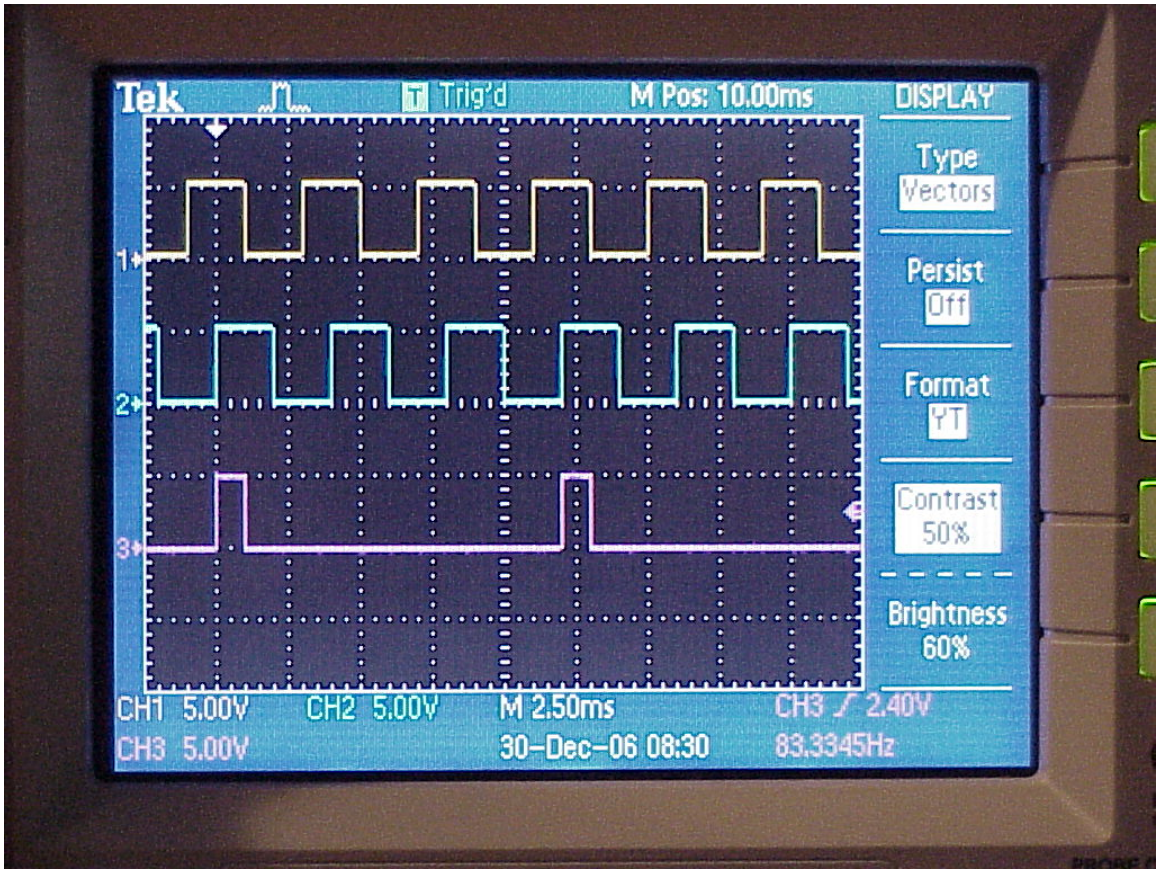
Now clear the RESETS register. The three electrical SYNC outputs should now be 1, 0, 1 respectively, corresponding to the LSB's of the respective waveform memories at address 00000.

Now one can ramp up the DDSA frequency to simulate clockwise encoder rotation. All three SNAn snapshot registers should display the realtime value of the waveform counters, beginning at 0 and incrementing each DDS clock tick. These counters correspond to angular position, 0...3999 equivalent to 0..359.9 degrees. Each 4000 clocks of DDSA will simulate one rotation.

If the DDSA clock is stopped, either suddenly or ramped down, the effective rotation will cease. While the clock is at zero frequency, the DOWN bits can be set in all three wave generator jump control registers, enabling CCW rotation.

If users desire to stop simulated motion at some exact position, it will be necessary to ramp down the DDSA frequency and monitor the angular positions (via any of the SNPn registers) to converge on the desired stop location. All three SNPn registers should remain equal, although realtime read skew may make them appear unequal if they are read while the DDS clock rate is nonzero.

The result will be similar to the scope waveforms below. For this illustration, the overall quadrature cycle was programmed with modulus 12 (TRGn = 11), giving three A or B cycles per reference pulse. The DDSA clock was set to 1 KHz, giving 83.333 effective rotations per second.



8. Burst Mechanism

Each of the four waveform generators 0…3 has its own set of burst control registers. Burst allows waveforms to be started under control of external TTL inputs or VME commands.

The burst capability is available on V375 module revision B or higher.

For each wave generator, two registers are associated with the burst function:

Burst Control BCCn

The burst control register includes the following bits:

15 GRAB	If set, the burst logic controls this channel; if clear, channel operates normally.
12 BUSY	Read-only bit indicates that the burst is running.
10 MANY	Enables infinite burst; ignores BCXn counter.
9 ONCE	Allows only one burst; ARM is cleared after one trigger/burst sequence.
8 ARM	When set, a burst is armed; when clear, the waveform generator is held reset.
7..4 MODE	The value of this nibble selects the burst gating mode, thus: 0 Rising edge starts waveform. 1 Falling edge starts waveform. 2 Static high enables waveform. 3 Static low enables waveform.
3..0 SRC	This nibble names the waveform trigger/gate source, thus: 0 VME; waveform starts at ARM time. 1 TTL input 0 J1, 21. 2 TTL input 1 J1, 22. 3 TTL input 2 J1, 23. 4 TTL input 3 J1, 24.

Burst Count BCXn

This is a 16-bit burst count register. Legal settings range from 1 to 65535. The value is ignored in static gate modes, or when the MANY bit is set.

The basic concept of the burst mechanism is that, when GRAB is in effect, the waveform generator is held reset until a start event occurs, then the current waveform block is repeated BCX times, then reset again.

The burst setup procedure is as follows:

- Set up the normal waveform generator frequency synthesizer selection and reset/release the DDS if desired.
- Set the GRAB bit; this may be done before or during the DDS reset if it is important that no waveform activity be allowed yet.
- Load the MODE and SRC nibbles to select the event that will start a burst. Load both fields with zeroes if the burst is to be started via the VMEbus (i.e., just the ARM bit.)
- Load the burst count for the number of times the active waveform block is to be executed. The counter is equivalently set to infinity if the MANY bit is set or static gating is selected.
- Set the ONCE bit if a single burst is desired. If this is set, the ARM bit will be cleared at the end of BCX waveform repetitions.
- Set the ARM bit to arm (or start) the waveform burst. If the SRC field is nonzero, the wave generator will be held reset until the selected TTL input becomes true. If SRC is zero, the burst begins when ARM is set. The BUSY flag indicates that the channel is active.
- The waveform block will then be executed BCX times; when done, BUSY will drop and the wave generator will be reset. If the SRC field is zero or ONCE is set, ARM will be cleared at the end of the burst.

A few notes:

The static TTL input modes (MODEs 2 and 3) ignore the counter setting and the ONCE and MANY bits. The waveform simply runs when the external permissive is true, and is reset when it is not.

The MANY bit causes the BCX count value to be ignored. Once a waveform is started, it will run continuously until the VME master drops the ARM bit.

The ONCE bit, if set, causes ARM to be cleared at the end of the burst. So an external trigger can be enabled to run a waveform when the trigger goes true, but not rerun the wave if the trigger was re-fired later.

ARM is cleared by the following:

- Reset of the assigned DDS frequency source
- The end of the burst if ONCE is set
- The end of the burst if SRC = 000 (i.e., VME burst mode)
- Clearing the GRAB bit

GRAB is not cleared by reset of the DDS source.

GRAB, SRC, MODE, ONCE, and MANY are cleared only at powerup.

The waveform generation counter is cleared if the assigned DDS clock is reset or if ARM is low while GRAB is high; reset returns the output to the value of the first entry in the current waveform block.

BUSY true indicates that a live waveform is being played. If BUSY is false while GRAB is true, the waveform generator is in reset and the first datapoint in the current wave block will be statically output.

To start a burst under software control, set SRC to 0; the burst will then begin when ARM is set. The waveform block will then be played BCX times, after which ARM will clear. If the MANY bit is set, the BCX value is ignored and the wave will run until ARM is cleared.

Multiple waveform generators can share a DDS clock source (even across multiple V375 modules) and still have independent burst control. One can also apply burst controls to two or more channels which are summed into a single analog output.

The four external TTL inputs have pullup resistors to +5 volts, so appear high if not otherwise driven.

Example

Suppose that we'd like to generate a single waveshape four times whenever the TTL2 input transitions low. We would set the up the wave channel for the desired DDS clock source, hold that DDS reset, set the GRAB bit, then release the DDS reset; this sequence ensures that we do not allow the waveform to free-run in normal mode before we are ready for a signal. Select the appropriate waveform block size, start address, gain, offset, and phase, and load the waveform into wave memory.

Set the burst count register BCXn to 4.

We now do the following:

- Set SRC nibble to 3 to use TTL2
- Set MODE nibble to 1 for falling edge trigger
- Set the ARM bit.

(This can be done by a single write of 0x0131 to the BCCn register.)

Now, every time the TTL2 input goes low, the waveform memory block will be executed four times, without further VME intervention. If a low-going transition occurs on TTL2 while BUSY is true, it is ignored.

If we had set the ONCE bit, only the first TTL falling edge would be serviced. If we had set MANY, the wave generator would start at the TTL falling edge but then run indefinitely, until ARM was cleared by the VME master.

9. Setup and Installation

9.1 Safety and Handling Precautions

The V375 module includes static-sensitive components; please observe antistatic procedures when handling the module outside of its antistatic packaging or outside of the VME cardcage.

Do not insert or remove the module from a crate with crate power on.
Do not apply any potential to any V375 outputs.

If explosion hazards are possible, connect V375 signals to field wiring through appropriate intrinsic safety barrier devices.

The V375 module has finite failure rates associated with its hardware, firmware, and documentation. Do not apply the V375 in data acquisition or control systems where a failure or defect in the module may result in injury, loss of life, or property damage.

9.2 Switch Setups

9.2.1 A16/A24 Addressing Mode Switch

One DIPswitch position is labeled =A16 =A24. Press the appropriate side of the switch to permit operation in VME systems which use 'A16' (16 bit) or 'A24' (24-bit) addressing.

In A16 mode, the module responds to VME address modifiers 29 and 2D hex. In A24 mode, address modifiers are 39 and 3D hex.

9.2.2 VMEBUS Address Switches

The module VME base address is set by on-board DIPswitches. The switches are labeled A9 through A23. To set an address bit true, press the side of the switch nearest the 'Axx' legend. If the module is in A16 mode, only switch positions A9 through A15 are decoded.

Example: to use the module at base address C000 in the A16 space, set the A24/A16 switch to its A16 position, and set the A15 and A14 address switches ON, with all others OFF, as shown:

9.3 Installation in a VME Crate

The V375 may be installed in any standard 6U VME backplane. The module connects to the backplane J1 connector only. The standard V375-1 does not use interrupts and passes all interrupt and bus grant signals. Seat the module firmly and secure both front-panel mounting screws before applying power.

⚠ **DO NOT INSERT OR REMOVE THE MODULE WITH CRATE POWER ON.**

10. The SABR.EXE Test/Demo Program

10.1 Program Basics

The SABR.EXE program allows users to directly exercise the V370/V375 module functions. It allows the following:

- Direct activation of module commands.
- Generation of basic waveforms.
- Import of external waveform files.
- Execution of single-line script commands to drive the module.
- Execution of external script files.

Realtime operations of the SABR program are described on the HELP pages provided on the various program screens. SABR.EXE is a real-mode DOS application, and requires a path to the DOS editor EDIT in order to edit script files.

10.2 Script Language

Script files consist of one or more text lines, each having up to 10 commands and an optional comment. The preferred filename extension is .ARB.

SABR.EXE executes script file START.ARB at startup, and will allow users to name, execute, create, and edit any other script files after startup. The program also allows single script lines to be entered manually and immediately executed. If script lines are executed while the module register display page is up, users can immediately see the effects of such operations on module registers.

SABR can be used in demo mode to show these register operations without VME hardware present. This can be useful in understanding register operations.

Typical lines in a script file might look like the following:

```
' file wiggle arb:
' make some test waveforms

INIT                          ' reset the module

DDSA 1.025M;DDSB 5.12M        ' set clock A, B synthesizer frequencies

SRC0 A  ;  SIZ0 1K            ' wave gen 0:  clock A,  1024 points
AMP0 10  ;  FLT0 OFF          ' amplitude 10v max, lowpass filter off
SUMW 0                        ' route wavegen 0 to output amplifier W
SIN0 2, 5                     ' 2 cycles of sine, 5v peak, 2 KHz
```

```
SRC2 B  ;  SIZ2 2K            ' wave gen 2:  clock B,  2048 points
AMP2 10  ;  FLT2 OFF          ' max amplitude, no lowpass filter
SQR1 12, 1                    ' 1-volt square wave, 30 KHz

SUMX 12                       ' add sine from wavegen 1 with square from
                              ' gen 2, output sum from amplifier X

SWEEP DDSB, 10, 10.24M        ' sweep the X waveform frequency up by
                              ' 2:1 over 10 seconds

END
```

These commands are case insensitive and ignore spaces, except that at least one space must follow a command word. The comment, if present, is the last thing on a line. Comment-only lines and blank lines are OK.

Multiple commands on a line are separated by semicolons, and a singletick < ' > begins a comment.

Numeric arguments default to decimal integers, but hex is allowed, as &H123. 'Volts' type arguments are decimal floaters, range -10.0 to 10.0. Times are in seconds. Bus and segment addresses are always assumed to be hex.

Script file execution may be aborted by hitting the <esc> key.

10.3 Command Summary

In the summary below,

n refers to a wave generator	0 1 2 or 3
a refers to a DDS synthesizer	A B C or D
z refers to an output summer/amplifier	W X Y or Z

GENERIC	**EXAMPLE**	**NOTES**
VME name	VME Tundra	Names the current VME interface.
SEGMENT hexval	SEGMENT E000	Declares the start of the VME window in the PC address space.
ADDRESS hexval	ADDRESS C000	Sets module bus address, as set on module dip switches.
MAD hexval	MAD 100	Alters actual physical address used to access module within VME segment.

GENERIC	EXAMPLE	NOTES
DOS command	DOS BIT3.EXE	Executes a DOS command.
INIT	INIT	Reinitializes the V370/V375.
DDSa freq	DDSA 2.4K	Sets DDS synthesizer frequency; K (kHz) and M (MHz) are allowed.
RESET dds's	RESET ABC	Sets RESET bits of DDS synthesizers.
	RESET	Clears all RESET bits.
MASTER	MASTER	Declares module to be clock master.
SLAVE	SLAVE	Declares module to be clock slave.
SRCn dds	SRC1 MA	Sets wave gen clock source: local A B C D or master MA MB MC MD.
DIVn val	DIV3 129	Sets wave generator clock divisor from 1 to 255.
SIZn val	SIZ0 8K	Sets wave gen block size range 0..10 or 64..512..1K..64K.
BASn val	BAS1 8192	Sets wave gen waveform start address as integer memory address.
BLKn val	BLK1 1	Sets wave gen waveform start address as block number, using current size.
PHIn val	PHI2 1024	Sets waveform phase, as integer.
PHAn val	PHA1 22.5	Sets wave phase, in degrees.
AMPn volts	AMP2 7.5	Sets max waveform amplitude scaler, +-10 volts max.
FLTn val	FLT3 100K	Sets wave gen lowpass filter 0..7 generic steps or 3K 6K 15K 60K 150K 300K OFF (V375) 1K 2K 5K 10K 20K 50K 100K OFF (V370).
OFSz volts	OFSW -5.00	Set amplifier DC offset, +-10 VOLTS.
SUMz list	SUMW 23	Route wave synthesizers to an output summer/amplifier stage.
PAR par#, val	PAR 0, 55 PAR 1, &H1234	Set a macro command parameter, integer (hex is allowed, too).
MACRO val	MACRO 15	Execute a macro command.

GENERIC	EXAMPLE	NOTES
SINn cyc, amp	SIN2 1, 7.5	Load a sine wave into current block; args are cycles/block, amplitude.
SQRn cyc, amp	SQR3 2, 5.5	Load a square wave into current block.
CONn val	CON2 -5.25	Fill current wave block with constant.
RANn ampl	RAN2, 2.5	Load wave block with random points, amplitude range +-ampl.
GAUn ampl	GAU1, 3.33	Load wave block with Gaussian noise, amplitude in volts RMS.
BURn cnt, ctrls	BUR2 100, TTL0+	Burst control; see below
SWEEP item, time, target	SWEEP DDSC, 2.5, 3M	Sweep a parameter; see below
REG reg, val	REG 15, &H10	Poke a 16-bit module register reg = 0 to 255.
SLEEP time	SLEEP 2.5	Pause file execution for 'time' seconds.
PAUSE text	PAUSE Check led on	Print text, wait for keystroke.
PRINT text	PRINT Ready	Prints text with cr/lf.
PRINT.text	PRINT.Bye	Print without cr/lf.
LOCATE y, x	LOCATE 10, 60	Locate cursor on screen.
COLOR f, b	COLOR 15, 12	Set display colors.
CLS	CLS	Clear screen.
BEEP	BEEP	beeps
FILn filename	FIL3 ROTOR.DAT	Loads waveform file into current block of wave memory.
CHAIN	CHAIN MORE.ARB	Start another script file; does not return. A file may chain to itself.
LINE text	LINE sweep ddsa,5,10m	Loads default script line.

10.4 Sine and Square Wave Loading

The SINn command loads a sine wave into channel 'n', into the currently-active waveform block. The 'cyc' argument specifies the number of cycles within the block, 50 max, and 'amp' is peak amplitude, 1/2 of p-p. DC offset is zero. Actual output frequency will be as follows:

```
Fn = DDSa * cyc / (DIVn * blocksize)
```

The SQRn command loads a square wave into channel 'n'. The 'cyc' argument specifies the number of cycles within the current block, and 'amp' is peak amplitude. The wave alternates between zero and 'amp' voltage levels.

10.5 Loading Waveform Files

The "FILn filename" command will open a disk file and load waveform memory of wave generator "n", beginning at the start of the currently-active wave block in memory. As many points will be loaded as there are entries in the file, possibly wrapping into subsequent blocks.

The file should be in plain comma-delimited text, with each point being a numeric value from -10 to +10 in any normal fixed or floating-point text format. Spaces separating entries are ignored, and a single-quote < ' > marks the beginning of a comment, effectively ending a line.

10.6 Executing Script Lines

The / command allows a single script line to be entered and immediately executed. The \ command recalls and displays the last script line, allowing <enter> to be hit to re-execute it.

10.7 Burst

Any of the four waveform generators may be operated in triggered burst mode. In this mode, the waveform generator is held reset until triggered, then executes N passes through the waveform block, then returns to the reset condition.

The script command is

BURn count, controls

where COUNT is how many times the waveform block will be run, and CONTROLS specifies options. Allowed text items in CONTROLS include the following:

```
TTL0+    trigger from J1, pin 21          rise
TTL0-            pin 21                   fall
TTL1+            pin 22                   rise
TTL1-            pin 22                   fall
TTL2+            pin 23                   rise
TTL2-            pin 23                   fall
TTL3+            pin 24                   rise
TTL3-            pin 24                   fall

GRAB     Enter burst mode.
VME      Trigger immediately, one burst of COUNT waves.
ONCE     Recognize only the first trigger.
MANY     Run indefinitely after trigger; COUNT Is ignored.
```

```
STATIC   TTL gate statically enables wave generation; COUNT
         ignored
OFF      Cancel burst mode.
```

So a burst command could be as follows:

```
BUR3 250, TTL0+ ONCE     ' wavegen 3, run 250 passes through
                         ' wave table when J1, 21 goes high;
                         ' ignore subsequent triggers
```

The command BUR3 OFF returns the wave generator to normal mode. BURST OFF cancels burst mode on all four wave generators.

10.8 Sweep

Many module variables may be swept smoothly from their initial value toward some final target, with total sweep time from 4 milliseconds to 32.76 seconds. To start a sweep, use the following command

```
SWEEP Itemname, time, target
```

where TIME is in seconds (0.004 to 32.767), TARGET is the desired final value, and ITEMNAME is the item to sweep.

ITEMNAME	**TARGET**
DDSA	synthesizer frequency, Hz, KHz, or MHz; 15 MHz max
DDSB	
DDSC	ex: SWEEP DDSC, 4.5, 455K ' 4.5 sec to reach 455 KHz
DDSD	
AMP0	wave amplitude scaler, range +-10 volts
AMP1	
AMP2	ex: SWEEP AMP2, 0.5, +5 ' 0.5 sec to reach +5 volts
AMP3	
PHA0	phase, degrees
PHA1	
PHA2	ex: SWEEP PHA2, 10, 45 ' 10 sec to reach 45 degrees
PHA3	
OFSW	amplifier DC offset, range +-10 volts

```
OFSX
OFSY      ex: SWEEP OFFY, 20, -5  ' 20 sec to reach -5 volts
OFSZ
```

To stop a sweep, use SWEEP PHA2, STOP. The value of the item will be frozen as of the instant the STOP is executed.

Do not attempt to load a variable during its sweep. Any number of different sweeps may be in operation concurrently. After the SWEEP line is executed, script execution does NOT wait for any sweeps to run to completion, so sleep commands may be appropriate before executing commands that might interfere with sweeps.

10.9 Examples

The simplest script command to make a waveform is as follows:

```
INIT ; AMP0 10 ; SIN0 1,5
```

which uses module initialization defaults to make a sine wave of 97.66 Hz at the W output.

To make a 1 KHz sine wave from the W output of a V375, the following line may be entered manually or evoked from within a script file thus:

```
INIT ; DDSA 1024K ; SRC0 A ; AMP0 10 ; SIZ0 1K; SUMW 0 ; SIN0 1, 5
```

where:

```
INIT          resets the module;
DDSA 1024k    sets clock synthesizer A to 1024 KHz;
SRC0 A        tells wave generator 0 to use clock A;
AMP0 10       sets wave generator 0 scaling to 10 volts max;
SIZ0 1k       sets wave generator block size to 1024 points;
SUMW 0        routes wave generator 0 to output amplifier W;
SIN0 1,5      pokes a full cycle sine waveform into wave gen 0
              memory, 5 volts peak.
```

Now the command

```
SWEEP DDSA, 15, 2.048M ; SWEEP AMP0, 15, +10
```

will cause the sine wave to smoothly increase in both amplitude and frequency by 2:1 over a period of 15 seconds.

10.10 VME Interface and Module Addressing

SABR.EXE requires a suitable PC-to-VME interface. Currently supported are the SBS Bit3 model 406, most VME-embedded PCs that use the Tundra bridge chip, and any other interface that can map the VME 16-bit space into a block of real memory between 640K and 1M.

When SABR is started, a window into the VME address space must be opened. This can be done before SABR is started (in AUTOEXEC.BAT, for example) or can be done using DOS commands within the START.ARB startup file. Use the SEGMENT command to tell SABR where the VME window is located, and use ADDRESS command to tell it the setting of the module DIP switches.

The MAD command may be used to set the access address used by the program to be different than the ADDRESS module dipswitch address if VME window mapping forces these to be different. The MAD command must follow the ADDRESS command.

SABR does not support A24 mode, so set the module dipswitch to 16-bit mode. For examples below, it is assumed that the V375 module switches are set for A16 mode, address C000.

```
SBS Bit3 model 406 ISA/VME interface:

DOS BIT3.EXE
SEGMENT D000
ADDRESS C000.

XYCOM XVME-653 (Tundra)

DOS TUNA  /T:D0000  /S:E0000  /E:F0000  /A:U16  /V:0  /K:234,C0
SEGMENT E000
ADDRESS C000.

VMIC 7698 (Tundra)

DOS TUNA  /T:D0000  /S:D1000  /E:D5000  /A:S16  /V:C000  /M:D800E,0801
SEGMENT D100
ADDRESS C000
MAD     0000
```

11. Versions

V375-2: 4-channel VME arbitrary waveform generator

12. Customization

Consult factory for information about additional custom versions.

13. Revision History

13.1 Hardware Revision History

ASSY 22A375-2E March 2013

Functionally equivalent to Revision D.

ASSY 22A375-2D November 2007

This rev does some minor circuit board cleanups. It still uses firmware version 22376-E. Rev 2D is backwards compatible to all previous versions and is currently the only V375 being shipped.

ASSY 22A375-2C January 2007

This rev upgrades the firmware to version 22376-E. This adds new control bits to the JUMP CONTROL register to allow arbitrary block sizes, bidirectional waveform scanning, realtime read of waveform counter value, and alternate signals selectable to drive channel SYNC outputs. This allows simulation of digital and analog-output quadrature encoders, simulation of general position-oriented sin/cos sensors, and quadrature stepper/microstepper motor drive.

This version is fully backward compatible to the 22376-D firmware. All standard (-2C) boards will now be shipped with the 22376-E firmware.

The ECO which implements the new firmware also removes four capacitors C20, C21, C33, and C36. If older boards are field upgraded to the new firmware, be aware that the SYNC outputs may not be fast enough to operate in some situations that are now possible in extended JUMP modes.

ASSY 22A375-5C February 2006

This rev was a single-unit special modified per ECO579. It allows generation of a 5 volt p-p sine wave at 500 KHz.

ASSY 22A375-2C May 2005

This hardware design incorporates all of the features of both the -2B and the -3B versions. It uses EPROM program 22376D.

ASSY 22A375-3B November 2004

Hardware and firmware changes were added to enable the phase snapshot registers. Uses firmware version 22376C.

Firmware 22376D adds digital debounce logic to allow removal of debounce capacitors per ECO 0481. This change minimizes time delay for phase snapshot operations. 22376D is the universal firmware for V375-2B,-3B, and -2C.

ASSY 22A375-2B June 2003

Hardware was revised to support BURST and add external analog signal summing. Layout changes also reduce channel crosstalk at high frequencies. Used firmware 22376A. Includes JUMP, BURST; has waveform glitches at high DDS rates.

Firmware 22376B was released in August 2003: fixes high-clock-speed glitches. All V375 rev B boards should be upgraded to this firmware. Note that the ROM revision VME register erroneously reports this rev as "A"; check the ROM labels to be sure of the firmware revision.

ASSY 22A375-1A March 2003

This was the original version of the V375, released with firmware 22375A: no JUMP, no BURST. Has small waveform glitches above about 10 MHz DDS rates.

Firmware revision 22375B, June 2003, adds JUMP, but still has glitches.

Firmware revision 22375C, August 2003, fixed glitches. It is recommended to upgrade all rev A hardware to 22375C firmware.

13.2 Firmware Revision History

A V375 incorporates two socketed ROM chips. A pair of chips might be labeled 22375A.HI and 22375A.LO; these chips plug into the HIGH and LOW ROM sockets respectively. The ROM chip set incorporates the microprocessor program and the configuration data for all five FPGA chips on the module.

If ROM sets are replaced in the field, please be certain that the ROM version is compatible with the hardware rev, and be very careful to properly seat all pins on both chips, and observe orientation.

14. Accessories

J53-1:	3' SMB to BNC cable
J53-2:	6" SMB to BNC cable
V372-X:	Daisy chain cable