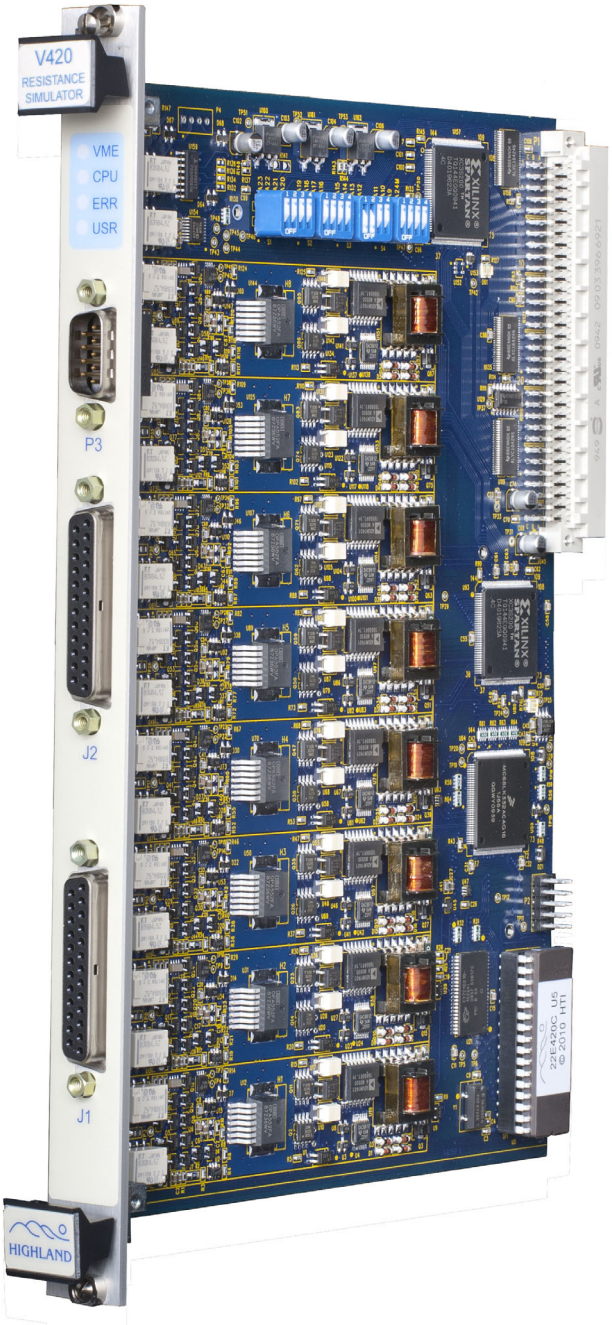
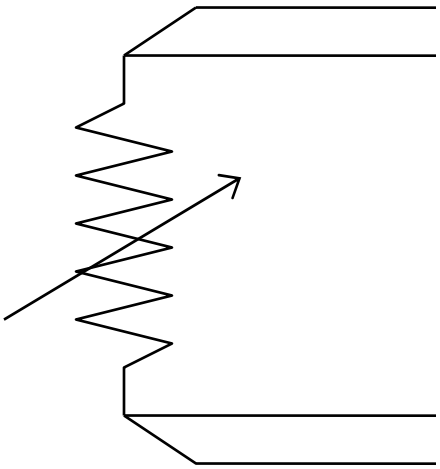
HIGHLAND TECHNOLOGY



V420 VME Isolated Resistance Simulator



Technical Manual

October 2, 2023

650 Potrero Avenue San Francisco, CA 94110 www.highlandtechnology.com tel: 415 551-1700 fax: 415 551-5129

650 Potrero Avenue, San Francisco, CA 94110
Phone 415-551-1700 • Fax 415-551-5129
www.highlandtechnology.com

NOTICE

HIGHLAND TECHNOLOGY, INC. PROVIDES THIS PUBLICATION “AS IS” WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

(Disclaimer of expressed or implied warranties in certain transactions is not allowed in some states. Therefore, the above statement may not apply to you.)

This manual may contain technical inaccuracies and/or typographical errors. Changes are periodically made to this manual which are incorporated in later editions. Highland Technology, Inc. may make changes and improvements to the product(s) and/or programs described in this publication at any time without notice.

The V420 has finite failure rates associated with its hardware, firmware, design, and documentation. Do not use the product in applications where a failure or defect in the instrument may result in injury, loss of life, or property damage.

IN NO EVENT WILL HIGHLAND TECHNOLOGY, INC. BE LIABLE FOR DAMAGES, INCLUDING LOST PROFITS, LOST SAVINGS OR OTHER INCIDENTAL OR CONSEQUENTIAL DAMAGES ARISING OUT OF THE USE OF OR INABILITY TO USE SUCH PRODUCT, EVEN IF HIGHLAND TECHNOLOGY, INC. OR AN APPROVED RESELLER HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, OR FOR ANY CLAIM BY ANY OTHER PARTY.

Table of Contents

1. Introduction

This is the technical manual for the Highland Model V420 eight-channel resistor/RTD simulator VME module.

The V420 is a VME module which simulates 8 isolated, high precision resistors or RTDs. Each resistor is independently programmable to one of five resistance ranges, or six RTD ranges. Within each range resistance changes are monotonic and glitch free.

Features of the V420 include:

- 8 channels of fully isolated 2/4 wire precision resistance/RTD simulation
- True 4-wire resistance measurements on all channels
- Suitable for simulating resistors, platinum/copper RTDs, thermistors, strain gauges, load cells
- Resistance programmable from 5 Ω to over 1 MΩ in five ranges
- RTD mode programmable for 100 Ω, 500 Ω and 1 kΩ platinum RTDs or 10 Ω copper RTDs
- Directly accepts temperatures in Celsius
- Fast, monotonic, glitch-free resistance changes allow for realistic RTD simulation with no dips or spikes
- Channels may be used in series or parallel for additional voltage and current capability
- Simple register based VME interface with no handshaking required
- Users may directly program resistances or RTD simulation (copper or platinum) temperatures
- Any channel is switchable to front-panel calibration check connector for in-system test without disconnecting field wiring
- Optional built-in self test (BIST)
- Clearly labeled dipswitches set VME address; no jumpers, headers, or trimpots

2. Specifications

FUNCTION	8-channel VME isolated resistance simulator
DEVICE TYPE	16-bit VME register-based slave: A24:A16:D16 Implements 256 16-bit registers at switch selectable addresses in the VME 16 or 24 bit addressing spaces
CHANNELS	8, 2-wire or 4-wire, galvanically isolated
RANGES	Standard resistance ranges: 5 Ω to 500 Ω 50 Ω to 5 kΩ 500 Ω to 50 kΩ 5 kΩ to 65 kΩ Extended resistance ranges: 5 kΩ to 1 MΩ Platinum RTD ranges: -125 °C to 700 °C 100 Ω Pt385 (α = .00385) -125 °C to 700 °C 1 kΩ Pt385 (α = .00385) -120 °C to 950 °C 100 Ω ITS-90 (α = .00393) -120 °C to 950 °C 1 kΩ ITS-90 (α = .00393) -120 °C to 950 °C 500Ω ITS-90 (α = .00393) Copper RTD ranges: -100 °C to 260 °C 10 Ω (α = .00427)
OPERATING RANGE	±35 V differential, ±50 mA DC or peak AC per channel
PROTECTION	±50 V differential ±750 V common-mode ESD to 5 kV, human body model
RESOLUTION	Standard resistance ranges: Variable from 12-15 bits with higher resolution at the lower end of the range (see section 5.4) RTD ranges: 0.0625 °C
ACCURACY	±0.1% typical (±1% max) of resistance setting

	±0.25 °C on RTD ranges DC offset error < 10 µV
NON-LINEARITY	± 5 ppm/V ± 25 ppm/W
TEMPERATURE COEFFICIENT	± 20 ppm/ºC
OPERATING TEMPERATURE	0 to 60°C; extended MIL/COTS ranges available
CALIBRATION INTERVAL	1 year
POWER	Standard VME supplies: +5 V, 1 A max +12 V, 1 A max -12 V, 1 A max
CONNECTORS	2 D25 female for channels D9 male for test
INDICATORS	LEDs indicate VME access, CPU activity, error conditions Additional user programmable LED
PACKAGING	6U single-wide VME module
CONFORMANCE	ANSI/VITA 1-1994 (R2002) VMEbus spec; does not support byte writes IEC-751 for "385" curve platinum RTDs ITS-90 for "393" curve platinum RTDs

3. Overview

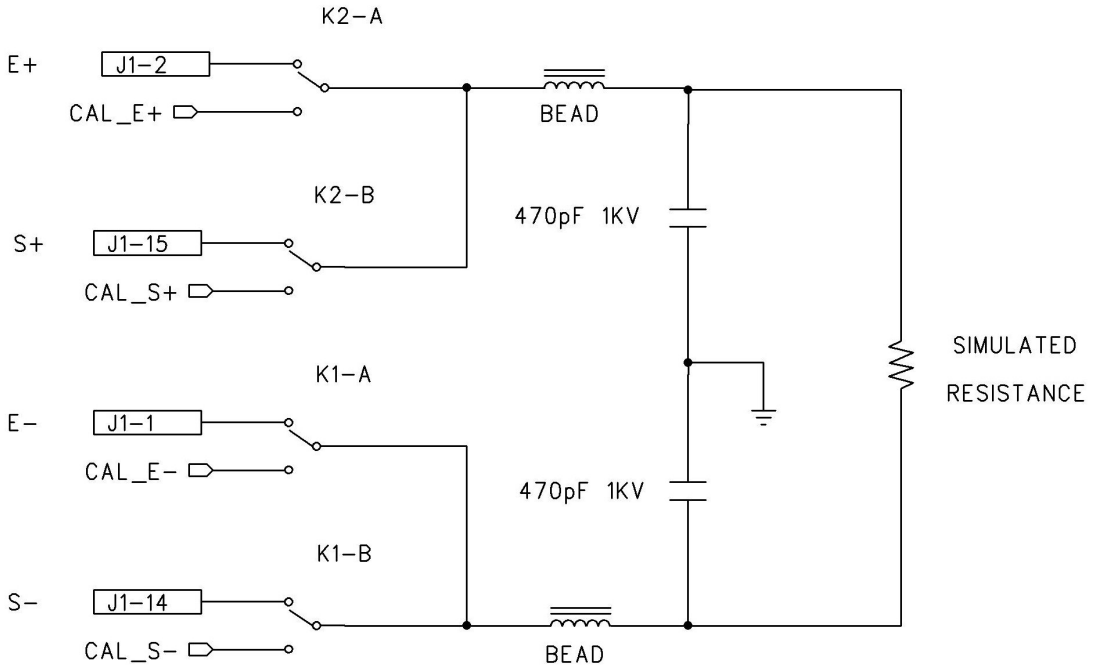
The V420 is a programmable resistance simulator with 8 independent, isolated channels. Each channel has an isolated DC power supply and digital interface, resistance simulation circuitry, signal conditioning, and input protection circuits.

Resistances are electronically simulated, and are accurate for DC, AC, or pulsed excitation. Unlike modules using relay-switched series or parallel combinations of discrete resistors, this entirely solid-state topology means that changes of resistance are monotonic, with no glitches during transition.

Setup consists of selecting a resistance or temperature range for each channel. Once set up, users can write desired resistance or temperature values to VME registers at any time, with no handshaking. The V420 will update actual resistances within 2 milliseconds of a VME write. Resistances are 32-bit unsigned fixed point numbers, consisting of 16 integer bits and 16 fractional bits on all standard resistance ranges (see section 5.4 for more information). RTD Temperatures are 16-bit signed fixed point, with 12 integer bits and 4 fractional bits, regardless of the selected RTD type.

Relays are provided to connect any input channel to the dedicated D9 calibration connector for accurate 4-wire verification of channel performance, or to the optional built-in self-test circuitry for automatic testing. Units are calibrated against a Keithley digital voltmeter accurate to 20 PPM and traceable to NIST.

The arrangement of a typical channel is...



The four connector pins are nominally called Excitation+, Sense+, Excitation-, and Sense-. Due to the symmetric architecture of the V420, excitation voltage of either polarity can be applied to the + and – signals, and the excitation and sense wires can be used interchangeably. Except for the 470 pF ESD/RFI capacitors to ground each channel is fully isolated from both ground and the other channels.

One normally makes 4-wire connections using the E terminals to provide current and the S terminals for sensing. Two-wire connections may be made to E+ and E-; this will add about 150 mΩ of trace and connector resistance. One can also parallel the E and S pins to reduce effective 2-wire resistance error to less than 100 mΩ. Note that a 100 Ω platinum RTD changes about 0.4 ohms per degree C, so 4-wire connections are required for high precision temperature simulation.

The maximum channel power dissipation happens at 30 V and 50 mA (600 ohms programmed, where dissipation is 1.5 W. When used at high power dissipation, the module requires normal VME crate forced-air cooling of 200 LFPM or better.

Channels may be used in series or in parallel to increase voltage or current handling capability, respectively. In series mode, all grouped resistors should be set to the same resistance and no channel’s voltage should be allowed to exceed the maximum voltage rating of 30V. In parallel mode, resistances should be programmed equally to balance channel power dissipation., and no channel’s current should be allowed to exceed 50 mA.

4. Connectors and Installation

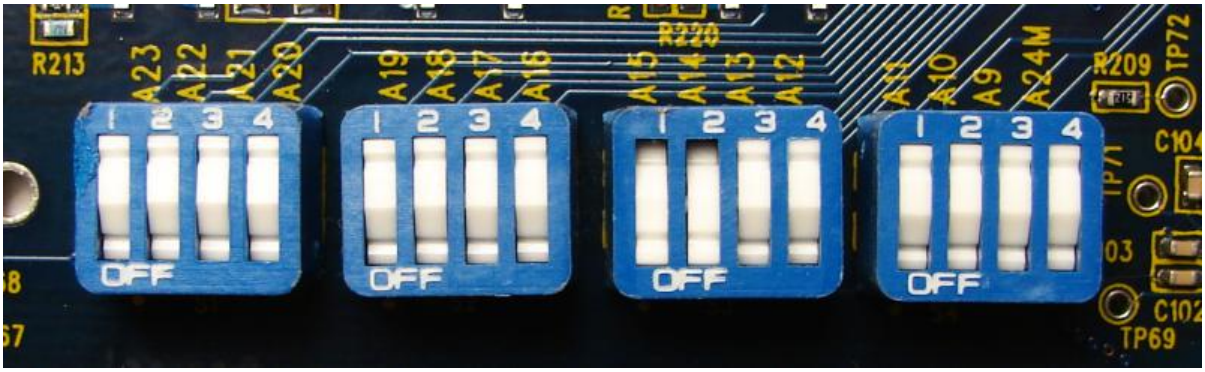
4.1. Address DIP Switches

Four 4-position rocker-type dipswitches are provided near the top edge of the board. The address switches are labeled "A23" through "A9" and finally "A24M". The V420 occupies 256 words (512 bytes) of VMEbus space, so bus addresses are multiples of 0x0200.

To set a switch to the logical "1" or "ON" position, press the side of the switch nearest its "Axx" lettering. Use a toothpick or paper clip, not a pen or pencil.

The A24M switch, when set, allows the board to operate in the VME 24-bit (A24) address space; in this case, address switches A23 through A9 are active and the board responds to VME address modifier codes 0x39 and 0x3D. If the A24M switch is off, the module resides in the A16 space and responds to address modifiers 0x29 and 0x2D. In this case, only address switches A15 through A9 are active.

Units are shipped with switches A15 and A14 on, all others off, locating the register base at 0xC000 in the A16 space, as shown in the figure below.



4.2. Installation

The V420 may be installed in any VME (IEEE 1014) crate, including VME64 variants. It uses only the P1 backplane connector. To meet specified accuracy, a minimum of 200 LFPM air flow is required across the circuit board surface.

The V420 passes all interrupt and bus grant signals, so may be used with backplane grant jumpers installed or not installed.

CAUTION: Do not install or remove the V420 with crate power on. VME modules are not hot-pluggable. The V420 will be damaged if hot-plugged.

CAUTION: Fully seat the module and secure front-panel screws before applying power.

CAUTION: Handle the V420 with proper ESD precautions to avoid static damage.

4.3. Connectors

4.3.1. Channel Output Connectors

Two front-panel female D-25 connectors are provided. Each connector accommodates four resistor channels.

The pinout of the D25 connectors are as follows:

Pin	Signal	Pin	Signal
J1-1	ch 0 E-	J1-14	ch 0 S-
J1-2	ch 0 E+	J1-15	ch 0 S+
J1-3	ch 1 E-	J1-16	ch 1 S-
J1-4	ch 1 E+	J1-17	ch 1 S+
J1-5	ch 2 E-	J1-18	ch 2 S-
J1-6	ch 2 E+	J1-19	ch 2 S+
J1-7	ch 3 E-	J1-20	ch 3 S-
J1-8	ch 3 E+	J1-21	ch 3 S+
J1-9	No Connection	J1-22	No Connection
J1-10	No Connection	J1-23	No Connection
J1-11	VME +5V	J1-24	No Connection
J1-12	No Connection	J1-25	No Connection
J1-13	VME GND		

Pin	Signal	Pin	Signal
J2-1	ch 4 E-	J2-14	ch 4 S-
J2-2	ch 4 E+	J2-15	ch 4 S+
J2-3	ch 5 E-	J2-16	ch 5 S-
J2-4	ch 5 E+	J2-17	ch 5 S+
J2-5	ch 6 E-	J2-18	ch 6 S-
J2-6	ch 6 E+	J2-19	ch 6 S+
J2-7	ch 7 E-	J2-20	ch 7 S-
J2-8	ch 7 E+	J2-21	ch 7 S+
J2-9	No Connection	J2-22	No Connection
J2-10	No Connection	J2-23	No Connection
J2-11	VME +5V	J2-24	No Connection
J2-12	No Connection	J2-25	No Connection
J2-13	VME GND		

Connector shells are bonded to the VME front panel, which connects to the crate frame through the module securing screws.

4.3.2. D9 Calibration Connector

A male D9 connector is provided for connection to an external 4-wire precision ohmmeter. Each input channel incorporates a relay which allows it to be switched, under software control, to this test connector.

Pinout of the D9 is...

Pin	Signal	Pin	Signal
P3-1	No Connection	P3-6	E-
P3-2	No Connection	P3-7	E+
P3-3	No Connection	P3-8	S-
P3-4	No Connection	P3-9	S+
P3-5	No Connection		

The RELAYS register is used to control the channel relays and the MODE register controls access to the cal bus and test resistor.

Refer to section 7 of this manual for a discussion of module calibration verification.

5. Basic Operation and Concepts

5.1. General Considerations

The V420 occupies 256 16-bit VME registers. DIP switches are provided to set the base address to any 256-word (address 0x0200) boundary in the A16 or A24 address spaces. All registers are implemented as true dual-port memory which is shared between the VMEbus and the internal microprocessor.

VME access time is typically 200 ns, measured from DS* to DTACK*.

The module is normally shipped configured for base address of 0xC000 in the A16 address space.

Certain register pairs represent 32-bit values and must be written atomically to ensure that updates do not create skew errors. Atomic pairs must be written in the order MS:LS, and will not be effective until the LS word is written.

The V420 does not support single-byte writes from VME.

5.2. Front-Panel LEDs

The blue VME LED will flash whenever the V420 is addressed from the VMEbus.

The green CPU LED will blink once about every two seconds to indicate that the internal firmware is operating normally. See section 8 for notes on LED operation during BIST self-test.

The red ERROR LED will normally be off. It will flash if any error flags are set. Blinks patterns are…

one blink	channel programming error
two blinks	internal error

The orange USER LED may be programmed from the VMEbus.

5.3. Channel Setup and Operation

After powerup, basic module operations can be established with two VME write operations per channel:

- Write a 16-bit channel control word to the channel control register to select a resistance or RTD range.
- Write either a 32-bit resistance value or a 16-bit effective RTD temperature to the resistance or temperature registers to set the channel output.

Channel range setups may take up to 10 milliseconds to be effective. Once a range has been selected, a resistance or temperature setting will update to the requested value within 2 milliseconds.

5.4. Simulating Resistance

The V420 can simulate any resistance from 5 to 1.048 MΩ. This span is divided up into four overlapping "standard resistance" ranges, as follows:

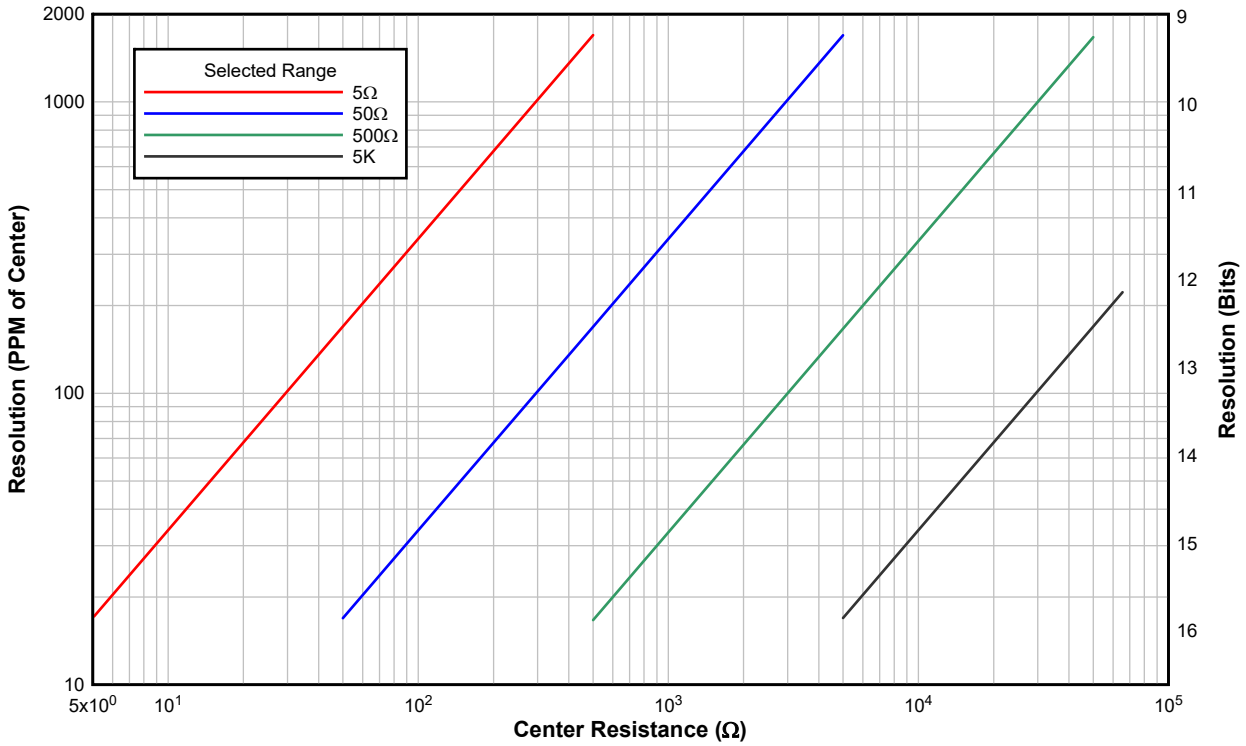
Range	R_{MIN}	R_{MAX}
0	5 Ω	500 Ω
1	50 Ω	5 kΩ
2	500 Ω	50 kΩ
3	5 kΩ	65 kΩ

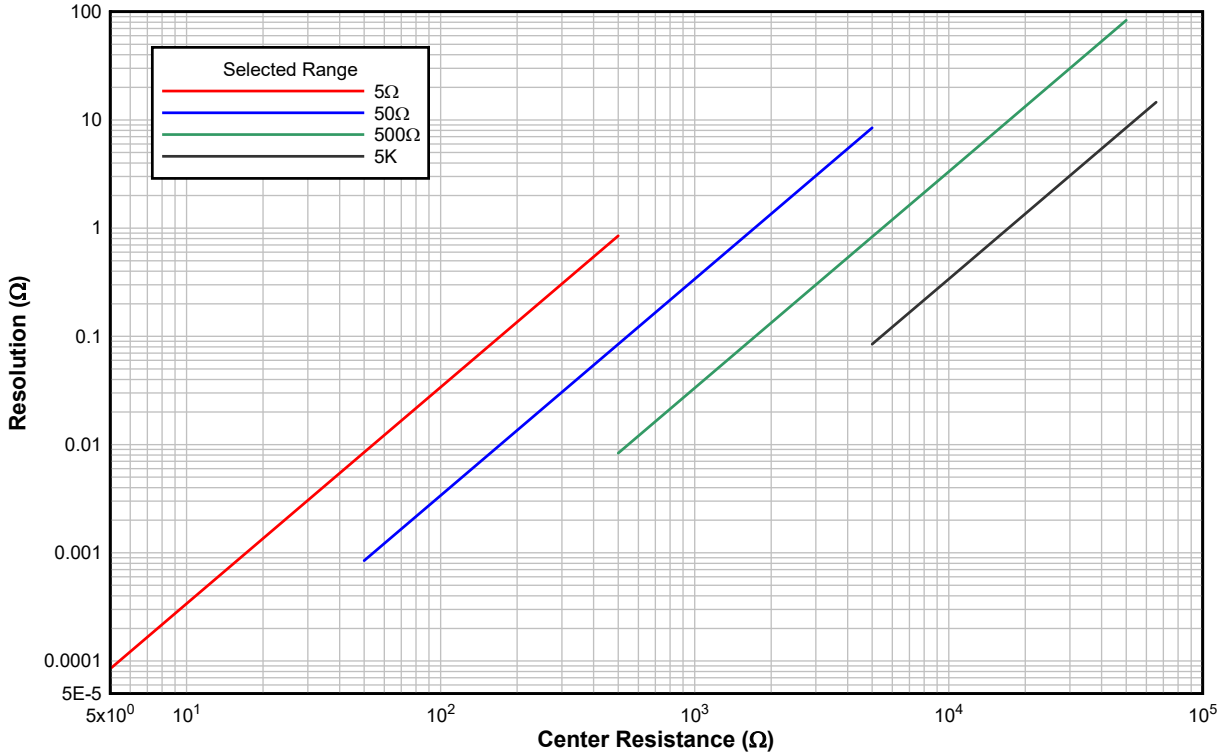
Additionally, extended resistance range 15 is from 5 kΩ to 1 MΩ, but requires formatting the resistance request differently.

5.4.1. Standard Resistance Ranges

First, set the resistance range by writing to the channel control register REGx. Once the resistance range is set, enter the desired resistance value by writing it to the RHx:RLx VME register pair. The unsigned 32-bit value is equal to $R_{REQ} \times 2^{16}$, making the upper word RHx equal to the whole number of ohms desired, and the lower word RLx equal to the fractional ohms. Thus, the largest resistance that may be requested is 65535.999985 Ω. The lowest resistance that may be requested is set by the range as described above. An attempt to set a resistance value below what is available for the range will set the channel to the range minimum and set the channel programming error bit for that channel. An attempt to set a resistance value above the recommended maximum for the channel will not set the channel to the range maximum and set the channel programming error bit for that channel.

Though at all times resistance is specified as a 32-bit value, the V420 will round this to the nearest value that can be represented by the hardware. The available resolution near a requested resistance is a function of the base resistance of the selected range. While the ranges are capable of simulation of resistances over a 100:1 span, on any given range the available resolution for a requested resistance R_{REQ} increases as R_{REQ}^2 / R_{MIN}, therefore for best performance use the highest R_{MIN} that will allow for the full simulation range. The resolution is described quantitatively in the figures below.


Selected Range
5Ω
50Ω
500Ω
5K
Resolution (PPM of Center)
Resolution (Bits)
Center Resistance (Ω)
2000
1000
100
10
9
10
11
12
13
14
15
16
5x10^0
10^1
10^2
10^3
10^4
10^5


Selected Range
5Ω
50Ω
500Ω
5K
Resolution (Ω)
Center Resistance (Ω)
100
10
1
0.1
0.01
0.001
0.0001
5E-5
5x10^0
10^1
10^2
10^3
10^4
10^5

The V420 is guaranteed to be able to reach the minimum resistance value of the range inclusively; therefore one can use the 50 ohm range to simulate 50.000 Ω.

Example: To set channel 2 to be a 78.75 Ω resistor, first write 0x0001 into CTL2, placing it in the 50 Ω – 5 kΩ range. Then write 78 (0x004E) into DH2 and 0.75 (0xC000) into DL2. Upon the write to DL2, channel 2 will change to simulating a 78.75 Ω resistor.

5.4.2. Extended Resistance Range

To use the extended resistance range, set the channel control register REGx to use the extended range. Once the resistance range is set, enter the desired resistance value by writing it to the RHx:RLx VME register pair. The unsigned 32-bit value is equal to R_{REQ} x 2^{12}, making the upper word RHx equal to the number of ohms divided by 16. As the extended resistance range tends to be used for lower accuracy applications, commonly the RLx register will simply be set to zero, however for resistance values below roughly 30 kΩ some additional resolution can be achieved by using it.

Example: To set channel 2 to be a 787.5 kΩ resistor, first write 0x000F into CTL2, placing it into the 5 kΩ – 1 MΩ range. 787,500 * 4096 = 3,225,600,000 = 0xC042:C000, so write 0xC042 into DH2 and 0xC000 into DL2. Upon the write to DL2, channel 2 will change to simulating a 787.5 kΩ resistor.

5.5. Simulating RTDs

The V420 allows the native simulation of precision RTDs, using internal lookup tables to convert a desired temperature into a resistance. The available RTD ranges are:

Range Code	RTD	Standard	Temperature Range
4	100 Ω Platinum	α = .00385 IEC 751	-125 °C to 700 °C
5	1 kΩ Platinum	α = .00385 IEC 751	-125 °C to 700 °C
6	100 Ω Platinum	α = .00393 ITS-90	-120 °C to 950 °C
7	1 kΩ Platinum	α = .00393 ITS-90	-120 °C to 950 °C
8	10 Ω Copper	α = .00427	-100 °C to 260 °C
9	500 Ω Platinum	α = .00393 ITS-90	-120 °C to 950 °C

Once the RTD range is set, enter the desired temperature by writing it to RTDx register. The signed 16-bit value is equal to the temperature in °C x 16, making the LSB equal to 1/16 °C, and the total range of the register -2048 °C to 2047.9375 °C.

An attempt to set the channel to a resistance outside the legal temperature limits for the type will set the resistance appropriately for the limiting value, and set the channel programming error bit for the channel.

6. VME Registers

6.1. Register Map

The V420 implements 256 16-bit VME registers. REG# below is the ordinal register number in decimal; OFFSET is the hex VMEbus offset from the module base address. The as-shipped default address is 0xC000 in the A16 space.

Registers identified as "RO" should be treated as read-only and should not be written from VME; these registers are periodically refreshed by the V420.

The letter "A" in the R/W column indicates that a register pair is atomically locked for 32-bit operations. Atomic pairs must be read or written in the order MS:LS.

Read-write (RW) registers are normally written from VME and, after powerup initialization, are not altered by the internal microprocessor.

REG NAME	REG#	OFFSET	R/W	Function
VXI MFR	0	0x00	RO	VXI mfr ID: reads 65262, 0xFEEE
VXITYPE	1	0x02	RO	module type, always 22420 decimal
SERIAL	3	0x06	RO	unit serial number
ROM ID	4	0x08	RO	firmware ID, typically 22420 decimal
ROM REV	5	0x0A	RO	Firmware revision, typically ASCII "C"
MCOUNT	6	0x0C	RO	microprocessor IRQ update counter
CFLAGS	8	0x10	RO	channel error indicators
SYSFLAGS	10	0x14	RO	System error indicators
RELAYS	11	0x16	RW	controls calibration-bus relays
ULED	12	0x18	RW	user LED control
MODE	13	0x1A	RW	module operating mode
CALID	14	0x1C	RO	calibration table status
BISS	15	0x1E	RO	built-in self-test control **
MACRO	16	0x20	RW	macro command register

REG NAME	REG#	OFFSET	R/W	Function
PARAM0	17	0x22	RW	macro parameter
PARAM1	18	0x24	RW	macro parameter
PARAM2	19	0x26	RW	macro parameter
YCAL	20	0x28	RO	calibration date, year
DCAL	21	0x2A	RO	calibration date, month/day
CTL0	32	0x40	RW	Channel 0 control
RTD0	33	0x42	RW	Channel 0 RTD temperature
CTL1	36	0x48	RW	Channel 1 control
RTD1	37	0x4A	RW	Channel 1 RTD temperature
CTL2	40	0x50	RW	Channel 2 control
RTD2	41	0x52	RW	Channel 2 RTD temperature
CTL3	44	0x58	RW	Channel 3 control
RTD3	45	0x5A	RW	Channel 3 RTD temperature
CTL4	48	0x60	RW	Channel 4 control
RTD4	49	0x62	RW	Channel 4 RTD temperature
CTL5	52	0x68	RW	Channel 5 control
RTD5	53	0x6A	RW	Channel 5 RTD temperature
CTL6	56	0x70	RW	Channel 6 control
RTD6	57	0x72	RW	Channel 6 RTD temperature
CTL7	60	0x78	RW	Channel 7 control
RTD7	61	0x7A	RW	Channel 7 RTD temperature

REG NAME	REG#	OFFSET	R/W	Function
RH0	64	0x80	RWA	Channel 0, integer ohms
RL0	65	0x82	RWA	Channel 0, fractional ohms
RH1	66	0x84	RWA	Channel 1, integer ohms
RL1	67	0x86	RWA	Channel 1, fractional ohms
RH2	68	0x88	RWA	Channel 2, integer ohms
RL2	69	0x8A	RWA	Channel 2, fractional ohms
RH3	70	0x8C	RWA	Channel 3, integer ohms
RL3	71	0x8E	RWA	Channel 3, fractional ohms
RH4	72	0x90	RWA	Channel 4, integer ohms
RL4	73	0x92	RWA	Channel 4, fractional ohms
RH5	74	0x94	RWA	Channel 5, integer ohms
RL5	75	0x96	RWA	Channel 5, fractional ohms
RH6	76	0x98	RWA	Channel 6, integer ohms
RL6	77	0x9A	RWA	Channel 6, fractional ohms
RH7	78	0x9C	RWA	Channel 7, integer ohms
RL7	79	0x9E	RWA	Channel 7, fractional ohms
LBHI	80	0xA0		BIST loopback hi **
LBLO	81	0xA2		BIST loopback lo **

Registers tagged ** and registers 128-255 are reserved for calibration and BIST.

Note that registers 64-81 accept data as 32-bit MS:LS register pairs. Each pair is atomically interlocked to avoid the possibility of a collision between a uP update and a VME read, which could result in incoherent data. To guarantee coherent data, the VME user must write the first (MS) word of each pair and then write the second (LS) word of that same variable.

6.2. Module Identification Registers

6.2.1. VXI MFR (0x00)

0xFEEE, Highland Technology's registered VXI ID code.

6.2.2. VXITYPE (0x02)

Module type identifier, always 22420 in decimal.

6.2.3. SERIAL (0x06)

Module serial number

6.2.4. ROM ID (0x08)

Firmware version, typically 22420 decimal representing a 22E420x ROM, where x is the revision code.

6.2.5. ROM REV (0x0A)

ASCII code identifying the revision letter of the firmware, typically 0x43 for “C”.

6.2.6. MCOUNT(0x0C)

The read-only MCOUNT register is an unsigned 16-bit integer which is incremented every microprocessor interrupt, about every 5 ms. Continued updates of this register serve as a “still alive” indicator from the VME bus.

6.3. System Control Registers

6.3.1. CFLAGS (0x10)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0	E7	E6	E5	E4	E3	E2	E1	E0

The read-only CFLAGS register displays 16 channel error flags. The high byte contains error flags for improper channel programming. The low byte contains error flags for a resistor excitation signal outside of the allowable range. In both cases, bits 0..7 of the byte correspond to resistor channels 0..7.

A Px flag will be set if a channel is programmed for a value which is out of the current range. In this case, the V420 will attempt to meet the requested value as well as the range allows. The flag will also be set if the channel is programmed for an undefined range; in this case the V420 will become a >65 kΩ resistor. Px error bits will self-clear once the channel is programmed properly.

Ex bits will be set when either the voltage or current limit of the device is exceeded. In this case the V420 will again become a >65K resistor to try to protect the internal electronics. Ex bits will clear within 250 ms of the input signal being returned to a valid range.

6.3.2. SYSFLAGS (0x14)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						BISO	BMEAS		FPGA	CAL				INP	PROG

The read-only SYSFLAGS register displays system wide error flags.

The PROG flag will be raised to indicate a channel programming error. The INP flag will be raised to indicate a channel input error. More information about these conditions is available by reading the CFLAGS register, which provides channel by channel error reporting. The CAL flag is raised to indicate that the module is using the default calibration table, and is thus acting as an uncalibrated board. The FPGA flag is raised to indicate that one of the two FPGAs is not working properly.

On V420-2 boards featuring BIST functionality, the BISO flag will be raised to indicate that an isolation fault has been detected by the self test, and the BMEAS flag will be raised to indicate a fault in the BIST measurement subsystem. On V420-1 boards without BIST, these flags will always be clear.

With the exception of the INP and PROG flags, all other flags in SYSFLAGS indicate hardware problems requiring the board to be returned to Highland.

6.3.3. RELAYS (0x16)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								K7	K6	K5	K4	K3	K2	K1	K0

The RELAYS register controls actuation of the channel test relays. If the user sets any bit ON, the corresponding channel test relay will be actuated. The associated channel will then be disconnected from the front-panel D25 connector and connected to the internal cal bus, which may in turn be routed to the D9 test connector, as noted in section 7.

In addition to providing a calibration path, activating a test relay disconnects the four-wire front panel D25 connection, allowing simulation of a break in field wiring.

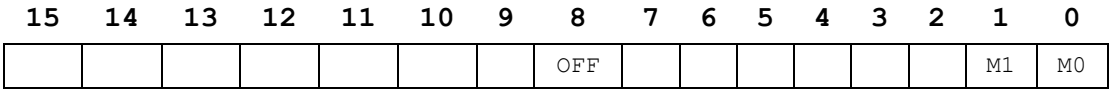
More than one relay may be operated at any time, resulting in the selected channels being connected in parallel to the cal bus. While not useful for calibration, this does allow for the disconnection of multiple channels at once.

6.3.4. ULED (0x18)

An orange LED is provided on the front panel for user application. The ULED register allows user flash patterns to be loaded. An internal shift register is periodically loaded from the contents of the ULED register, and the MS bit of this register operates the orange LED. The shift register is left-shifted every 125 milliseconds, and the register is reloaded every 16 shifts, namely every 2 seconds.

ULED pattern 0x0000 turns the user LED off. Pattern 0xFFFF turns it steady on. Pattern 0xF000 would result in a blink pattern, 0.5 seconds on and 1.5 seconds off.

6.3.5. MODE (0x1A)



Sets the operating mode of the calibration bus. The fixed reference BIST modes are used primarily for factory calibration; for general use the autoranging mode is probably the right one to use.

Mcode	M1	M0	Effect
0	0	0	Calibration bus -> BIST (autoranging)
1	0	1	Calibration bus -> D9 test connector
2	1	0	Calibration bus -> BIST (200 Ω reference)
3	1	1	Calibration bus -> BIST (5100 Ω reference)

Setting the OFF bit will disable the isolated power supplies of all 8 resistance channels. This is intended for factory test only; users whose systems require this feature should further discuss their application with Highland Technology.

6.3.6. CALID (0x1C)

The CALID register displays a value which reflects the currently installed calibration table. The normal value for the V420-1 and V420-2 modules is 22420 decimal, 0x5794. If the factory calibration table is corrupted, the firmware will install the default calibration table, the CALID register will display value 0xDEFC, the CERR bit will appear in the SYSFLAGS register, and the red LED will flash.

6.3.7. BISS (0x1E)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCH		ISO	MEA					BSY							BAV

The BISS register is the BIST status. The high byte indicates errors, and the low byte indicates status information.

In the high byte, BCH indicates BIST detected a channel failure. ISO indicates a detected isolation failure. MEA indicates a failure in the BIST measurement subsystem.

In the low byte, the BAV bit indicates that the BIST facility is available. BSY is true while the BIST self-test is in progress.

6.4. Macro Registers

6.4.1. MACRO (0x20)

Code	Operation	Max Time
0x8400	no operation	250 us
0x8404	Set all channels to 5 Ω – 500 Ω range	4 ms
0x8405	Set all channels to 50 Ω – 5 kΩ range	4 ms
0x8406	Set all channels to 500 Ω – 50 kΩ range	4 ms
0x8407	Set all channels to 5 kΩ – 65 kΩ range	4 ms
0x8410	BIST – Full test	70 sec
0x8409	BIST – Single channel	10 sec
0x8420	Hard reboot; reloads FPGAs, restarts code; disappears from VMEbus for about 4 seconds	5 sec
0x8421	Soft reboot the module; remains on bus.	20 ms

The macro control register allows invocation of microprocessor service routines. Some macros take or return data in the PARAM0 through PARAM2 registers. MACRO codes not defined above may be used in factory test and calibration; poking around at them is not advised.

To execute a macro,

Verify that the MS bit (bit 15) of the MACRO register is clear, indicating that the microprocessor is ready to accept a command.

Write any required macro parameters.

Write a 16-bit macro code to the MACRO register.

Wait until the MS bit again clears, or wait longer than the maximum macro execution time. If any other bits are then set in MACRO, an error has occurred.

Read any returned parameters.

6.4.2. PARAM0 – PARAM2 (0x22-0x26)

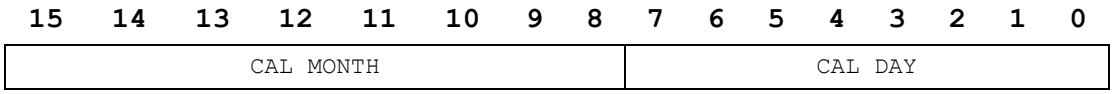
Macro parameter registers. The use of these depends on the macro that will be executed. See the macro descriptions in the chapters for more details.

6.5. Calibration Date Registers

6.5.1. YCAL (0x30)

Stores the year of the calibration date as an integer, i.e. 2008 (0x07D8) for the year 2008.

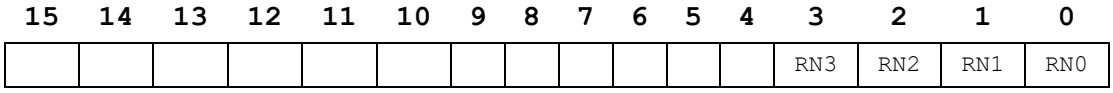
6.5.2. DCAL (0x32)



Stores the day of the calibration date as two byte-wide integers, i.e. Feb 29 is 02 (0x02) : 29 (0x1D) is 0x021D.

6.6. Channel Control Registers

6.6.1. CTLx (0x40, 0x48, 0x50, …0x78)



Each of the eight isolated resistance channels has an associated channel control register, CTL0 through CTL7. Users must initialize the control registers of any channels which will be active.

The RN bits select the resistor type and range for this channel; with the four RN bits encoded 0 through 15 decimal. Ranges are...

RN CODE	CHANNEL TYPE		RANGE		
0	resistor		5 Ω	to	500 Ω
1	resistor		50 Ω	to	5 kΩ
2	resistor		500 Ω	to	50 kΩ
3	resistor		5 kΩ	to	65 kΩ
4	RTD	100 Ω (Pt385)	-125°C	to	700°C
5	RTD	1 kΩ (Pt385)	-125°C	to	700°C
6	RTD	100 Ω (Pt393)	-120°C	to	950°C
7	RTD	1 kΩ (Pt393)	-120°C	to	950°C
8	RTD	10 Ω (Cu492)	-200°C	to	260°C
9	RTD	500 Ω (Pt393)	-120°C	to	950°C
15	resistor	(extended)	5 kΩ	to	1 MΩ

6.6.2. RTDx (0x42, 0x4A, 0x52, …0x7A)

For channels programmed as RTD simulators (RN codes 4 to 8) the resistance is controlled by writing to the corresponding RTDx registers. The data is formatted as a signed 16-bit value with an LSB of 1/16 °C as described in section 5.5 - Simulating RTDs.

6.6.3. RHx:RLx (0x80, 0x84, 0x88 … 0x9C)

For channels programmed as resistors (RN codes 0 to 3) the resistance is controlled by writing to the corresponding RHx:RLx register pair. The data is formatted as an unsigned 32-bit value with an LSB of 2^{-16} Ω, which is the equivalent of writing the integer part of the resistance into RHx, and the fractional part into RLx. This is more fully described in section 5.4 - Simulating Resistance.

For channels on the extended resistance range 15, the data is formatted as an unsigned 32-bit value with an LSB of 2^{-12} Ω.

This pair must be read or written in the order RHx followed by RLx; writes takes effect when RLx is written.

6.7. Manual Self-Test Registers

6.7.1. LBHI:LBLO (0xA0)

The LBHI:LBLO reports back the resistance on the calibration bus, as measured by the built-in self-test circuitry. This register pair is inoperative when the MODE register is set to 1, which routes the calibration bus to the D9 test connector rather than to BIST.

The data format is unsigned fixed point with 15 fractional bits. This is one fewer fractional bit (and one more integer bit) than the normal resistance format used by the channels, and results in a maximum expressible value of roughly 131 kΩ (2^{17} Ω to be exact). The extra bit is necessary to provide room for the BIST to express slightly over the 65 kΩ maximum resistance that the channels can provide.

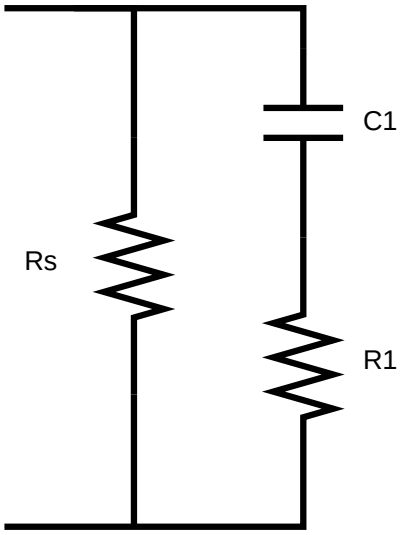
More information about the loopback test is available in section 9 - BIST.

7. Realtime Considerations

7.1. Channel Dynamic Performance

As each V420 channel is an electronically simulated resistor, the dynamic performance has somewhat complex behavior when presented with a changing stimulus. We will present a simplified first-order model of the channel behavior here; this should not be relied upon to be more than an approximation.

The programmed resistance Rs appears in parallel with a combination of transient behavior components R1 and C1. This causes the step response to be an initial step, followed by an exponential approach to the final DC value. These components are a function of the selected range, and can be approximated as



Range	R1	C1
0	20 Ω	700 nF
1	70 Ω	70 nF
2	400 Ω	7 nF
3	ZERO	1.5 nF

For RTD ranges, the dynamics are the same as the resistance range used to emulate that RTD. For instance, 100 Ω RTDs are simulated on range 1, 50 Ω – 5K

This makes the effective bandwidth a function of both the programmed resistance and the driving circuit; a low impedance voltage source will be able to overcome the capacitance more quickly than a high impedance current source. So, for instance, a programmed 100 Ω resistor on range 0 will be down to 50 Ω at approximately 3.5 kHz, whereas the same programmed 100 Ω on range 1 will not be down to 50 Ω until nearly 40 kHz. On any given range, bandwidth will be roughly inversely proportional to programmed resistance, as it is determined by the time constant set by the product of Rs and C1.

8. Calibration Verification

It is recommended that the V420 receive annual calibration in order to maintain specified accuracy. Users may also check channel calibration on a regular basis to verify that the module meets their specific system requirements.

A precision 4-wire DVM may be used to verify channel resistances without removing field wiring connectors. The procedure is...

Connect a precision DVM to the D9 male test connector P3 on the V420 front panel. The connections should be...

P3 Pin	V420 Signal	DVM Connection
P3-6	E-	IN-
P3-7	E+	IN+
P3-8	S-	SENSE-
P3-9	S+	SENSE+

Now write 0x0001 to the MODE register, and write a single bit to the RELAYS register, where bits 0 (0x0001) through 7 (0x0080) activate the test relays of channels 0 through 7 respectively. Now the DVM may be used to verify the resistance programmed on the selected channel.

9. BIST

The V420 is optionally available with Built-In Self Test. There are two BIST operating modes, full and single-channel.

In full-test mode, a full self-test is invoked by writing command code 0x8410 to the MACRO register. The test checks resistor accuracy on all ranges and checks channel isolation to ground. When the test is over, the MACRO register goes to 0x0000 for the no-error condition, or 0x0100 if any errors are detected.

In the interest of saving time, single channel tests can be invoked instead. In order to test just a single channel, write the number of that channel to the PARAM0 register, then write command code 0x8411 to the MACRO register. This test will check resistor accuracy on the specified channel only, and report the same result code as the full test.

In addition to the automated tests, BIST can also be operated manually by selecting a channel onto the calibration bus using the RELAYS register, setting the MODE register to 0 (connecting the calibration bus to the self-test circuitry), and reading the resulting resistance from the LBHI:LBLO register pair. The loopback resistance is a 32-bit unsigned number, with an LSB representing 2^{-15} Ω, and is updated roughly once per second.

10. Versions

V420-1: 8-channel VME isolated resistance simulator 0° to 60°C

V420-2: 8-channel VME isolated resistance simulator 0° to 60°C with BIST

11. Customization

Consult factory for information about additional custom versions.

12. Hardware and Firmware Revision History

12.1. Hardware Revision History

Revision E Sep 2023

Revision D Mar 2012

Revision C Jan 2010

Revision B Sep 2009

Revision A Sep 2006
Initial PCB release

12.2. Firmware Revision History

Revision G March 2017
Fixed bug leading to incorrect out of range errors on RTDs

Revision F August 2015
Fixed math error in BIST

Revision E May 2014
Adds 1 MEG range

Revision D Feb 2012
Adds 500R PT393 RTDS

Revision C Apr 2010
Fixes some problem cases in BIST routines

Revision B Apr 2010
Supports BIST and changes BIST scaling from U16.16 to U17.15
Fixes overflow in quadratic term of MDAC math
Fixes relay power-on glitch
First production release

Revision A Mar 2010
Initial firmware package

13. Accessories

J55-1:	6' shielded D25 male to D25 male cable
J56-1:	10' shielded D25 male to D25 male cable
J475-1:	8-channel D25 female Din rail termination panel

650 Potrero Avenue San Francisco, CA 94110 www.highlandtechnology.com tel: 415 551-1700 fax: 415 551-5129