HIGHLAND TECHNOLOGY

T660

DIGITAL DELAY GENERATOR

Technical Manual

January 25, 2024

650 Potrero Avenue San Francisco, CA 94110 www.highlandtechnology.com tel: 415 551-1700 fax: 415 551-5129

650 Potrero Avenue, San Francisco, CA 94110
Phone 415-551-1700 • Fax 415-551-5129
www.highlandtechnology.com

NOTICE

HIGHLAND TECHNOLOGY, INC. PROVIDES THIS PUBLICATION “AS IS” WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

(Disclaimer of expressed or implied warranties in certain transactions is not allowed in some states. Therefore, the above statement may not apply to you.)

This manual may contain technical inaccuracies and/or typographical errors. Changes are periodically made to this manual, which are incorporated in later editions. Highland Technology, Inc. may make changes and improvements to the product(s) and/or programs described in this publication at any time without notice.

This product has finite failure rates associated with its hardware, firmware, design, and documentation. Do not use the product in applications where a failure or defect in the instrument may result in injury, loss of life, or property damage.

IN NO EVENT WILL HIGHLAND TECHNOLOGY, INC. BE LIABLE FOR DAMAGES, INCLUDING LOST PROFITS, LOST SAVINGS OR OTHER INCIDENTAL OR CONSEQUENTIAL DAMAGES ARISING OUT OF THE USE OF OR INABILITY TO USE SUCH PRODUCT, EVEN IF HIGHLAND TECHNOLOGY, INC. OR AN APPROVED RESELLER HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, OR FOR ANY CLAIM BY ANY OTHER PARTY.

Table of Contents

1 Introduction

The T660 is a small, enclosed digital delay/pulse generator which is intended for use in embedded OEM applications. Given an internal or external trigger, it outputs four precisely timed pulses. It is a drop-in, backward compatible replacement for the T560 and T564 digital delay and pulse generators.

Standard features include:

- Four TTL-level delay outputs, individually programmable for delay and pulse width
- 10 picosecond delay and width resolution, 10 second range
- 22 nanosecond insertion delay, 16 MHz max trigger rate
- <35 picoseconds typical jitter
- Highly accurate DSP phase lock system provides crystal-clock delay accuracy with zero indeterminacy from asynchronous external trigger
- Internal 10 MHz crystal oscillator time base with external lock capability
- 0-16 MHz DDS synthesizer for internal trigger rates
- Programmable-level trigger input with divide and burst features and trigger enable GATE input
- Needs +12-volt power from external universal power supply; can be operated all the way to +24 volts
- RS-232 serial interface standard; 10/100 mbps Ethernet interface
- Extruded enclosure with removable mounting flange
- Output impedance switch allowing for 50 Ω source termination or low impedance
- Trains/Frames advanced option (T660-2) includes timing lists and multiple pulses per trigger
- Web page controls from any browser

2 Specifications

FUNCTION	Four channel digital delay/pulse generator
CHANNELS	A B C D
OUTPUT VOLTAGE	+5V Zout selectable 50 Ω (+2.5V into 50 Ω loads) low z (+5V into 50 Ω loads) Rise/Fall < 750 ps typ
DELAY RANGE	0 to 10 seconds
WIDTH RANGE	0 to 10 seconds
INSERTION DELAY	Normal Mode: Trigger to any output 55 ns ± 400 ps Fast Mode: Trigger to any output 21 ns ± 400 ps
REP RATE	0 to 16 MHz, limited to 1/ (max d + w + 70 ns)
ACCURACY	Trigger to rising or falling edges ± 400 ps ± 7.5 ps/°C ± clock accuracy
RESOLUTION	Edge times, 1 ps Trigger level, 10 mV
JITTER	Typical 35 ps RMS + timebase jitter Max 50 ps RMS + timebase jitter Add clock jitter for delays > 500 µs
TRIGGER	External, internal, software (remote command) Burst, divide-by-N, N-of-M pulse picking External trigger range ± 5 volts rising/falling edge impedance selectable 2K + 15 pF or 50 Ω minimum recommended amplitude 0.25 volts p-p 125 MHz maximum repetition rate input Internal DDS, 0 to 16 MHz, 0.02 Hz resolution Internal clock: 80 MHz source, use Trigger Divisor for Max 16 MHz rep rate

VCXO TIMEBASE	Initial accuracy: ±1 PPM Aging: < ±5 ppm/1000 hours Jitter: 10ns/s RMS max Lockable to external 10MHz ± 10 PPM
CLOCK INPUT	10 MHz, sine or square 0.5 to 5 volts p-p 1kΩ nominal input impedance
CLOCK OUTPUT	10 MHz, square wave, 3 volts p-p AC coupled 50 Ω nominal output impedance
COUNTDOWN	Provides trigger divide-by-N or N-of-M burst/pulse picker mode, up to 125 MHz external trigger
POWER	External +12 ±0.25 volts DC from universal adapter supplied 0.5 amps max +24 ±0.25 Volts absolute max voltage input; no guarantee of accuracy performance Includes standard IEC60320 C13 line cord
COMMUNICATIONS	RS-232 standard, 38.4 Kilobaud (configurable up to 115.2 Kilobaud) 10/100 Ethernet standard (configurable with serial commands)
PACKAGING	4.84” (L) x 4.06” (W) x 1.20” (H) blue extruded aluminum enclosure
TEMPERATURE	Specifications apply over 10-40 °C ambient Operating range 0 to 50 °C Storage range -20 to 80 °C
CONFORMANCE	RoHS
WARRANTY	One year limited
CALIBRATION INTERVAL	One year
OPTIONS	Frame and train engine

3 Overview

The T660 is an embedded digital delay/pulse generator. It accepts a trigger pulse and generates up to four output pulses, with each pulse being individually programmable in delay and width. Triggers may be external, internal, or evoked through the communications interface. Timing has crystal-clock precision with picosecond jitter relative to an external trigger.

Each output is user programmable for delay (0-10 seconds) and width (0-10 seconds) with 1 ps resolution.

3.1 Basic Timing

A T660 timing event begins with a trigger, which can originate from an external source, the internal rate generator, or a single-shot remote command. Once triggered, the T660 goes busy until all four channels have generated the requested pulses, with each pulse having a user-defined delay and width. All channel timings are measured relative to the start of the rising edge of the Trigger source + the insertion delay. This sequence, from trigger to the firing of all enabled channels, is referred to as a *shot*.

When all enabled channels are done, Triggers are inhibited during the end-of-delay EOD recovery time.

The trigger path includes divide-by-K and N-of-M burst/pulse pick logic.

The T660 requires sometime between the arrival of the trigger and the time that the first output edge goes high; this is the *insertion delay* of the T660.

The insertion delay of the T660 is 22 ns. The T660 makes a best faith effort to freeze the new timings prior to their use. However, it can accidentally catch timings that are not correct if times are very near to 0 and were changed just prior to the arrival of the trigger (roughly 18 ns for the sum of those two factors). If times are changed during a shot the T660 will execute an FEOD command, truncating the shot in progress before it has finished.

3.2 Overall Block Diagram

When a trigger is accepted, a coherent timing set is committed, and a precision instant-start oscillator is initiated. This oscillator is used by the FPGA to count out coarse channel delays. Analog vernier circuits fine-tune the rising and falling edges of all channel output pulses to 1 ps resolution. All timings are agile and accurate on a per-shot basis.

The triggered oscillator is phase-locked to the internal temperature-compensated crystal oscillator, which may be optionally locked to an external reference. The digital phase-lock system maintains the triggered oscillator phase relative to the asynchronous trigger but enforces the long-term quality of the crystal clock.

The internal trigger generator is a precision DDS with very low jitter and is as accurate as the internal crystal oscillator.

The four output stages are programmable for pulse polarity. They generate clean, fast 50-ohm-source pulses from 0 to 5volts p-p.

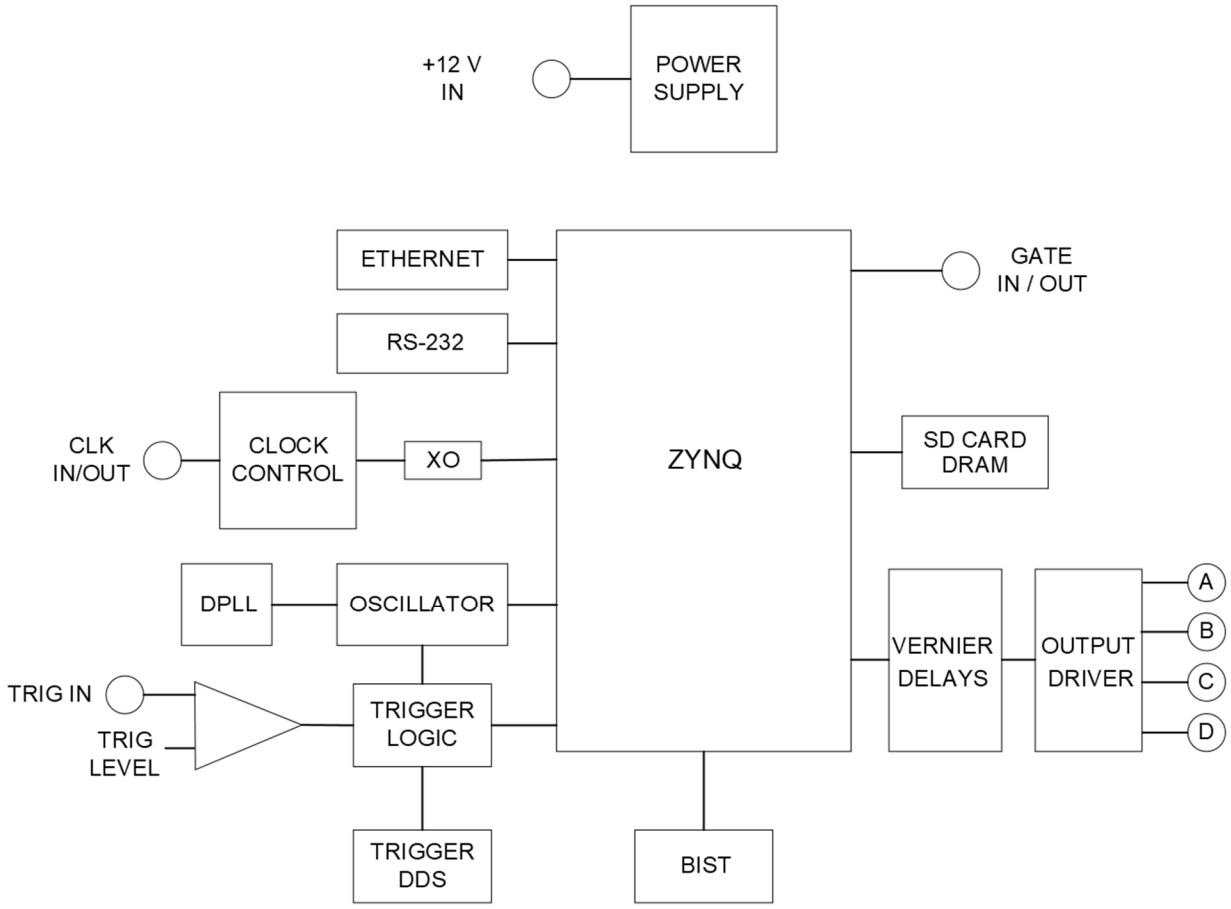


Figure 3-1: T660 Basic Block Diagram

The optional frames/trains engine (FTE) stores a list of timings that can apply to any channels on a per-trigger basis and can schedule multiple pulses on any channel per trigger. This facility can also be used to generate timing sweeps and programmable jitter. The FTE sequence can be conditional on external GATE inputs. See section **Error! Reference source not found.** - **Error! Reference source not found.**.

3.3 Crystal Oscillator Timebase

The standard T660 includes a 10 MHz VCXO crystal oscillator timebase. It is factory-set to an accuracy of ±1 PPM and may be expected to drift less than 2 PPM per year.

A connector is provided which allows the internal oscillator to provide a 10-MHz output or allows an external 10-MHz source to be accepted. This allows multiple T660s to be synchronized to each other or to an external 10-MHz reference. The external clock levels are 3.3-volt square-wave CMOS logic levels. The T660 can lock to an externally applied square wave of 10 MHz +-50 PPM, 3.3-to-5-volt positive logic levels, or to a 1-volt RMS sine wave.

The long-delay (millisecond range) jitter performance of the T660 is dominated by the phase noise of the internal crystal oscillator or the equivalent phase noise of a user-provided external reference.

3.4 Trigger Inputs

Figure 3.2 is a simplified diagram of the T660 trigger and sequence logic. Any one of five available trigger sources may be selected to fire the system: External+, External-, an internal 80-MHz clock, the internal 0-16 MHz DDS synthesizer, and the user software trigger. The selected trigger is divided by a programmable factor K from 1 to 2^32-1 and supplied to the cycle-start HIT flipflop. The hit flip-flop is enabled by the gating/burst logic. Once the flipflop is fired, eight identical timing blocks generate delays A1 through D2, each programmable from 0 to 20 seconds in 10-ps steps. Pairs of delays are combined to result in four outputs, each a pulse whose delay and width are programmable with respect to the common trigger. When all delay blocks have timed out, the EOD (end-of-delay) logic resets the hit flipflop for about 50 ns, after which the system is enabled to accept another trigger.

The standard external trigger is a positive level, with trigger threshold programmable from +0.25 to +3.3 volts and selectable rising/falling edge. The trigger input may be programmed to be high impedance or a 50-ohm termination to ground. Maximum safe input levels are -0.3 to +5.0 volts.

The maximum allowed trigger rate is:

$$R = 1 / (D + W + 70\ ns)$$

where D + W is the greatest channel sum of programmed delay plus width, and R is limited to 16 MHz max. If a channel is programmed OFF, its time settings are not relevant. If the T660 receives an internal or external trigger while a timing cycle is still busy, that trigger will be ignored. Some additional timing restrictions apply in QUEUE, TRAIN, and FRAME modes.

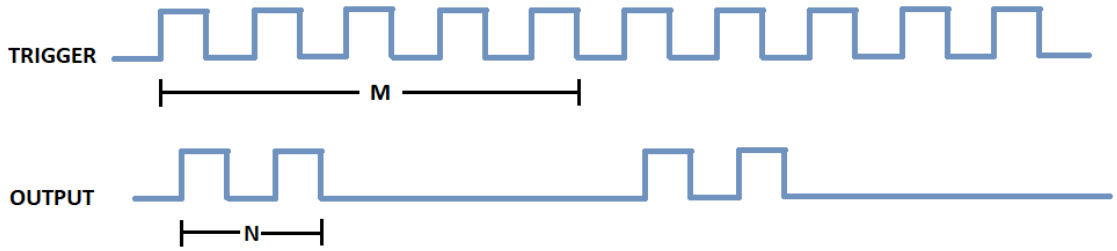
An internal 80 MHz clock (exactly 8x the main 10 MHz clock) may also be selected as the trigger source. When it is used, a trigger divisor K must be programmed to keep the trigger rate at or below 16 MHz.

The internal DDS synthesizer allows internal triggering at rates from 0 to 16 MHz with 0.02-Hz resolution. The DDS synthesizer has a period jitter of about 1 part in 20,000, which can be substantial in absolute terms at lower requested frequencies. Both period jitter and resolution can be improved by keeping the DDS frequency in the 2-10 MHz range and using the internal trigger divisor facility to get lower trigger rates.

External triggers up to 125 MHz can be accepted, given that a programmed divisor or the inherent busy-cycle limitation will restrict the actual trigger rate to some countdown fraction of the input frequency below 16 MHz.

3.5 Burst Logic

The burst logic allows the user to define two integers N and M, each in the range of 1 to 2^32-1. When Burst mode is enabled, lets the unit when triggered to Fire N number of triggers out of M number of them. Which means that if N=2 and M=5, the T660 will have two active pulses for every 5 triggers, as shown in the following image:



Whenever N or M equal 0, burst logic is disabled and allows for continuous triggering, meaning that every trigger can fire an output pulse. If N=M, every trigger shot will be fired. M must always be greater or equal to N, if this is not the case the unit will start to operate in continuous triggering mode. Burst mode functions for all trigger sources.

Burst cycles may "free run", continuously generating N of every M possible cycle. The internal burst logic may be reset by a user command, so that the next trigger will start a new burst of N outputs.

A single burst of N cycles may be started under control of the GATE input or on software command. If GATE mode is set to BURST, the next active edge of the GATE input will enable a single burst of N cycles. Similarly, the **`GAte REmote`** mode enables a user-fired burst, started by the **`GAte FIre`** serial command. In all BURST cases, M must be set greater than or equal to N.

3.6 Pulse Outputs

Four pulse outputs are provided, called channels A, B, C, and D. Outputs are +5-volt CMOS levels with a settable 50-ohm or Lo-Z source impedance. If the outputs are set to be 50-ohm source impedance, they can drive 5 volts into a non-terminating load, or 2.5 volts into a 50-ohm load. In case the Lo-Z source impedance is chosen, the outputs can drive 5 volts into a non-terminating load and into a 50-Ohm load. Because their outputs can be source terminated, they may drive a 50-ohm coaxial cable any distance into any termination impedance without significant reflection problems. For example, a 100-ohm termination will provide a clean 0-to-+3.3-volt logic swing, and a high-impedance (such as CMOS) load will swing 5 volts. External passive components can be used to convert to ECL or PECL levels.

Each output is programmable for pulse delay and width relative to the trigger. If an output is programmed for delay D, the actual output pulse will occur at D + 22 ns after the external trigger, where 22 ns is the basic insertion delay of the T660. Pulse outputs are normally active-high but may be programmed to operate active-low.

3.7 Gate I/O

A GATE coaxial connector is provided; it is pulled up to +5 volts through a 1K resistor or may, under software control, be terminated at 50 ohms to ground. GATE may be programmed as an input or as an output. As an input, it may be programmed to enable triggers, with high or low being the active level. As an output, it will go true (selectable high or low) to indicate that the HIT flipflop is armed and ready to accept triggers. The gate logic may also be used to enable a single burst of N pulses, with the burst being evoked by a rising edge at the GATE connector input or by remote command.

3.8 Communications and Control

All versions of the T660 are equipped with a 38.4-kbaud RS-232 interface and 10/100 Ethernet interface. Ethernet and RS-232 communications could be functional at the same time, but commands should not be sent to the T660 through both ports simultaneously.

3.9 Connectors

Standard logic-level connectors are right-angle SMBs.

A three-foot SMB-to-BNC cable is available as Highland part number J53-1 and two of them are included with every purchase.

A miniature 2.5-mm stereo phone jack is used for the RS-232 serial interface; a mating connector and cable is available, terminated with a female D9 connector, and may be plugged into the serial port of a standard PC. The RS-232 cable assembly is Highland part number T565-1, and one is included with every purchase.

Pinout of the serial connector is:

Tip	RXD	serial data to T660	to PC D9-3
Ring	TXD	serial data from T660	to PC D9-2
Ground			to PC D9-5

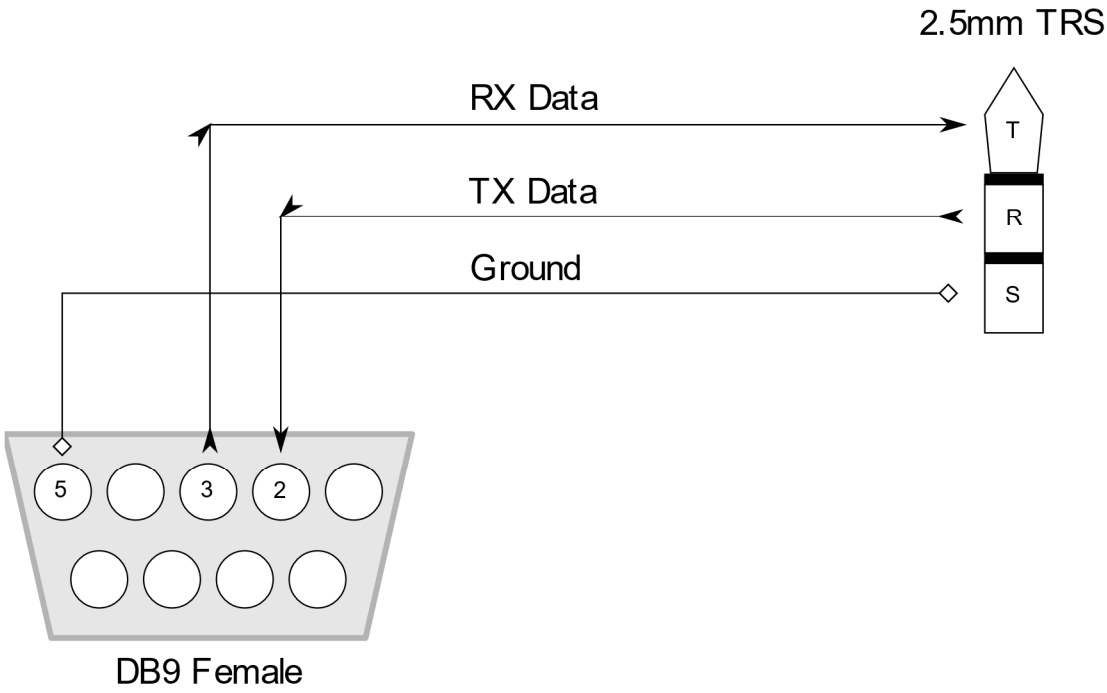


Figure 3-2: 2.5-mm Stereo Audio Jack to D9 cable connections

3.10 Power Input

The T660 requires +12 volts DC at 0.5 amps max. A wall-plug universal power supply is furnished with the evaluation kit, or users may supply +11.75 to +12.25 VDC power. A Highland J12 +12 Volts wall-wart power supply and an international AC plug adapter kit is provided with every purchase.

The standard power connector is a 2.1 x 5 mm coaxial power type, center positive.

The T660 power input is protected by a self-resetting polyfuse and a transzorb zener diode and will withstand all the way to +24 volts.

3.11 Indicators

Two RGB LED indicators are provided with the T660.

When the PWR LED lights green indicates that power is available. It also blinks at a 1-Hz rate to indicate CPU heartbeat. Its color changes to RED if any internal error conditions are sensed. The PWR LED will flash yellow when any communication is received or a T660 formats a reply.

3.12 Train and Frame Features

An advanced version of the T660 know as a dash 2(T660-2), provides TRAIN and FRAME capability.

The TRAIN feature allows a single trigger to invoke a sequence of as many as 2^32 sets of programmed delays. See section 8.

The FRAME feature allows users to pre-load a list of up to 8192 delay and width settings and enable the unit to rapidly reload these settings between shots, without real-time per-shot serial commands. See section 9.

TRAIN and FRAME may be used separately or together.

4 Programming

4.1 General Comments

The T660 accepts ASCII serial commands from the standard RS-232 interface or from the 10/100 Ethernet adapter.

For evaluation, serial commands may be typed using any common serial communications program, for example TeraTerm or Putty. A family of **`HElp`** commands is available, summarizing serial commands and operating modes. The **`STatus`** command will send back a summary of T660 settings.

In the following sections, text using this font...

`TLevel <cr>`

represents a command string sent to the T660, terminated with a carriage return character <cr>, and italic text...

`1.25 <cr> <lf>`

represents the reply from the T660. All commands must be terminated with semicolon or <cr>, and all reply lines are terminated by <cr> <lf>.

4.2 RS-232

The RS-232 port uses the following protocol:

Baud	38400 Kilobaud, configurable up to 115200 Kilobaud
Data Bits	8
Stop Bits	1
Parity	None

4.3 Ethernet

The Ethernet connector is a standard RJ45 10/100 connection.

By default, the T660 uses a DHCP client to request an IP address from the network's DHCP server. This may be changed to a static IP address using serial commands. The T660 uses a host name of the form "T660-xxxxx", where xxxxx is the serial number of the unit padded with zeroes on the left to five digits, for example "T660-00012" for serial number twelve.

4.4 TCP Interface

Port 2000 is used for the ASCII serial commands described in the serial command reference. This is a raw TCP socket. Users can use a telnet or raw-TCP client to send serial commands or queries.

4.5 ASCII Command Reference

Users send serial ASCII command strings to the T660, to which the T660 immediately replies. Because the standard baud rate is high, and because the T660 may spend a millisecond or more to process commands, user software must wait for a response to each command line before sending another command.

Each command consists of a command keyword, followed by an optional alpha or numeric argument. Multiple commands may be sent in a single line, separated by semicolons. When a full line is received, indicated by the final <cr> character, the buffered line is executed, in the order received.

Keywords may be fully spelled out or may be sent as their first two letters; only the first two letters are significant. In this documentation, a word that has two possible forms is written with the short form capitalized, and the rest of the word in lower-case letters. The actual T660 protocol is case insensitive.

> For example, **`TRigger`** indicates that the short form is **`TR`**, and the long form is **`TRIGGER`**, both of which are recognized commands.

All forms are case insensitive. One or more spaces are required to separate keywords from arguments.

A delay or width is sent as

```
ADelay 23.5u
CWidth 40n
```

Acceptable suffixes are:

p	-	pico	(1E-12)
n	-	nano	(1E-9)
u	-	micro	(1E-6)
m	-	milli	(1E-3)
s	-	seconds	

and exponential notation is not supported. Default is nanoseconds.

Trigger levels are sent in volts, as **`TLevel 1.50`**

Most value-setting commands may be sent without an argument, in which case they become queries of the associated value.

`ADelay` (no argument)

evokes the reply

`02.123456789123`

which represents the delay setting for the rising edge of the A output in seconds.

Since such long strings of numbers are difficult to read, a "verbose" mode is available, which will send times and other long numbers in the form

`02.123,456,789,123`

Certain incoming ASCII characters are treated specially:

- All lowercase letters are converted to uppercase
- TAB is treated as a space
- ETX, ESC, and DEL are equivalent to BS, command line abort.
- Colon is translated to semicolon, the command separator
- Most other characters, including + - , * ? and linefeed, are ignored.
- A "blank" input line, <cr> only, evokes the response ***`T660 <cr> <lf>`***

4.6 Command Structure

A command line begins with a command keyword (or its 2-letter abbreviation), followed by optional arguments. Multiple commands on a line may be separated by semicolons.

One or more spaces are required between a keyword and its argument. Whitespace may not break up a command token or an argument but is otherwise allowed.

Query commands are requests for specific data. A query is often a "set"- type command without an argument.

Time-set commands are expressed as channel delays and widths, with the four pulse outputs identified as A, B, C, or D, corresponding to the four output pulse connectors.

All commands must be terminated by either an end of line indicator (carriage return, ASCII 13, denoted <cr>) or the separator (***;***) for multiple commands on a line. Linefeeds are ignored.

Since the T660 receive buffer is limited to 256 bytes, users should not program multiple commands per line that might exceed this length. If at any time the <backspace> character (ASCII code 8) is received, the T660 will flush its receive buffer and ignore any previous input.

Each received command will evoke a reply indicating the execution status of the command. For query commands, the reply is the requested data. For other commands, successful completion will yield a reply of ***OK***. If multiple commands are issued on one line, multiple responses will be sent back on a single line, separated by semicolons. For the command line...

```
1.25; TLEVEL; TRIG POS
```

the reply will be of the form

```
OK;1.25;OK
```

All reply strings are terminated with carriage return/linefeed <cr> <lf> characters.

If an error occurs while processing a command, the reply ***??*** will be returned. If multiple commands are present on a command line, and any command produces an error, the erroneous command will respond with the ***??*** indicator and no remaining commands will be processed.

Numerical replies to queries will be in fixed-point decimal numeric form, with embedded commas included if Verbose mode is set.

4.7 Realtime Issues

User command lines are stored in a buffer until the <cr> character is received, at which time the entire command line is parsed and executed in the order received. Each command sends its reply characters, typically a requested value or the ***OK*** response, as the command is executed. Any additional incoming characters following the command-line <cr> are ignored until the entire command line is processed and the final response-line <cr> <lf> is returned.

Most simple commands execute in hundreds of microseconds, and their realtime execution rate is dominated by the 38.4 kbaud (3840 characters/second) serial communications rate. Shortform commands reduce communications overhead. Long reports are of course baud rate limited, with the **STatus** report or the longer **HElp** pages taking as long as 500 milliseconds.

When delay/width settings are changed via the **INstall** command (or an end-of-line autoinstall) or the trigger, burst, or gate parameters are changed, the firmware will immediately force the end-of-delay reset state, which will abort any timing cycles currently in progress. EOD will be asserted for about 350 microseconds, after which triggers will be re-enabled.

If aborting timing cycles is undesirable, one can disable triggers, wait until any possible timing cycle has finished, then do the desired operation. For example, if it were known that all delay+width settings total under 40 milliseconds, one could send the T660 the sequence...

```
TRIGGER OFF; WAIT 50000; CDELAY 2.5m; INSTALL; TRIGGER POS
```

to which it would reply

```
OK;OK;OK;OK;OK
```

with an additional 50 millisecond pause before the second ***OK***.

One can also use the realtime USEC counter to measure actual command execution times in microseconds...

```
US 0; SY 3.579545M; US
```

which might respond

```
OK;OK;0,000,001,128
```

Again, command execution times are usually dominated by the 38.4 kbaud communications rate.

The T660-2 also features a **QUEUE** install mode, which allows delays to be reprogrammed without disrupting ongoing triggers; see section 4.9.2.

4.8 T660 Command Summary

The following is a summary of commands which may be sent to the T660.

Long Form	*Short Form*	*Function*
ADELAY 45u	**AD 45u**	set A delay
AWIDTH 25.5n	**AW 25.5n**	set A width
ADELAY	**AD**	delay A query
AWIDTH	**AW**	width A query
ASET ON	**AS ON**	enable A output
ASET OFF	**AS OF**	disable A output
ASET POS	**AS PO**	set A polarity positive (normal)
ASET NEG	**AS NE**	set A polarity negative (inverted)
ASET	**AS**	query channel A settings
APENDING	**AP**	query channel A pending settings

BDELAY 45u	**BD 45u**	set B delay
BWIDTH 25.5n	**BW 25.5n**	set B width
BDELAY	**BD**	delay B query
BWIDTH	**BW**	width B query
BSET ON	**BS ON**	enable B output
BSET OFF	**BS OF**	disable B output
BSET POS	**BS PO**	set B polarity positive (normal)
BSET NEG	**BS NE**	set B polarity negative (inverted)
BSET	**BS**	query channel B settings
BPENDING	**BP**	query channel B pending settings
CDELAY 45u	**CD 45u**	set C delay
CWIDTH 25.5n	**CW 25.5n**	set C width
CDELAY	**CD**	delay C query
CWIDTH	**CW**	width C query
CSET ON	**CS ON**	enable C output
CSET OFF	**CS OF**	disable C output
CSET POS	**CS PO**	set C polarity positive (normal)
CSET NEG	**CS NE**	set C polarity negative (inverted)
CSET	**CS**	query channel C settings
CPENDING	**CP**	query channel C pending settings
DDELAY 45u	**DD 45u**	set D delay

DWIDTH 25.5n	**DW 25.5n**	set D width
DDELAY	**DD**	delay D query
DWIDTH	**DW**	width D query
DSET ON	**DS ON**	enable D output
DSET OFF	**DS OF**	disable D output
DSET POS	**DS PO**	set D polarity positive (normal)
DSET NEG	**DS NE**	set D polarity negative (inverted)
DSET	**DS**	query channel D settings
DPENDING	**DP**	query channel D pending settings
QDELAY 45u	**QDELAY 45u**	set all four (“quad”) delays
QD 45u	**QD 45u**	set all four (“quad”) widths
INSTALL	**IN**	apply pending channel settings immediately
INSTALL 24	**IN 24**	apply Frame settings immediately
QUEUE	**QU**	synchronous install at next EOD
QUEUE 24	**QU 24**	synchronous install Frame at next EOD
AUTOINSTALL 1	**AU 1**	apply pending settings at end of line
AUTOINSTALL 2	**AU 2**	queue pending settings at end of line
AUTOINSTALL 0	**AU 0**	cancel automatic mode
UNDO	**UN**	cancel all pending channel settings
TLEVEL 1.25	**TL 1.25**	set external trigger level
TLEVEL	**TL**	query trigger level

TRIGGER POS	**TR PO**	trigger on external rising edge
TRIGGER NEG	**TR NE**	trigger on external falling edge
TRIGGER INT	**TR IN**	select internal 80 MHz trigger
TRIGGER SYN	**TR SY**	select internal DDS synthesizer
TRIGGER REMOTE	**TR RE**	select remote trigger
TRIGGER OFF	**TR OF**	disable triggers
TRIGGER HIZ	**TR HI**	trigger input is 10K to ground
TRIGGER TERMINATE	**TR TE**	trigger input is terminated at 50 ohms
TDIV 5000	**TD 5000**	set trigger divisor
TDIV	**TD**	query trigger divisor
TRIGGER	**TR**	trigger setup query
TFREQ INPUT	**TF IN**	set TFREQ to count trigger input signal
TFREQ HITS	**TF HI**	set TFREQ to count actual triggers
TFREQ	**TF**	return trigger frequency, Hz
TPER	**TP**	return trigger period, in ns
FIRE	**FI**	fire remote trigger
FEOD	**FE**	force End Of Delay, abort timing cycle
SYNTHESIZE 3.579M	**SY 3.579M**	set optional DDS synthesizer rate
SYNTHESIZE	**SY**	query DDS synthesizer rate
CLOCK HIZ	**CL HI**	clock connector is unused

CLOCK OUT	**CL OU**	connector outputs 10 MHz
CLOCK IN	**CL IN**	external 10 MHz is accepted
CLOCK	**CL**	query clock settings and temperature
CTRIM 2048	**CT 2048**	set 10 MHz clock trim, 0...4095
CTRIM	**CT**	query clock trim value
CLOCK SAVE	**CL SA**	save clock trim to flash memory
BNUM 555	**BN 555**	set burst N, pulses output in burst
BMOD 2000	**BM 2000**	set burst M, total triggers/cycle
BURST ON	**BU ON**	enable burst mode
BURST OFF	**BU OF**	disable burst
BURST RESET	**BU RE**	reset burst counters
GATE OFF	**GA OF**	disable gate functions
GATE OUTPUT	**GA OU**	make gate connector an output
GATE INPUT	**GA IN**	make gate an input
GATE POS	**GA PO**	gate in/out is active high (normal)
GATE NEG	**GA NE**	gate in/out is active low (inverted)
GATE TERMINATE	**GA TE**	gate input is terminated at 50 ohms
GATE HIZ	**GA HI**	gate input is 1K to +5 volts
GATE BURST	**GA BU**	enable single burst at gate input rise
GATE REMOTE	**GA RE**	enable single burst on command
GATE FIRE	**GA FI**	fire a single remote burst

TCOUNT OFF	**TC OFF**	cancel pulse Train mode
TCOUNT 2000	**TC 2000**	add N pulses per trigger
TSPACE 88U	**TS 88U**	set train pulse spacing
FRAME OFF	**FR OF**	cancel frame mode
FRAME 12	**FR 12**	store current settings into frame nnn
FA 4	**FA 4**	set start frame
FB 24	**FB 24**	set end frame
FC 999	**FC 999**	set frame repeat count
FN	**FN**	report frame load count. FN 0 clears
FP	**FP**	report realtime frame pointer
FRAME GO	**FR GO**	start frame operation
FRAME LAST	**FR LA**	report last available frame index
FRAME	**FR**	report frame system status
FDUMP 8190	**FD 8190**	display frame N contents, internal format
FX	**FX**	display frame diagnostic report
RTEST	**RT**	test frame memory
RZAP	**RZ**	clear frame memory
STATUS	**ST**	show T660 status report
SAVE	**SA**	save current setup
RECALL	**RE**	recall saved setup
LOAD DEFAULT	**LO DE**	load default setup
RUN DEMO	**RU DE**	run demonstration setup

RSET	**RS**	reset the T660
SHOTS	**SH**	query shot counter
SHOTS 0	**SH 0**	reset shot counter
USEC	**US**	query microsecond counter
USEC 0	**US 0**	reset microsecond counter
IRQ	**IR**	query 40 Hz interrupt counter
WAIT 3400	**WA 3400**	wait specified number of microseconds
IDENTIFY	**ID**	return ID string
ERRORS	**ER**	return error status
ERRORS 0	**ER 0**	clear error flags
VERBOSE 1	**VE 1**	show long numbers with commas
VERBOSE 0	**VE 0**	show long numbers without commas
VERBOSE	**VE**	query verbose setting
COMMENT	**CO**	command is ignored
HELP	**HE**	return general HELP message
HELP CHANNELS	**HE CH**	return help on channel operations
HELP TRIGGER	**HE TR**	return Trigger help
HELP CLOCK	**HE CL**	return Clock help
HELP BURST	**HE BU**	return Burst help
HELP GATE	**HE GA**	return Gate help

HELP PULSETRAIN	**HE PU**	return Train help
HELP FRAMES	**HE FR**	return Frames help
HELP MISC	**HE MI**	return miscellaneous help

4.9 Command Details

4.9.1 CHANNEL SET COMMANDS

The channel commands allow channel delays, widths, and modes to be set or queried.

Set a delay or width with the appropriate command, such as

ADelay 65.81n

DWidth 55.2u

where times may be specified with suffix characters s,m,u,n, or p for seconds, milliseconds, microseconds, nanoseconds, and picoseconds. The default is nanoseconds.

Interrogate a time setting with

ADelay which evokes the reply, in seconds,

00.000000065810 in terse mode, or
00.000,000,065,810 in verbose mode.

All channel settings are stored in a "pending" buffer until applied to the timing hardware. Two modes are available: INSTALL and QUEUE. See section 4.9.2.

The **UNdo** command cancels any pending channel settings.

ASet ON enables channel A output

ASet OFf	disables channel A output. Its electrical output will stay low (or high, if channel is inverted) and its time settings are ignored
ASet POs	sets channel A polarity positive (normal)
ASet NEg	sets A polarity negative (inverted)
ASet	query channel A settings. A string will be returned ***Ch A POS ON Dly 00.123456789012 Wid 01.234567890123***
APending	query channel A pending settings. This produces a response identical to **ASet**, except that the pending values are presented

The **QDelay** and **QWidth** "quad" commands set all four delays or widths to the same value.

Note that the channel polarity and on/off settings must be installed before taking effect, just as the channel delays and widths.

4.9.2 INSTALL AND QUEUE COMMANDS

After one or more channel delay and width setting commands are transmitted, the new settings must be loaded into the delay generator hardware. This is inherently tricky, as delays may be in progress when the timing settings are changed.

When delay/width settings are changed via the **INstall** command (or an end-of-line autoinstall) or the trigger, burst, or gate parameters are changed, the firmware will immediately force the end-of-delay reset state, which will abort any timing cycles currently in progress. The EOD system reset will be asserted for about 300 microseconds, after which triggers will be re-enabled.

Use **INSTALL** when it is necessary to ensure that the very next trigger will use the latest-commanded timings.

The T660 also features a queued install mode, which allows delays to be reprogrammed without disrupting ongoing triggers. A **QUEUE** command will load the current time settings into the hardware at the next EOD, namely at the **end** of the next timing cycle. No cycles are lost or aborted.

QUEUE allows timings to be changed during ongoing triggers, without truncating timing cycles. The **QUEUE** operation requires a minimum delay from EOD until the next trigger

of 10 microseconds, to allow vernier delay circuits to settle. Less delay may result in timing errors of as much as 20 ns.

The **AUtoinstall n** command enables either install or queue operations to be performed at the end of parsing the current command line.

AUtoinstall 1	enables "install" operation at end of line
AUtoinstall 2	enables "queue" operation at end of line
AUtoinstall 0	cancels automatic installs

A typical command line might be

```
ADelay 45n; AWidth 130u; INstall
```

or

```
CDelay 33u; DWidth 500u; QUeue
```

where the final verbs are not needed if the appropriate autoinstall mode is enabled.

Both **INstall** and **QUeue** can accept an optional numeric argument to load frame data; see section 8.

4.9.3 TRIGGER SETUP COMMANDS

The **TRigger** family of commands select the T660 trigger source and associated parameters.

TLevel 2.50	Sets external trigger level; legal range is 0.25 to 3.30
TLevel	Queries trigger level. The response would be ***2.50***
TRigger POs	Trigger on external input, rising edge.
TRigger NEg	Trigger on external input, falling edge.

TRigger INt	Selects an internal 80 MHz trigger, 8x the internal 10 MHz clock. A divisor K of at least 5 is required to limit the trigger rate to the 16 MHz limit.
TRigger SYn	Selects optional internal DDS synthesizer as the trigger source. Its frequency may be set from 0.018 Hz to 16 MHz using the SYN command.
TRigger REmote	Enables software triggers, via the FIRE command.
Fire	Fires one remote trigger.
TRigger OFf	Disables triggers
TDivisor 80000	Sets a trigger divisor integer K, from 1 to 2^{32}-1. When the divisor is loaded, the next trigger will fire the T660 (subject to other restraints) and then K-1 triggers will be skipped before another is enabled. **TD 0** disables the divide function. Divide can be combined with BURST. CAUTION: a large trigger divisor can create the appearance of a triggering failure.
TRigger HIz	Trigger input is 10K to ground.
TRigger TErminate	Enables 50 ohms terminator on TRIGGER input.
TRigger	Trigger setup query, evokes a response of...

Trig REM 50R Level 1.250 Div 0000000000 SYN 00010000.00

The frequency of the electrical trigger source, or the actual DDG hit frequency, may be measured. The hit frequency can be lower than the incoming trigger rate if a divisor is programmed, gating is in use, or long delays result in missed triggers. After switching the measurement selection, wait at least two seconds for counts to settle. The frequency measurement timebase is one second.

TFreq INput	selects the trigger input for measurement
TFreq HIt	selects the actual DDG hit rate for measurement
TFreq	returns the current trigger or hit frequency, in Hz
TPer	returns the corresponding period, in ns

4.9.4 SYNTHESIZE COMMAND

The T660 is furnished with a direct-digital frequency synthesizer that may be used to generate internal triggers from 0 to 16 MHz with 0.018 Hz resolution. This is not functional on the T660-10.

SYn 123.456K	sets the frequency. Suffix characters may be K (kilohertz) or M (megahertz). The default is Hertz.
SYn	queries the current frequency

4.9.5 BURST COMMANDS

The **BURst** commands control the trigger burst logic. Burst allows a group of N pulses to be fired out of each group of M input triggers; that is, N successive triggers will be accepted, then M-N triggers will be skipped.

It is also possible to generate a burst of N triggers, invoked by the rising edge of the GATE input, or by remote command. See 4.9.6 - GATE COMMANDSGATE COMMANDS

BNum 555	sets burst N, pulses output in burst
BNum	queries burst N value
BMod 2000	sets burst M, total triggers/cycle
BMod	queries burst M value
BUrst ON	enables burst mode
BUrst OFf	disables burst
BUrst REset	reset burst counters; next trigger will be the first of N.
BUrst	queries burst settings. This will return a string...

Burst OFF N 0000000555 of M 0000002000

4.9.6 GATE COMMANDS

The GATE coaxial connector may be used as an input or an output. As an input, it can enable or disable triggers under the control of an external TTL level. As an output, it can indicate when the internal hit flipflop is enabled to accept triggers.

If the gate is configured as an input, a true level allows triggers and a false level disables them. If BURST is also enabled, then whenever the input level is in the trigger disable state, the burst counter logic is reset; the next time gate goes true, the burst logic will immediately enable a group of N triggers.

If gate is set to be an output, it will go active (high or low, as programmed) whenever the hit flipflop is armed to accept triggers. So in burst mode, it will go true during the active "N" pulses of the burst sequence. If a trigger divisor is programmed, it will go high only when the divisor enables triggers.

GAte OFf	disable gate functions
GAte OUtput	make gate connector an output. The output level will be true when the hit flipflop is enabled to accept triggers
GAte INput	make gate an input. When the external TTL level is true, triggers will be enabled.
GAte POs	gate in/out is active high (normal)
GAte NEg	gate in/out is active low (inverted)
GAte TErminate	gate input is terminated at 50 ohms
GAte HIz	gate input is 1K to +5 volts
GAte BUrst	enable single burst at gate input rise
GAte REmote	enable single burst on **GATE FIRE** command
GAte FIre	fire a single burst
GAte	gate setup query. Returns...

Gate OFF POS HIZ Shots 0000000066

4.9.7 CLOCK COMMANDS

T660 timings are based on an internal 10 MHz crystal oscillator clock. The function or the CLOCK coaxial connector is controlled by this group of commands. If the connector is declared to be an input, the T660 accepts a 10 MHz TTL square wave input, or a sine wave of about 1 volt RMS, and will lock its crystal oscillator to this source. If the connector is set to be an output, the local 10-MHz oscillator frequency will be output from this connector.

The value used to trim the internal oscillator frequency is an integer in the range 0 to 4095, with 2048 being roughly the nominal center frequency. Since the internal crystal

oscillator might be expected to drift 1-2 ppm per year, users may wish to occasionally trim its frequency if precise delays are required.

Clock-group serial commands are...

CLock HIz	clock connector is unused
CLock Out	connector outputs internal 10 MHz oscillator
CLock IN	external 10 MHz is accepted; oscillator phaselocks
CTrim 2048	sets 10 MHz clock trim, 0...4095, about 0.1 ppm/lsb
CTrim	queries clock trim value
CLock Save	save clock trim to flash memory. This value will be restored at powerup
CLock	query clock settings; returns...

Clock OUT *Trim* 02048 Temp +32.4

The ***Temp*** item is circuit board temperature in degrees C. It is typically about 10 degrees above ambient.

4.9.8 FEOD COMMAND

The **FEod** (force end-of-delay) command briefly resets the timing hardware, aborting any timing cycle in progress. This is useful for terminating long delays.

4.9.9 SAVE, RECALL, LOAD COMMANDS

The **SAve** command will save the overall T660 setup into nonvolatile memory. This setup will be restored at powerup or may be installed via the **REcall** command.

SAve	save current setup to nonvolatile memory
REcall	recall saved setup.
	Train and frame parameters are saved and recalled, but frame memory is not saved.
LOad DEfault	load default setup; see Figure 4-1 Typical T564 Status Report

RUn Demo	run demonstration setup. This is the default setup, except that the T660 self-triggers at 20 KHz

4.9.10 USEC, WAIT, IRQ, SHOTS, TEMP COMMANDS

The **USec** command returns the value of a free-running 32-bit counter that increments once each microsecond. **USec 0** resets the counter.

The **WAit nnn** command pauses command execution for a specified number of microseconds, up to 2^{32}-1, or about 4294 seconds.

The **IRq** command returns the value of the internal 40 Hz interrupt counter.

The **SHots** query returns the 32-bit shot counter. This counter increments every time the T660 is fired. **SHots 0** will clear the shot counter.

The following command line will return the approximate trigger rate in Hz:

```
SHOTS 0; WAIT 1000000; SHOTS
```

4.9.11 IDENTIFY COMMAND

The **IDentify** command returns a string which identifies the T660 firmware version. The returned form is ***T660-1 Firmware 28E560-A***

4.9.12 ERRORS COMMAND

The **ERrors** command returns a string which identifies any T660 errors. The returned form is...

```
Errs None
```

Or

```
Errs 00127  XTRIM RECAL CALIB LOGIC XLOCK TUNE DPLL
```

where the integer value represents the error flags word. Bits are...

Bit	*Value*	*Flag*	*Meaning*
0	1	***XTRIM***	VCXO trim value lost
1	2	***RECAL***	saved setup recall failed
2	4	***CALIB***	calibration table lost; default cals are used
3	8	***LOGIC***	internal logic error
4	16	***XLOCK***	VCXO failed to lock to external source
5	32	***TUNE***	powerup DPLL calibration error
6	64	***DPLL***	DPLL stability error

If any error bits are set, the string will also explicate the error bits in text. The "power" LED will turn yellow if any error bits are up.

The **`ERrors 0`** command will clear the error flags word.

4.9.13 VERBOSE COMMAND

The **`VErbose 1`** command places the T660 in verbose mode, where commas are included in all long numeric strings that are returned. This mode makes time settings and 32-bit integers easier to read but may not be compatible with external software.

The **`VErbose 0`** command will cancel verbose mode.

`VErbose` alone will query this setting.

4.9.14 HELP COMMANDS

The **`HElp`** command, with no arguments, will display a short command summary, listing top-level commands. Specific commands will be explained with requests of the form **`HElp TRigger`** and such.

`HElp`	return general HELP message
`HElp CHannels`	return help on channel operations
`HElp TRigger`	return Trigger help
`HElp CLock`	return Clock help

HElp BUrst	return Burst help
HElp GAte	return Gate help
HElp PUlsetrain	return Train help
HElp FRames	return Frames help
HElp MIsc	return miscellaneous help

4.9.15 STATUS COMMAND

The **STatus** query returns a full report of T660 settings. A typical report is shown below. Verbose mode was enabled. The status shown is the default setup.

```
     Highland Technology  Model T660  Digital Delay Generator

Firmware 28E560-A  1034                Cal date January 31, 2014

Trig   REM  50R  Level 1.250   Div   0,000,000,000  SYN 00,010,000.00
Hit Freq Hz 0,000,000,000      Period ns 0,000,000,000

Gate   OFF  POS  HIZ           Shots 0,000,000,066
Burst  OFF  N  0,000,000,016   of M  0,000,000,064

Verbos ON   Autoinstall FEOD   Usec 0,306,931,240  DPLL 00000
Clock  OUT  Trim 02048         Temp +35.6

Errs   None

Train count 0,000,000,000      Train spacing 0,000,000,003

Frames  OFF     FA 00000   FB 00009   FC 00000   FN 0,000,000,000

Ch A  POS  ON     Dly  00.000,000,000,000  Wid  00.000,002,000,000
Ch B  POS  ON     Dly  00.000,002,000,000  Wid  00.000,002,000,000
Ch C  POS  ON     Dly  00.000,004,000,000  Wid  00.000,002,000,000
Ch D  POS  ON     Dly  00.000,006,000,000  Wid  00.000,002,000,000
```

Figure 4-1 Typical T564 Status Report

Since the report is subject to change of both format and contents, it is recommended that it not be parsed to extract T660 parameters.

4.9.16 RSET COMMAND

The **RSet** command performs a hardware reset/restart of the T660, equivalent to a power off/on cycle. The reset takes about 4 seconds, after which the T660 will respond with the string ***Highland Technology T660 DDG <cr> <lf>***

The last-saved setup will be installed.

4.9.17 PTRAIN, PSPACE, FRAME, AIM, GET COMMANDS

See sections 7-Pulse Trains and 8-Frames.

5 Powerup States and Saved Setups

Users may program the T660 as desired and then use the **SAve** command to copy all setups to nonvolatile flash memory. That saved setup may be recalled at any time via the **REcall** command. The saved setup is also recalled and installed at powerup, allowing the T660 to resume operation without any serial commands.

The powerup sequence takes about 4 seconds. During this time, channel outputs are electrically low and terminations are high-Z.

If the saved configuration programs channels to be inverted polarity, those outputs will transition from low to high when the initial powerup sequence is over.

6 Jitter Notes

Jitter is defined as the 1-sigma standard deviation of delay. It is the shot-to-shot time uncertainty from the external trigger to any output's rising or falling edge, or the uncertainty between edges of channel outputs. Jitter is measured in RMS picoseconds. Visual peak-to-peak jitter is roughly 5 times that of RMS.

"Jitter" is usually accepted to indicate time variance as observed over an interval of 0.1 seconds, with the term "wander" used to describe slower changes of delay. Wander thus encompasses changes in delay driven by temperature changes and other slow effects. The T660 jitter specs are valid for observation periods up to 10 seconds in the absence of radical temperature changes. Note that coaxial cable propagation delay can change considerably with temperature and can contribute to observed timing variance.

Uncorrelated jitters add trigonometrically, as the square root of the sum of the squares of all jitter contributors.

Jitter can be difficult to measure. The trigger input to the T660 must be clean and fast (< 2 ns risetime) and the measuring instrument must have a jitter noise floor well below that of the T660. Most oscilloscopes and counters are not capable of resolving T660 jitter performance, especially so for longer delays. For example, a Tektronix 11801C sampling oscilloscope (or the newer DSA8200 without the optional phaselock module) has a short-delay jitter well below that of the T660 but has added jitter on the order of 20 microseconds per second of delay, whereas the T660 starts with a greater basic jitter but typically adds about 4 ns of jitter per second of delay.

For lowest jitter from an external trigger, the T660 trigger level should be set to the steepest part of the input edge, typically 1/3 to 1/2 of the peak amplitude.

Jitter is a function of the generated time delays. Very short delays have a baseline jitter that depends on fundamental triggered-oscillator phase noise. After about 500 ns, the DSP stabilization loop becomes active and disciplines the triggered oscillator, limiting its jitter accumulation.

Long delays, in the milliseconds range, become dominated by the phase noise of the internal crystal oscillator, typically about 4 ns per second of delay. Long-delay effects are zero relative to a user-provided 10 MHz reference clock.

Jitter between successive triggers, referred to as "period jitter", depends on the quality of the trigger source. The internal DDS trigger synthesizer has jitter typically about one part in 20,000 of the trigger period. DDS jitter is best if its frequency is in the 2-10 MHz range, where the period jitter, measured at a channel output, is typically about 25 ps RMS. For lowest DDS jitter at lower rates, keep the DDS synthesizer frequency in this range and use a trigger divisor to get lower trigger rates.

7 Pulse Trains

The T660 may be programmed to produce pulse trains, namely, to make a sequence of delay cycles starting with a single trigger. See Figure 7-1 for pulse train waveforms.

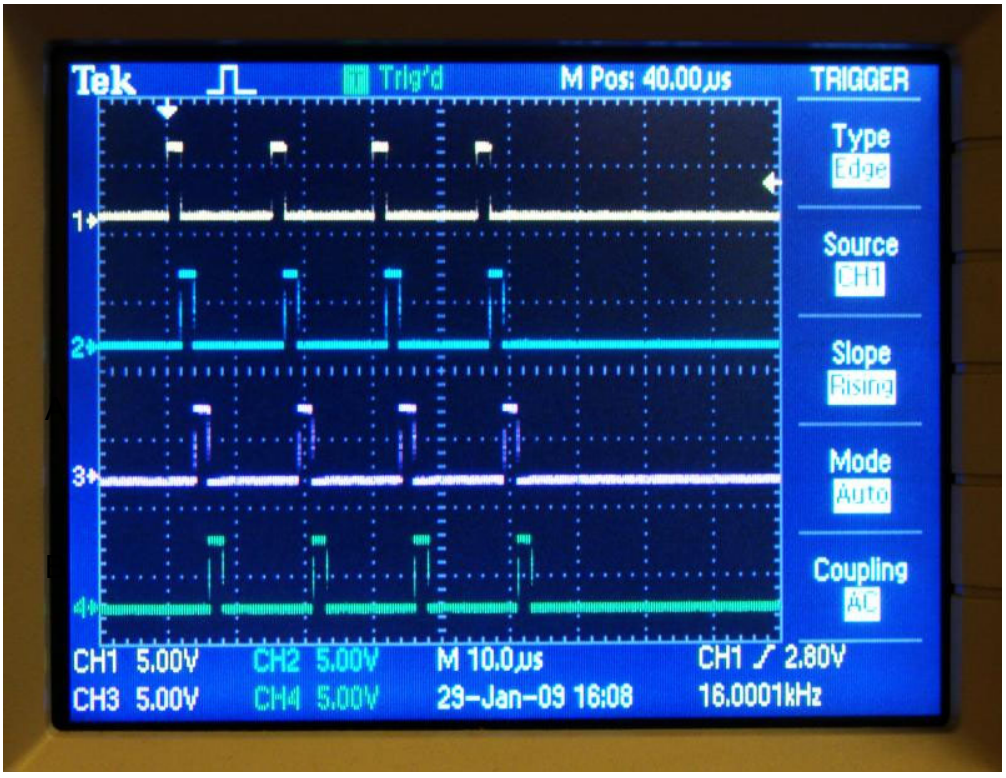


Figure 7-1: T660 Channels with Pulse Train Outputs

The first set of A/B/C/D outputs are the usual ones, as programmed by the standard channel delay and width commands. After these are finished, additional sets are generated, spaced from the original set by time T2. This particular sequence was invoked by the **TCount 3** command. Note that the numeric argument to the **TCount nnn** command is the number of additional pulses added to the normal pulse output.

The pulse spacing T2 is set by the **TS ddd** command, **TS 750** for a 15 us group spacing in this example. The time is expressed in units of 20 ns. Up to 2^32-1 pulses can be generated by the train facility, with spacing T2 from 80 ns to 10 seconds. T2 must be set to time W+80 ns minimum, where W is the time from the first edge (here, the rise of A) to the last edge (here, the fall of D.)

The T2 intervals are quantized to 20 ns and are exact to the accuracy of the internal crystal oscillator timebase.

After all pulses are over, the standard EOD (end-of-delay) system reset occurs.

The associated serial commands are...

TCOUNT OFF **TC OFF** cancel Train mode

TCOUNT 2000 **TC 2000** make a train of 2001 pulses per trigger

TSPACE 88 **TS 88**
set train T2 spacing to 1760 ns

TCount OFF resets the train subsystem. This immediately clears the pending, actual, and hardware Tcount values. **TCount 0** disables train operation but operates like a normal timing parameter, requiring an **INSTALL** or **QUEUE** command to become effective.

The train parameters must be installed before becoming active, using the **INSTALL** or **QUEUE** commands, or their autoinstall equivalents. Train parameters are saved in Frames.

If any channel is programmed for a delay below 20 ns in Train mode, only the first, single pulse will appear. This is defined as a feature, as it allows a single "train start"

output pulse to be generated. In the example below, the channel A delay is set to zero, so it makes only one initial pulse in Train mode.

8 Frames

The T660 allows a schedule of multiple delay setups to be stored in local volatile memory, with new settings loaded rapidly after each trigger/delay sequence.

Delay setups are compiled and stored in "frames". Each frame includes channel delays, widths, channel enable bits, channel polarities, and TRAIN parameters. Users may program a group of settings and store that setup to a numbered frame.

At runtime, initializing the frame system will allow a number of DDG shots to be fired, using parameters extracted from sequential frames. The T660 can store up to 8192 frames.

The frame controller logic has three states:

OFF	frame system is disabled. DDG operates normally.
RUN	frames are being loaded at each end-of-delay, namely at the end of each timing cycle.
DONE	last frame has been loaded and run, and triggers are inhibited.

The associated serial commands are:

FRAME OFF	disable frame mode
FRAME nnn	save current settings to frame nnn, in range 0 to 8191.
FA nnn	set first frame to execute. **FA** with no argument is a query.
FB nnn	set last frame to execute. FB must be greater than FA

FC nnn	set frame loop count, 0 to 65534. Value 65536 sets infinite loop.
FRAME GO	enter RUN state and start frame execution, from first to last.
FRAME LAST	report maximum available frame index, usually 8191
FN	report number of frames loaded into hardware. **FN 0** clears count
FP	report realtime frame pointer
FRAME	report frame system state
INSTALL nnn	unpack frame nnn and load immediately into DDG hardware
QUEUE nnn	unpack frame nnn and queue into DDG hardware

The **FRAME GO** command loads the start (FA) frame into the hardware and queues the next sequential frame to be installed into the timing registers at the next EOD, namely at the end of the next shot sequence. Subsequent triggers use the timings extracted from sequential frames. After the last (FB) frame is used, triggers are disabled until another **FRAME GO** or **FRAME OFF** command is issued.

FRAME GO will produce the error response **??** if FB is not greater than FA.

The **FRAME** command, with no argument, returns ***OFF*** or ***DONE*** if frame execution is not active, or an integer from 0 to 8191 identifying the next frame to be executed if the sequence is active.

The **FRAME OFF** command returns the DDG to normal operating mode. The last-sent group of channel settings is re-installed, and triggers will be re-enabled if the trigger settings allow. One can issue the **TRIGGER OFF** command before the **FRAME OFF** command if this sequence might produce undesired outputs.

If the FC parameter is zero, a **FRAME GO** command will load frames FA through FB into the hardware then stop, responding to (FB-FA+1) triggers. If the FC loop parameter is in the range of 1 to 65534, that sequence will be repeated FC times, responding to (FB-FA+1) * (FC+1) triggers, about 536 million triggers in the extreme case. If FC is set to 65535 and **FRAME GO** is executed, the frame system will loop forever, executing frames FA through FB until terminated by **FRAME OFF.**

To speed up loading frames, it is recommended that Autoinstall be off (zero), and it is not necessary to issue an **INSTALL** command before saving a frame.

The FA, FB, and FC parameters may be queried at any time, but it is illegal to change them while frames are actively running. The command **FB 222** will invoke the ***??*** response if frames are running.

There are some realtime limitations to frame performance. Trigger rate may not exceed 15 KHz, and there must be a minimum delay between EOD and the next trigger of 10 microseconds, where EOD is the time of the trailing edge of the last active channel. Violating these limits may cause triggers to be missed.

Another note is that calibration and delay temperature compensation math is performed at the instant a frame is compiled and saved, so later playback of frames may result in more than normal temperature drift, as much as 20 ps per degree C. So it is best to load "fresh" frames for maximum accuracy.

If frames have been loaded but frame operation is inactive, one can issue the **INSTALL nnn** or **QUEUE nnn** commands to load the setup of frame nnn into the DDG timing hardware. This allows the frame buffer to be used to store up to 8192 saved timing setups, any of which can be recalled with a relatively short serial command. These commands are also useful for testing frame setups. Set Autoinstall mode to zero when using these commands; otherwise an end-of-line autoinstall will override any recalled frame settings.

After such an **INSTALL nnn** or **QUEUE nnn** command, queries of channel delay or width settings will reflect the last values sent by normal **DELAY** or **WIDTH** commands, and not the values just recalled from frame memory.

Since channel on/off and pos/neg polarity states are saved in frames, it is possible to have channels selectively fire on a frame-by-frame basis. One can also program a

channel to be off, but still flip its polarity on a per-frame basis, effectively creating a static TTL output that is controllable in each frame.

Some diagnostic commands are...

FDUMP 8190	**FD 8190**	display frame N contents, internal format
FX	**FX**	display frame diagnostic report
FM	**FM**	display frame trigger down-counter
RTEST	**RT**	test frame memory
RZAP	**RZ**	clear frame memory

The following is a simple example of frame operation. The following serial commands are sent to the T660:

```
LOAD DEFAULT
QDELAY 0
QWIDTH 100U; FRAME 1
QWIDTH 200U; FRAME 2
QWIDTH 300U; FRAME 3
QWIDTH 400U; FRAME 4
FA 1; FB 4
TDIV 80000
FRAME GO
TRIGGER INTERNAL
```

This will result in four triggers being fired at a 1 KHz rate, producing pulses of 100, 200, 300, and 400 microseconds on all four output connectors. The **LOAD DEFAULT** command cleared the frame loop counter FC, so frames 1 through 4 are scanned only once. The FN counter is incremented by five, the number of triggers plus one.

The resulting waveform is shown left, with the A and B outputs displayed.

Another **FRAME GO** command will repeat this sequence.

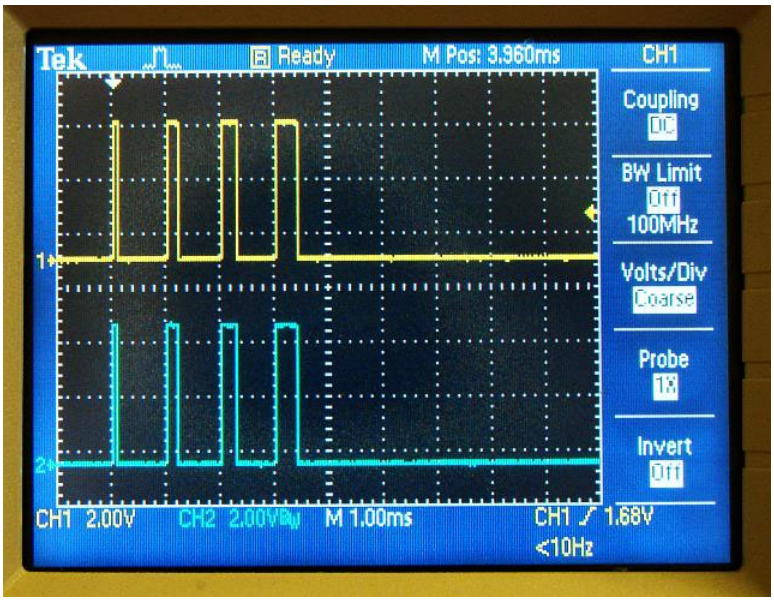


Figure 8-1: Frame output example

If we then issue the commands

```
FC 1
FRAME GO
```

the four programmed frames will be executed twice, accepting a total of 8 triggers. The FN count will increase by 9

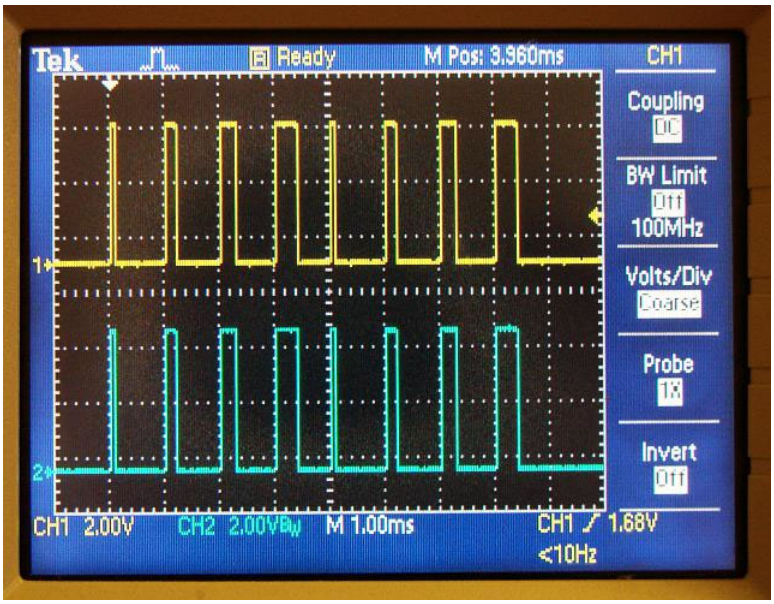


Figure 8-2: Repeating FRAME example

9 Dimensions and Mounting

T660 mechanical dimensions are shown below. The unit may be mounted with four 4-4-machine screws from below the box.

CAUTION: Mounting screws may not penetrate more than 0.160 inches (4 mm) into the T660 enclosure.

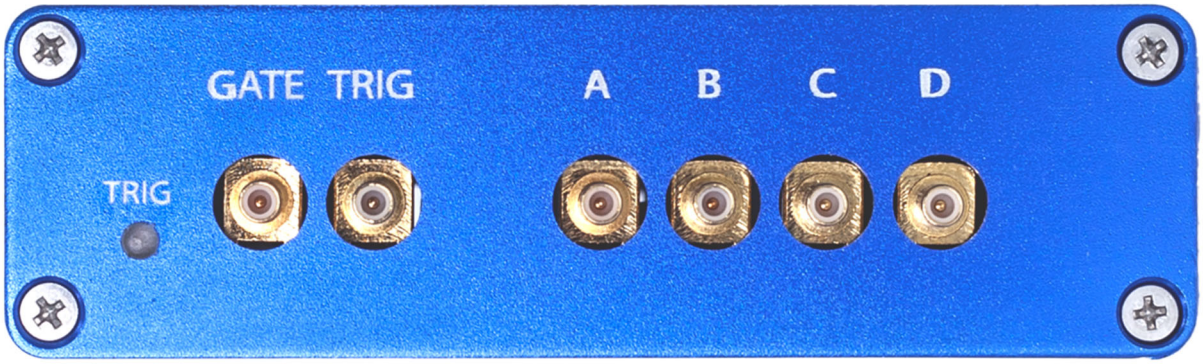


Figure 9-1: T660 Front Panel

Figure 9-2: T660 Rear Panel

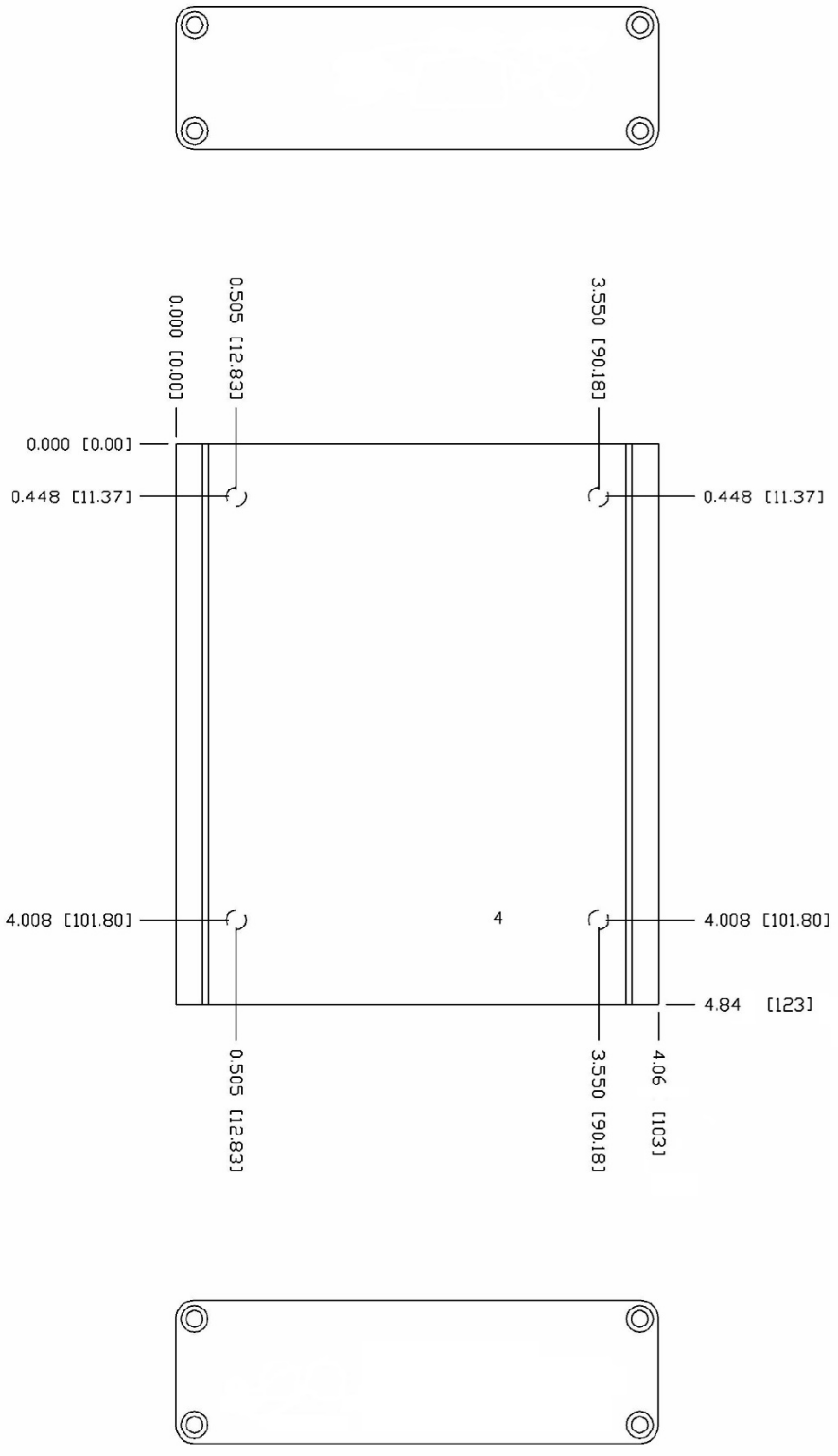


Figure 9-3: T660 enclosure and mounting locations

10 Versions

T660-1: 4-channel compact digital delay and pulse generator

T660-2: 4-channel compact digital delay and pulse generator with TRAINS and FRAMES capability

11 Revision History

11.1 Hardware Revision History

Revision D	Feb 2024
	Initial release

11.2 Software Revision History

12 Accessories

J12-1: 12 volt power supply (1 included with purchase)

J53-1: 3' SMB to BNC cable (2 included with purchase)

J53-2: 6" SMB to BNC cable

P10-1: 19" rack mount shelf (four t-boxes per rack)

T565-1: RS-232 cable (1 included with purchase)

T566-1: mounting flange