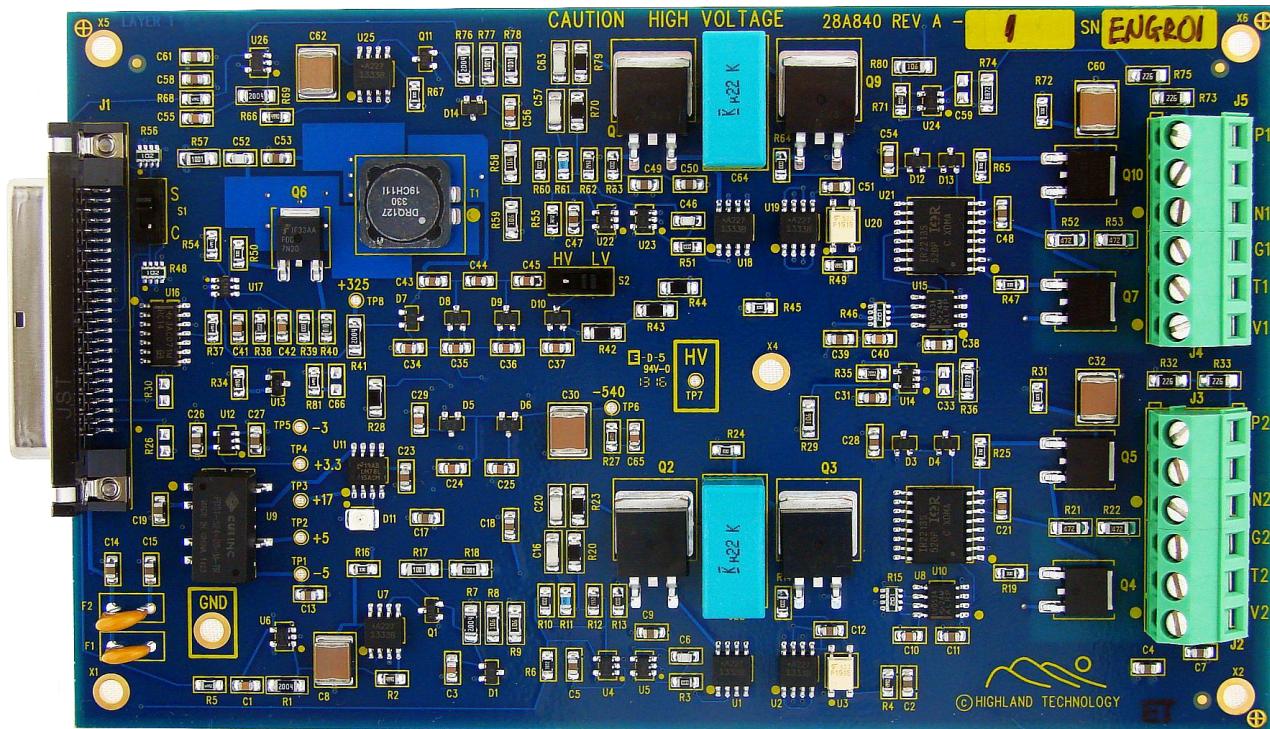




Model T840

2-Channel High Voltage Driver



Technical Manual

July 26, 2023

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1. Introduction

The Highland model T840 is a two-channel high-voltage pulser intended to drive PLZT electro-optical modulators, piezo elements, vacuum photo devices, and similar capacitive loads.

Features of the T840 include:

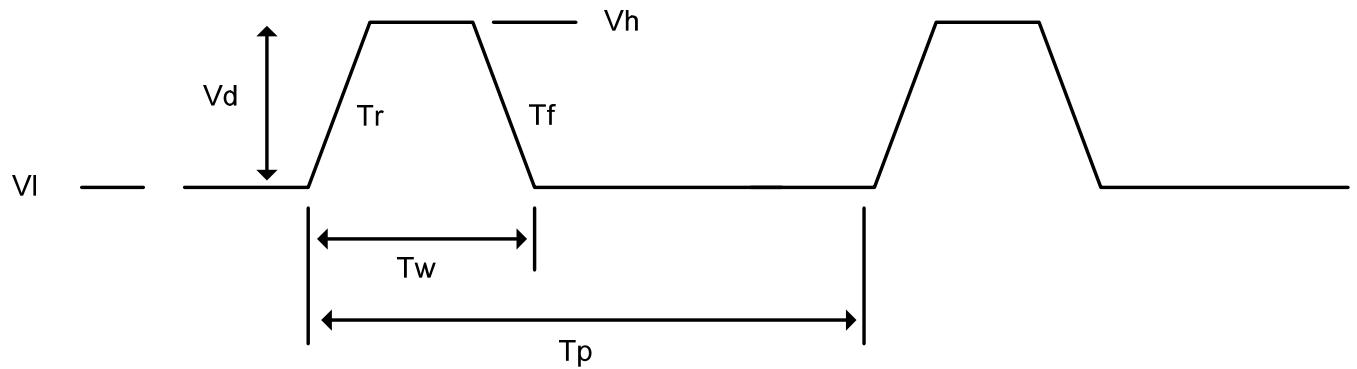
- Two independently controlled channels
- Generates 0 to +1200 volt fast pulses into PLZT elements, piezos, e/o modulators, or vacuum electronic devices
- Each channel is separately triggered and programmable for pulse voltage and DC bias
- TTL trigger
- OEM circuit board uses external 24-volt power; packaged versions optional
- 3.9" x 6.5" PCB for embedded application

See section 8, ELECTRICAL SAFETY.

2. Specifications: Model T840 Dual PLZT Driver

FUNCTION	Embedded 2-channel pulsed driver
VOLTAGE	VP Pulsed voltage, 0 to +1200 volts, applied to PLZT terminal 1 0 to 900 volts in LV mode
BASELINE	VN 0 to -400 volts bias applied to PLZT terminal 2 Optional bipolar bias
LOAD	Approximately 50 pF capacitive load per channel
RISETIME	Tr, Tf 10 µs max
PULSE WIDTH	Tw 50 µs min
PULSE PERIOD	Tp 100 µs min, 10 KHz max pulse rate
PULSE DUTY CYCLE	90% max
CONTROL	TTL trigger input sets Tw and Tp for both channels Switchable common/individual channel triggers Four 0-10 volt analog inputs set bias and pulse amplitudes
CONNECTORS	One D25 female connector 24 volts DC power in Two trigger inputs, TTL, optionally commoned Four output level programs, 0-10 volts in Two 500:1 attenuated signal monitors out Two temperature monitors out Grounds Two PLZT interfaces, 5 wires each, Phoenix terminal strips VP positive HV pulse out VN negative bias voltage out +24 for PLZT heater out Temperature monitor in Ground
PACKAGING	OEM embedded, printed-circuit board, approx. 6.5 x 3.9 x 1"
CONFORMANCE	Best-effort conformance to UL/IEC 60950 and FCC/CE requirements No formal testing or certifications at board level ROHS compliant

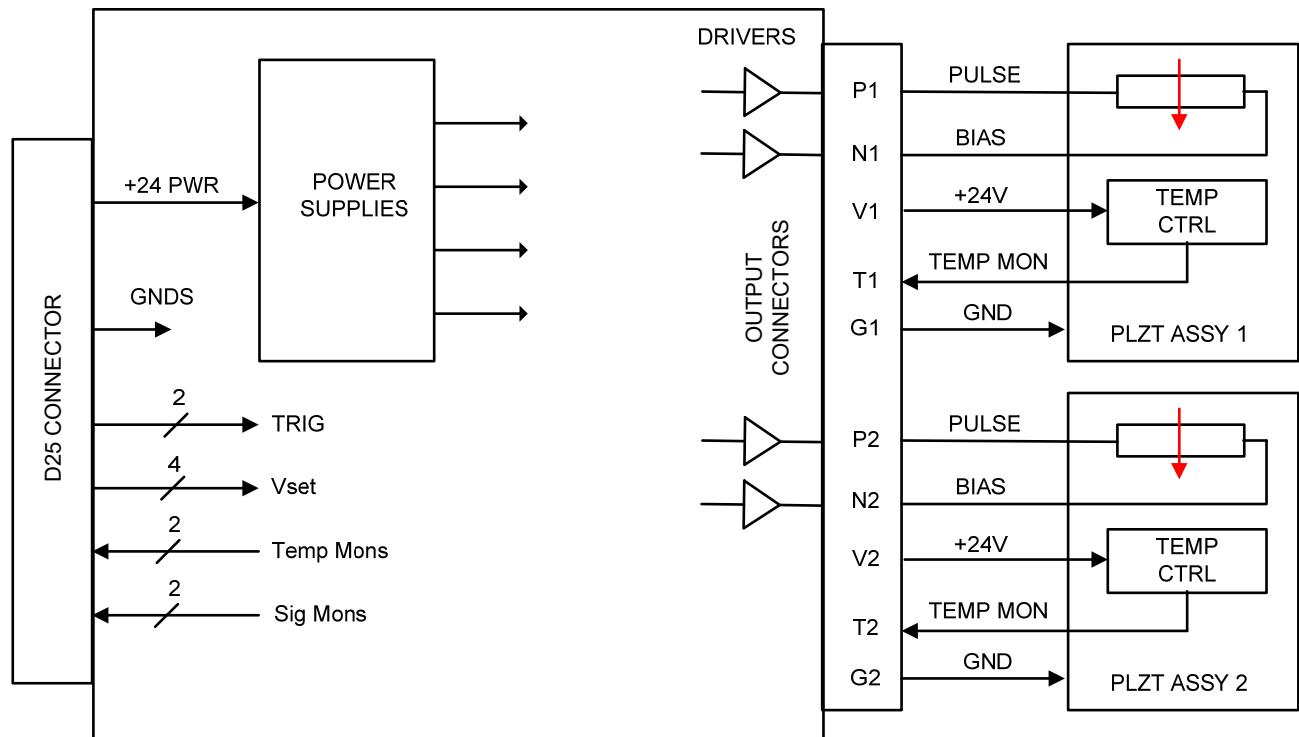
The following waveform is used for definition of output pulses at the P1 and P2 terminals. Channels have individually programmable voltage levels. TTL triggers are optionally common or separate.



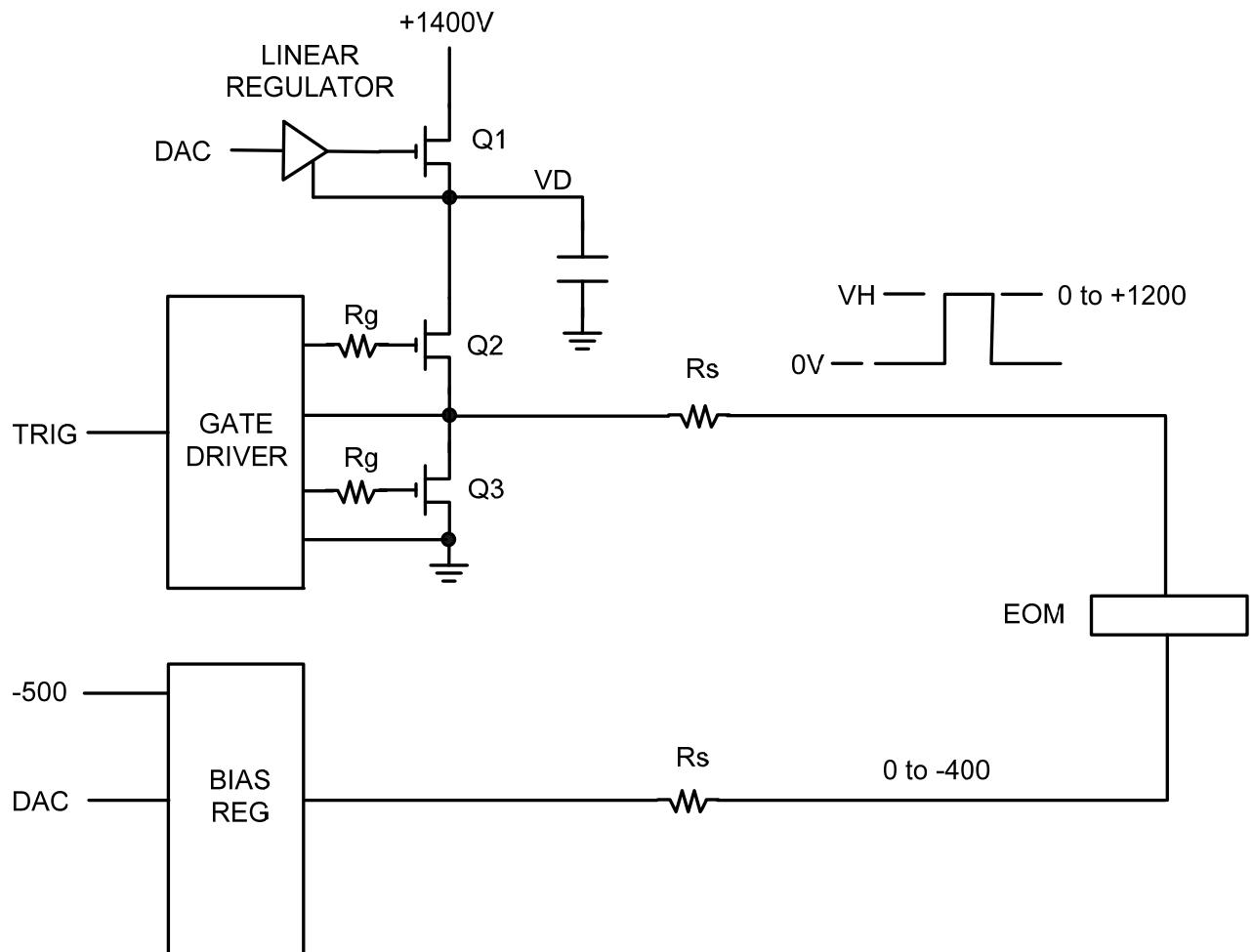
VL is zero. PLZT bias is via the separate negative DC bias supplies at the N1 and N2 terminals.

3. Architecture

- The overall block diagram is pictured below:



The individual channel drivers are pictured below:



The DACs and TRIG are user furnished signals.

The architecture is a half-bridge switchmode driver. The output voltage excursion **VD** is set by the linear regulator, which is programmed from 0 to +1200 volts, using a roughly 1400 volt common HV power supply. When the 0-10 volt **VD** DAC programming voltage changes, the high voltage regulator will track up or down with a slew rate of about 750 KV/s.

The bias supply applies 0 to -400 volts to the low side of the PLZT device.

The user will furnish all DAC signals as 0 to +10 volts analog.

The output resistors **Rs** (nominal 10K ohms) damp any ringing.

Total stored energy on the board is less than 1 joule.

The T840 may be damaged by a shorted load.

4. Power Considerations

The internal HV power supply is nominally 1350 volts and can source up to 4 mA. The pulse outputs are programmable up to +1200 volt peak pulse voltage.

The current required in the pulse generators is proportional to output voltage and to total load capacitance. For each channel,

$$I = C * V * F \quad (\text{units amps, volts, farads, Hz})$$

C above is the sum of internal capacitance (nominally 40 pF), PLZT capacitance (typically 47 pF) and wiring capacitance (estimated at 22 pF). So at 10 KHz pulse rate, each channel requires about 1.3 mA at 10 KHz, 1200 volts. If the two channels simultaneously average 900 volts out, the total current will be about 2 mA.

Each channel's voltage regulator is current-limited to 3 mA nom.

Higher pulse rates (say, 20 KHz) and larger capacitive loads (such as a thicker PLZT element) could exceed the 3 mA channel capability.

Wiring capacitance should be minimized by isolating the P1 and P2 pulse wires away from other conductors and minimizing wire diameter and lengths. P1 and P2 could each be run through plastic tubing to improve isolation. Do not use coaxial cables.

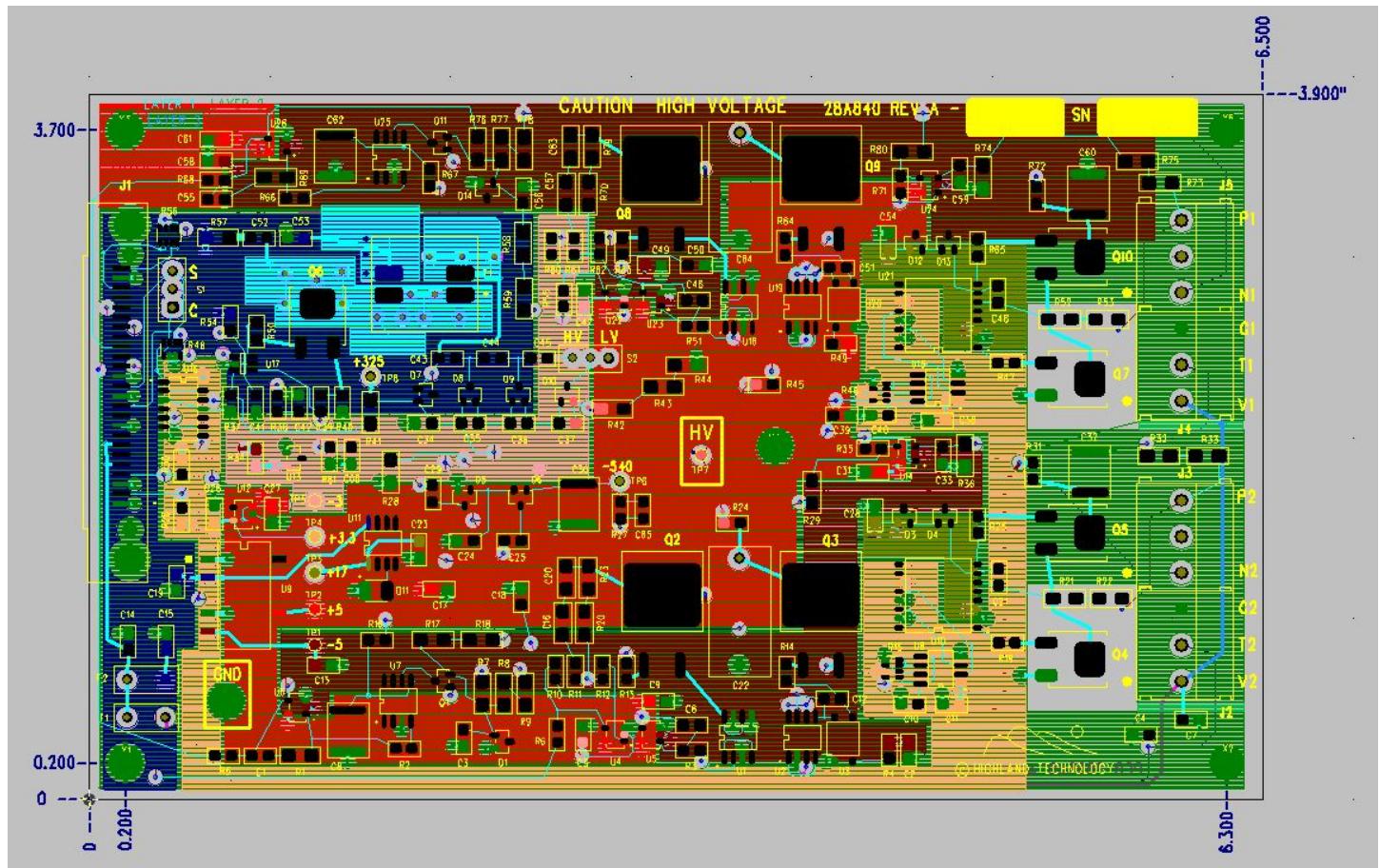
A slide switch in the HV supply may be set to the HV or LV position. HV is the normal setting, which allows 1200 volt output pulses. If the switch is set to LV, the power supply is more efficient and can furnish up to 6 mA, but output pulses are limited to 900 volts peak.

The power dissipation of the high-voltage power supply increases with pulser load current. Cooling is required for total total loads above 3 mA. Cooling can be by means of forced air flow across the PCB surface, or by conduction cooling to the metallic enclosure. Conduction cooling requires that a thermally conductive, electrically insulating gap-pad be used between the PCB and the enclosure; the recommended material is Bergquist GP2200SF-0.125-02-0816.

5. Packaging and Mounting

The 2-channel driver is supplied as an unpackaged printed-circuit board, to be mounted inside the user enclosure. Size is 3.90 by 6.50 inches. The board thickness is nominally 0.070", and the tallest component is 0.65" high. Packaged versions are optionally available.

It is suggested that the board be mounted 0.125" above a metal surface, using five aluminum spacers. The mounting holes are 0.125" diameter. This mounting allows for addition of the Bergquist conductive-cooling gap-pad if needed.



The fifth mounting hole is at coordinate X 3.800, Y 1.950.

6. Connectors

The system interface is a 25 pin female D-sub connector. The connector pinout is

PIN	NAME	NOTES
1	GND	
2	GND	
3	+24 in	
4	+24 in	
5	GND	
6	TRIG 1	trig1, trig2 optionally commoned
7	TRIG 2	
8	P1 PGM	P1 pulse amplitude, 0/+10 creates 0/+1200 pulse
9	N1 PGM	N1 bias, 0/+10 creates 0/-400 bias
10	P2 PGM	P2 pulse amplitude, 0/+10 creates 0/+1200 pulse
11	N2 PGM	N2 bias, 0/+10 creates 0/-400 bias
12	MON1	P1 monitor
13	MON2	P2 monitor
14	TEMP1	temperature monitor
15	TEMP2	temperature monitor
16		
17		
18		
19	GND	
20	GND	
21		
22		
23		
24		
25		
shell	GND	all GND pins are common to PCB mounting holes

A slide switch is located near the D25 interface connector. If it is set to "S" (separate), the two triggers are independent. If it is set to "C" (common), the TRIG1 input will drive both channels.

TEMP1 and TEMP2 are driven directly from temperature sensors in the load assemblies, namely from the T1 and T2 Phoenix connections. The T840 adds a 1 uF capacitor to ground on each TEMP signal to reduce noise coupled from the high-voltage pulses.

MON1 and MON2 are output monitors from the respective drivers, attenuated 500:1 from the high-voltage outputs. Output impedance is 500 ohms nominal. The reported signal includes the bias voltage, namely

$$\text{MON1} = (\text{VP1} - \text{VN1}) / 500$$

The monitor outputs are relatively slow, with a roughly 10 microsecond rise time.

Typical waveforms were acquired at

Pulse rate 2 KHz

Pulse width 120 us

Pulse amplitude 1000 volts

Bias 300 volts



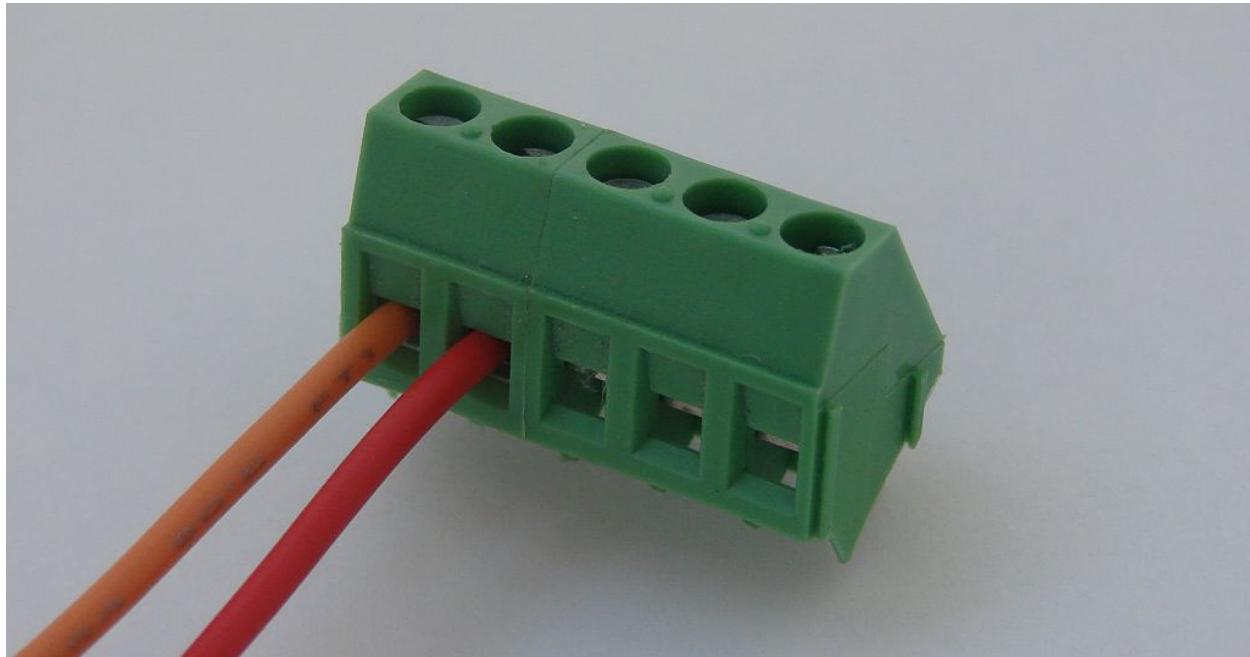
Yellow is the trigger input, 5 v/div

Blue is the P1 HV pulse, 500 v/div

Violet is the monitor 1 output, 1 v/div, which scales to 500v/div at P1. This peaks at equivalent 1300 volts, the sum of pulse amplitude plus bias.

Timebase is 20 us/div.

The connections to the two PLZT assemblies are via Phoenix wire-clamp barrier strips.



NAME	FUNCTION	NOTES	
P1	PLZT1 positive pulse	0 to +1200 volts pulse	PLZT HV1
N1	PLZT1 negative bias	0 to -400 volts DC	PLZT HV2
G1	GND		PLZT COM
T1	temperature monitor 1	from LM62	PLZT Tout
V1	+24 volts	for PLZT heater	PLZT +V
P2	PLZT2 positive pulse	0 to +1200 volts pulse	PLZT HV1
N2	PLZT2 negative bias	0 to -400 volts DC	PLZT HV2
G2	GND		PLZT COM
T2	temperature monitor 2	from LM62	PLZT Tout
V2	+24 volts	for PLZT heater	PLZT +V

Care should be taken to avoid

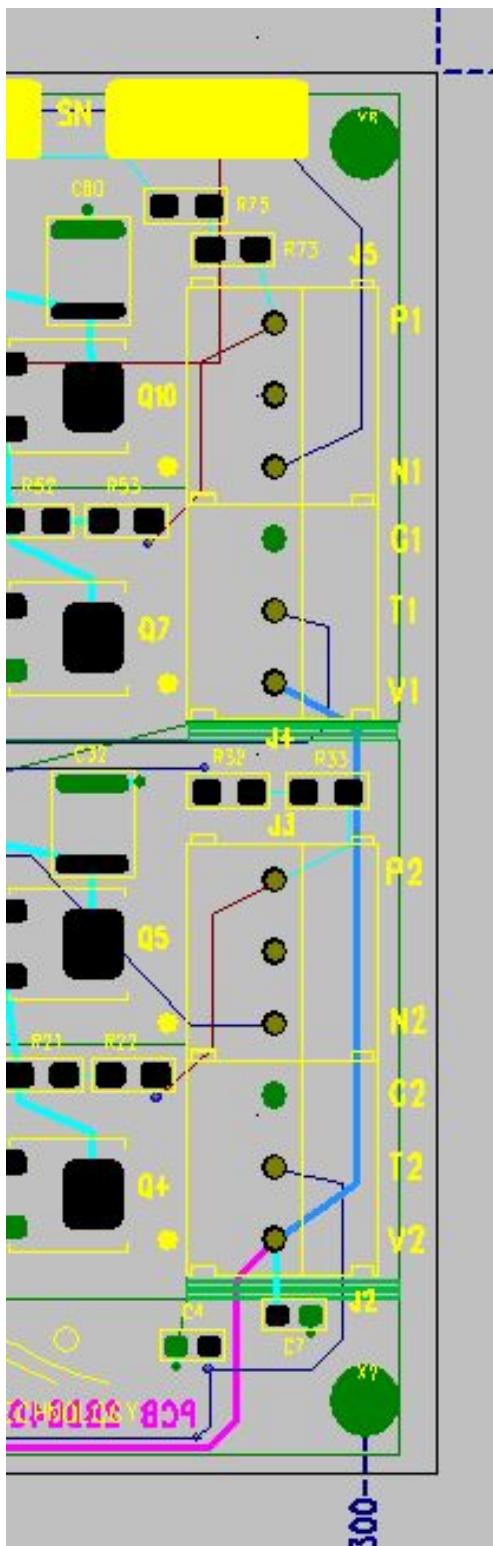
Electrical shock hazards

High voltage breakdown

Capacitive coupling from HV pulses into LM62 temperature sensors

Voltage drop in GND wires creating temperature measurement errors

The PCB arrangement of the PLZT connections:



7. Installation Summary

The basic installation steps for the T840 are:

1. Set switch S1 to position "S" if separate triggers will be used. Set to "C" to use TRIG1 as the common trigger.

Set switch S2 to "HV" if high voltage operation (1200 volt pulses) is required. Set it to "LV" for more efficient 900 volt pulsing.

2. Arrange to secure the module to a flat, grounded metal surface, using the five mounting holes provided. Mount with aluminum or stainless steel spacers and #4-40 or equivalent hardware. It is suggested that the spacers be 0.125 inches high, to allow optional insertion of gap-pad thermal transfer material between the board and the baseplate.

3. Verify that the PLZT devices are not shorted across either device or to ground. Shorts can damage the T840.

4. Connect the two PLZT load devices to the barrier strips.

5. Connect the D25 connector with connections as required. BE SURE 24 VOLT POWER IS OFF.

6. Mount the protective cover over the module.

7. Apply 24 volt power and note the orange POWER led. Start pulse operation and verify at the MON outputs.

8. ELECTRICAL SAFETY

VOLTAGES UP TO 1400 VOLTS MAY BE PRESENT IN MULTIPLE LOCATIONS ON THE T840 CIRCUIT BOARD.

The T840 board has multiple sources of high voltage located throughout the board surface, on both sides. As an embedded subassembly product, the T840 must not be accessible to end users or service personnel.

It is strongly recommended that the board be mounted with five metallic spacers to a grounded metal baseplate.

Each unit should be provided with a perforated plastic or metal cover that prevents contact with the surface of the board. This cover should display suitable safety warnings.

To avoid contact with high voltages, measure component temperatures with an infrared thermal imager only.

The Phoenix barrier strip and its screws and any external wiring can present up to +1400 volts and should be considered hazardous.

The T840 can store high voltages for several minutes after 24 volt power is removed. The power LED does not indicate stored charge.

The bleeder resistors internal to the board could fail, allowing high voltages to remain stored indefinitely.

Before handling the T840 outside of its protective barrier, proceed as follows:

Remove any possible source of 24 volt power.

Wait three minutes.

Use a voltmeter with high-voltage probe safe for at least 2KV. Ground the voltmeter to the "GND" test point and measure the "HV" test point. Verify that the voltage is below +20 volts.

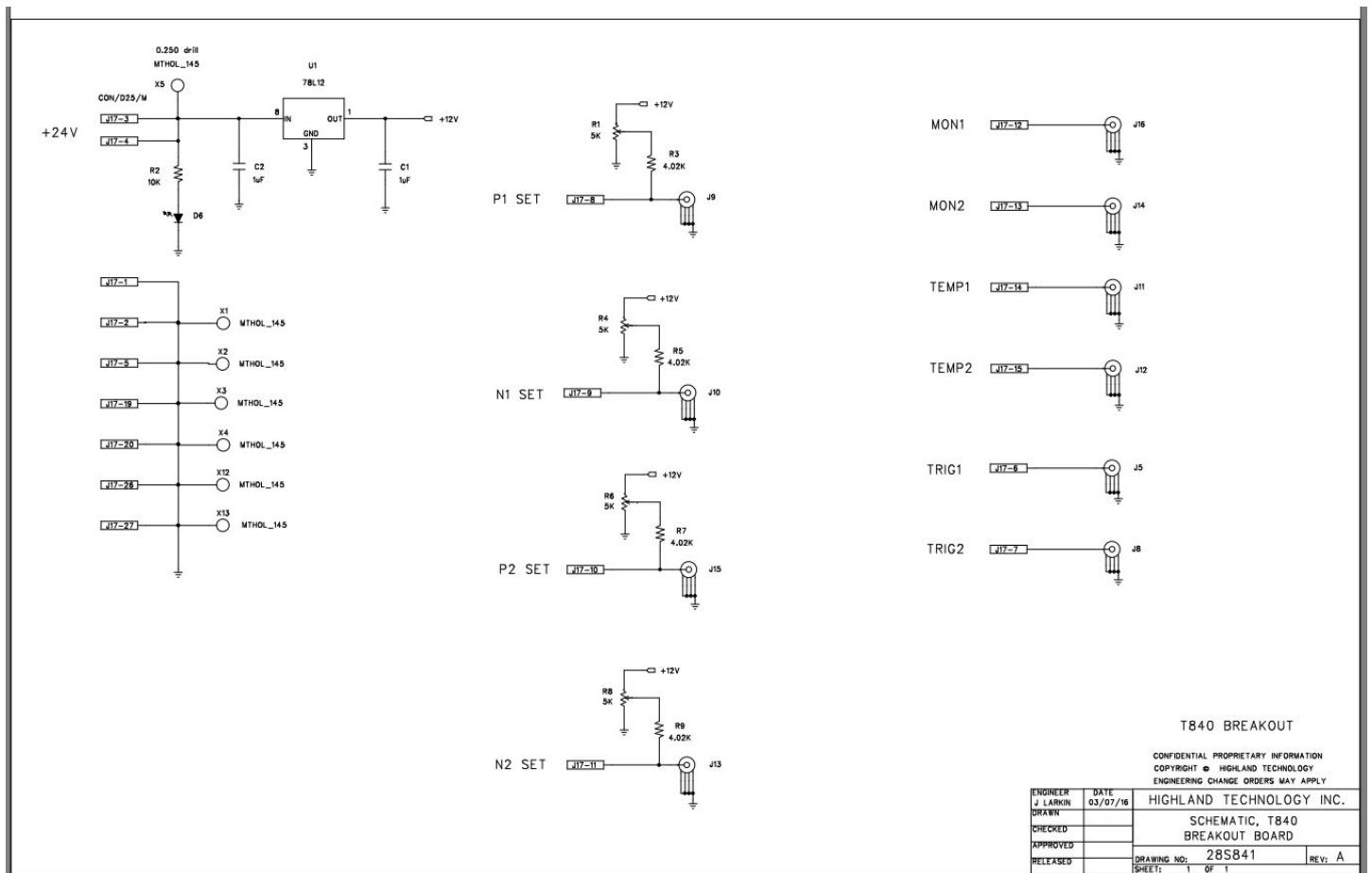
Both test points are marked by yellow boxes and appropriate lettering on the board surface.

DO NOT SHORT THE "HV" TEST POINT OR ANY COMPONENTS TO GROUND. THE T840 MAY BE DAMAGED

Use only appropriately-rated high-voltage voltmeter and oscilloscope probes.

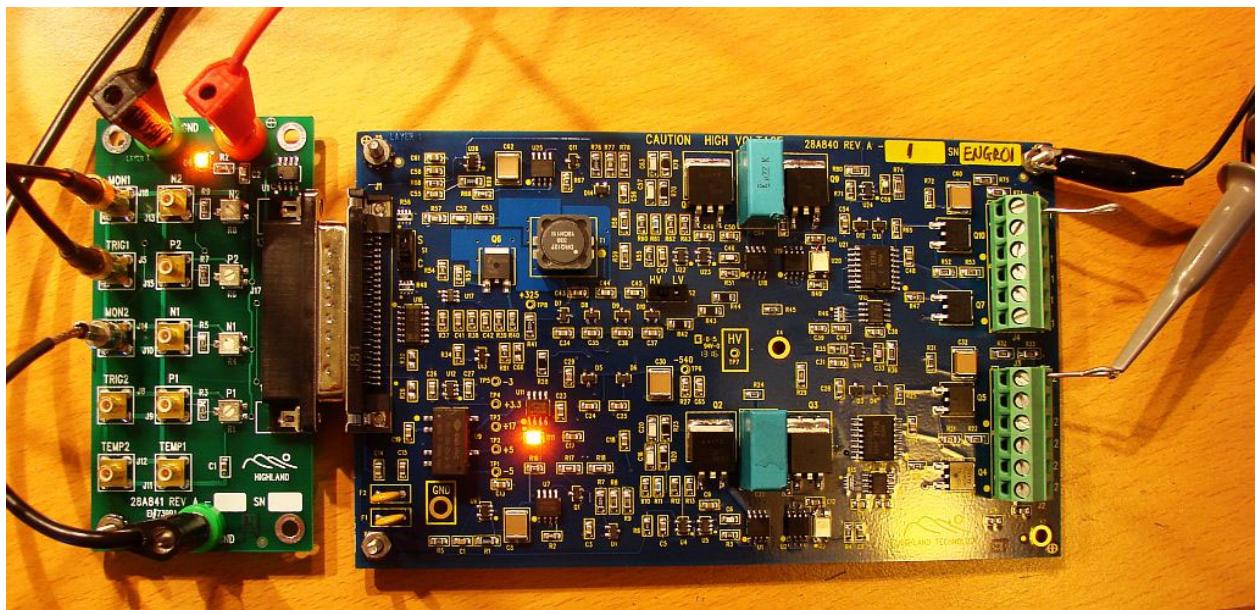
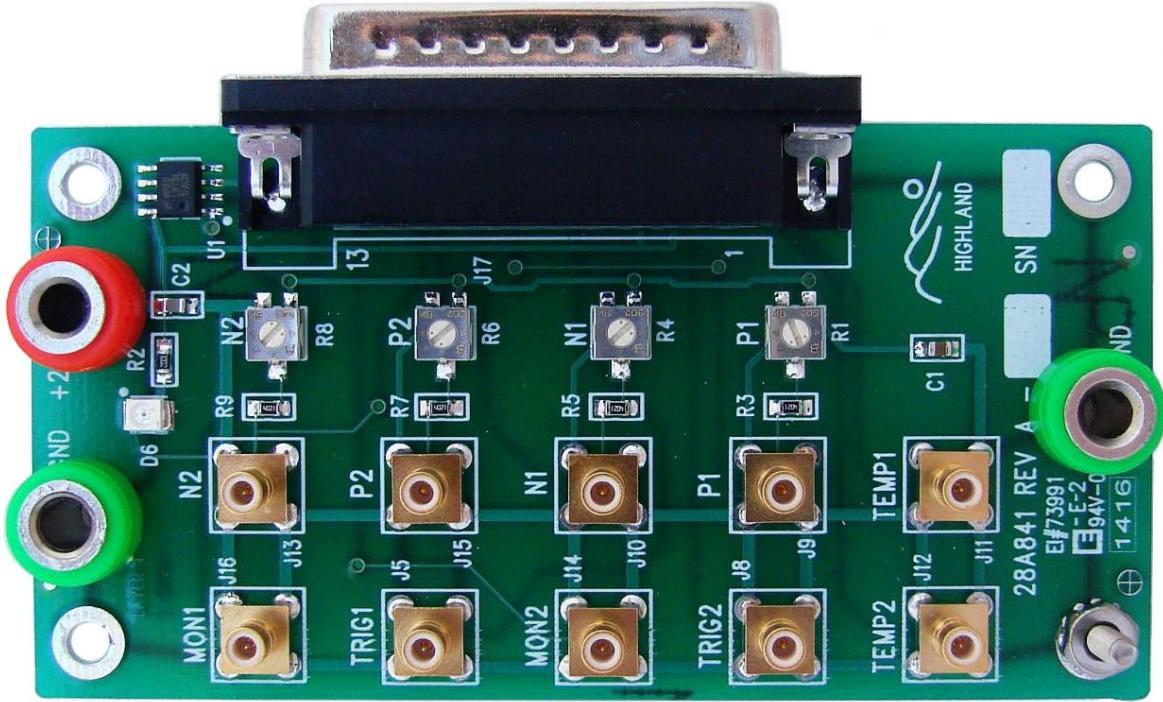
9. T841 Breakout Board

The T841 breakout board is available to assist in bench testing the T840 pulser. The schematic and board layout are:



The male D25 connector mates with the female D25 on the T840. Banana jacks are provided for +24 volt power input and grounds. Major inputs and outputs are available on SMB connectors. The four voltage programming signals can be generated by trim pots on the breakout board, or applied externally; set the pots CCW when external 0-10 volt signals are applied.

Highland can supply SMB-to-BNC cables, model J53.



10. Versions

Standard versions of the T840 include:

T840-1 2-channel high voltage driver

11. Customization

Consult factory for information on additional custom versions.

12. Hardware Revision History

Revision A Mar 2016
Initial PCB release

13. Accessories

J53-1: 3' SMB to BNC cable
J53-2: 6" SMB to BNC cable
T841-1: Breakout board for T840 pulser bench testing