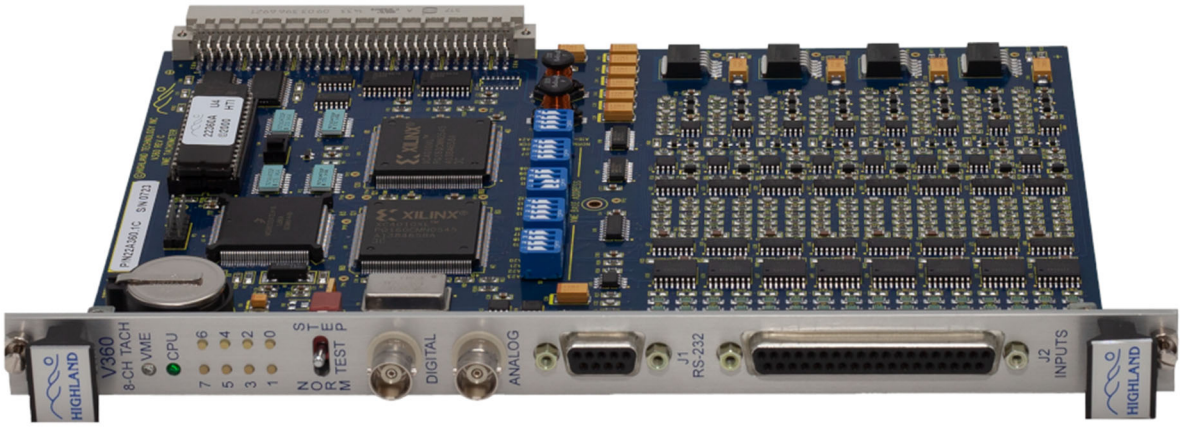
HIGHLAND TECHNOLOGY

V360 VME

TACHOMETER MODULE



Technical Manual

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650 Potrero Avenue San Francisco, CA 94110 www.highlandtechnology.com tel: 415 551-1700 fax: 415 551-5129

650 Potrero Avenue, San Francisco, CA 94110
Phone 415-551-1700 • Fax 415-551-5129
www.highlandtechnology.com

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CAUTION: Please note safety and handling precautions in Section 6.1.

1 *Introduction*

The V360 is a single-width, 6U height VME module designed specifically to acquire low frequency inputs from industrial speed sensors. The module can measure frequency and period over a wide dynamic range, and is specifically designed to ensure reliable measurement in high-noise industrial environments.

Features of the V360 include:

- Intelligent 8-channel period/frequency/RPM measurement
- Ideal for signal conditioning of magnetic speed pickups, flowmeters, and encoders
- High noise immunity ensures accurate measurement in industrial environments
- Internal signal conditioning accepts direct input from common speed sensors
- Register-based 16-bit VME module
- Clean, simple architecture simplifies programming

Differential signal inputs are signal conditioned, filtered and presented to the inputs of a custom gate array chip which manages period and frequency measurement. An on-board microprocessor periodically reads the timer chip, checks and scales data, and loads measured values into a dual-port memory interfaced to the VMEbus.

The input signal conditioners can be connected directly to common transducer types including:

- variable reluctance or hall-effect magnetic speed pickups
- AC line voltage or alternator windings up to 150 volts RMS
- optical pickups
- reed-switches or unconditioned fuel flow meters
- contact closures or other special levels

2 Specifications

FUNCTION	8-channel signal conditioner/tachometer module
DEVICE TYPE	16-bit VME register-based slave: A24:A16:D16:D08(EO) Implements 32 16-bit registers at switch selectable addresses in the VME 16 or 24 bit addressing spaces
INPUTS	Eight channels, numbered 0 through 7 Each channel has differential inputs, ground, and auxiliary +12 volt source Input impedance is > 60 K to ground on differential inputs Signal level inputs are configurable for standard TTL, open collector, AC generator, and variable reluctance sensor pickups Onboard signal conditioning includes VME-selectable gains, filtering/integration, and trigger levels to accept 10 mV to 150 volt RMS signals up to 100 kHz Inputs will tolerate 1000 volt transients for 50 µs
RANGE	32 bit period measurement with 20 ns LSB resolution, approximately 85 seconds maximum period Transparent interlock logic allows skew-free reading of 32-bit period data
ACCURACY	± 0.005% ±1 LSB
RS-232 PORT	9600 baud RS-232 port is provided This provides for monitoring of module performance and permits channel configuration without requiring host CPU programming
OPERATING TEMPERATURE	0 to 60°C; MIL/COTS ranges available
CALIBRATION INTERVAL	No factory calibration required
POWER	Standard VME supplies: +5 V: 0.5 A +12 V: 0.2 A -12 V: 0.15 A

CONNECTORS	D37 female connector for signal inputs and current-limited +12 volt excitation outputs D9 female connector for RS-232 serial port Two BNC signal monitor connectors present analog and digital signal levels of any selected channel
INDICATORS	Ten LEDs indicate processor heartbeat, VME access, and individual channel trigger activity
PACKAGING	6U single-wide VME module
CONFORMANCE	VMEbus per ANSI/VITA 1-1994 (R2002)

3 *Function Model*

3.1 *General Architecture*

Figure 1 is the block diagram of the V360 VME Tachometer module.

The V360 functions as follows:

The module provides eight input channels, numbered 0 through 7. Each input channel includes a differential input amplifier with two user selectable gain settings, and choice of signal conditioner: a programmable second-order lowpass filter (best for conditioned logic-level or switch inputs) or an integrator (best for velocity-type sensors such as variable-reluctance pickups or alternator windings). The lowpass filter is selectable to have bandwidths of 100 Hz, 1 KHz, 10 KHz, or 100KHz.

Each processed analog signal is compared by two fast precision comparators which define user selectable high and low trigger thresholds.

The digital trigger signals are processed by a custom reconfigurable gate array. For each channel, the gate array implements a programmable divide-by-N prescaler followed by a 32-bit timestamper and an associated pulse edge counter.

For each channel, the comparators provide a pulse for each sensor edge, typically corresponding to one gear tooth, one contact closure, or one AC voltage cycle. The prescaler may be programmed to divide this pulse train by a user-selectable factor between 1 and 255. This feature can reduce measurement jitter when the sensed device does not have perfect rotational symmetry or when noisy signals are processed. For example, if a 36-tooth gear is sensed with a VR pickup and the gear teeth are not precisely identical, a pre-divisor of 36 will ensure that only full shaft rotations are measured, using the same gear tooth to measure each period.

The output of the divide-by-N stage is routed to a per-channel edge counter and edge timestamper, with the timestampers capable of measuring the time-of-pulse-edge to a resolution of 20 nanoseconds.

The processor periodically polls the gate array to read all 8 sets of latched counter data, at about a 1 KHz rate. Each time the processor scans the gate array, it reads the timestamp and edge counts for each channel and computes period. At high input frequencies (above about 1 KHz), the processor will typically observe multiple edges and thus transparently revert to a multiple-period averaging mode, reducing reported period jitter. The “last best” period value of each channel is thus computed and posted to VME at the 1 KHz rate.

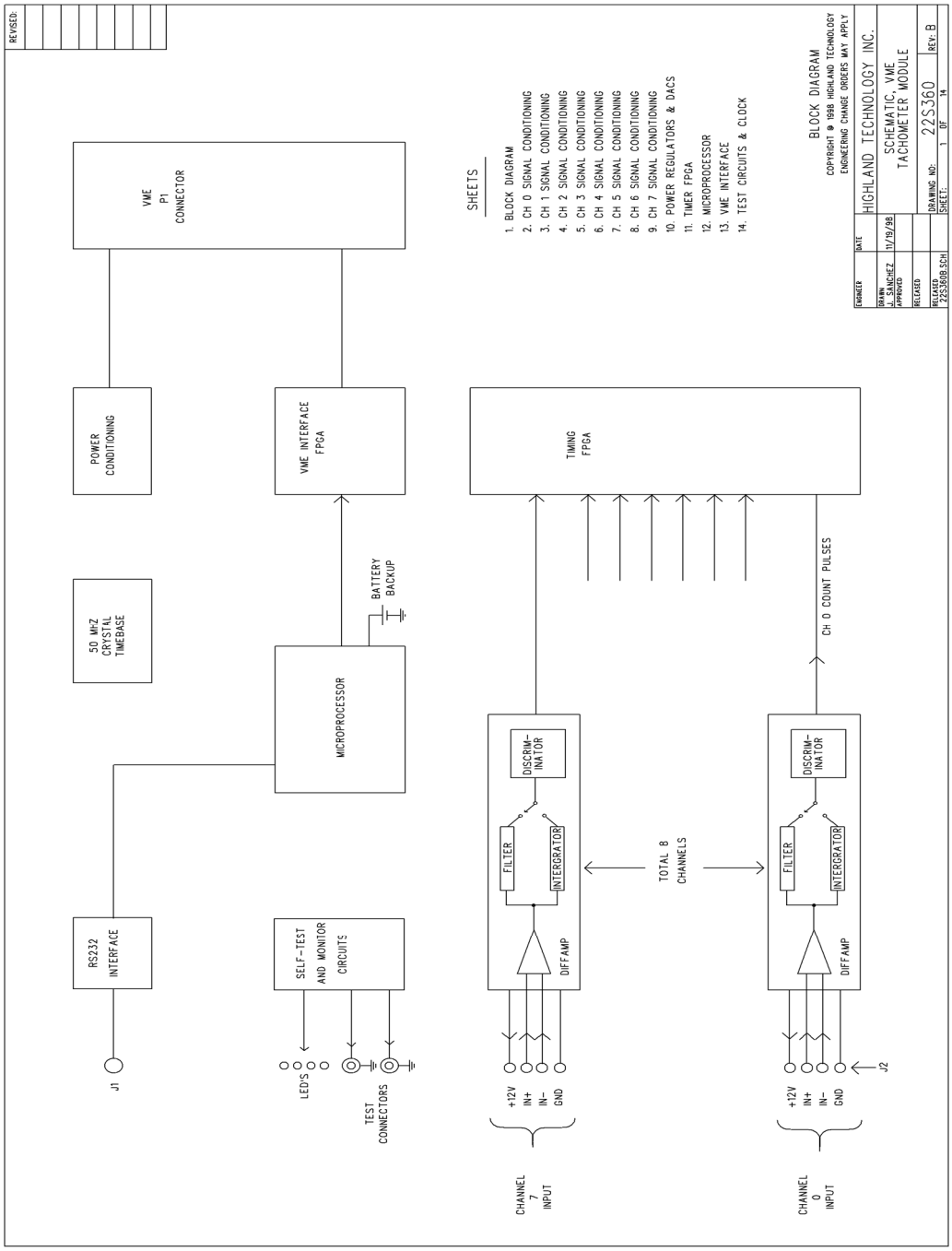


FIGURE 1. V360 BLOCK DIAGRAM

The microprocessor formats measured periods into 32-bit data words for presentation to a second gate array. This second FPGA includes a 32-bit wide dual-port memory which allows the microprocessor to write period data which is then readable by the VMEbus.

When the VME master reads a period value, it must read the data as two separate 16-bit words. In order to ensure that the read is atomic, the FPGA logic senses when the first word (at the

lowest VME address) is read, and coherently saves the second 16-bit word of the 32-bit period value. The user then reads the second word without hazards associated with asynchronous update of period values by the local microprocessor.

The data is always “high endian,” with the most significant 16 bits in the first, lowest, VME address.

Period is reported as a 32-bit value with LSB resolution of 20 nanoseconds, equivalent to a 50 MHz clock. If a channel is prescaled, the reported time is that of “N” input pulses.

3.2 *Input Signal Conditioning*

Each of the eight input channels has an input signal conditioning circuit as illustrated in Figure 2. The channel electronics consists of

An input resistor network which provides high-voltage withstand capability, high-frequency rolloff, switchable attenuation, and provision for injection of a test signal.

±5 volt signal swing clamps.

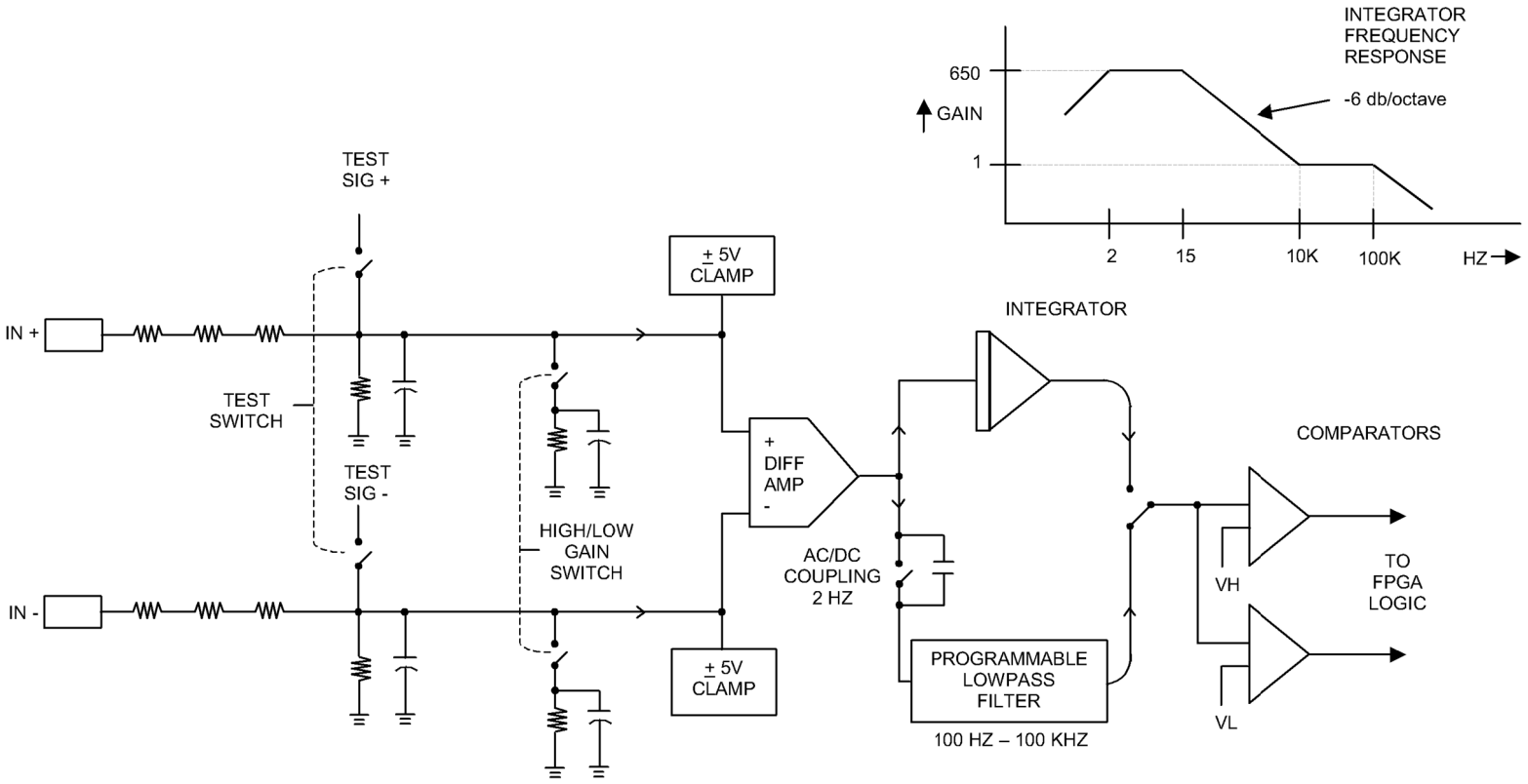
A unity-gain differential amplifier.

A switchable signal path, incorporating either

an AC/DC coupling circuit followed by a switchable-bandwidth lowpass filter, or

an integrator for equalization of rate-type signals.

A dual-level discriminator.



ALL SWITCHES ARE SOLID-STATE PROGRAMMABLE
INPUT ATTENUATOR HAS 100 KHZ LOWPASS
RESPONSE AT ALL GAIN SETTINGS

V360 CHANNEL INPUT
SIGNAL CONDITIONING
FIG 2

3.3 *Trigger Discriminators*

The conditioned signal, from either the lowpass filter or the integrator, is applied to two precision comparators, each of which has a trigger threshold set by a programmable digital-to-analog converter. The comparators are used in two different modes:

If the input path enables the lowpass filter, both comparators are programmed to have positive thresholds, with one level establishing the “signal high” threshold and the other setting the “signal low” threshold. The difference between these two levels is the trigger hysteresis. Users may select low or high hysteresis levels, which the onboard microprocessor translates into appropriate comparator thresholds.

If the signal is a reasonably symmetric sinusoid or rectangular pulse train, the lowpass filter should be programmed to pass the highest expected input frequency. Filter selections are 100 Hz, 1 KHz, 10 KHz, and 100 KHz. Avoid enabling excessive bandwidth to keep noise and jitter to a minimum.

If the input signal consists of narrow positive pulses, the DC-coupled mode and dual above-zero trip points are appropriate to ensure reliable triggering. In this case, the filter bandwidth should be selected to pass the narrow pulses irrespective of the pulse reprate. The 100 KHz range will pass 10 microsecond or longer pulses, and the 100 Hz range will pass 10 millisecond or wider pulses. If the input is narrow negative pulses, the differential input leads should be reversed to effectively make the pulses positive.

If the input path enables the integrator, the user-furnished thresholds are set symmetrically above and below zero volts, as the “high” and “low” trigger levels. The effective trigger level is then zero volts, with a hysteresis of two times the threshold setting. With the attenuator off, the integrator gain is about 650 from 2 Hz to 15 Hz, falls off at 6 dB/octave to unity gain at 10 KHz, and is flat from 10K to 100KHz. This curve is a good match for many velocity-type sensors, whose signal level varies linearly with frequency and may be very small at low speeds. The integrator is symmetrically clamped to overload cleanly.

3.4 *Period Measurement Algorithms*

The algorithm used to measure period is as follows:

Trigger pulses are received from the input signal conditioning logic, one pulse per rising edge of the sensor input.

The pulse train is divided by the programmable divide-by-N prescaler, with division ratio of 1 to 255.

Every resulting pulse edge simultaneously increments an edge counter and snapshots a master timestamp counter. The master timestamp is a 32-bit free-running 50 MHz binary counter.

At a rate of 1024 times per second, the microprocessor reads the latest channel edge count and timestamp. If one or more edges have been counted since the last read, the number of edges and the timestamp are used to compute the signal period.

Each channel may be placed in one of three timing modes:

MODE 0: RUNDOWN. If no count edges are seen by the timing system, it is possible that the pulse train has stopped; this would leave the last- good period measurement in force, falsely implying that the input period remains at the old value. To prevent this error, the processor, when it checks a channel's counters and discovers “no edges,” computes what the period would have been had an edge been sensed. If this value is greater (longer period) than the last real period, the substitute value is posted as the channel period. The net effect is that, if a pulse train abruptly ceases, the reported period will increase smoothly to the maximum (all 1s, 85.899 seconds) value. When the pulse train resumes, a new period will be posted whenever a valid period is sensed.

MODE 1: PERIOD. In this mode, the module reports the last measured full period. After 85.5 seconds of inactivity, the reported period will be set to the maximum value, and two new triggers will be required before a new, valid period can be reported.

MODE 2: USER TIMEOUT. In this mode, the user may specify a no-signal timeout interval of up to 64 seconds. The last valid period will be reported, unless no signal edges have been seen for more than the specified timeout. After the timeout is exhausted, the maximum period is posted.

See Section 5.7.1 for a discussion of channel configuration.

4 *Front-Panel Connectors and LEDs*

4.1 *Connector J1: RS-232 Interface*

A female DB-9 connector J1 is provided to interface to a PC serial port for configuration settings and test. Connection to a typical laptop PC will require a straight-through male-to-female D9 serial cable.

A DOS-based test/display program, V360.EXE, can be downloaded from Highland's website.

4.2 *Connector J2: Channel Inputs 0…7*

The 8 channel inputs are wired to the female D-37 connector J2. Plus and minus balanced input signals, 12 VDC excitation, and ground pins are provided for each channel as follows:

Pin #	Signal Name
1	VME signal ground
2	VME signal ground
3	+12 excite
4	VME signal ground
5	+12 excite
6	VME signal ground
7	+12 excite
8	VME signal ground
9	+12 excite
10	VME signal ground
11	+12 excite
12	VME signal ground
13	+12 excite
14	VME signal ground
15	+12 excite
16	VME signal ground
17	+12 excite
18	VME signal ground
19	VME signal ground
20	VME signal ground

Pin #	Signal Name
21	channel 7 input -
22	channel 7 input +
23	channel 6 input -
24	channel 6 input +
25	channel 5 input -
26	channel 5 input +
27	channel 4 input -
28	channel 4 input +
29	channel 3 input -
30	channel 3 input +
31	channel 2 input -
32	channel 2 input +
33	channel 1 input -
34	channel 1 input +
35	channel 0 input -
36	channel 0 input +
37	VME signal ground

Note that if an open-collector or switch input is used, the IN- terminal should be connected to ground and the IN+ terminal connected to +12V through a pullup resistor; 2.7 K, 1/4 W is suggested.

The +12 volt pins may be used to power external pullups or signal conditioners. All are commoned, and share a single foldback current limiter device from the VME +12 volt supply. Total current drain should not exceed 0.5 amps for all excitation loads. If the load current exceeds 0.5 amps and the current limiter is activated, it may be necessary to remove loads or cycle power to reset the current limiter.

4.3 *BNC Test Connectors J10 and J11*

The two BNC connectors allow the user to connect a dual-trace oscilloscope to the module to observe the analog input signals and resulting conditioned digital signal which is used for period measurement. A front-panel-accessible switch selects the channel to be monitored.

BNC connector J11 provides for monitoring the selected signal-conditioned analog signal input. This signal is the output of the lowpass filter or integrator. The “raw” input signal may be observed by temporarily reprogramming the channel config register to operate in wideband (100 KHz) filter mode.

BNC connector J10 provides for monitoring the actual digital timing trigger of the selected pulse signal input. This is the signal on which period measurement is performed, with the rising edge defining the end of each period. This signal is sampled before the programmable divide-by-N prescaler.

4.4 *LED Indicators and Test Switch*

The module is equipped with 10 LED indicators.

The green “CPU” LED flashes once per second to indicate that the on- board microprocessor program is executing. The blue “VME” LED flashes whenever the module is addressed from the VMEbus.

There are eight amber channel LEDs, labeled “0” through “7.” When the test select switch is in its leftmost NORM position, each LED flashes when the corresponding channel receives active input signal transitions. If prescaling is enabled, the LED flashes are activated from the output of the divide-by-N prescaler.

When the select switch is in the center TEST position, the eight LEDs serve to indicate which channel's signals are routed to the two BNC test connectors. Pressing the test switch to the momentary right STEP position steps through the channel selections, with one amber LED steadily illuminated to indicate which channel is selected. In this case, the conditioned analog channel signal will appear at the ANALOG BNC connector and the discriminated digital signal will appear at the DIGITAL connector.

When the test switch is in its NORM position, the digital test connector output will be a 5 MHz square wave which may be used to check the accuracy of the internal 50 MHz oscillator.

5 *VME Register Map and Programming*

The following is a summary of the VME-accessible registers implemented by the V360-series module. The module follows VXI conventions, having 32 each 16-bit registers beginning at the base address. Switches on the module set the base address, anywhere in the 24-bit or 16-bit VME address spaces.

All registers are 16 bits wide. Reg # below is the ordinal register number in decimal; OFFSET is the VMEbus address offset from the module base address, shown in hex. The R/W column indicates whether the register is readable and/or writable from the VMEbus.

Reg Name	Reg #	Offset	R/W	Function
VXI MFR	0	0x0	R	VXI manufacturer ID: always 65262, FEEE hex
VXITYPE	1	0x2	R	module type, always 22360, 5758 hex
VXI STS	2	0x4	R	VXI status register
--	3	0x6	R	unused; always 0
ROM ID	4	0x8	R	firmware ROM ID, typically 22360 decimal
ROM REV	5	0x0A	R	firmware ROM revision, typically ASCII “A”
MCOUNT	6	0x0C	R	microprocessor update counter
TDIV	7	0x0E	R	test signal frequency divisor
CMD	8	0x10	RW	module command register
PARM1	9	0x12	RW	command parameter 1
PARM2	10	0x14	RW	command parameter 2
PARM3	11	0x16	RW	command parameter 3
PARM4	12	0x18	RW	command parameter 4
PARM5	13	0x1A	RW	command parameter 5
--	14	0x1C	R	unused, always 0
--	15	0x1E	R	unused, always 0
P0HI	16	0x20	R	channel 0 high word period data
P0LO	17	0x22	R	channel 0 low word period data
P1HI	18	0x24	R	channel 1 high word period data
P1LO	19	0x26	R	channel 1 low word period data
P2HI	20	0x28	R	channel 2 high word period data
P2LO	21	0x2A	R	channel 2 low word period data
P3HI	22	0x2C	R	channel 3 high word period data
P3LO	23	0x2E	R	channel 3 low word period data

Reg Name	Reg #	Offset	R/W	Function
P4HI	24	0x30	R	channel 4 high word period data
P4LO	25	0x32	R	channel 4 low word period data
P5HI	26	0x34	R	channel 5 high word period data
P5LO	27	0x36	R	channel 5 low word period data
P6HI	28	0x38	R	channel 6 high word period data
P6LO	29	0x3A	R	channel 6 low word period data
P7HI	30	0x3C	R	channel 7 high word period data
P7LO	31	0x3E	R	channel 7 low word period data

VME Registers are described in detail below. Within each register, bits are numbered 0 (LSB) through 15 (MSB). Bits 0...7 are the LS byte, and bits 8...15 are the MS byte.

5.1 *VXI MFR Register: VXI Manufacturer's ID*

This register displays the VXI-registered manufacturer's ID code. It always reads as 0xFEEE.

5.2 *VXI Type Register: Module Type*

This register displays the module type. It normally reads as 22360 decimal, 0x5758.

5.3 *VXI STS Register: VXI Status Register*

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	S7	S6	S5	S4	S3	S2	S1	S0	1	1	1	1

Bits 4 through 11 of this register reflect the realtime states of the channel 0 through 7 inputs respectively, with a high bit corresponding to an electrically positive input level. These bits are updated 1024 times per second. The remaining status register bits are always all 1s. The bit assignments within this register are in conformance with VXI standards.

5.4 *ROMID Register: Firmware Version*

The MC68332 microprocessor software version ID is read here, with a typical value of 22360 decimal (0x5758). Other code versions, having different functionality, may have different ID codes.

5.5 *ROMREV Register: Firmware Revision*

The revision letter of the firmware may be read at this location, as an ASCII character, “A” (0x41) for the initial firmware release.

5.6 *MCOUNT/TDIV Registers*

The MCOUNT register appears as a 16-bit binary counter which is incremented by the microprocessor just after all eight measured period values are refreshed into the VME-readable dual-port memory. Refresh occurs every 976 microseconds and lasts for about 50 micro-seconds.

TDIV is the 16-bit test oscillator divisor, as discussed in Section 5.7.5.

5.7 *CMD Register: Module Command*

Certain data transfers are managed using the module COMMAND register and the associated PARAMETER registers. The bits in the COMMAND register are:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR								DONE	CC6	CC5	CC4	CC3	CC2	CC1	CC0

Bit	Name	Function
6...0	CCODE	command code
7	DONE	set by V360 to indicate operation complete
15	ERR	set by V360 to indicate error

The protocol for executing commands is as follows:

The VME master reads the COMMAND register and waits for the DONE bit to be true.

If DONE is true,

write parameter registers as desired;
write a command code (bits 0...6 only, other bits OFF) to the COMMAND register; this may be a word or LS byte write.

Wait for the DONE bit to reappear.

Check the ERR bit to see if the command was rejected.

Read any parameter registers if appropriate.

After a command has been executed, the module will simultaneously set the DONE and (if an error) ERR bits. The old command bits 0...6 will be unchanged.

Bits 8...14 of the command register may return error codes or other status information.

Defined commands are as follows:

Command Code Hex	Function
0x8	read module name
0x9	write module name
0x0A	reset module
0x0B	set self-test frequency divisor
0x10	read channel 0 configuration
0x11	read channel 1 configuration
0x12	read channel 2 configuration
0x13	read channel 3 configuration
0x14	read channel 4 configuration
0x15	read channel 5 configuration
0x16	read channel 6 configuration
0x17	read channel 7 configuration
0x18	write channel 0 configuration
0x19	write channel 1 configuration
0x1A	write channel 2 configuration
0x1B	write channel 3 configuration
0x1C	write channel 4 configuration
0x1D	write channel 5 configuration
0x1E	write channel 6 configuration
0x1F	write channel 7 configuration
0x20	read channel 0 name
0x21	read channel 1 name
0x22	read channel 2 name
0x23	read channel 3 name
0x24	read channel 4 name
0x25	read channel 5 name
0x26	read channel 6 name

Command Code Hex	Function
0x27	read channel 7 name
0x28	write channel 0 name
0x29	write channel 1 name
0x2A	write channel 2 name
0x2B	write channel 3 name
0x2C	write channel 4 name
0x2D	write channel 5 name
0x2E	write channel 6 name
0x2F	write channel 7 name

5.7.1 *Channel Configuration Command*

Each of the eight channels must be configured for the transducer type and measurement options. To configure a channel, load the three command parameter registers and execute the appropriate command, as noted above. The WRITE CONFIGURATION commands are illegal in LOCK mode.

Bits in the configuration registers establish type, gain, filter, threshold, rundown, and hysteresis settings, and engage the self test signal.

When configuring a channel, the parameter register functions are as follows:

PARM1: channel control bits

PARM2: trigger threshold

PARM3: prescaler count

PARM4: mode 2 period timeout

The channel control bits (transferred in PARM1) are as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					M2	M1	M0	TEST	FLT1	FLT0	INT	ATTN	HYST	AC	

Bit	Name	Function
0	--	Not used.
1	AC	When set, enables AC coupling of the input signal.

2	HYST	Sets hysteresis HIGH in filter mode.
3	ATTN	Engages the 25:1 signal input attenuator.
4	INT	If set, selects the wide range integrator for velocity-type magnetic pickups. If this bit is off, channel works in filter mode.
5	FLT0	Selects filter cutoff frequency.
6	FLT1	Selects filter cutoff frequency.
7	TEST	Engages self-test override signal to channel input.
8	M0	Channel timing mode.
9	M1	Channel timing mode.
10	M2	Channel timing mode.
11-15	--	Not used.

The three MODE bits establish channel timing mode. Currently-defined modes are

M2 Bit10	**M1 Bit9**	**M0 Bit8**	**Timing Mode**
0	0	0	Period measurement, rundown enabled.
0	0	1	Period measurement, rundown disabled.
0	1	0	Period with user-specified timeout

The AC bit, when set, enables AC coupling of the signal into the trigger comparators. The low-frequency cutoff point is about 2 Hz. This bit is ignored in integration mode.

The HYST bit is functional only in filter mode. If set, it selects high (50%) hysteresis, and when clear selects low (10%) hysteresis.

The ATTEN bit, when set, activates the channel input-signal attenuator, reducing front-end gain by 25:1. This bit should be set when interfacing with high-level transducers. The inputs are protected to 150 VRMS each regardless of the ATTEN bit setting.

The TEST bit, if set, replaces the input signal with a 2 volt p-p test signal; see Section 5.7.5. The ATTEN bit is inoperative during test.

The INT bit, when set, routes the input signal through the wide-range integrator, and allows the user to set symmetric positive and negative trigger thresholds. Integrator mode should be used for devices that have an analog signal level which is proportional to frequency, such as unconditioned magnetic pickups or alternators. The HYST, AC, and filter-select bits are ignored when in INT mode.

If INT is false, the module works in lowpass filter mode. In this case, the FILT1 and FILT0 bits set the filter bandwidth, as follows:

FILT1	FILT0	Filter Bandwidth
0	0	100 Hz
0	1	1 KHz
1	0	10 KHz
1	1	100 KHz

In filter mode, the Tn bits set the positive trigger threshold, and the HYST bit selects low or high hysteresis.

The trigger threshold is communicated in the low eight bits of PARM2. This value can be considered to be the trigger level, scaled from 0 to 255, corresponding to electrical trigger levels from 0 volts to +5 volts... about 20 millivolts per LSB. If the input attenuator is set to ATTEN mode, the effective (relative to input) trigger level scaling becomes 0 to +125 volts for trigger level codes 0 to 255, about 0.5 volts/LSB.

The count prescaler value is transmitted in the PARM3 register. Legal values may be from 0 to 255. If the value is 0 or 1, the input prescaler is disabled and every input pulse is applied to the period measurement logic. For higher values of PARM3, the input pulse train is divided by the specified value before period measurement is made.

If channel mode 2 is specified, channel parameter 4 must be loaded when the channel is configured. This is a 16-bit unsigned integer which defines the desired no-signal timeout interval. Timing is in units of 1/1024 seconds, for a maximum range of 64 seconds.

Example

To set up channel 5, one might do the following:

Read the command register, verify DONE bit true.

Write 0x0044 to PARM1 (DC, no attn, high hyst, 10 KHz filter, mode 0).

Write 0x0040 to PARM2 (trigger level 1.25 volts).

Write 0x0024 to PARM3 (prescale divisor = 36).

Write 0x1D to the command register (write channel 5 config).

Read command register; loop till DONE bit true, check for error.

To read back channel setups, execute the appropriate “read config” command code, verify DONE, and then read the four parameter registers.

Since all commands are guaranteed to execute in less than two milliseconds, users may prefer a non-handshake method of executing commands. To do this, the sequence is

write parameter registers if appropriate,
write command register,
wait at least two milliseconds,
read parameter registers if appropriate.

Note that the V360.EXE program may optionally be used to assist in configuring modules in two different ways:

1. Modules may be configured by running V360.EXE on a PC which is connected to a V360 module via a serial cable. This allows configuration to be done without the requirement that the VME host deal with the configuration rules.

2. V360.EXE may be run on any PC without connection to a V360, and be used as a “configuration compiler.” One can configure a hypothetical module and save the configuration to a disk file. The readable disk file will summarize the module setup and list a table of hex channel parameters and command codes required to set the module into that configuration. The literal hex values may then be written by the VME host to the actual V360 module.

5.7.2 *Set Channel Name Command*

The V360 will store a 10-character name for each channel. This may be useful for tracking channel setups, especially when setup is done from the serial port but data readout is via VME.

A name is a 1- to 10-character ASCII string. To write the name, load the five parameter registers with the desired text and execute the appropriate WRITE NAME command. To read back names, execute a READ NAME command, and then read the parameter registers. If the module is in LOCK mode, the VME master cannot write channel names.

By convention, the first character of the name is the MS byte of the first parameter word, and the last character is the LS byte of the fifth parameter word. Factory default names are " Channel 0" through "Channel 7.” If the user writes any control codes (0x1F and below) within the name, the V360 will convert them to spaces.

5.7.3 *Set Module Name Command*

The module may be assigned a 10-character name, using the associated WRITE MODULE NAME and READ MODULE NAME commands. These commands are similar to the channel name commands discussed above. The default is "V360 Tach."

5.7.4 *Module Reset Command*

The module may be reset to a default state by executing the RESET command. To execute this operation, set PARM1 to 0x1129 and then write command code 0x0A to the command register.

All channels will be configured to the following:

Mode 0 (period measurement, rundown enabled).
TTL-compatible trigger level: +1.25 volts.
Channel gain = 1 (attenuator off).
Filter mode, 100 KHz lowpass.
Hysteresis low.
DC coupled.
Prescale disabled (divisor = 1).
Integrator off.
Channel self-test off.

The test oscillator frequency will be set to 1000.072 Hz, and all default names will be installed.

If the module is in the LOCK mode (as set by the LOCK DIPswitch) the reset request will be ignored; the module may still be reset via the RS-232 port. Refer to Section 6.2.3 for a discussion of LOCK mode.

5.7.5 *Test Oscillator Set Command*

Any channel may be placed in self-test mode, where an internal square-wave frequency is forced into the channel front-end inputs. A command is provided to set the oscillator frequency. To set this, write a divisor into the PARM1 register and write command code 0x0B to the command register. The test oscillator frequency in Hertz is

Ftest = 4,194,304 / Divisor

The legal range of divisors is from 20 (209.715 KHz) to 32767 (128.004 Hz).

The powerup/reset default divisor is 4194 (0x1062) for 1000.072 Hz. The test oscillator is independent of the module timebase oscillator, and the test frequency value may vary by up to ±0.01%. The internal test oscillator is enabled only when one or more channels are in TEST mode. It is possible that the test oscillator may inject a small leakage signal into channels which are not in test mode, increasing measurement jitter slightly; if marginally low signals are to be timed, it may be better to place no channels into test mode on a permanent basis.

5.7.6 *Test Dual-Port Memory Command*

A data test pattern may be run on the VME dual-port memory. To invoke this function, load a time interval value “K” into the PARM1 register and load command code 0x0C into the command register. The test pattern will be run for K/1024 seconds. During the test interval, the first 16 VME registers will not be modified by the module and are available to the VMEbus master for full read/write testing access. The high 16 registers remain read-only, with preassigned test patterns appearing instead of the normal eight longword time period values.

Each channel period value is alternately written with a defined 32-bit pattern alternating with its 1s complement. The test patterns are:

Channel	Reg #	Offset	Test Pattern
0	16	0x20	0x0123ABCD
1	18	0x24	0x13F634D1
2	20	0x28	0x2C634B71
3	22	0x2C	0x3AA86C4D
4	24	0x30	0x47BA652F
5	26	0x34	0x5D5A4B62
6	28	0x38	0x67C2A551
7	30	0x3C	0x70A53CF2

These patterns may be read and verified as being either the correct test pattern or its complement. This verifies all VME data and address paths and tests the 32-bit “atomic read” logic.

5.8 *Period Readout Registers*

Each channel has a pair of associated period readout registers, named PxHI and PxLO. To ensure coherent data, the PxHI register must be read before reading the PxLO register. When PxHI is addressed, both the HI and LO period data are read from dual-port memory, and the PxLO data is buffered for the subsequent read of the low data.

Even if the host CPU operates in low-endian mode and assumes that less significant data resides in lower memory locations, it is still imperative that the data be read in the HI:LO sequence.

Each channel has its own low data buffer latch so that, in a multi-tasking environment, one task can read certain of the time registers and a different task can read others without creating hazards. If multiple tasks must be able to read all registers, another mechanism should be used to ensure that 32-bit period values are correct; double-read-and-compare is suggested.

6 *Setup and Installation*

6.1 *Safety and Handling Precautions*

The V360 module includes static-sensitive components; please observe antistatic procedures when handling the module outside of its antistatic packaging or outside of the VME cardcage.

CAUTION: Do not insert or remove the module from a crate with crate power on. Do not power up the crate unless front-panel mounting screws are secure.

Certain transducers and frequency-signal sources may produce dangerous voltage and energy-level signals. To ensure safety, always observe the following precautions:

CAUTION: Connect only known human-safe and energy-limited signals to the V360.

CAUTION: Route all module wiring as low-voltage signals in conformance with appropriate electrical codes.

CAUTION: Never apply more than 150 volts RMS to any input, either across a differential input or from any input to ground.

CAUTION: Do not connect signal (VME) ground or the 12-volt excitation signal to any possible external potential sources.

CAUTION: If explosion hazards are possible, connect V360 signals to field Wiring through appropriate intrinsic safety barrier devices.

The V360 module has finite failure rates associated with its hardware, firmware, and documentation. Do not apply the V360 in data acquisition or control systems where a failure or defect in the module may result in injury, loss of life, or property damage.

6.2 *Switch Setups*

6.2.1 *A16/A24 Addressing Mode Switch*

One DIPswitch position is labeled A16=/=A24. Press the appropriate side of the switch to permit operation in VME systems which use “A16” (16-bit) or “A24” (24-bit) addressing.

In A16 mode, the module responds to VME address modifiers 0x29 and 0x2D. In A24 mode, address modifiers are 0x39 and 0x3D.

6.2.2 *VMEbus Address Switches*

The module VME base address is set by on-board DIPswitches. The switches are labeled A06 through A23. To set an address bit true, press the side of the switch nearest the “Axx” legend. If the module is in A16 mode, only switch positions A06 through A15 are decoded.

The as-shipped module base address is 0xC000 in the A16 space. The A24/A16 switch is in its A16 position, and the A15 and A14 address switches are ON, with all others OFF. This configuration is pictured below:

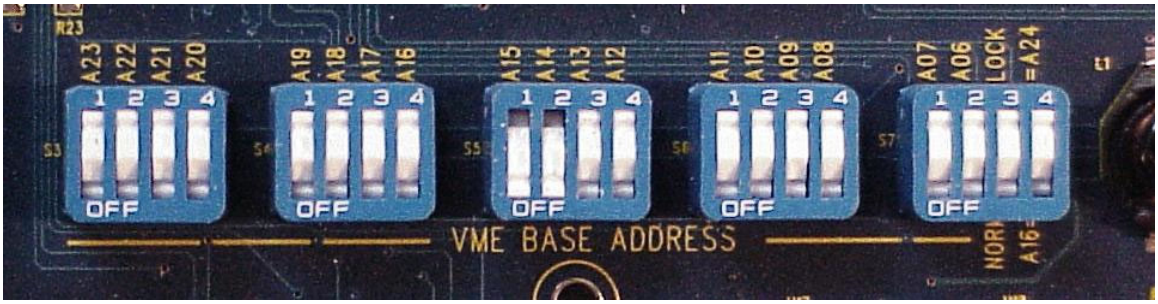


FIGURE 3. VMEBUS ADDRESS SWITCH CONFIGURATION

6.2.3 *Lock Mode Switch*

One DIPswitch position is labeled NORM/LOCK. For normal operation, press the side labeled NORM, as pictured above.

If the LOCK position is pressed, the module operates in LOCK mode. In this state, the VME interface cannot alter channel configurations, and the module can be programmed from the RS-232 serial port only. This is intended for situations where it is not appropriate to program the host system to do module setups (say, when the host is a VME-compatible PLC) and it is desired that the host not be able to accidentally change channel configurations. Since configuration memory is nonvolatile, one can also configure a module on one system (using VME or the serial port), power down, remove and LOCK the module, then install it in another system which cannot alter channel setups.

6.3 *Installation in a VME Crate*

The V360 may be installed in any standard 6U VME backplane. The module connects to the backplane J1 connector only. The standard V360-1 does not use interrupts and passes all interrupt and bus grant signals. Seat the module firmly and secure both front-panel mounting screws before applying power.

The module uses the standard VME power supplies:

+5 volts at 700 mA max

+12 volts at 250 mA max

-12 volts at 200 mA max

If external transducer excitation is provided by the V360, the +12 volt current drain will increase, up to the 0.5 amp current limit.

6.4 *Installation Verification*

Once the module is installed and secured, crate power may be applied. At powerup time the following LED sequence should be observed:

Green LED on; indicates ROM checksum OK,

1 second delay,

blue and green LEDs on; indicates VME FPGA programmed,

1 second delay,

green and blue off; indicates TIMER FPGA programmed,

green now blinks once per second, and blue flashes on VME access.

The TEST switch may now be used to select a channel for test access, or to indicate channel trigger activity via the eight yellow LEDs.

Users may now access the module via the VMEbus. It is recommended that the module MFR ID and MODULE TYPE registers be read and verified correct, ensuring that there are no gross VME access or conflict problems.

6.5 *Using the Signal Monitor Features*

The front panel of the module is furnished with a test switch, two BNC connectors, and eight channel-monitor LEDs. The switch functions are discussed in Sections 4.3 and 4.4.

During system checkout, it is often convenient to use the test provisions to adjust input signal conditioning and trigger level options. The procedure is:

Setup such as to be able to program channel configurations, either through a VME setup program or by running V360.EXE on a laptop PC connected to the module serial port.

Connect a dual-channel oscilloscope to the ANALOG and DIGITAL front-panel test connectors.

Apply an actual or simulated transducer signal to the channel under test.

Set the TEST toggle switch to its center position, and move it to the right STEP position as required, until the correct channel-select LED is lit.

Adjust channel configuration until both the displayed analog and digital signals are clean and uniform over the range of expected signal levels and frequencies.

6.6 *Backup Battery*

The V360 uses a coin-cell lithium battery to maintain module configuration in static RAM. The battery is a Panasonic type CR2354 or equivalent. The battery has an expected lifetime of at least ten years, and should be replaced at least that often. The module will lose its current configuration when the battery is replaced. The battery saves channel configuration data only, and is not otherwise required for operation.

7 Test Software

The V360.EXE program can be downloaded from Highland's website. It will run on a PC under DOS Version 6 or later, or in a Windows DOS box.

V360.EXE communicates serially to the V360. Use an ordinary modem-type serial cable (straight-through, non null modem) to connect the PC's COM1 or COM2 port to the female D9 connector on the front of the module. The program can also communicate to the module over the VMEbus, using one of several available PC-to-VME interfaces.

Functions supported include

Display of all module registers, including periods, frequency, and equivalent RPM or other engineering units.

Plotting of frequency/RPM versus real time.

Channel configuration. The program may be used to configure the module in situations where it is undesirable to use the VME host computer to do so. The V360.EXE program will also compute channel configuration register hex values "offline" so that a host system can load these literal values into config registers with a minimum of programming.

The following figures are typical plots produced by the V360.EXE program.

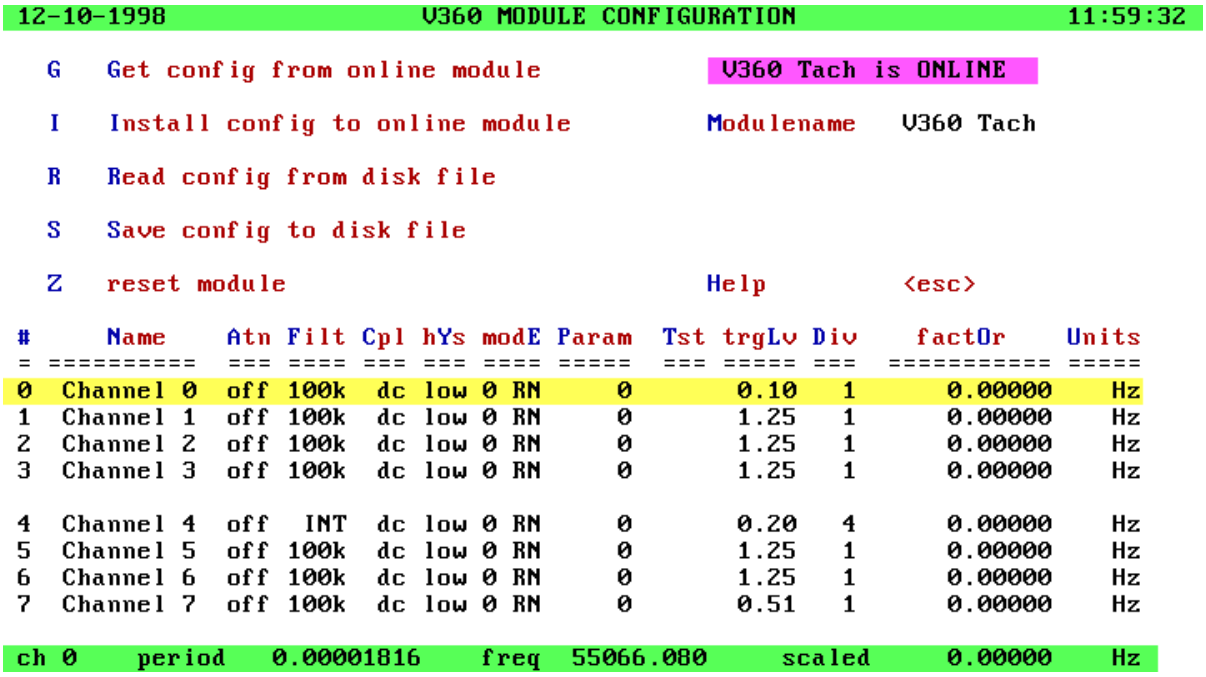


FIGURE 4. MODULE CONFIGURATION SCREEN OF THE V360 TEST PROGRAM

The V360.EXE test program, which is supplied with the unit, may be run on a laptop PC connected to the V360 RS-232 port, and may be used to configure the module and display/plot channel data. The module configuration is stored in on-board battery-backed static RAM.

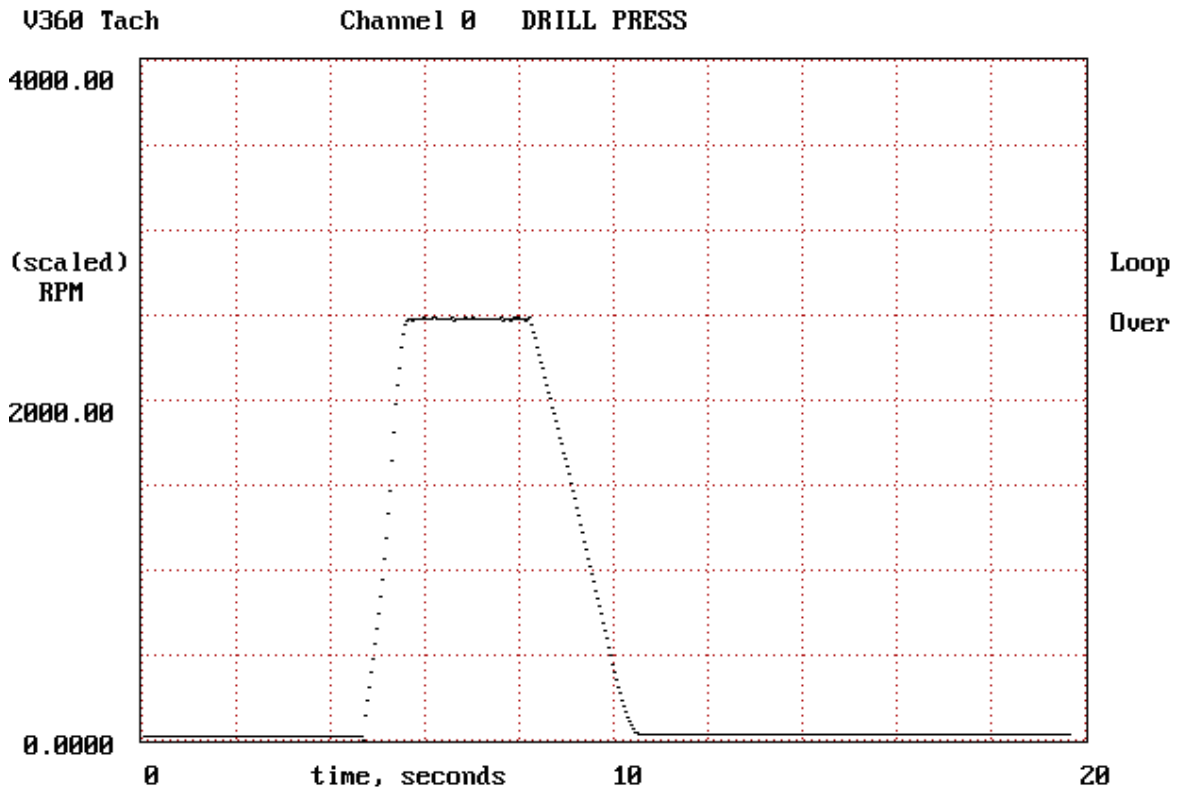


FIGURE 5. ACCELERATION-DECELERATION CURVE OF A DRILL PRESS

To measure the acceleration-deceleration curve of a drill press, a magnetic speed sensor was wired to the V360 through 120 feet of unshielded twisted-pair wire run outdoors, on the ground, between buildings.

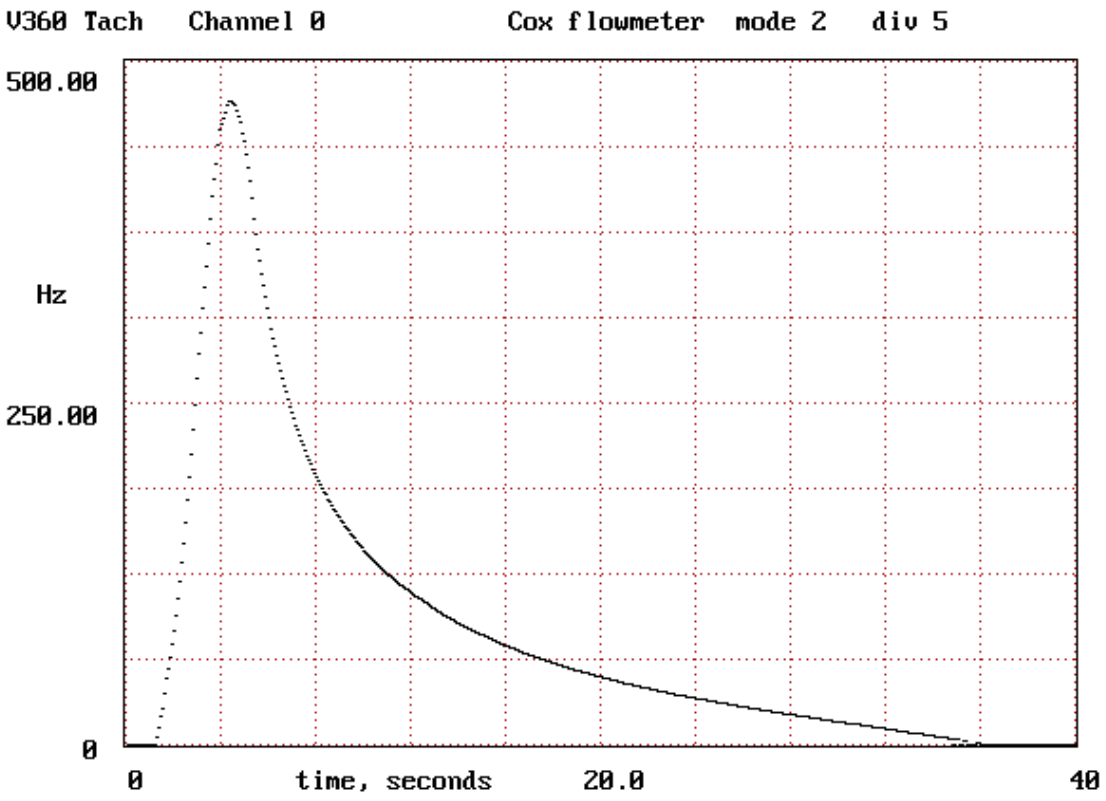


FIGURE 6. V360 FREQUENCY-TIME PLOT OF COX TURBINE-TYPE AIRCRAFT FUEL FLOW TRANSDUCER

A Cox aircraft fuel flow transducer was tested with a compressed air jet.

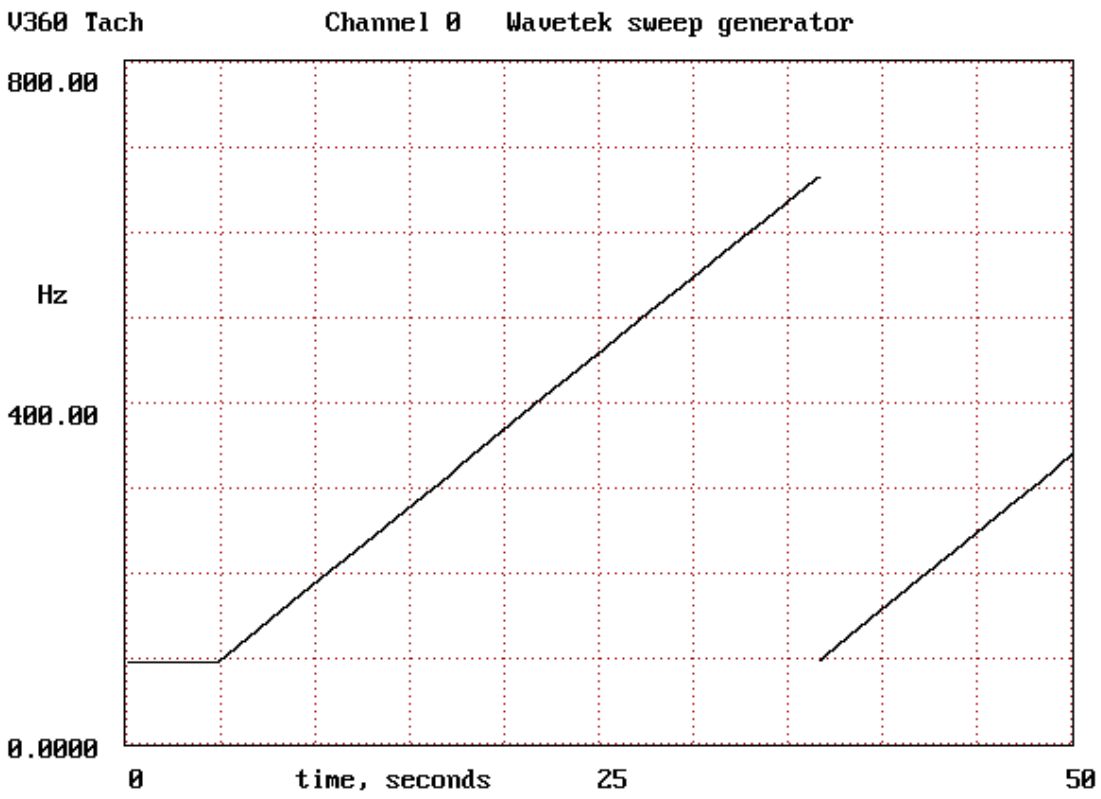


FIGURE 7. V360 FREQUENCY-TIME PLOT WITH WAVETEK SWEEP GENERATOR AS THE SIGNAL SOURCE

8 *Versions*

V360-1: 8-channel VME tachometer module

9 *Customization*

Consult factory for information about additional custom versions.

10 *Revision History*

10.1 *Hardware Revision History*

Revision C	January 2013 Functionally equivalent to Revision B
Revision B	November 1998
Revision A	October 1998 Initial Hardware Release

10.2 *Firmware Revision History*

Revision A	October 1998 22360A Initial Firmware Release

11 *Accessories*

J43-1: 3' BNC to BNC cable