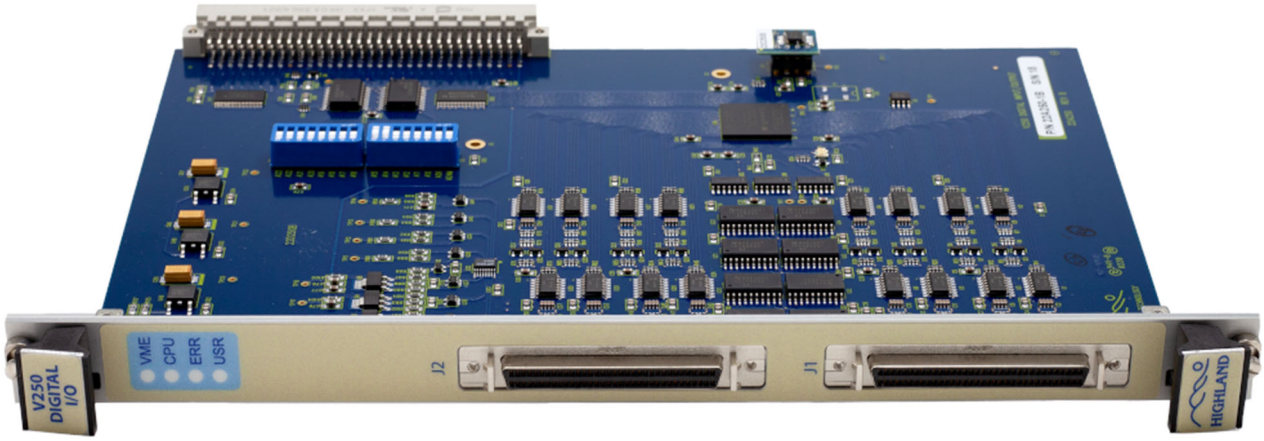
HIGHLAND TECHNOLOGY

V250

64-CHANNEL VME

DIGITAL I/O MODULE



Technical Manual

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Contents

1 *Introduction*

This is the manual for the V250, a 64 channel digital input/output VME module.

Features of the V250 include:

- 64 independent channels, each programmable as a digital input or output
- Open-drain outputs can sink loads up to 200 mA and 40 volts
- Inductive-load flyback clamping is included
- Logic-level inputs have programmable thresholds from 0 to +10 volts
- In/Out resistor pull-ups are programmable from 0 to +10 volts
- Programmable input debounce allows direct interface to switches and relay contacts
- Can directly drive LEDs, SSRs, and FET gates
- Clearly labeled dipswitches set VME address; no jumpers, headers, or trimpots

2 *Specifications*

FUNCTION	64-channel digital input/output module
DEVICE TYPE	16-bit VME register-based slave: A24:A16:D16; Implements 256 16-bit registers at switch selectable addresses in the VME 16 or 24 bit addressing spaces
OPEN-DRAIN OUTPUTS	Closure to ground, 200 mA max, 40 volts max, 2 Ω typical on resistance Internal Zener clamp outputs to +45 volts nom. See section 5.4
LOGIC INPUTS	Inputs grouped into four banks of 16 channels. Each bank has programmable threshold of 0 to +10V Nominal 200KΩ impedance to ground, 40V max, 100 µs time constant hardware filtering
PULL-UPS	1 KΩ, each bank has programmable pull-up voltage of 0 to +10 V
DIGITAL DEBOUNCE	Programmable per channel: off, 1 ms, 10 ms, 100 ms
OPERATING TEMPERATURE	0 to 60°C; extended MIL/COTS ranges available
STORAGE TEMPERATURE	-40 to 70°C
CALIBRATION INTERVAL	Two years
POWER	Standard VME supplies: + 5 volts, 0.8 amp. max + 12 volts, 0.75 amp. max - 12 volts, 0.75 amp max
CONNECTORS	P1 VME connector Two 68-pin SCSI females, each 32 channels

INDICATORS	LEDs indicate VME access, CPU activity, error conditions Additional LED is user programmable
PACKAGING	6U single-wide VME module
CONFORMANCE	ANSI/VITA 1-1994 (R2002) VMEbus spec

3 *Overview*

The V250 provides 64-non-isolated digital input/output pins, each with a dedicated ground pin. The equivalent circuit of each pin driver is as follows:

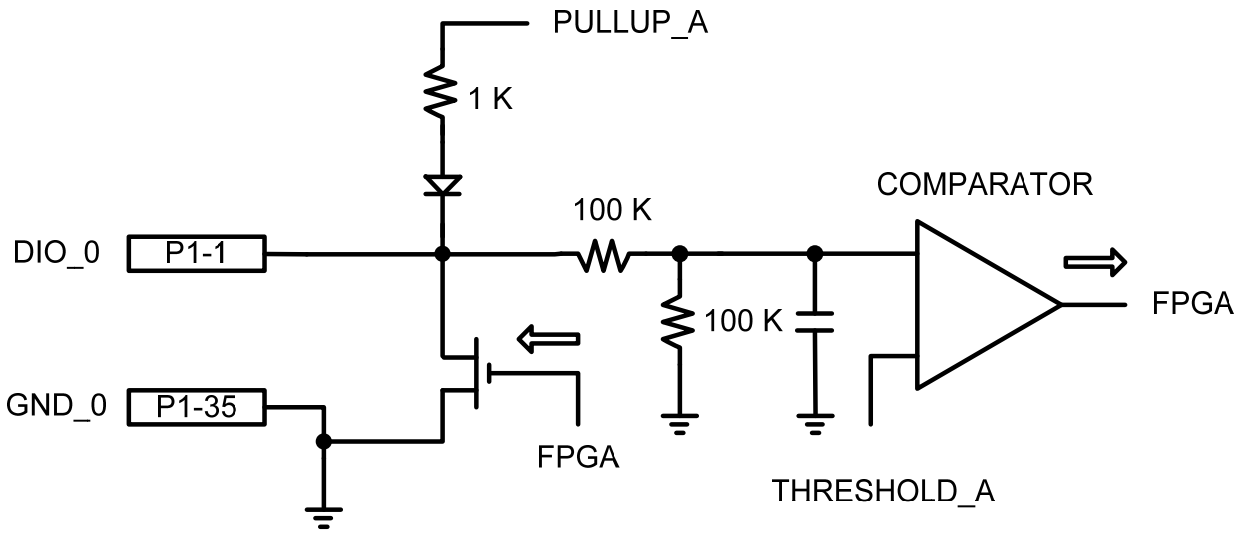

Figure 1: V250 Digital Input/Output Channel

The 64 channels are divided into four banks, called A, B, C and D; each bank consists of 16 channels.

Shared programmable pull-ups and input thresholds are available on each bank, each programmable from 0 to +10 V.

The open-drain drivers can each sink up to 200 mA and withstand up to +40 volts. ON resistance to ground is nominally 2 Ω. The drivers include flyback clamps which conduct at nominally +45 volts. The output drivers are TI part number TPIC6595DW; refer to the TI data sheet for details.

The input RC time constant is nominally 100 microseconds. Users can select downstream digital debouncing with delay of 1ms, 10 ms, or 100 ms.

An FPGA manages the interface between the I/O channels and the VME bus.

⚠ **CAUTION: If each driver sinks its maximum 200 mA, total ground return current can be 12.8 amps. It is strongly recommended that each I/O pin have a dedicated ground return connection to share this current.**

⚠ **CAUTION: Inductive flyback energy must be limited. See section 5.4.**

4 *Connectors and Installation*

4.1 *Address DIP Switches*

The V250 appears as 256 16-bit registers (512 bytes) in the VME 16 or 24-bit addressing spaces. The base address of the 256 registers is set by dip switches.

Two rocker-type dipswitches are provided near the top edge of the board. They are labeled, “A23" through "A09" and finally "A24M".

To set a switch to the logical "1" or "ON" position, press down the side of the switch nearest its "Axx" lettering. Use a toothpick or paper clip, not a pen or pencil.

The A24M switch, when set, allows the board to operate in the VME 24-bit (A24) address space; in this case, all address switches are active and the board responds to VME address modifier codes 0x39 and 0x3D.

If the A24M switch is off, the module resides in the A16 space and responds to address modifiers 0x29 and 0x2D. In this case, only address switches A15 through A9 are active.

Units are shipped with switches A15 and A14 on, all others off, locating the register base at 0xC000 in the A16 space.

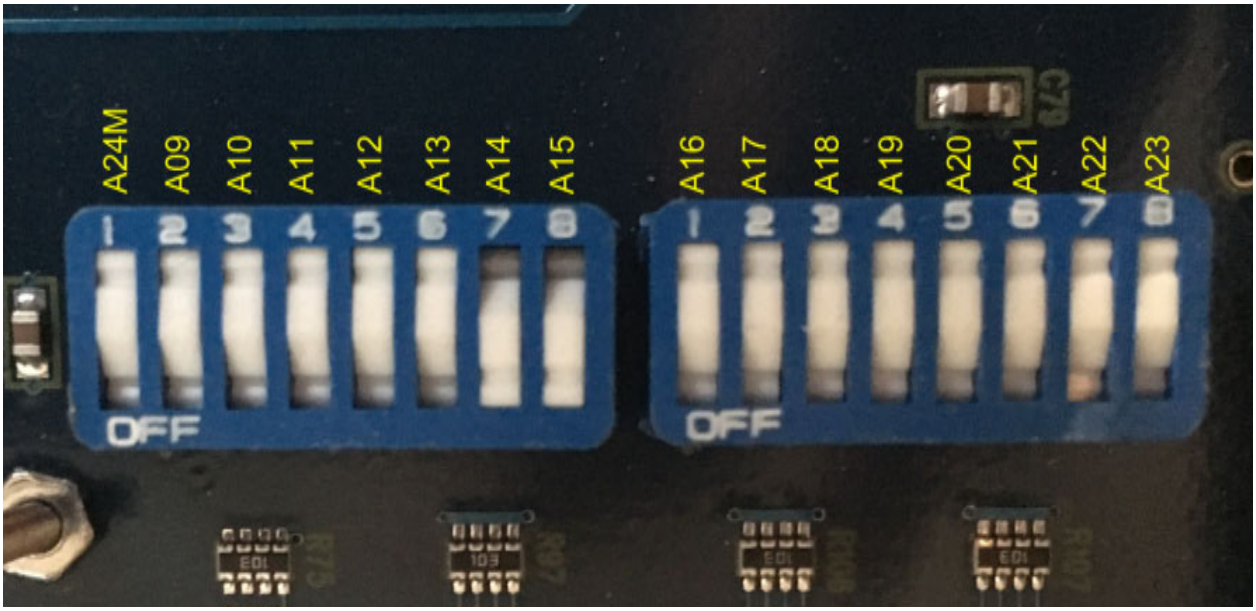

Figure 2: Address DIP Switch

4.2 *Installation*

The V250 may be installed in any standard 6U VME crate, including VME64 variants. It supports 16-bit data transfers using the P1 connector.

The V250 passes all interrupt and bus grant signals, and may be used with backplane grant jumpers installed or not installed.

CAUTION: Do not install or remove the V250 with crate power on. VME modules are not hot-pluggable. The V250 will be damaged if hot-plugged.

CAUTION: Fully seat the module and secure front-panel screws before applying power.

CAUTION: Handle the V250 with proper ESD precautions to avoid static damage.

4.3 *SCSI-68 Input Connectors*

Two front-panel female 68-pin SCSI connectors are provided. Pin out is as follows:

Channel	Connector	DIO Pin	GND Pin	Bank
0	J1	1	35	A
1	J1	2	36	A
2	J1	3	37	A
3	J1	4	38	A
4	J1	5	39	A
5	J1	6	40	A
6	J1	7	41	A
7	J1	8	42	A
8	J1	9	43	A
9	J1	10	44	A
10	J1	11	45	A
11	J1	12	46	A
12	J1	13	47	A
13	J1	14	48	A
14	J1	15	49	A
15	J1	16	50	A
16	J1	19	53	B

17	J1	20	54	B
18	J1	21	55	B
19	J1	22	56	B
20	J1	23	57	B
21	J1	24	58	B
22	J1	25	59	B
23	J1	26	60	B
24	J1	27	61	B
25	J1	28	62	B
26	J1	29	63	B
27	J1	30	64	B
28	J1	31	65	B
29	J1	32	66	B
30	J1	33	67	B
31	J1	34	68	B
-	J1	-	17	-
-	J1	-	18	-
-	J1	-	51	-
-	J1	-	52	-
32	J2	1	35	C
33	J2	2	36	C
34	J2	3	37	C
35	J2	4	38	C
36	J2	5	39	C
37	J2	6	40	C
38	J2	7	41	C
39	J2	8	42	C
40	J2	9	43	C
41	J2	10	44	C
42	J2	11	45	C
43	J2	12	46	C
44	J2	13	47	C
45	J2	14	48	C
46	J2	15	49	C
47	J2	16	50	C
48	J2	19	53	D
49	J2	20	54	D
50	J2	21	55	D
51	J2	22	56	D
52	J2	23	57	D
53	J2	24	58	D
54	J2	25	59	D

55	J2	26	60	D
56	J2	27	61	D
57	J2	28	62	D
58	J2	29	63	D
59	J2	30	64	D
60	J2	31	65	D
64	J2	32	66	D
62	J2	33	67	D
63	J2	34	68	D
-	J2	-	17	-
-	J2	-	18	-
-	J2	-	51	-
-	J2	-	52	-

The GND pins listed above are PCB/VME backplane grounds. Connector shells are bonded to the VME front panel, which connects to the crate frame through the module securing screws.

Highland can furnish SCSI cable assemblies and screw-type termination panels. See Section 10.

5 *Operation*

5.1 *LEDs*

There are 4 front-panel LED indicators: VME, CPU, ERR and USR.

The blue VME LED flashes whenever the module is accessed from the VME bus.

The green CPU LED flashes about once a second to indicate FPGA activity.

The red ERR LED will flash to indicate errors.

The orange USR LED displays a user-defined blink pattern. See section 6.4

There is an additional LED on the PCB surface which illuminates green when the FPGA is properly configured.

5.2 *Power up Defaults*

At power up the module setup will be:

Setting	Value
Channel Mode	input
Threshold	+2 v
Pull-ups	0 v
Debounce	10 ms
User LED	off

The red ERR LED will be on at power up, and will go off when the FPGA is properly initialized and operating.

Users can immediately read input TTL logic levels in the RDATA through RDATD real-time data registers.

The power up sequence takes about 2 seconds.

5.3 *Quick Start Procedure*

Basic operation of the V250 can be demonstrated by the following steps:

A 6U VME crate and computer interface is required. The crate must be compliant with the IEEE 1014 VME specification, or the equivalent ANSI/VITA 1-1994 (R2002) VMEbus spec. Any crate with the standard power supplies (+12, +5, -12) and the 16-bit "P1" bus is adequate.

The computer interface must allow, as a minimum, reading and writing 16-bit registers in the A16 or A24 address spaces.

Pick an address space and module base address and set the V250 dip switches accordingly. See section 4.1. The as-shipped default is address 0xC000 in the 16-bit address space.

With crate power off, insert the V250 into any crate slot and firmly secure its mounting screws. **Do not hot-plug VME modules.**

Power up the crate. After a few seconds, the V250 green "CPU" LED should flash, and the other LEDs should be off.

Now run software that can display the contents of VME registers.

Read the manufacturer ID register, the 16-bit VME register at the module base address. The default address would be 0xC000. The blue "VME" LED should flash, and the register value should be 0xFEEE, identifying this as a Highland VME module.

Read the next register, offset address 2, default 0xC002. It should read 22250 decimal, 0x56EA, identifying the module as a V250.

All 64 I/O pins are now configured as logic-level inputs with +2 V thresholds and no pullups. Bits in the RDATA-RDATD (real-time data) and DDATA-DDATD (debounced data) registers will reflect the high/low levels on each pin. With no connections to these pins, all the RDAT and DDAT register bits should be low.

To change the logic level pullup voltages, write to the four PUPx registers. Each controls the pullup voltage for 16 channels.

To change the logic-input thresholds, write to the four THRx registers. Each sets the input threshold for 16 channels.

To set a pin to be an output, set the M0 bit (lsb) of its channel control register. After that, writing a "1" to the appropriate KDAT bit will turn on the pin's power mosfet, grounding the pin.

5.4 *Output Limitations*

The V250 uses one TPIC6595DW power driver chip to drive each group of eight outputs. One chip services channels 0 to 7, one services 8 to 15, etc.

Each driver is an n-channel power mosfet with a flyback clamp circuit that turns on at about +45 volts, sinking any inductive flyback current to ground. This protects the driver from overvoltage damage, but power is dissipated by the clamping action.

If an inductive load, like a relay coil, is connected with one end to some external V+ power supply, and the other end to a V250 I/O pin, the V250 output can be set ON, which will ground the low side of the coil.

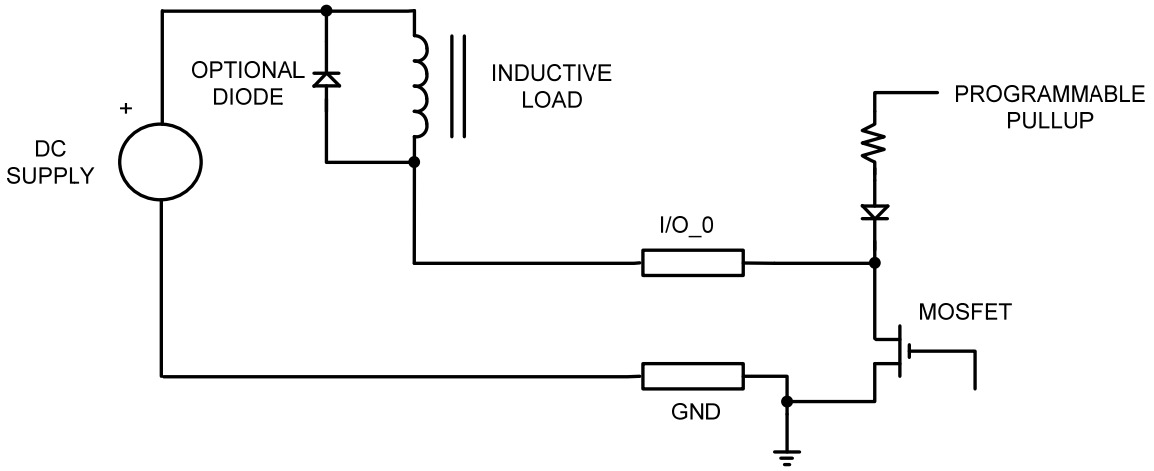

Figure 3: Clamp circuit configuration

The programmable pull-up would normally be set to zero volts, but a pull-up will generally not interfere with driving an external load in this configuration.

Let L be the coil inductance, in Henries.

R be the coil resistance, in Ω.

V be the DC supply voltage, +40 volts max.

The steady-state operating current of the load is I = V/R amps, which must be limited to 0.2 A or 200 mA.

Assuming that no external clamp diode is provided, every time the driver turns off, the inductive flyback will briefly spike to about +45 volts, where it is clamped within the driver chip. The energy dissipated in the chip, per event, is

$$E = 0.5 \times L \times I^2 \; Joules$$

which must not exceed 0.075 J.

If then on/off event repeat periodically at frequency F, the average power dissipation of the flyback clamp circuit is

$$P = F \times E$$

$$P = F \times 0.5 \times L \times I^2$$

which must be limited to a maximum of 0.8 watts for the entire 8-channel driver chip.

One advantage of not using the external diode is that the stored energy in the inductance is dissipated very quickly by the high voltage clamp, which provides fast dropout for relay coils.

If the above flyback energy or power limits might be exceeded, it is recommended that an external flyback diode be connected across inductive loads, so that the +45 volt clamp internal to the driver is not engaged. An external diode will also reduce EMI and potential coupling of flyback spikes and ringing into nearby wiring.

Each output can sink up to 400 mA provided that the total sink current of all eight drivers in one chip does not exceed 2 A.

The threshold can be set to 0 V, making the corresponding inputs into zero-crossing detectors. This can be useful in some situations, but note that the mosfet output drivers have substrate diodes to ground, preventing inputs from being pulled more negative than about -0.7 volts. No more than -50mA should be allowed to flow into an I/O pin if it’s driven below ground.

6 *VME Registers*

The V250 implements 256 16-bit VME registers. REG# in the table below is the ordinal register number in decimal; OFFSET is the hex VMEbus offset from the module base address.

Registers identified as “RO” are read-only and should not be written from VME.

Read-write (RW) registers are written and read back by VME and, after power-up initialization, are not altered by the internal logic.

6.1 *VME Register Map*

Reg Name	REG#	Offset	R/W	Function
VXI MFR	0	0x00	RO	Highland ID: reads 65262, xFEEE
VXI TYPE	1	0x02	RO	V250 module ID, 22250, 0x56EA
SERIAL	3	0x06	RO	unit serial number
ROM ID	4	0x08	RO	FPGA ID, typically 22250 decimal
ROM REV	5	0x0A	RO	FPGA revision, typically ASCII "A"
MCOUNT	6	0x0C	RO	1 KHz real-time counter
DASH	7	0x0E	RO	module version (dash) number
ULED	12	0x18	RW	user LED control
MACRO	14	0x1C	RW	Macro control register
PARAM0	16	0x20	RW	Macro parameter
PARAM1	17	0x22	RW	Macro parameter
PARAM2	18	0x24	RW	Macro parameter
PARAM3	19	0x26	RW	Macro parameter
RDATA	32	0x40	RO	channels 0 - 15 real-time input
RDATA	33	0x42	RO	channels 16 - 31 real-time input
RDATC	34	0x44	RO	channels 32 - 47 real-time input
RDATD	35	0x46	RO	channels 48 - 63 real-time input
DDATA	36	0x48	RO	channels 0 - 15 debounced input

Reg Name	REG#	Offset	R/W	Function
DDATB	37	0x4A	RO	channels 16 - 31 debounced input
DDATC	38	0x4C	RO	channels 32 - 47 debounced input
DDATD	39	0x4E	RO	channels 48 - 63 debounced input
KDATA	40	0x50	RW	channels 0 - 15 output drive
KDATB	41	0x52	RW	channels 16 - 31 output drive
KDATC	42	0x54	RW	channels 32 - 47 output drive
KDATD	43	0x56	RW	channels 48 - 63 output drive
THRA	48	0x60	RW	Bank A input comparator threshold
THRB	49	0x62	RW	Bank B input comparator threshold
THRC	50	0x64	RW	Bank C input comparator threshold
THRD	51	0x66	RW	Bank D input comparator threshold
PUPA	52	0x68	RW	Bank A output pullup voltage
PUPB	53	0x6A	RW	Bank B output pullup voltage
PUPC	54	0x6C	RW	Bank C output pullup voltage
PUPD	55	0x6E	RW	Bank D output pullup voltage
CTL0	64	0x80	RW	channel 0 control
CTL1	65	0x82	RW	channel 1 control
...				
CTLn	64+n		RW	channel n control
...				
CTL62	126	0xFC	RW	channel 62 control
CTL63	127	0xFE	RW	channel 63 control
BUFFER0	128	0x100	RW	
...				
BUFFERn	128+n		RW	
…				
BUFFER127	256	0x17F	RW	

6.2 *Register Descriptions*

6.2.1 *Module Overhead Registers*

There are a number of read-only overhead registers are provided.

VXI MFR Always reads 0xFEEE, which is Highland's registered VXI module ID code.

VXI TYPE Always reads 0x56EA or 22250 in decimal which identifies as a V250 module.

SERIAL The module serial number

ROM ID Always reads 0x56EA or 22250 which is the FPGA code version

ROM REV ASCII code identifying the revision letter of the FPGA code, typically 0x0041, ascii "A"

MCOUNT A 16-bit counter that is incremented by the internal logic at 1KHz.

DASH The module version (dash) number.

6.2.2 *User Led Control Register (ULED)*

This register controls the orange user LED. The ULED register allows user flashing patterns to be loaded. An internal shift register is periodically loaded with the contents of the ULED register and the MS bit of this register operates the orange LED. The shift register is updated every 125 milliseconds, and the register is reloaded every 16 shifts or every 2 seconds.

ULED pattern 0x0000 turns the orange user LED off. Pattern 0xFFFF turns it steady on.

6.2.3 *MACRO and PARAMn Registers*

The MACRO and PARAMn registers are used to invoke special module operations. These registers are not user defined and are reserved for factory use only.

6.2.4 *Channel Real-Time Data Registers (RDATx)*

There are four “real-time” input registers:

RDATA

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0

RDATB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R31	R30	R29	R28	R27	R26	R25	R24	R23	R22	R21	R20	R19	R18	R17	R16

RDATC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R47	R46	R45	R44	R43	R42	R41	R40	R39	R38	R37	R36	R35	R34	R33	R32

RDATD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R63	R62	R61	R60	R59	R58	R57	R56	R55	R54	R53	R52	R51	R50	R49	R48

These registers reflect the states of the 64 input pins. If the voltage on input channel “n” is above its programmed threshold, the associated “Rn” bit will be set. These bits are not affected by the digital debounce settings.

The RDATx bits are functional in both input and output modes. This allows for self-test of the V250.

6.2.5 *Channel Debounced Data Registers (DDATx)*

There are four “debounced” input registers:

DDATA

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

DDATB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16

DDATC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D47	D46	D45	D44	D43	D42	D41	D40	D39	D38	D37	D36	D35	D34	D33	D32

DDATD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D63	D62	D61	D60	D59	D58	D57	D56	D55	D54	D53	D52	D51	D50	D49	D48

These registers represent the states of the 64 input pins as processed through the programmable debounce logic. If a channel's debounce selection is 0, its "Dn" bit will be identical to its real-time "Rn" bit.

The DDATx bits are functional in both input and output modes. This allows for self-test of the V250.

6.2.6 *Channel Output Data Registers (KDATx)*

There are four channel output registers:

KDATA

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
K15	K14	K13	K12	K11	K10	K9	K8	K7	K6	K5	K4	K3	K2	K1	K0

KDATB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
K31	K30	K29	K28	K27	K26	K25	K24	K23	K22	K21	K20	K19	K18	K17	K16

KDATC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
K47	K46	K45	K44	K43	K42	K41	K40	K39	K38	K37	K36	K35	K34	K33	K32

KDATD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
K63	K62	K61	K60	K59	K58	K57	K56	K55	K54	K53	K52	K51	K50	K49	K48

These registers control the open-drain output drivers of the 64 channels. They are only active for channel configured as outputs (see CTLn registers, section 6.2.9). Setting a “Kn” bit turns on the corresponding channel driver, pulling it to ground. Cleaning the bit shuts off the driver.

6.2.7 *Threshold Registers (THRx)*

These registers set the threshold voltages for the logic-level inputs. Each controls a bank of 16 inputs.

THRA Sets threshold for, bank A, channels 0 to 15.

THRB Sets threshold for, bank B, channels 16 to 31.

THRC Sets threshold for, bank C, channels 32 to 47.

THRD Sets threshold for, bank D, channels 48 to 63.

The data is an unsigned integer in which the LSB of the register represents 1 mV. The acceptable range of values is from 0 (0 V) to 10000 (+10 V). A value outside the limit will cause the threshold voltage to clip at +10V.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TH14	TH13	TH12	TH11	TH10	TH9	TH8	TH7	TH6	TH5	TH4	TH3	TH2	TH1	TH0

6.2.8 *Pull-up Registers (PUPx)*

These registers set the pull-up voltages for the I/O channels. Each controls a bank of 16 channels.

PUPA Sets pull-up voltage for, bank A, channels 0 to 15.

PUPB Sets pull-up voltage for, bank B, channels 16 to 31.

PUPC Sets pull-up voltage for, bank C, channels 32 to 47.

PUPD Sets pull-up voltage for, bank D, channels 48 to 63.

The data is an unsigned integer in which the LSB of the register represents 1 mV. The acceptable range of integer values is from 0 (0 volts) to 10000 (+10 V). A value outside the limit will cause the threshold voltage to clip at +10V.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PU14	PU13	PU12	PU11	PU10	PU9	PU8	PU7	PU6	PU5	PU4	PU3	PU2	PU1	PU0

As shown in Figure 1 in section 3, inputs are connected to their bank pull-up bus through a 1 KΩ resistor and a series diode. A programmed value of zero effectively removes pull-up capability. If the register is set to a non-zero value, on-board logic sets the pull-up bus voltage to the requested value plus 0.6 volts, to correct for nominal diode drop.

6.2.9 *Channel Control Registers (CTLn)*

Each of the 64 I/O channels has a control register. This registers range from CTL0 to CTL63. These registers control mode (input/output) and debounce time for each channel.

CTLn

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
										F1	F0				M0

M0 is the Mode bit. When this bit is cleared, the channel operates in input mode, and the open-drain output driver is disabled. When this bit is set the channel operates in output mode and the open-drain output drivers can be controlled by the KDATx registers.

The Fn bits select the timing of the input debounce filter. Options are:

Fn Codes	Debounce Time
0	No debounce (100 us input RC from board hardware)
1	1 ms debounce
2	10 ms debounce
3	100 ms debounce

6.2.10 *Buffer Registers (BUFFn)*

The BUFFn registers are for internal use of Highland Technology. These registers are not user defined and are reserved for factory use only.

7 Versions

V250-1: 64-channel VME digital input/output module

8 Customization

Consult factory for information about additional custom versions.

9 Hardware and Firmware Revision History

9.1 Hardware Revision History

22A250-1A	Initial PCB release
22A250-1B	Improved manufacturability Functionality equivalent to Rev. A

9.2 Firmware Revision History

22C250 Rev A	Initial FPGA release
22C250 Rev B	FPGA for Rev. B Fixes a bug with the red ERR LED

10 *Accessories*

J58-1: 3′ 68 pin male SCSI to 68 pin male SCSI

V232-1: 68-pin female SCSI connector to 96-pin female DIN connector adapter cable

V233-1: 32-channel SCSI termination panel