HIGHLAND TECHNOLOGY

T680
5-CHANNEL ETHERNET TIME INTERVAL COUNTER

Technical Manual

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1. Introduction

This is the technical manual for the Highland Model T680 Ethernet Time Interval Counter.

Features of the T680 include:

- Five-channel time-interval counter and time stamper
- Five channels usable as TIC start plus four stops, or five time stampers
- 12.2 picoseconds resolution with 48-bit (3236 second) range
- Common GATE input
- 1023 sample FIFO per channel
- External universal power supply or 12-volt DC power
- 100 Mbit Ethernet and USB interfaces
- Compact extruded enclosure with optional mounting flange

Custom versions can include DRAM and perform internal histogramming or accumulate array data for applications like fluorescent decay and 2D delay line imaging.

2. Specifications

Specifications are typical unless otherwise noted.

FUNCTION	5-channel time interval counter/time stamper
TRIGGER INPUTS	Rising-edge trigger, 50 Ω input impedance, DC coupled Threshold is programmable from -2.5 to +2.5 volts Max safe input is ± 3.3 volts
TIME RESOLUTION	12.207031 ps LSB (12.5ns/1024) 48 bit range, 3435.97 seconds
DEAD TIME	100 ns max
GATE INPUT	50 ohms, 2 volt minimum, active high
CLOCK	Internal 10 MHz, available as TTL output Lockable to external 10 MHz ±10 PPM reference, 1 volt p-p min
JITTER	< 50 ps typical, <75 ps max RMS for time intervals below 1ms < 10 ns/second for longer measurements using internal clock
RELATIVE CHANNEL ACCURACY	< 100 ps channel to channel
CONTROL	10/100 Ethernet and USB
POWER	+12 volts at 500 mA, nominal Highland Model J12 12 volt power supply furnished
CALIBRATION INTERVAL	One year
CONNECTORS	Ch 0-4, GATE, CLOCK: SMB RJ45 Ethernet Micro/AB for USB control 2.5 mm barrel for power, center positive

LED INDICATORS	Green POWER Blue TRIGGER Orange COMM
PACKAGING	Extruded anodized aluminum enclosure

Operation

2.1. Channel Architecture

The T680 has a master 38-bit counter called MC. MC is clocked at 80 MHz from an internal crystal oscillator.

Each channel 0-4 has an input comparator which recognizes the rising edge of incoming triggers. At trigger time, MC is frozen into a latch, forming the 38 MS bits of a time stamp. An interpolation circuit appends 10 LSBs to each time stamp, making the stamp the equivalent of a snapshot of a 48-bit free-running counter being clocked at 81.920 GHz.

Each channel has a 1023-entry FIFO memory which stores time stamps.

Channel 0 always reports latched MC time stamps. Channels 1 through 4 can be programmed to report latched MC time stamps, or can be programmed to report times relative to channel 0 triggers. The five channels can be used as independent time stampers, or channel 0 can be considered to be the "start" trigger, with channels 1-4 being timed "stop" events.

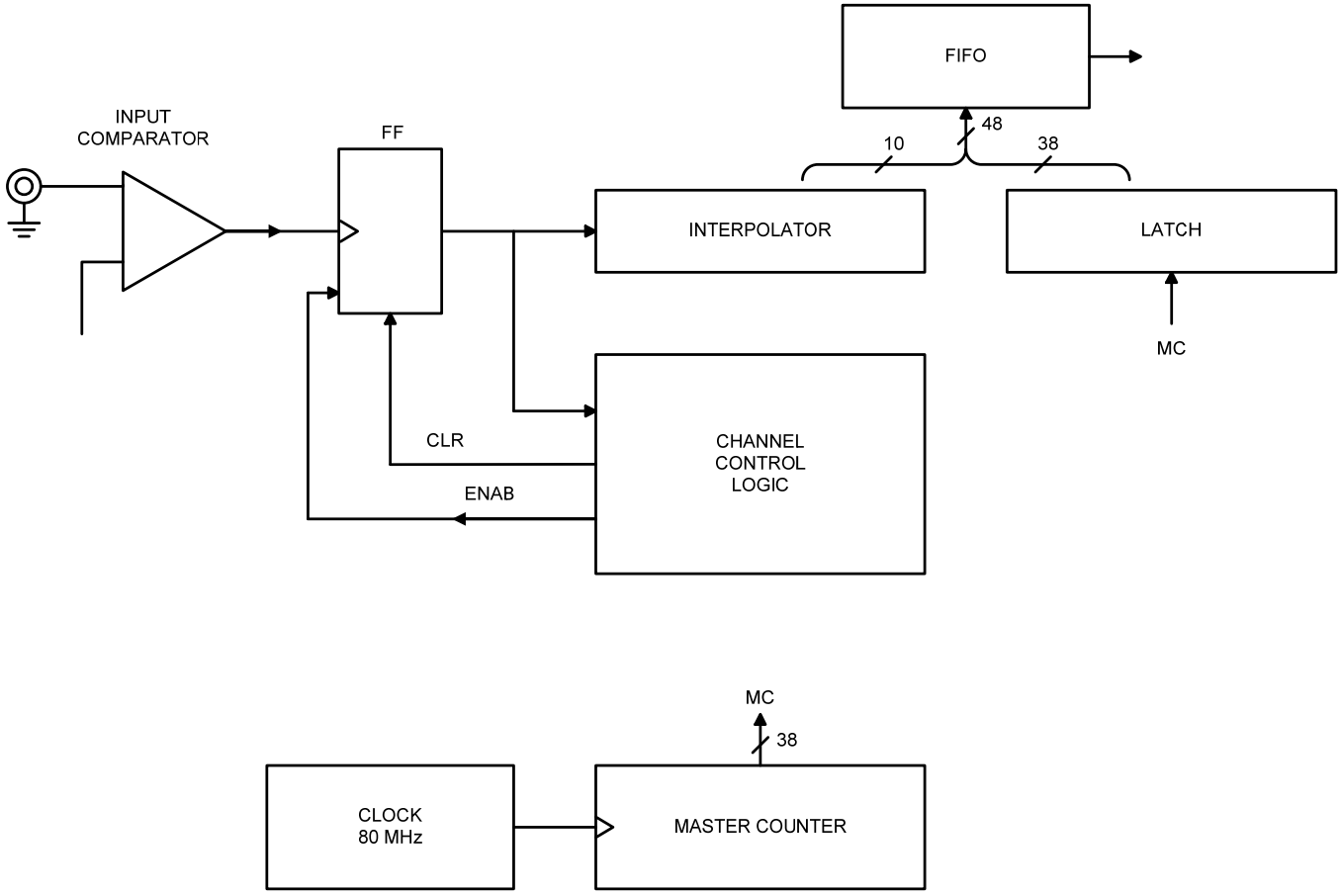
A GATE input is provided. Each channel can be programmed to be enabled, disabled, or can use various gate modes to enable trigger recognition.

Operation is supervised by an ARM microprocessor.

The overall block diagram of the T680 is shown below:

BLOCK DIAGRAM
CONFIDENTIAL PROPRIETARY INFORMATION
COPYRIGHT © 2012 HIGHLAND TECHNOLOGY
ENGINEERING CHANGE ORDERS MAY APPLY
ENGINEER J LARKIN DATE 8/27/12
DRAWN L LARKIN DATE 8/27/12
CHECKED
APPROVED
RELEASED
HIGHLAND TECHNOLOGY INC.
SCHEMATIC, T680
ETHERNET TDC
DRAWING NO. 28S681
REV: A
SHEET: 1 OF 16
+7.5
+5
+3.3
+1.8
+1.2
-5
POWER SUPPLY
+12V
DACS
FTDI
MICRO A/B USB
USB
PHY
RJ45
ETHERNET
CAL FLASH
PGM FLASH
ARM CPU
TEMP SENSOR
JTAG
JTAG
50
OPTIONAL DRAM
CLOCK OSC
CLOCK I/O
LEDS
FPGA
CLOCK
TIME STAMPER
10
3
TRG LVL 0
TRG LVL 1/4
EN
TRG LVL GATE
IN 0
IN 1
IN 2
IN 3
IN 4
GATE I/O

The logic associated with one channel is as follows:



The channel control logic manages arming and reset of the trigger-recognition flip-flop. Each channel has independent gating logic and a dedicated holdoff timer to prevent accidental double-triggering.

Channels can report timestamps in either absolute or relative timing modes. Absolute time is relative to the power-up of the T680, this is generally not useful in and of itself, but allows the end user of the data to work with the data without having to second-guess any internal math performed by the T680. In relative time mode (only available for channels 1-4), the reported time is relative to the last timestamp on channel 0. This is computed by subtracting the latest channel 0 time stamp from the channel 1-4 stamp, using a 48-bit 2's complement subtraction. Channel 0 hits are always reported in MC-absolute units.

Due to inherent ambiguities in timestamping, if channels 1-4 are in REL mode, and triggers arrive near to a trigger on channel 0, these timestamps may be registered as either large positive numbers relative to the earlier channel 0 timestamp, or as small negative numbers relative to the next timestamp. To avoid this, Highland recommends that REL mode only be used with the LINKED gating mode, as described in section 2.5.

2.2. FIFOs and STAMPs

The channels FIFOs are 1023 elements deep, with some additional storage in the channel logic. The channel logic is responsible for generating the STAMP information as well; the latest timestamp recorded on that channel.

In the event that the FIFOs are allowed to overflow, the oldest data will be kept and the newest discarded. The channel logic, however, will have kept running the entire time so as to keep updating the STAMP. Therefore, assuming the FIFOs have not overflowed, the data in them will represent all the accepted triggers with the last data element in them being the same as that channel's STAMP. If they overflow, however, the STAMP data will flow into the FIFO as the older data is unloaded, and so the data will have a gap where the overflow occurred.

Clearing the FIFOs also clears the backlogged STAMP data.

2.3. Controlling a Channel

There are several controls associated with each channel. The first is the analog threshold level used to recognize a pulse. T680 channels are triggered only by rising edges, i.e. the voltage on the connector is becoming more positive. The threshold level can be adjusted in the range of -2.5 to +2.5 volts, allowing for signal levels as diverse as NIM, NECL, and TTL, but regardless of whether the threshold is negative or positive it is the rising edge that will trigger timestamping in the T680. The threshold voltage is programmed using the `TRIG` command, see section 4.6.1 for details.

A pulse rising through the threshold voltage has the potential to cause a timestamp to be captured, assuming that the channel is currently enabled. This is a function of the channel gating mode, set using the `CHAN` command as described in section 4.6.2.

M	Name	Description
0	OFF	No triggers are accepted. The channel holdoff counter is cleared.
1	ON	Triggers are accepted, timestamped, and the resulting timestamp is loaded into the channel FIFO memory. Timestamps represent the value of MC at the instant of trigger. The channel ignores additional triggers until the channel holdoff time expires.
2	GATED	Like mode 1, but triggers are enabled by a (TTL) logic high on the external GATE input.
3	LINKED	This mode is available only for channels 1-4. Channels are enabled by the fact that the holdoff timer for channel 0 is running. This makes channel 0 the device master, and creates a window of time relative to channel 0 that gates the other channels.

Assuming that the channel is enabled, this will cause a timestamp to be captured on this channel, and begin running the channel holdoff timer. The holdoff timer prevents accidentally capturing multiple timestamps due to noise on signal edges by enforcing a minimum time between timestamps. Subsequent rising edges inside of the holdoff window will be ignored; they neither generate a new timestamp nor cause the holdoff timer to restart. Thus, a 1 MHz square wave connected to a channel with a 4.5 µs holdoff will emit timestamps every 5 µs. The holdoff time is set using the `HOLD` command, described in section 4.6.4.

The holdoff timer of channel 0 is a special case; in addition to acting as the channel 0 holdoff it can also be used as the gating signal for channels 1-4 by setting them to use the LINKED gating mode. See Section 2.5 for more information on channel linking.

For channels 1-4, the stamped time can be registered in absolute time or relative to the most recent timestamp on channel 0, by setting the REL bit in the channel control register. There being nothing for channel 0 to be relative to, it can only run in absolute time mode. The REL bit is set using the `CHAN` command as described in section 4.6.2.

2.4. Independent Time Stamping

The most general operating scenario is to disable all the channels, clear all the FIFOs, enable all the channels, in ON or GATED mode with the REL bits off. Then turn the channels OFF if an experiment is known to be over

Read the channel FIFO counts, and unload FIFO data. The STAMP command can be also used to read just the latest, non-FIFO timestamp data.

The resulting data will present the interpolated values of MC at the instant of all triggers received on all enabled channels. User software will then be responsible for interpreting the meaning of these time stamps in the experimental context.

2.5. Relative Time Stamping

A common timestamper application is measuring events relative to a common start time. The T680 contains dedicated logic for this, using channel 0 as the start time signal. In this mode, generally the other channels should be configured to use the LINKED gating mode and relative time stamping. The channel 0 holdoff timer should be set to be somewhat less than the minimum repetition period.

For example, assume a time-of-flight mass spectrometry system, with ion emission triggered every 200 µs, and a maximum expected TOF of 100 µs. First, turn off all the channels, then clear all the FIFOs. Set channel 1 (the detection plate) to LINKED mode, with relative time stamps and the minimum holdoff time of 37.5 ns. It will not acquire any data yet because its gate (the channel 0 holdoff timer) is not active. Next set the channel 0 (the trigger) holdoff time to 180 µs, and set the mode to ON.

This will start data streaming into the channel 1 FIFO, which will capture a series of increasing timestamps as the different weights of molecules hit the detector. After a few of these ascending timestamps, the next timestamp will drop back to a lower number, nearly the same as the first one. This represents the end of the data from the first trigger and the start of the second. The timestamps will track the original sequence and then repeat again. This will continue for as long as channel 0 receives triggers. The channel 0 FIFO will also be capturing data, the absolute timestamps at which triggers occurred. This data can be fetched to confirm the frequency of triggers, but can also simply be ignored.

3. Connection and Operation

The standard T680-1 receives power from a Highland J12 wall-plug universal power supply or equivalent 12 volt source.

⚠ **The very high speed components of the T680 are sensitive to electrostatic damage. To maintain picosecond performance, no explicit ESD protection is included.**

⚠ **Discharge coaxial cables before connecting to the T680. Do not apply trigger inputs over ± 3.3 volts, and do not connect outputs to loads terminated at more than ± 3.3 volts.**

4. Remote Setup and Protocol

4.1. Ethernet Communications

The T680 provides simple line-delimited ASCII control commands over TCP/IP.

The firmware supports both static IP addressing and DHCP. A static IP address can be changed, using the IP command over Ethernet or through the USB port. The default IP address as shipped is 192.168.254.183 with a subnet mask of 255.255.255.000.

To use DHCP instead, use the IP command to set the IP address to 0.0.0.0. This will cause the T680 to query the network for a local DHCP server, and attempt to resolve the addressing issue itself. For DHCP servers that also support DNS resolution, the T680 will identify itself with a hostname of t680-nnnnn, where “nnnnn” is the serial number, zero-padded to five digits, e.g. t680-00123.

Communication is to a raw TCP socket on port 2000. Most telnet clients can connect to this with no further configuration; customers writing their own software can use basic line-oriented send and receive commands.

Note on TCP on firmware revisions A to G

The T680 uses a single TCP state machine. On firmware revisions A to G, if a remote client does not properly close the connection with the appropriate TCP control packet, or prompt the T680 to close the connection with the EXIT serial command, the T680’s TCP state will remain open to a connection that does not exist, thereby requiring a reboot before a user can connect to it again.

On firmware revision H, if a connected remote client does not send a serial command within ten seconds, the T680 will send TCP “keep-alive” packets to see if the connection is alive. (TCP keep-alive is managed at the transport layer, so if the remote client properly supports TCP, this should have no impact on the flow of higher-level data such as serial commands.) If the T680 does not receive replies to these packets, for example due to an unexpected reboot of the remote client, then the T680 will reset its TCP state, and the remote client will be able to reconnect without requiring the T680 to reboot.

4.2. USB Communications

The T680 enumerates as a USB serial port and uses the same ASCII communications protocol as Ethernet. USB and Ethernet operate concurrently. Most operating systems will recognize the FTDI FT230XS chip without additional drivers. The OS-side baud rate should be set to 115K.

4.3. Command Protocol

A command to the T680 is a line of text beginning with a keyword command followed by optional arguments, terminated with either a carriage return, linefeed, or CR+LF pair. Input is case insensitive and does not echo. Commas are ignored. In general, a command without an argument is a query. Any keyword can be truncated to its first two characters.

The T680 only transmits in immediate reply to a serial command. All replies are lines of text terminated by a CR+LF. Commands with arguments evoke the reply:

```
OK<cr><lf>
```

Or, to indicate an error:

```
Enn: message<cr><lf>
```

Numeric arguments are assumed decimal, but 0xnnnn is interpreted as hex.

Inquiry type commands evoke:

```
Requested_data<cr><lf>
```

Having finished processing the previous command (including a blank line, which is a null command), the T680 will provide a command prompt:

```
T680>
```

4.4. System Commands

4.4.1. IDENT

```
T680> IDENT
T680-1B SN 00001 Highland Technology Inc
```

Returns an identification string, with the unit identification, dash number, and serial number.

4.4.2. STATUS

```
T680> STATUS
T680-1B sn 00004 Highland Technology Inc

CH0 Trig +1.25 ON     ABS count 1021
CH1 Trig -1.35 ON     ABS count 102
CH2 Trig -1.35 LINKED REL count 0
CH3 Trig -1.35 GATE   ABS count 333
CH4 Trig -1.35 OFF    ABS count 1023

Clock IN trim 32910 LOCKED SIG Temp 31.5C

MC 123456789123 Uptime 418753

Host T680-0004  IP 192.168.254.185

Firmware 28E680-B  Cal date: 11/30/2012 OK
```

Returns a multi-line status report. The final OK indicates that the calibration table is valid.

4.4.3. CLOCK

```
T680> CLOCK IN
OK
T680> CLOCK
IN 12340 ERR SIG
T680> CLOCK
IN 12340 LOCK SIG
T680> CLOCK OUT
OK
T680> CLOCK
OUT 12340 NA NONE
```

Queries the status of the CLOCK system. Fields in the result are:

Field	Options	
1	IN	CLOCK IN mode
	OFF	CLOCK OFF mode
	OUT	CLOCK OUT mode
2	A number from 0-65,535 representing the current CLOCK TRIM value.	
3	LOCKED	In CLOCK IN mode, indicates PLL lock to an external 10 MHz signal.
	ERR	In CLOCK IN mode, indicates no PLL lock.
	NA	In CLOCK OUT or CLOCK OFF mode.
4	SIG	In CLOCK IN or CLOCK OFF mode, indicates external 10 MHz signal present.
	NONE	In CLOCK IN or CLOCK OFF mode, indicates external 10 MHz signal absent. This is always the result in CLOCK OUT mode.

4.4.4. CLOCK OUT

Sets the clock connector to OUT mode. CLOCK OUT drives the clock SMB connector with a 10 MHz TTL output. The clock runs in internal trimmed mode, according to the CLOCK TRIM command. The resulting output can be used to drive and lock other T680 units.

4.4.5. CLOCK IN

Sets the clock connector to IN mode. CLOCK IN attempts to lock the internal oscillator to a 10 MHz signal applied to the clock SMB connector from an external source.

4.4.6. CLOCK OFF

Sets the clock connector to be high impedance. The clock runs in internal trimmed mode.

4.4.7. CLOCK TRIM n

```
T680> CLOCK TRIM 40000
OK
T680> CLOCK
OFF 40000 NA NONE
```

Trims the internal clock frequency. The trim value is factory set but may be adjusted to correct for long-term aging of the oscillator. The value of n is 0 to 65,535, with 32,768 being the center of the adjust range, and higher values representing higher frequencies. Use the SAVE command to save this value to nonvolatile memory.

4.4.8. SAVE

Saves current channel settings, IP address, subnet mask, and the clock trim value in nonvolatile memory. Saved values will be restored on power-up.

4.4.9. TEMP

```
T680> TEMP
40.0
```

Returns the PCB surface temperature. Resolution is ½ degree C.

4.4.10. UPTIME

Returns the time since power-up, in seconds

4.4.11. HELP

Returns a brief command summary.

4.4.12. RESET

Reboots the T680.

4.5. Ethernet Commands

4.5.1. NETSTAT

```
T680> NETSTAT
HOSTNAME: T680-12345
MAC: 12-34-56-78-9A-BC
LINK: 10
IP: 192.168.254.35 (DHCP)
SUBNET: 255.255.255.0
```

Returns a summary status report of the current network conditions. Link may be 10, 100, or NONE. The parentheses after the IP address may hold DHCP or STATIC.

4.5.2. IP [a.b.c.d]

```
T680> IP 192.168.254.185
OK
T680> IP
192.168.254.185
T680> IP 0.0.0.0
OK
T680> IP
0.0.0.0
```

Sets or returns the requested IP address. Use an IP address of 0.0.0.0 to request dynamic allocation through DCHP. Use the SAVE command to save this in nonvolatile memory.

IP change requests take effect immediately. If the connection to the T680 is made via Ethernet, this means that the connection will drop, and have to be established at the new address. Therefore, we recommend using the USB connection when configuring the IP.

4.5.3. SUBNET [a.b.c.d]

```
T680> SUBNET 255.255.0.0
OK
T680> SUBNET
255.255.0.0
```

Sets or returns the requested subnet mask. Use the SAVE command to save this in nonvolatile memory. Requested subnet mask is ignored in DHCP mode.

IP change requests take effect immediately. If the connection to the T680 is made via Ethernet, this means that the connection will drop, and have to be established at the new address. Therefore, we recommend using the USB connection when configuring the IP.

4.6. Timestamper Commands

4.6.1. TRIG [ZERO v| COM v]

```
T680> TRIG ZERO -1.35
OK
T680> TRIG COM +2.4
OK
T680> TRIG
-1.35 2.4
```

TRIG ZERO and TRIG COM set the input trigger level for channel 0, or the common group of channels 1-4, respectively. Trigger levels must be in the range -2.5 to +2.5 volts.

TRIG queries the trigger levels, reporting first ZERO then COM.

4.6.2. CHAN c [n]

```
T680> CHAN 2 0x13
OK
T680> CHAN 2
19
```

Sets or queries a channel control register, where c is the channel number, 0-4, and n is the new channel configuration, an 8 bit number encoding the fields:per the table in section 2.1.

7	6	5	4	3	2	1	0
			REL			M1	M0

M is the gating mode, according to the following table.

M	Name	Description
0	OFF	No triggers are accepted. The channel holdoff counter is cleared.
1	ON	Triggers are accepted, timestamped, and the resulting timestamp is loaded into the channel FIFO memory. Timestamps represent the value of MC at the instant of trigger. The channel ignores additional triggers until the channel holdoff time expires.
2	GATED	Like mode 1, but triggers are enabled by a (TTL) logic high on the external GATE input.
3	LINKED	This mode is available only for channels 1-4. Channels are enabled by the fact that the holdoff timer for channel 0 is running. This makes channel 0 the device master, and creates a window of time relative to channel 0 that gates the other channels.

The REL bit, when set, puts the channel into relative time mode, where the reported time stamp is relative to the trigger time of channel 0. This is operative only for channels 1-4.

4.6.3. CHAN ALL [n0 n1 n2 n3 n4]

```
T680> CHAN ALL 0x01 0x13 0x13 0x13 0x00
OK
T680> CHAN ALL
1 19 19 19 0
```

Sets or queries all five channel control values at once, into channels 0-4 in that order. When used to set the control values, the write to the hardware is coherent and atomic, ensuring that channels are enabled and disabled simultaneously.

4.6.4. HOLD c [n]

```
T680> HOLD 2 1000
OK
T680> HOLD 2
1000
```

Sets or queries a channel holdoff register. The channel will not accept a second trigger until the holdoff delay has expired. The LSB is 6.25 ns; the request of 1000 in the above example would represent a 6.25 µs holdoff.

The valid range for **n** is 7 (43.75 ns) to 65535 (about 4.096 ms). If **n** is outside of this range, an invalid-argument error will be replied.

4.6.5. FIFO STATUS

```
T680> FIFO STATUS
244 289 16 411 1023
T680> FIFO CLEAR
OK
T680> FIFO STATUS
0 0 0 0 0
```

Returns five FIFO fill counts, for channels 0 to 4 respectively. A fill of 0 means that the FIFO is empty; a fill of 1023 means that the FIFO is full, and potentially overflowing. There is no explicit overflow indicator.

4.6.6. FIFO CLEAR

Clears all 5 FIFO buffers and zeroes their fill counts

4.6.7. FIFO READ c [n]

```
T680> FIFO READ 3 5
12345678
23456789
34567890
67890123
74321695
```

Returns the contents of the timestamp FIFO for channel c. Optional parameter n is the number of FIFO timestamps to return; if not provided then only a single stamp is returned.

The LSB of each timestamp is 12.207031 picoseconds. The first value returned is the output of the FIFO, namely the oldest time stamp. All valid values are unsigned integers mod 2^48.

If an empty FIFO value is read, by requesting a count nnnn larger than the number of time stamps in the FIFO, the empty values will be returned as -1.

Channel 0 timestamps are always absolute, namely interpolated latched copies of the free-running MC master counter. Channel 1-4 stamps will be absolute unless the channel is set to relative mode, in which case the time stamp is the time relative to the channel 0 trigger.

4.6.8. STAMP c

```
T680> STAMP 0
34567890
```

Returns the latest time stamp for one channel. Time stamp data is the same format as the FIFO READ command data.

4.6.9. STAMP ALL

```
T680> STAMP ALL
12345678 23456789 34567890 67890123 74321695
```

Returns five time stamps, channels 0 to 4, separated by spaces. Time stamp data is the same format as the FIFO READ command data.

4.6.10. MC

```
T680> MC
180069
```

Returns the current value of the 38-bit master counter. LSB is 12.5 ns.

4.6.11. BURST ABS|REL mask n [FP] [NUM]

Returns an average of *n* samples from the FIFOs in channels selected by *mask*, rather than reply the raw samples. When this command is used, the raw samples retrieved to calculate this average are discarded. This is used to reduce serial-command overhead and network chatter.

The replied average will have the same time-base as the FIFO READ command. Unless FP is used (see below), the reply will be an integer as with the FIFO READ command.

mask is a bitmask of the five channels in which channel zero corresponds to bit zero, channel one corresponds to bit one, and so on. If *mask* selects more than one channel, the replies will be in order of the lowest-number channel, and each channel will be delimited by a comma.

BURST REL returns the average offset in time of a channel's samples relative to channel zero. The channels in *mask* may NOT include channel zero or any channels that do not have their REL bit set. *n* represents the number of FIFO samples averaged; it must be at least 1. For BURST REL to reliably calculate this average, the channel should have been in LINKED mode while its FIFO was acquiring the samples to be averaged.

BURST ABS returns the average time in between adjacent samples on the same channel. The channels in *mask* may NOT include channels that have their REL bit set, except for channel zero, whose REL bit is unused. *n* represents the number of FIFO samples (not the number of time differences), so the denominator used for the average is *n* minus one, and the argument for *n* must be at least 2.

FP and NUM are optional. They may be in either order, but they must fall after *n*.

If NUM is used, the average will be followed by the number of FIFO samples actually used. (This will be the same as *n* only if there are at least *n* samples in the FIFO.)

If FP is used, then the reply for the channel average will be a floating point expression of the form "n.nnnnnE±nn," instead of the default base-ten integer. (This format can be easily parsed with standard C library functions such as strtod or scanf.) This may be useful when small-number round-off errors are a concern. For example, an integer of 50 could represent any number between 49.5 and 50.5. The unit value of the floating point reply has the same time-base as the integer reply.

```
T680> BURST ABS 0x1 10
188901
T680> BURST ABS 0x1 10 NUM
188901 10
T680> BURST ABS 0x3 10
188901,188903
T680> BURST REL 0xC 15 FP NUM
1.34556E+02 15,1.34519E+02 15
```

4.7. Serial Reflash Commands

A USB or Ethernet serial-command reflash session will look like the example below. The entire Highland-provided S28 text file is sent to the T680, one line at a time. The erase/reflash session might take about two minutes. The sequence is...

```
T680> FLASH UNLOCK
T680> FLASH ERASE
Erasing sector 16 of 31
Erasing sector 17 of 31
. . .
Erasing sector 31 of 31
T680> FLASH WRITE s28_line_1
. . .
T680> FLASH WRITE s28_line_n
T680> FLASH STATUS
<status report>
T680> RESET
```

The final RESET command reboots the controller and runs the new code.

4.7.1. FLASH UNLOCK

Unlock the serial flash. As a redundant measure the flash is locked at startup to prevent accidental use of the reflashing commands. Once unlocked, the flash will remain unlocked until reboot.

4.7.2. FLASH WRITE srec

Write a line of a Motorola-format S-Record to the "upgrade" portion of the flash. An invalid address in the S-Record, a failed checksum, or invalid S-Record format will result in an error. Use FLASH UNLOCK to enable this command.

4.7.3. FLASH ERASE

Erase the "upgrade" portion of the flash. Use FLASH UNLOCK to enable this command.

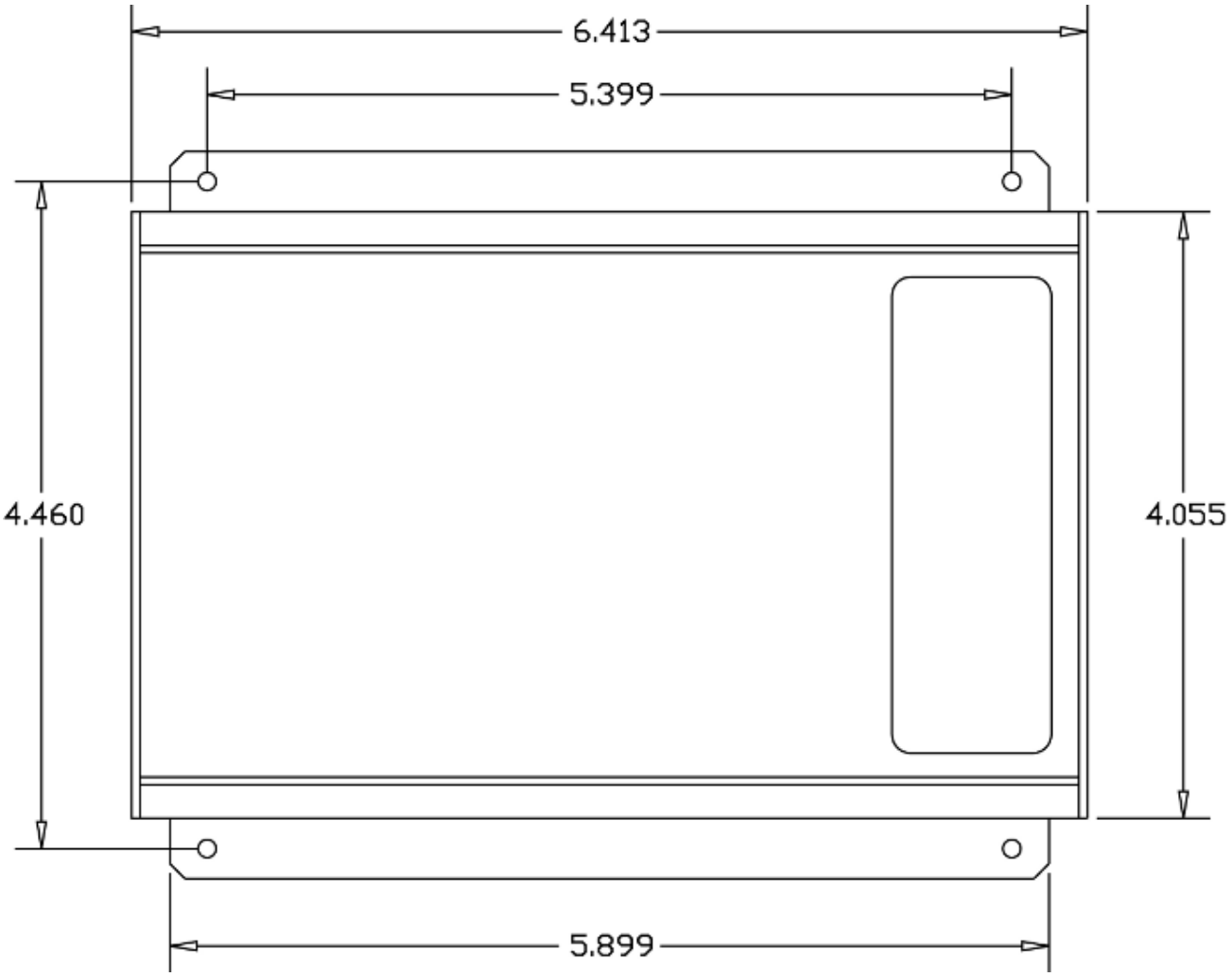
4.7.4. FLASH STATUS

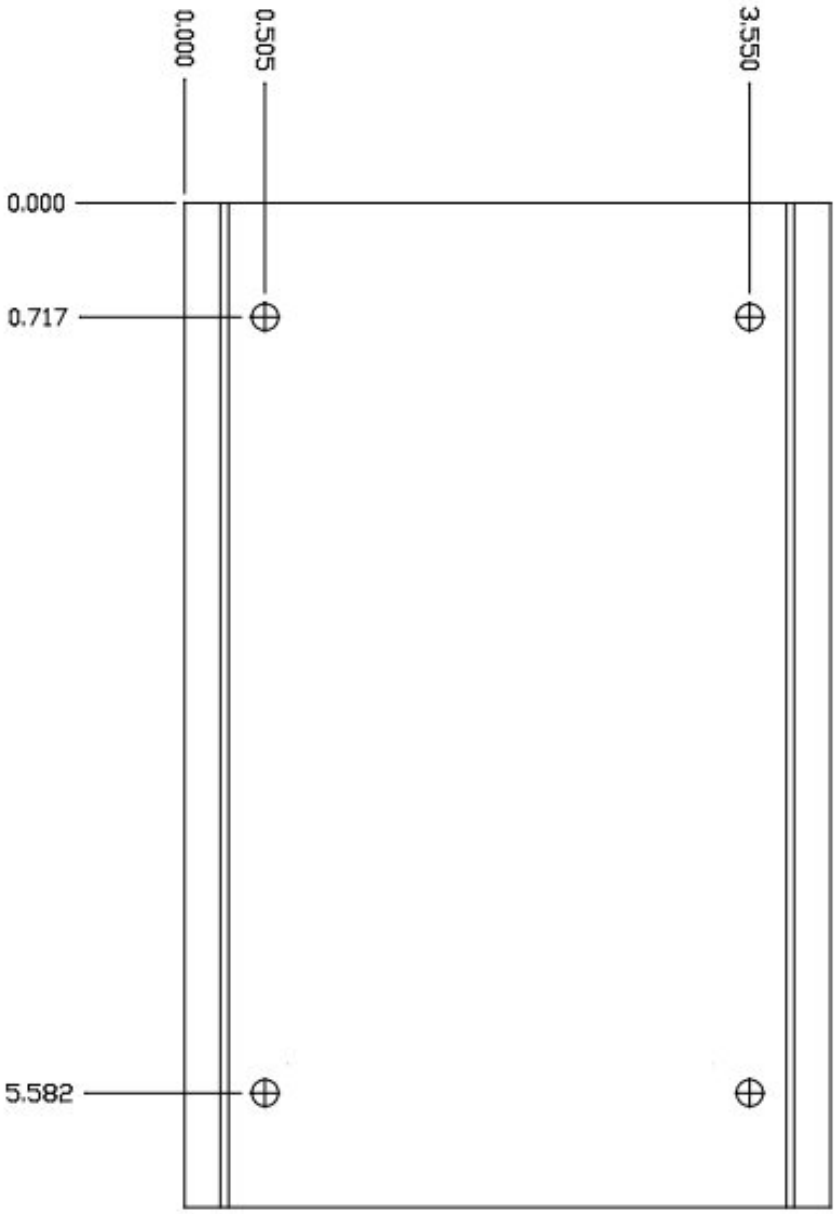
This command returns a brief report identifying the factory and optional upgrade code images and their status. A typical report might look like:

```
Highland T680-1A          SN 0007
Factory Code    28E681A   05-Jan-2013  OK
Factory FPGA    28C681A   05-Jan-2013  OK
Upgrade Code    28E681B   15-Mar-2013  OK    (or None or FAIL)
Upgrade FPGA    28C681B   15-Mar-2013  OK    (or None or FAIL)
Running  UPGRADE          FPGA  OK
```

5. Dimensions

Enclosure, shown with optional mounting flange:




0.000
0.505
3.550
0.000
0.717
5.582

6. Versions

The standard part is the model T680-1, Highland part number 28A680-1. It is supplied with the J12 wall-plug 12 volt power supply.

T680-1: 5-channel ethernet time interval counter

7. Customization

Consult factory for information about additional custom versions.

8. Hardware and Firmware Revision History

9.1 Hardware Revision History

Revision C	Sep 2014 Runs firmware version 28E681 Functionally equivalent to Revision B
Revision B	Jun 2013 Runs firmware version 28E681 Reduces ADC ramp swing and improves lock dynamics and jitter
Revision A	Aug 2012 Runs firmware version 28E680

9.2 Firmware Revision History

28E681 Revision H	Oct 2019 Adds BUSRT ABS and BURST REL commands and TCP keep-alive.
28E681 Revision G	Dec 2017 Corrects a bug that prevents use of the TEMP command.
28E681 Revision F	Sep 2016 Corrects a bug so firmware throws an invalid-argument error if the value for a HOLD command is less than 7 or greater than 65535. It also prevents the HOLD from getting implemented to less than 7 even if the unit has a previously-saved HOLD value less than 7.
28E681 Revision E	Jun 2016 Corrects a bug in a serial command used for Calibration. Added a hardware calibration factor, which will be reported in the ID command.

28E681 Revision D	Jun 2016 Corrects a printing bug in USB that results in some lost characters when a serial command has a long reply.
28E681 Revision C	Dec 2015 Corrects a printing bug that displayed incorrect values in the T680's STATUS serial command.
28E681 Revision B	Jul 2013 Corrects a bug that caused some connection problems with USB For hardware revision B or later only
28E681 Revision A	Jul 2013 For hardware revision B or later only
28E680 Revision B	Nov 2012 Changes to boot loader and Ethernet controller configuration
28E680 Revision A	Oct 2012 Initial serial flash image
28C680 Revision A	Nov 2012 Initial channel FPGA

9. Accessories

J12-1: 12 volt power supply (furnished with purchase)

J53-1: 3′ SMB to BNC cable

P10-1: 19" rack mount shelf (four t-boxes per rack)

T567-1: mounting flange