

T560 DIGITAL DELAY GENERATOR



Technical Manual

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1. Introduction

The T560 is a small, enclosed digital delay/pulse generator which is intended for use in embedded OEM applications. Given an internal or external trigger, it outputs four precisely-timed pulses.

Standard features include:

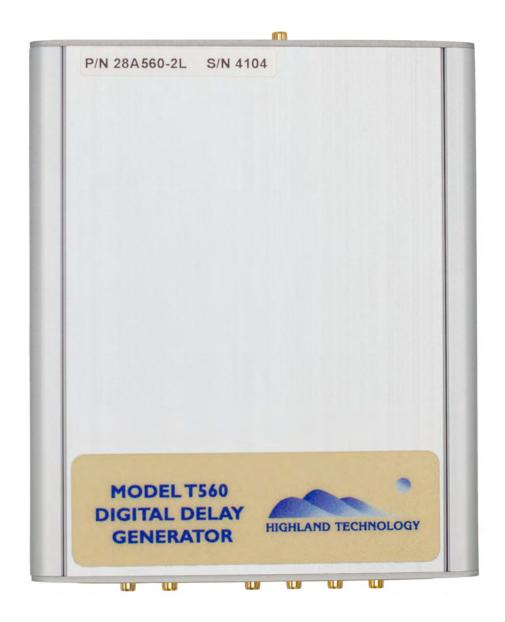
- Four TTL-level delay outputs, individually programmable for delay and pulse width
- 10 picosecond delay and width resolution, 10 second range
- 21 nanosecond insertion delay, 16 MHz max trigger rate
- < 35 picosecond typical jitter
- Highly accurate DSP phaselock system provides crystal-clock delay accuracy with zero indeterminancy from asynchronous external trigger
- Internal 10 MHz crystal oscillator timebase with external lock capability
- 0-16 MHz DDS synthesizer for internal trigger rates
- Programmable-level trigger input with divide/burst features and trigger enable GATE input
- Needs only +12 volt power from external universal power supply
- RS-232 serial interface standard; 10/100-mbps Ethernet interface optional
- Extruded enclosure with removable mounting flange

Customizable features include:

- OEM packaged or board-only custom versions
- Alternate timing algorithms
- Number of timing channels, 1 to 8
- Alternate connector types and locations
- OCXO timebase
- Low impedance outputs, 4 volts min into 50 ohms
- Extended temperature ranges and conformal coating

Highland can also provide benchtop pulse/delay generators or OEM timing packages that include picosecond-resolution time-interval measurement, ultrafast or high-voltage outputs, optical interfaces, and precision analog measurement.

Because creating new versions of the T560 involves hardware or firmware changes, customization is normally done under a contractual OEM agreement with associated purchase commitments.



2. Specifications: T560 Delay/Pulse Generator

| I digital delay and pulse generator |
|--|
| nable as level sensitive enable input, edge triggered |
| ble input, or divisor enabled output |
| nable termination, 50 Ω or 500 Ω to +2.5 V |
| -0.3 V min, +0.7 V max |
| n +2 V min, +5 V max |
| +0.1 V typical, +0.4 V max @ 50 mA |
| n +5 V typical, +4 V min @ 50 mA |
| DDS: 0 to 16 MHz, 0.02 Hz resolution |
| lock: 80 MHz |
| command or External signal |
| , 125 MHz max input |
| nable termination, 50 Ω or 10 k Ω to ground |
| nable trigger level (+0.25 to +3.3 volts) and slope |
| e outputs, 5 V, 50 Ω source impedance, each |
| nable for delay, width, polarity |
| econds, 10 ps resolution |
| seconds, 10 ps resolution |
| 00 ps, external trigger to any output |
| or po, omerina ingger to any output |
| |
| pical (50 ps max) RMS, external trigger to any output or |
| any outputs |
| c jitter for delays > 500 μs |
| Hz, limited to 1/(delay+width+60 ns) max |
| ax |
| ax |
| 0 MHz VCXO, 1 ppm initial accuracy, < 2 ppm/year drift |
| er below 10 ns per second of delay |
| 0.2 PPM/°C |
| or provides clock in/out |
| external source |
| er and delay errors are zero relative to external source |
| i and acial circle are zero relative to external source |
| |
| nigher-performance OCXO |
| higher-performance OCXO ± 7.5 ps/°C ± clock accuracy |
| nigher-performance OCXO |
| higher-performance OCXO ± 7.5 ps/°C ± clock accuracy nable to fire N times out of each M triggers and M are 1 to 2 ³² -1 |
| higher-performance OCXO ± 7.5 ps/°C ± clock accuracy hable to fire N times out of each M triggers |
| higher-performance OCXO ± 7.5 ps/°C ± clock accuracy nable to fire N times out of each M triggers and M are 1 to 2 ³² -1 |
| higher-performance OCXO ± 7.5 ps/°C ± clock accuracy nable to fire N times out of each M triggers and M are 1 to 2 ³² -1 , non-condensing |
| higher-performance OCXO ± 7.5 ps/°C ± clock accuracy nable to fire N times out of each M triggers and M are 1 to 2 ³² -1 , non-condensing |
| higher-performance OCXO ± 7.5 ps/°C ± clock accuracy nable to fire N times out of each M triggers and M are 1 to 2 ³² -1 , non-condensing |
| higher-performance OCXO ± 7.5 ps/°C ± clock accuracy nable to fire N times out of each M triggers and M are 1 to 2 ³² -1 , non-condensing |
| |

| COMMUNICATIONS | RS-232 standard, 38.4 kbaud |
|----------------|--|
| | Optional 10/100 Ethernet |
| CONNECTORS | 7 SMB for trigger, gate, clock, outputs |
| | 2.5 mm stereo jack for RS-232 |
| | 0.25" power connector |
| | Optional RJ45 for Ethernet |
| INDICATORS | LEDs indicate shot, communications |
| PACKAGING | 4.75" (L) x 4.0" (W) x 1.25" (H) extruded aluminum enclosure |
| CONFORMANCE | OEM product has no UL/FCC/CE compliance requirements |
| | Designed to meet UL/FCC/CE requirements |

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3. Overview of the T560

The T560-1 is an embedded digital delay/pulse generator. It accepts a trigger pulse and generates up to four output pulses, with each pulse being individually programmable in delay and width. Triggers may be external, internal, or evoked through the communications interface. Timing has crystal-clock precision with picosecond jitter relative to an external trigger.

Each output is user programmable for delay (0-10 seconds) and width (0-10 seconds) with 10 ps resolution. When externally triggered, all delays are relative to the basic 20 ns insertion delay.

3.1. Standard Packaging

The standard T560-1 unit is packaged in a small extruded aluminum enclosure. The Ethernet connector is provided on the T560-2 version. Section 7 of this manual provides detailed dimensions.

3.2. Overall Block Diagram

Figure 3-1 T560 Basic Block Diagram is the block diagram of the T560-1. OEM versions may include various features of the module. The optional Ethernet interface is not furnished on the standard T560-1 version.

The T560 digital delay generator creates delays by digitally counting a basic clock to create coarse delays to a resolution of 20 nanoseconds, and then adding a fine analog delay to interpolate the final times to picosecond resolution. The timing clock is derived from a 50 MHz gated oscillator which is started when an internal or external trigger is received. A DSP-based phaselock system digitizes and compares the waveforms generated by this oscillator to that of a precision 10 MHz crystal oscillator and servoes the gated oscillator to be as accurate as the crystal while still maintaining the timing relationship to the original trigger.

The T560-1 supplies four TTL pulse outputs, each programmable in delay and width. Custom versions of the T560 can provide up to eight independent delay outputs.

Because the all-digital phaselock system uses no drift-prone analog signal storage elements, long-delay accuracy and jitter depend only in the quality of the internal or external 10 MHz timebase.

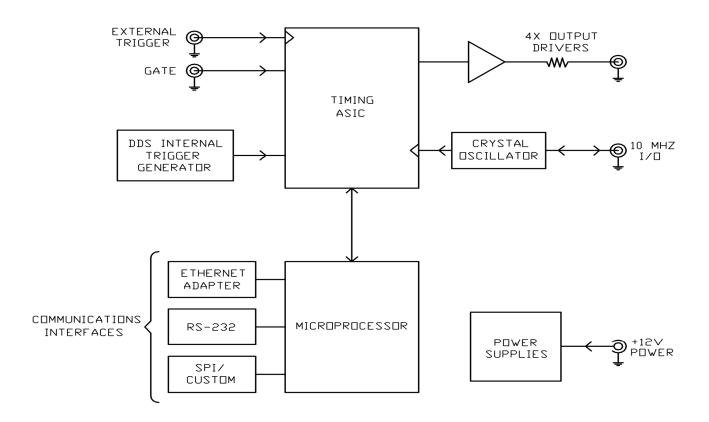


Figure 3-1 T560 Basic Block Diagram

3.3. Crystal Oscillator Timebase

The standard T560 includes a 10 MHz VCXO crystal oscillator timebase. It is factory-set to an accuracy of ±1 PPM and may be expected to drift less than 2 PPM per year. A trim DAC is provided to allow user commands to readjust the oscillator frequency as desired, with the setting stored in nonvolatile memory.

A connector is provided which allows the internal oscillator to provide a 10-MHz output, or allows an external 10-MHz source to be accepted. This allows multiple T560s to be synchronized to each other or to an external 10-MHz reference. The external clock levels are 3.3 volt square-wave CMOS logic levels. The T560 can lock to an externally-applied square wave of 10 MHz +-50 PPM, 3.3 to 5 volt positive logic levels, or to a 1 volt RMS sine wave.

The long-delay (millisecond range) jitter performance of the T560 is dominated by the phase noise of the internal crystal oscillator or the equivalent phase noise of a user-provided external reference.

Custom versions may include a higher-precision OCXO timebase. Multiple T560 units may be locked to one another to ensure timing coherence.

3.4. Trigger Inputs

Figure 3.2 is a simplified diagram of the T560 trigger and sequence logic. Any one of five available trigger sources may be selected to fire the system: External+, External-, an internal 80-MHz clock, the internal 0-16 MHz DDS synthesizer, and the user software trigger. The selected trigger is divided by a programmable factor K from 1 to 2^32-1 and supplied to the cycle-start HIT flipflop. The hit flopflop is enabled by the gating/burst logic. Once the flipflop is fired, eight identical timing blocks generate delays A1 through D2, each programmable from 0 to 20 seconds in 10-ps steps. Pairs of delays are combined to result in four outputs, each a pulse whose delay and width are programmable with respect to the common trigger. When all delay blocks have timed out, the EOD (end-of-delay) logic resets the hit flipflop for about 50 ns, after which the system is enabled to accept another trigger.

The standard external trigger is a positive level, with trigger threshold programmable from +0.25 to +3.3 volts and selectable rising/falling edge. The trigger input may be programmed to be high impedance or a 50-ohm termination to ground. Maximum safe input levels are -0.3 to +5.0 volts.

The maximum allowed trigger rate is

$$R = 1 / (D + W + 60 \text{ ns})$$

where D + W is the greatest channel sum of programmed delay plus width, and R is limited to 16 MHz max. If a channel is programmed OFF, its time settings are not relevant. If the T560 receives an internal or external trigger while a timing cycle is still busy, that trigger will be ignored.

An internal 80 MHz clock (exactly 8x the main 10 MHz clock) may also be selected as the trigger source. When it is used, a trigger divisor K must be programmed to keep the trigger rate at or below 16 MHz.

The internal DDS synthesizer allows internal triggering at rates from 0 to 16 MHz with 0.02-Hz resolution. The DDS synthesizer has a period jitter of about 1 part in 20,000, which can be substantial in absolute terms at lower requested frequencies. Both period jitter and resolution can be improved by keeping the DDS frequency in the 2-10 MHz range and using the internal trigger divisor facility to get lower trigger rates.

External triggers up to 125 MHz can be accepted, given that a programmed divisor or the inherent busy-cycle limitation will restrict the actual trigger rate to some countdown fraction of the input frequency below 16 MHz.

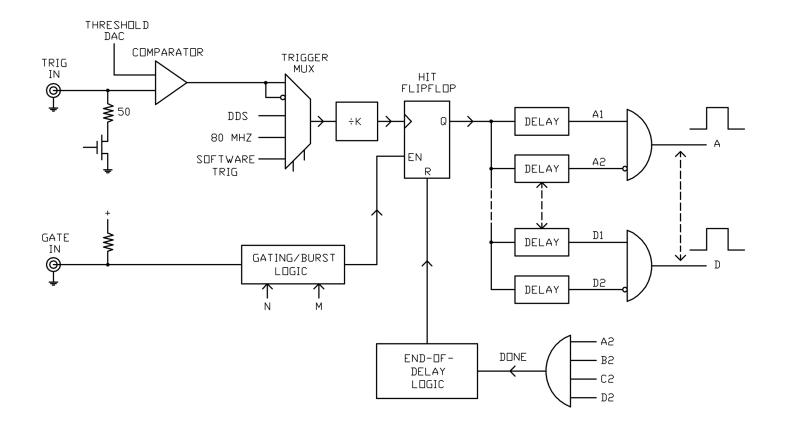


Figure 3-2 Trigger and Sequencing Logic

3.5. Burst Logic

The burst logic allows the user to define two integers N and M, each in the range of 1 to 2^32-1 . The T560, when triggered, will respond to a burst of N triggers every M triggers. For example, if N = 2 and M = 5, trigger response will be Fire, Fire, Skip, Skip, Skip, repeated indefinitely. N/M is thus the trigger duty cycle.

If either N or M is programmed to be 0, the burst logic is disabled.

Burst cycles may "free run", continuously generating N of every M possible cycles. The internal burst logic may be reset by a user command, so that the next trigger will start a new burst of N outputs.

A single burst of N cycles may be started under control of the GATE input or on software command. If GATE mode is set to BURST (command GAte BUrst), the next active edge of the GATE input will enable a single burst of N cycles. Similarly, the GAte REmote mode enables a user-fired burst, started by the GAte FIre serial command. In both cases, M must be set greater than or equal to N. If M is greater than N, additional burst starts will be locked out until a full M triggers have been received.

3.6. Pulse Outputs

Four pulse outputs are provided, called channels A, B, C, and D. Outputs are +5 volt CMOS levels with a 50-ohm source impedance. They can drive 5 volts into a non-terminating load, or 2.5 volts into a 50-ohm load. Because they are source terminated, they may drive a 50-ohm coaxial cable any distance into any termination impedance without significant reflection problems. For example, a 100 ohm termination will provide a clean 0 to +3.3 volt logic swing. External passive components can be used to convert to ECL or PECL levels.

Each output is programmable for pulse delay and width relative to the trigger. If an output is programmed for delay D, the actual output pulse will occur at D + 20 ns after the external trigger, where 20 ns is the basic insertion delay of the T560. Pulse outputs are normally active-high, but may be programmed to operate active-low.

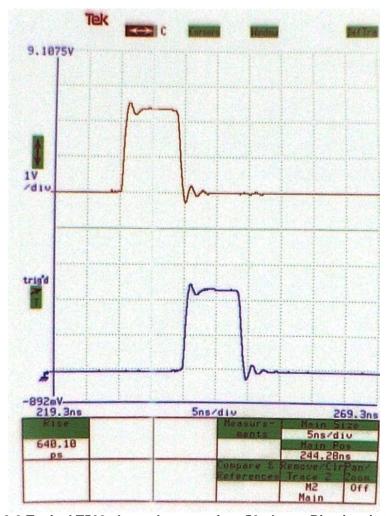


Figure 3-3 Typical T560 channel outputs into 50 ohms. Risetime is 640 ps.

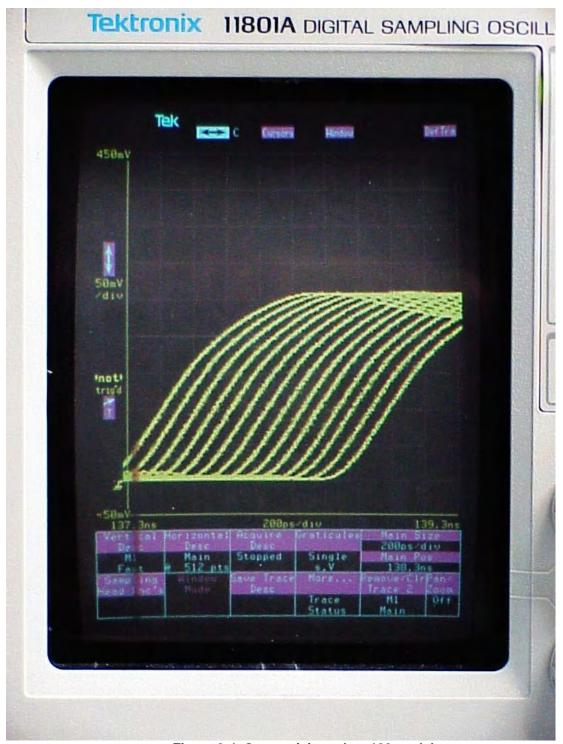


Figure 3-4 Output rising edge, 100 ps delay steps

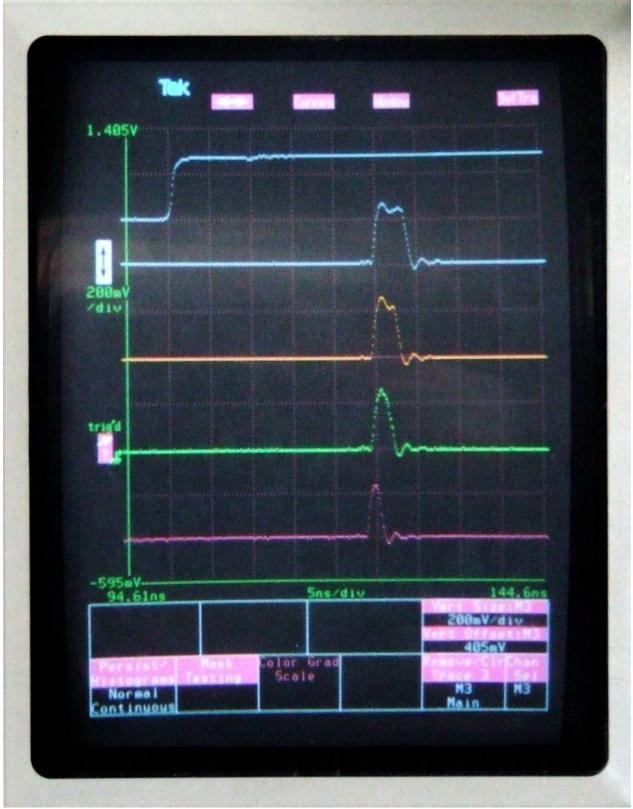


Figure 3-5 Trigger and output pulses, widths 4ns, 3 ns, 2 ns, and 1.5 ns

3.7. Gate I/O

A GATE coaxial connector is provided; it is pulled up to +5 volts through a 1K resistor or may, under software control, be terminated at 50 ohms to ground. GATE may be programmed as an input or as an output. As an input, it may be programmed to enable triggers, with high or low being the active level. As an output, it will go true (selectable high or low) to indicate that the HIT flipflop is armed and ready to accept triggers. The gate logic may also be used to enable a single burst of N pulses, with the burst being evoked by a rising edge at the GATE connector input or by remote command.

3.8. Communications and Control

The standard T560-1 is equipped with a 38.4-kbaud RS-232 interface. The T560-2 version adds a 10/100 Ethernet interface. If the Ethernet option is installed, both the Ethernet and RS-232 ports will be functional, but commands should not be sent to the T560 through both ports simultaneously.

3.9. Connectors

Standard logic-level connectors are right-angle SMBs.

Other connector types are available on OEM versions. Connectors may be straight or right-angle, SMB, MCX, or LEMO, mounted topside or bottom. Hirose H.FL or U.FL surface-mount connectors can also be provided on either side of the circuit board. Because of the close spacing of the connectors, SMA types are not recommended.

A three-foot SMB-to-BNC cable is available as Highland part number J53-1.

A miniature 2.5-mm stereo phone jack is used for the RS-232 serial interface; a mating connector and cable is available, terminated with a female D9 connector, and may be plugged into the serial port of a standard PC. The RS-232 cable assembly is Highland part number T565-1, and one is included with every purchase.

Pinout of the serial connector is:

| Tip | RXD | serial data to T560 | to PC D9-3 |
|--------|-----|-----------------------|------------|
| Ring | TXD | serial data from T560 | to PC D9-2 |
| Ground | | | to PC D9-5 |

3.10. Power Input

The T560 requires +12 volts DC at 0.3 amps max, 0.4 amps for the Ethernet version. A wall-plug universal power supply is furnished with the evaluation kit, or users may supply +11.75 to +12.25 VDC power. The evaluation power supply with US plug is Highland part number J12. The international AC plug adapter kit is part number J14.

The standard power connector is a 2.1 x 5 mm coaxial power type, center positive. OEM versions can alternately be provided with a Phoenix terminal block for power input, or a D9 combined power/RS232 connector.

The T560 power input is protected by a self-resetting polyfuse and a transzorb zener diode, and will withstand reasonable overvoltage or polarity reversal.

3.11. Custom Logic

Custom logic functions are available. Since the T560 incorporates eight internal delay generators, up to eight delay-only or delay-plus-fixed-width outputs can be provided.

3.12. Indicators

Three LED indicators are provided:

The green PWR LED indicates that power is available. It also blinks at a 1-Hz rate to indicate CPU heartbeat. Its color changes to yellow if any internal error conditions are sensed.

The blue TRIG LED flashes whenever the T560 is triggered.

The COMM LED flashes yellow when any serial character is received and green when the T560 formats a reply.

4. Programming

4.1. General Comments

The T560 accepts ASCII serial commands from the standard RS-232 interface or from the optional 10/100 Ethernet adapter. Refer to Section 6 for details about configuring the Ethernet interface.

For evaluation, serial commands may be typed using any common serial communications program, for example HyperTerminal (for RS-232) or the standard "Telnet" utility for the Ethernet version. A family of HElp commands is available, summarizing serial commands and operating modes. The STatus command will send back a summary of T560 settings.

The standard baud rate is 38,400. The receive buffer is limited to 256 bytes, and the T560 ignores serial input while it is processing the current command line.

In the following section, text using this font...

TLevel <cr>>

represents a command string sent to the T560, terminated with a carriage return character <cr>, and italic text...

1.25 <cr> <1f>

represents the reply from the T560. All commands must be terminated with semicolon or <cr>, and all reply lines are terminated by <cr> <lf>.

4.2. Command Strings

Users send serial ASCII command strings to the T560, to which the T560 immediately replies. Because the standard baud rate is high, and because the T560 may spend a millisecond or more to process commands, user software must wait for a response to each command line before sending another command.

Each command consists of a command keyword, followed by an optional alpha or numeric argument. Multiple commands may be sent in a single line, separated by semicolons. When a full line is received, indicated by the final <cr> character, the buffered line is executed, in the order received.

Keywords may be fully spelled out, or may be sent as their first two letters; only the first two letters are significant. In this documentation, a word that has two possible forms is written with the short form capitalized, and the rest of the word in lower-case letters. The actual T560 protocol is case insensitive.

For example, TRigger indicates that the short form is TR, and the long form is TRIGGER, both of which are recognized commands.

All forms are case insensitive. One or more spaces are required to separate keywords from arguments.

A delay or width is sent as

```
ADelay 23.5u
CWidth 40n
```

Acceptable suffixes are:

```
p - pico (1E-12)
n - nano (1E-9)
u - micro (1E-6)
m - milli (1E-3)
```

and exponential notation is not supported. Default is nanoseconds.

Trigger levels are sent in volts, as TLevel 1.50

Most value-setting commands may be sent without an argument, in which case they become queries of the associated value.

```
ADelay (no argument)
```

evokes the reply

```
02.123456789123
```

which represents the delay setting for the rising edge of the A output in seconds.

Since such long strings of numbers are difficult to read, a "verbose" mode is available, which will send times and other long numbers in the form

```
02.123,456,789,123
```

Certain incoming ASCII characters are treated specially:

- All lowercase letters are converted to uppercase
- TAB is treated as a space
- ETX, ESC, and DEL are equivalent to BS, command line abort.
- Colon is translated to semicolon, the command separator
- Most other characters, including + , * ? and linefeed, are ignored.
- A "blank" input line, <cr> only, evokes the response T560 <cr> <1f>

The T560 does not support hardware or software flow control. Other baud rates are available on special order.

4.3. Command Structure

A command line begins with a command keyword (or its 2-letter abbreviation), followed by optional arguments. Multiple commands on a line may be separated by semicolons.

One or more spaces are required between a keyword and its argument. Whitespace may not break up a command token or an argument but is otherwise allowed.

Query commands are requests for specific data. A query is often a "set"- type command without an argument.

Time-set commands are expressed as channel delays and widths, with the four pulse outputs identified as A, B, C, or D, corresponding to the four output pulse connectors.

All commands must be terminated by either an end of line indicator (carriage return, ASCII 13, denoted <cr>) or the separator (;) for multiple commands on a line. Linefeeds are ignored.

Since the T560 receive buffer is limited to 256 bytes, users should not program multiple commands per line that might exceed this length. If at any time the <backspace> character (ASCII code 8) is received, the T560 will flush its receive buffer and ignore any previous input.

Each received command will evoke a reply indicating the execution status of the command. For query commands, the reply is the requested data. For other commands, successful completion will yield a reply of $o\kappa$. If multiple commands are issued on one line, multiple responses will be sent back on a single line, separated by semicolons. For the command line...

1.25; TLEVEL; TRIG POS

the reply will be of the form

All reply strings are terminated with carriage return/linefeed <cr> <lf> characters.

If an error occurs while processing a command, the reply ?? will be returned. If multiple commands are present on a command line, and any command produces an error, the erroneous command will respond with the ?? indicator and no remaining commands will be processed.

Numerical replies to queries will be in fixed-point decimal numeric form, with embedded commas included if Verbose mode is set.

4.4. Realtime Issues

User command lines are stored in a buffer until the <cr> character is received, at which time the entire command line is parsed and executed in the order received. Each

command sends its reply characters, typically a requested value or the $o\kappa$ response, as the command is executed. Any additional incoming characters following the command-line <cr> are ignored until the entire command line is processed and the final response-line <cr> <lf> is returned.

Most simple commands execute in hundreds of microseconds, and their realtime execution rate is dominated by the 38.4 kbaud (3840 characters/second) serial communications rate. Shortform commands reduce communications overhead. Long reports are of course baud rate limited, with the STatus report or the longer HElp pages taking as long as 500 milliseconds.

When delay/width settings are changed via the INstall command (or an end-of-line autoinstall) or the trigger, burst, or gate parameters are changed, the firmware will immediately force the end-of-delay reset state, which will abort any timing cycles currently in progress. EOD will be asserted for about 350 microseconds, after which triggers will be re-enabled.

If aborting timing cycles is undesirable, one can disable triggers, wait until any possible timing cycle has finished, then do the desired operation. For example, if it were known that all delay+width settings total under 40 milliseconds, one could send the T560 the sequence...

TRIGGER OFF; WAIT 50000; CDELAY 2.5m; INSTALL; TRIGGER POS

to which it would reply

OK;OK;OK;OK;OK

with an additional 50 millisecond pause before the second ox.

One can also use the realtime USEC counter to measure actual command execution times in microseconds...

US 0; SY 3.579545M; US

which might respond

OK;OK;0,000,001,128

Again, command execution times are usually dominated by the 38 kbaud communications rate.

4.5. T560 Command Summary

The following is a summary of commands which may be sent to the T560.

| Long Form | Short Form | Function |
|---------------------|------------|---|
| ADELAY 45u | AD 45u | set A delay |
| AWIDTH 25.5n | AW 25.5n | set A width |
| ADELAY | AD | delay A query |
| AWIDTH | AW | width A query |
| ASET ON | AS ON | enable A output |
| ASET OFF | AS OF | disable A output |
| ASET POS | AS PO | set A polarity positive (normal) |
| ASET NEG | AS NE | set A polarity negative (inverted) |
| ASET | AS | query channel A settings |
| APENDING | AP | query channel A pending settings |
| | | 1 - 3 - 3 - 3 - 3 - 3 - 3 - 3 - 3 - 3 - |
| BDELAY 45u | BD 45u | set B delay |
| BWIDTH 25.5n | BW 25.5n | set B width |
| BDELAY | BD | delay B query |
| BWIDTH | BW | width B query |
| BSET ON | BS ON | enable B output |
| BSET OFF | BS OF | disable B output |
| BSET POS | BS PO | set B polarity positive (normal) |
| BSET NEG | BS NE | set B polarity negative (inverted) |
| BSET | BS | query channel B settings |
| BPENDING | BP | query channel B pending settings |
| | | |
| CDELAY 45u | CD 45u | set C delay |
| CWIDTH 25.5n | CW 25.5n | set C width |
| CDELAY | CD | delay C query |
| CWIDTH | CW | width C query |
| CSET ON | CS ON | enable C output |
| CSET OFF | CS OF | disable C output |
| CSET POS | CS PO | set C polarity positive (normal) |
| CSET NEG | CS NE | set C polarity negative (inverted) |
| CSET | CS | query channel C settings |
| CPENDING | CP | query channel C pending settings |
| DDELAY 45u | DD 45u | set D delay |
| DWIDTH 25.5n | DW 25.5n | set D delay set D width |
| DDELAY | DD 25.511 | |
| DWIDTH | DW | delay D query width D query |
| DSET ON | DS ON | enable D output |
| DSET ON DSET OFF | DS OF | disable D output |
| DSET POS | DS PO | set D polarity positive (normal) |
| DSET NEG | DS NE | set D polarity positive (normal) |
| DSET NEG | DS NE | query channel D settings |
| DPENDING | DP | query channel D pending settings |
| DI HIIDING | | query charmer o penumy seminys |

| Long Form | Short Form | Function |
|--|---|--|
| QDELAY 45u | QDELAY 45u | set all four ("quad") delays |
| QD 45u | QD 45u | set all four ("quad") widths |
| 25 104 | <u> </u> | Set all four (quad) widths |
| INSTALL | IN | apply all pending channel settings |
| AUTOINSTALL 1 | AU 1 | automatically apply pending settings |
| AUTOINSTALL 0 | AU 0 | cancel automatic mode |
| UNDO | UN | cancel all pending channel settings |
| | | i ü |
| TLEVEL 1.25 | TL 1.25 | set external trigger level |
| TLEVEL | TL | query trigger level |
| TRIGGER POS | TR PO | trigger on external rising edge |
| TRIGGER NEG | TR NE | trigger on external falling edge |
| TRIGGER INT | TR IN | select internal 80 MHz trigger |
| TRIGGER SYN | TR SY | select internal DDS synthesizer |
| TRIGGER REMOTE | TR RE | select remote trigger |
| TRIGGER OFF | TR OF | disable triggers |
| TRIGGER HIZ | TR HI | trigger input is 10K to ground |
| TRIGGER | TR TE | trigger input is terminated at 50 ohms |
| TERMINATE | | |
| TDIV 5000 | TD 5000 | set trigger divisor |
| TDIV | TD | query trigger divisor |
| TRIGGER | TR | trigger setup query |
| FIRE | FI | fire remote trigger |
| FEOD | FE | force End Of Delay, abort timing cycle |
| | | <u> </u> |
| SYNTHESIZE | SY 3.579M | set optional DDS synthesizer rate |
| 3.579M | | |
| SYNTHESIZE | SY | query DDS synthesizer rate |
| CLOCK HIZ | CL HI | alack connector is unused |
| CLOCK HIZ | CL OU | clock connector is unused |
| CLOCK UN | CL UN | connector outputs 10 MHz external 10 MHz is accepted |
| CTOCK TIA | CTI TIA | CALCITIAL TO IVIDA 15 ACCEDIEU |
| CT.OCK | | |
| CLOCK | CL | query clock settings and temperature |
| CTRIM 2048 | CL CT 2048 | query clock settings and temperature set 10 MHz clock trim, 04095 |
| CTRIM 2048 CTRIM | CL CT 2048 CT | query clock settings and temperature set 10 MHz clock trim, 04095 query clock trim value |
| CTRIM 2048 | CL CT 2048 | query clock settings and temperature set 10 MHz clock trim, 04095 |
| CTRIM 2048 CTRIM | CL CT 2048 CT | query clock settings and temperature set 10 MHz clock trim, 04095 query clock trim value |
| CTRIM 2048 CTRIM CLOCK SAVE | CL CT 2048 CT CL SA | query clock settings and temperature set 10 MHz clock trim, 04095 query clock trim value save clock trim to flash memory |
| CTRIM 2048 CTRIM CLOCK SAVE BNUM 555 | CL CT 2048 CT CL SA BN 555 | query clock settings and temperature set 10 MHz clock trim, 04095 query clock trim value save clock trim to flash memory set burst N, pulses output in burst |
| CTRIM 2048 CTRIM CLOCK SAVE BNUM 555 BMOD 2000 | CL CT 2048 CT CL SA BN 555 BM 2000 | query clock settings and temperature set 10 MHz clock trim, 04095 query clock trim value save clock trim to flash memory set burst N, pulses output in burst set burst M, total triggers/cycle |
| CTRIM 2048 CTRIM CLOCK SAVE BNUM 555 BMOD 2000 BURST ON | CL CT 2048 CT CL SA BN 555 BM 2000 BU ON | query clock settings and temperature set 10 MHz clock trim, 04095 query clock trim value save clock trim to flash memory set burst N, pulses output in burst set burst M, total triggers/cycle enable burst mode |
| CTRIM 2048 CTRIM CLOCK SAVE BNUM 555 BMOD 2000 BURST ON BURST OFF | CL CT 2048 CT CL SA BN 555 BM 2000 BU ON BU OF BU RE | query clock settings and temperature set 10 MHz clock trim, 04095 query clock trim value save clock trim to flash memory set burst N, pulses output in burst set burst M, total triggers/cycle enable burst mode disable burst reset burst counters |
| CTRIM 2048 CTRIM CLOCK SAVE BNUM 555 BMOD 2000 BURST ON BURST OFF | CL CT 2048 CT CL SA BN 555 BM 2000 BU ON BU OF | query clock settings and temperature set 10 MHz clock trim, 04095 query clock trim value save clock trim to flash memory set burst N, pulses output in burst set burst M, total triggers/cycle enable burst mode disable burst |

| Long Form | | Short Form | Function |
|----------------|----|------------|--|
| GATE INPUT | GA | IN | make gate an input |
| GATE POS | GA | PO | gate in/out is active high (normal) |
| GATE NEG | GA | NE | gate in/out is active low (inverted) |
| GATE TERMINATE | GA | TE | gate input is terminated at 50 ohms |
| GATE HIZ | GA | HI | gate input is 1K to +5 volts |
| GATE BURST | GA | BU | enable single burst at gate input rise |
| GATE REMOTE | GA | RE | enable single burst on command |
| GATE FIRE | GA | FI | fire a single remote burst |
| | | | <u> </u> |
| STATUS | ST | | show T560 status report |
| SAVE | SA | | save current setup |
| RECALL | RE | | recall saved setup |
| LOAD DEFAULT | LO | DE | load default setup |
| RUN DEMO | RU | DE | run demonstration setup |
| RSET | RS | | reset the T560 |
| | | | |
| SHOTS | SH | | query shot counter |
| SHOTS 0 | SH | 0 | reset shot counter |
| USEC | US | | query microsecond counter |
| USEC 0 | US | 0 | reset microsecond counter |
| IRQ | IR | | query 40 Hz interrupt counter |
| WAIT 3400 | WA | 3400 | wait specified number of microseconds |
| | | | |
| IDENTIFY | ID | | return ID string |
| ERRORS | ER | | return error status |
| ERRORS 0 | ER | 0 | clear error flags |
| | | | |
| VERBOSE 1 | VE | | show long numbers with commas |
| VERBOSE 0 | VE | 0 | show long numbers without commas |
| VERBOSE | VE | | query verbose setting |
| COMMENT | CO | | command is ignored |
| | | | |
| HELP | HE | | return general HELP message |
| HELP CHANNELS | | CH | return help on channel operations |
| HELP TRIGGER | | TR | return Trigger help |
| HELP CLOCK | | CL | return Clock help |
| HELP BURST | | BU | return Burst help |
| HELP GATE | | GA | return Gate help |
| HELP MISC | HE | MI | return miscellaneous help |

4.6. Command Details

4.6.1.CHANNEL SET COMMANDS

The channel commands allow channel delays, widths, and modes to be set or queried.

Set a delay or width with the appropriate command, such as

ADelay 65.81n

DWidth 55.2u

where times may be specified with suffix characters s,m,u,n, or p for seconds, milliseconds, microseconds, nanoseconds, and picoseconds. The default is nanoseconds.

Interrogate a time setting with

| ADelay | which evokes the reply, in seconds, |
|--------|-------------------------------------|
|--------|-------------------------------------|

00.00000065810 in terse mode, or 00.000,000,065,810 in verbose mode.

All channel settings are stored in a "pending" buffer until applied to the timing hardware by an Install command. If the Autoinstall mode is set to 0, users must send the discrete Install command to apply pending time settings. If Autoinstall is set to 1, any new settings are installed when the <cr>
commands on that line have been processed.

The **undo** command cancels any pending channel settings.

| ASet ON | enables channel A output |
|----------|--|
| ASet OFf | disables channel A output. Its electrical output will stay low (or high, if channel is inverted) and its time settings are ignored |
| ASet POs | sets channel A polarity positive (normal) |
| ASet NEg | sets A polarity negative (inverted) |
| ASet | query channel A settings. A string will be returned Ch A POS ON Dly 00.123456789012 Wid 01.234567890123 |
| APending | query channel A pending settings. This produces a response identical to ASet , except that the pending values are presented |

The QDelay and QWidth "quad" commands set all four delays or widths to the same value.

4.6.2.TRIGGER SETUP COMMANDS

The **TRigger** family of commands select the T560 trigger source and associated parameters.

| TLevel 2.50 | Sets external trigger level; legal range is 0.25 to 3.30 |
|-------------|--|
| TLevel | Queries trigger level. The response would be 2.50 |
| TRigger POs | Trigger on external input, rising edge. |
| TRigger NEg | Trigger on external input, falling edge. |
| TRigger INt | Selects an internal 80 MHz trigger, 8x the internal 10 MHz clock. A divisor K of at least 5 is required to limit the trigger rate to the 16 MHz limit. |

| TRigger SYn | Selects optional internal DDS synthesizer as the trigger source. Its frequency may be set from 0.018 Hz to 16 MHz using the SYN command. | | |
|-------------------|--|--|--|
| TRigger REmote | Enables software triggers, via the FIRE command. | | |
| Fire | Fires one remote trigger. | | |
| TRigger OFf | Disables triggers | | |
| TDivisor 4194304 | Sets a trigger divisor integer K, from 1 to 2^{32} -1. When the divisor is loaded, the next trigger will fire the T560 (subject to other restraints) and then K-1 triggers will be skipped before another is enabled. TD 0 disables the divide function. Divide can be combined with BURST. | | |
| TRigger HIz | Trigger input is 10K to ground. | | |
| TRigger TErminate | Enables 50 ohms terminator on TRIGGER input. | | |
| TRigger | Trigger setup query, evokes a response of | | |
| Trig REM 50R Le | evel 1.250 Div 0000000000 SYN 00010000.00 | | |

4.6.3.SYNTHESIZE COMMAND

The T560 is furnished with a direct-digital frequency synthesizer that may be used to generate internal triggers from 0 to 16 MHz with 0.018 Hz resolution.

syn 123.456K sets the frequency. Suffix characters may be K (kilohertz) or M

(megahertz). The default is Hertz.

syn queries the current frequency

4.6.4.BURST COMMANDS

The BURSt commands control the trigger burst logic. Burst allows a group of N pulses to be fired out of each group of M input triggers; that is, N successive triggers will be accepted, then M-N triggers will be skipped.

It is also possible to generate a burst of N triggers, invoked by the rising edge of the GATE input, or by remote command. See GATE COMMANDS.

| BNum 555 | sets burst N, pulses output in burst | | | |
|--|--------------------------------------|--|--|--|
| BNum | queries burst N value | | | |
| BMod 2000 | sets burst M, total triggers/cycle | | | |
| BMod | | | | |
| BUrst ON | enables burst mode | | | |
| BUrst OFf | disables burst | | | |
| BUrst REset reset burst counters; next trigger will be the first of N. | | | | |
| BUrst queries burst settings. This will return a string | | | | |
| Burst OFF | N 000000555 of M 000002000 | | | |
| | | | | |

4.6.5.GATE COMMANDS

The GATE coaxial connector may be used as an input or an output. As an input, it can enable or disable triggers under the control of an external TTL level. As an output, it can indicate when the internal hit flipflop is enabled to accept triggers.

If the gate is configured as an input, a true level allows triggers and a false level disables them. If BURST is also enabled, then whenever the input level is in the trigger disable state, the burst counter logic is reset; the next time gate goes true, the burst logic will immediately enable a group of N triggers.

If gate is set to be an output, it will go active (high or low, as programmed) whenever the hit flipflop is armed to accept triggers. So in burst mode, it will go true during the active "N" pulses of the burst sequence. If a trigger divisor is programmed, it will go high only when the divisor enables triggers.

| GAte | OFf | disable gate functions | | | | | |
|------|---|--|--|--|--|--|--|
| GAte | OUtput | make gate connector an output. The output level will be true when the hit flipflop is enabled to accept triggers | | | | | |
| GAte | te INput make gate an input. When the external TTL level is true, triggers will be enabled. | | | | | | |
| GAte | POs | gate in/out is active high (normal) | | | | | |
| GAte | NEg | gate in/out is active low (inverted) | | | | | |
| GAte | e TErminate gate input is terminated at 50 ohms | | | | | | |
| GAte | HIz | gate input is 1K to +5 volts | | | | | |
| GAte | te BUrst enable single burst at gate input rise | | | | | | |
| GAte | REmote | enable single burst on GATE FIRE command | | | | | |
| GAte | FIre | fire a single burst | | | | | |
| GAte | GAte gate setup query. Returns | | | | | | |
| G | ate OFF | POS HIZ Shots 000000066 | | | | | |

4.6.6.CLOCK COMMANDS

T560 timings are based on an internal 10 MHz crystal oscillator clock. The function or the CLOCK coaxial connector is controlled by this group of commands. If the connector is declared to be an input, the T560 accepts a 10 MHz TTL square wave input, or a sine wave of about 1 volt RMS, and will lock its crystal oscillator to this source. If the connector is set to be an output, the local 10-MHz oscillator frequency will be output from this connector.

The value used to trim the internal oscillator frequency is an integer in the range 0 to 4095, with 2048 being roughly the nominal center frequency. Since the internal crystal oscillator might be expected to drift 1-2 ppm per year, users may wish to occasionally trim its frequency if precise delays are required.

Clock-group serial commands are...

| CLock HIz | clock connector is unused | | | |
|--|--|--|--|--|
| CLock OUt | connector outputs internal 10 MHz oscillator | | | |
| CLock IN | external 10 MHz is accepted; oscillator phaselocks | | | |
| CTrim 2048 | sets 10 MHz clock trim, 04095, about 0.1 ppm/lsb | | | |
| CTrim | queries clock trim value | | | |
| CLock SAve save clock trim to flash memory. This value will be restored at powerup | | | | |
| CLock query clock settings; returns | | | | |
| Clock OUT | Trim 02048 Temp +32.4 | | | |

The *Temp* item is circuit board temperature in degrees C. It is typically about 10 degrees above ambient.

4.6.7.FEOD COMMAND

The **FEod** command briefly resets the timing hardware, aborting any timing cycle in progress. This is useful for terminating long delays.

The SAve command will save the overall T560 setup into nonvolatile memory. This setup will be restored at powerup or may be loaded via the REcall command.

| SAve | save current setup to nonvolatile memory | | |
|--------------|--|--|--|
| REcall | recall saved setup | | |
| LOad DEfault | load default setup; see Figure 4-1 Typical T560 Status Report | | |
| RUn DEmo | run demonstration setup. This is the default setup, except that the T560 self-triggers at 20 KHz | | |

The Usec command returns the value of a free-running 32-bit counter that increments once each microsecond. Usec 0 resets the counter.

The WAit nnn command pauses command execution for a specified number of microseconds, up to 2^{32} -1.

The IRq command returns the value of the internal 40 Hz interrupt counter.

The shots query returns the 32-bit shot counter. This counter increments every time the T560 is fired. Shots 0 will clear the shot counter.

The following command line will return the approximate trigger rate in Hz:

4.6.10. IDENTIFY COMMAND

The IDentify command returns a string which identifies the T560 firmware version. The returned form is T560-1 Firmware 28E563-A

4.6.11. ERRORS COMMAND

The Errors command returns a string which identifies any T560 errors. The returned form is...

Errs None

Errs 00127 XTRIM RECAL CALIB LOGIC XLOCK TUNE DPLL

where the integer value represents the error flags word. Bits are...

| Bit | Value | Flag | Meaning |
|-----|-------|-------|---|
| 0 | 1 | XTRIM | VCXO trim value lost |
| 1 | 2 | RECAL | saved setup recall failed |
| 2 | 4 | CALIB | calibration table lost; default cals are used |
| 3 | 8 | LOGIC | internal logic error |
| 4 | 16 | XLOCK | VCXO failed to lock to external source |
| 5 | 32 | TUNE | powerup DPLL calibration error |
| 6 | 64 | DPLL | DPLL stability error |

If any error bits are set, the string will also explicate the error bits in text. The "power" LED will turn yellow if any error bits are up.

The Errors 0 command will clear the error flags word.

4.6.12. VERBOSE COMMAND

The **VErbose** 1 command places the T560 in verbose mode, where commas are included in all long numeric strings that are returned. This mode makes time settings and 32-bit integers easier to read but may not be compatible with external software.

The **VErbose** 0 command will cancel verbose mode.

VErbose alone will query this setting.

4.6.13. HELP COMMANDS

The HElp command, with no arguments, will display a short command summary, listing top-level commands. Specific commands will be explained with requests of the form HElp TRigger and such.

| HElp | return general HELP message |
|---------------|-----------------------------------|
| HElp CHannels | return help on channel operations |
| HElp TRigger | return Trigger help |
| HElp CLock | return Clock help |
| HElp BUrst | return Burst help |
| HElp GAte | return Gate help |
| HElp MIsc | return miscellaneous help |

4.6.14. STATUS COMMAND

The STatus query returns a full report of T560 settings. A typical report is shown below. Verbose mode was enabled. The status shown is the default setup.

Highland Technology Model T560 Digital Delay Generator

| Firmware | 28E560-7 | 1034 |
|-----------|----------------|-------|
| rırılware | スの Pi つり U = A | 10.54 |

Cal date January 31, 2014

| Trig 00,01 | REM 0,000 | | Level | 1.250 | Div | 0,000 | ,000, | 000 | SYN | | |
|----------------|--------------|------|----------------|---------|--------------|------------------|-------|-----|-------|--------|-------|
| Gate | OFF | POS | HIZ | | Shots | 0,000 | ,000, | 066 | | | |
| Burst | OFF | N 0, | 000,00 | 00,016 | of M | 0,000 | ,000, | 064 | | | |
| Verbo Clock | | | nstal 02048 | l FEOD | Usec Temp | 4,009,4 +36.3 | 459,0 | 10 | DPLL | 00000 | |
| Errs | Non | е | | | | | | | | | |
| Ch A | POS | ON | Dly | 00.000, | 000,00 | 0,000 | Wid | 00. | 000,0 | 02,000 | 0,000 |
| Ch B | POS | ON | Dly | 00.000, | 002,00 | 0,000 | Wid | 00. | 000,0 | 02,000 | 0,000 |
| Ch C | POS | ON | Dly | 00.000, | 004,00 | 0,000 | Wid | 00. | 000,0 | 02,000 | 0,000 |
| Ch D | POS | ON | Dly | 00.000, | 006,00 | 0,000 | Wid | 00. | 000,0 | 02,000 | 0,000 |

Figure 4-1 Typical T560 Status Report

4.6.15. RSET COMMAND

The RSet command performs a hardware reset/restart of the T560, equivalent to a power off/on cycle. The reset takes about 4 seconds, after which the T560 will respond with the string Highland Technology T560 DDG <cr>

The last-saved setup will be installed.

4.7. Firmware Upgrade Procedure

T560 firmware may be field-upgraded, from a Windows PC with an RS-232 serial-port connection to the unit.

The PC must have the following Highland-provided files in a common folder:

| Flash1.bat | batch file for COM1 port |
|------------------|--------------------------------------|
| Flash2.bat | batch file for COM2 port |
| 28E560z.fls | script file to flash version 28E564z |
| 28E560z.rom | application file to be loaded |
| Flash560_Win.exe | Windows flash manager program |

To reflash the T560 firmware, connect PC serial port COM1 or COM2 to the T560 using Highland cable part number T565 or equivalent, and start the appropriate Flash1.bat or Flash2.bat batch file.

The flash procedure should now run, reporting progress. At the end, verify that the displayed file and actual flash checksums are equal.

5. Powerup States and Saved Setups

Users may program the T560 as desired and then use the **SAve** command to copy all setups to nonvolatile flash memory. That saved setup may be recalled at any time via the **REcall** command. The saved setup is also recalled and installed at powerup, allowing the T560 to resume operation without any serial commands.

The powerup sequence takes about 4 seconds. During this time, channel outputs are electrically low and terminations are high-Z.

If the saved configuration programs channels to be inverted polarity, those outputs will transition from low to high when the initial powerup sequence is over.

6. Xport Ethernet Module Setup

The T560-2 and T560-32 use a Lantronix Xport module as the Ethernet/TCP-IP interface. It can be accessed by connecting to the device via either its IP address or DHCP-provided hostname, on TCP port 2000. The interface is the same line-oriented ASCII interface as provided over the serial interface, but can be accessed through a standard telnet client such as TeraTerm, puTTY, or the OS-provided telnet command.

To confirm that the T560 has been connected successfully, type **st** followed by <Enter>. You should see the status report as defined in 4.6.14.

6.1. DHCP

The factory default setting for the T560 has its IP address assigned by the network's DHCP server. The T560 can be accessed by either IP address or hostname, which will be in the form: t560-xxxxx, where the xxxxx is the 5-digit unit serial number. If the serial number is fewer than five digits long, pad it on the left with zeros.

6.2. Static IP Assignment

The XPort also supports static IP address assignment.

Lantronix provides a PC utility "XportInstaller" to locate an Xport module by MAC address and assign it an IP address. The Lantronix software utilities may be downloaded from http://www.lantronix.com.

To find the IP address of a T560 unit, the T560 should be connected to the local network. The Lantronix DeviceInstaller software should be started from a Windows PC connected to the same network.

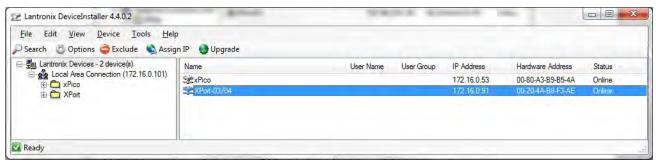


Figure 6-1. Lantronix DeviceInstaller Main Screen

Find the T560 in the software by its hardware MAC address. The MAC address can be found on one of the sides of the T560 and will follow the form xx-xx-xx-xx-xx. In the above image, the MAC address is 00-20-4A-B8-F3-AE. The IP address will appear in the software next to the MAC address.

To assign a static IP address, click on the T560, and then click on the Assign IP button. After clicking the button, the Lantronix DeviceInstaller IP address assignment pane should appear:



Figure 6-2. IP address assignment pane

Once the IP address has been identified or assigned, a web browser (preferably the web browser provided by DeviceInstaller) can be used to access the XPort module as a web page; just type the IP address into the browser's address bar, after which settings may be edited. Initially, no user name or password need be entered; simply leave both fields blank and hit Enter. The web page interface can also be used to change the IP address.

6.3. Factory XPort Settings

The following images represent the setup in which the XPort in the T560 is shipped.



Figure 6-3. XPort Home Web Page

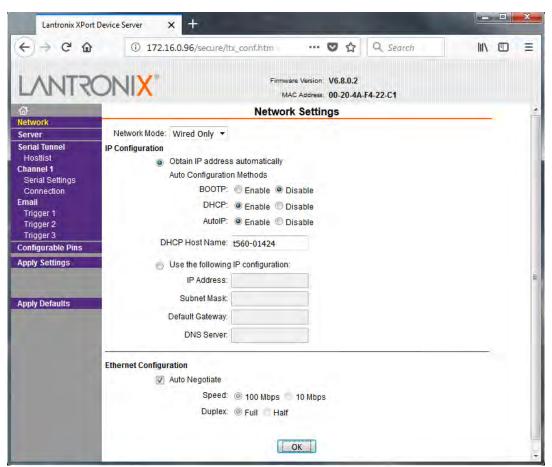


Figure 6-4. XPort Network Settings

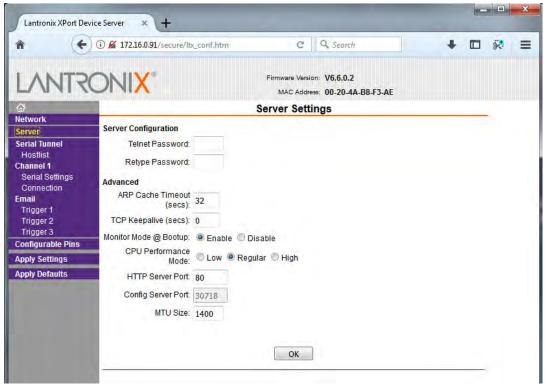


Figure 6-5. XPort Server Settings

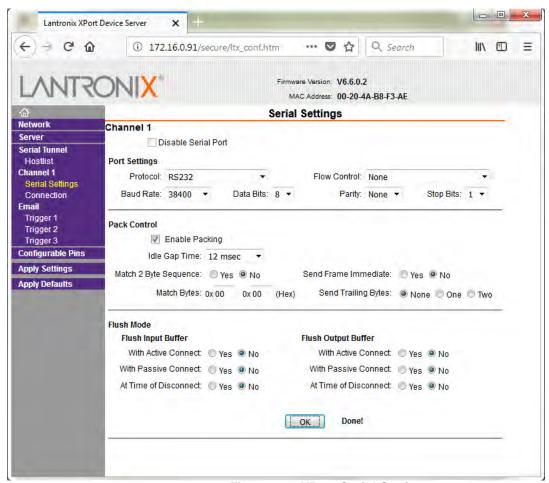


Figure 6-6. XPort Serial Settings

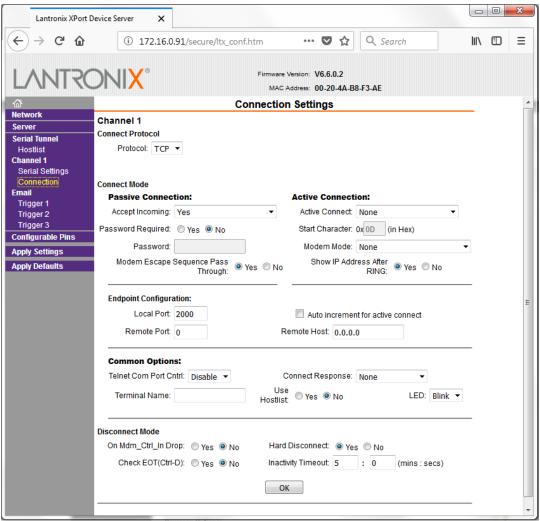


Figure 6-7. XPort Connection Settings

Note that the XPort allows only one TCP/IP connection to be open at any one time, and will time out and disconnect after the time set for a hard disconnect. Enter 0 to disable automatic disconnect. It is usually prudent to set up the XPort to disconnect after some inactivity period to avoid having an inactive connection lock out access.

A periodic ping, such as sending a single null character every minute or so, will keep a TCP/IP session open.

7. Jitter Notes

Jitter is defined as the 1-sigma standard deviation of delay. It is the shot-to-shot time uncertainty from the external trigger to any output's rising or falling edge, or the uncertainty between edges of channel outputs. Jitter is measured in RMS picoseconds. Visual peak-to-peak jitter is roughly 5 times that of RMS.

"Jitter" is usually accepted to indicate time variance as observed over an interval of 0.1 seconds, with the term "wander" used to describe slower changes of delay. Wander thus encompasses changes in delay driven by temperature changes and other slow effects. The T560 jitter specs are valid for observation periods up to 10 seconds in the absence of radical temperature changes. Note that coaxial cable propagation delay can change considerably with temperature and can contribute to observed timing variance.

Uncorrelated jitters add trigonometrically, as the square root of the sum of the squares of all jitter contributors.

Jitter can be difficult to measure. The trigger input to the T560 must be clean and fast (< 2 ns risetime) and the measuring instrument must have a jitter noise floor well below that of the T560. Most oscilloscopes and counters are not capable of resolving T560 jitter performance, especially so for longer delays. For example, a Tektronix 11801C sampling oscilloscope (or the newer DSA8200 without the optional phaselock module) has a short-delay jitter well below that of the T560, but has added jitter on the order of 10 microseconds per second of delay, whereas the T560 starts with a greater basic jitter but typically adds about 4 ns of jitter per second of delay.

For lowest jitter from an external trigger, the T560 trigger level should be set to the steepest part of the input edge, typically 1/3 to 1/2 of the peak amplitude.

Jitter is a function of the generated time delays. Very short delays have a baseline jitter that depends on fundamental triggered-oscillator phase noise. After about 500 ns, the DSP stabilization loop becomes active and disciplines the triggered oscillator, limiting its jitter accumulation.

Long delays, in the milliseconds range, become dominated by the phase noise of the internal crystal oscillator, typically about 4 ns per second of delay. Long-delay effects are zero relative to a user-provided 10 MHz reference clock.

Jitter between successive triggers, referred to as "period jitter", depends on the quality of the trigger source. The internal DDS trigger synthesizer has jitter typically about one part in 20,000 of the trigger period. DDS jitter is best if its frequency is in the 2-10 MHz range, where the period jitter, measured at a channel output, is typically about 25 ps RMS. For lowest DDS jitter at lower rates, keep the DDS synthesizer frequency in this range and use a trigger divisor to get lower trigger rates.

Dividing down the internal 80 MHz clock results in period jitter in the neighborhood of 40 ps RMS, until millisecond-range periods when crystal oscillator phase noise again becomes important.

The graph below summarizes typical T560 jitter versus delay. Here, "delay" refers to the time from an external trigger to any output edge. The rise which begins at about 1 millisecond is caused by internal crystal oscillator phase noise, and will not be present relative to an external 10 MHz reference. The T560 is also available with optional, lower phase-noise OCXO oscillators. The graphed data includes jitter contributed by the P400 trigger source and the 11801A oscilloscope, so actual T560 jitter is somewhat less.

Jitter between outputs is similar.

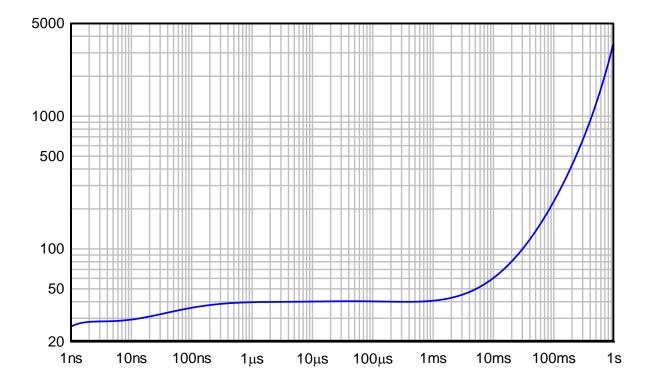


Figure 7-1 Typical T560 jitter in ps RMS versus delay

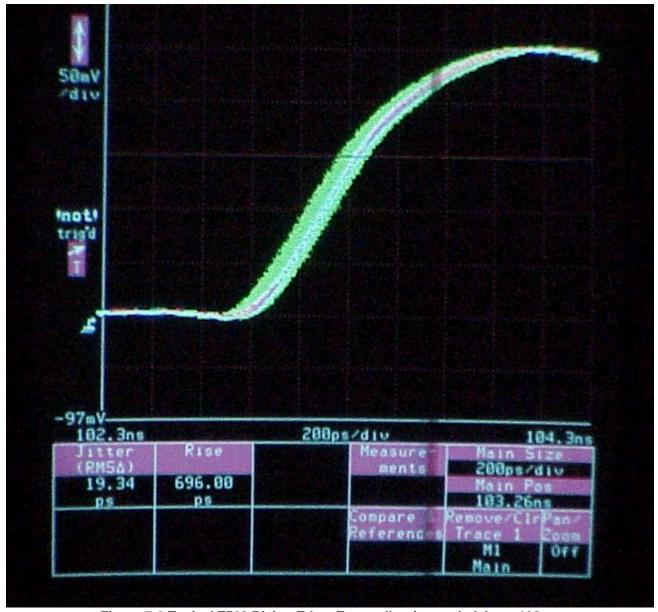


Figure 7-2 Typical T560 Rising Edge, Externally triggered, delay = 100 ns

This was measured on a Tektronix 11801A sampling oscilloscope, with the scope and the T560 triggered by a Highland P400 digital delay generator. Indicated jitter is 19.3 ps RMS, risetime 696 ps.

8. Dimensions and Mounting

T560 mechanical dimensions are shown below. The evaluation T560 is furnished with the T566 mounting flange bolted to the bottom of the extruded enclosure to make it easier to install on mounting surfaces which do not have rear access.

The T560 may be mounted using the flange supplied, or the flange may be removed and the unit mounted with four 4-40 machine screws from below.



CAUTION: Mounting screws may not penetrate more than 0.160 inches (4 mm) into the T560 enclosure.

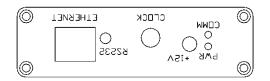
The T560-1 does not include the Ethernet connector

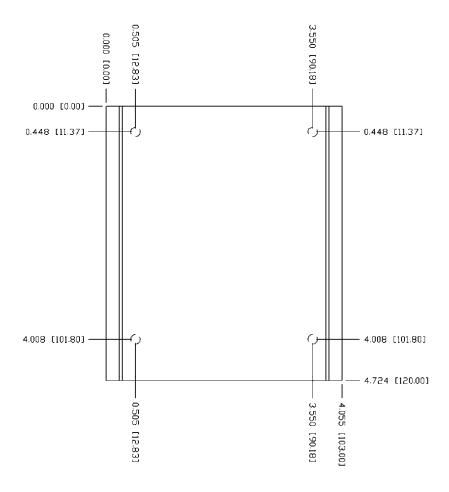


T560-2 includes Ethernet and the 2.5 mm RS-232 connector



Further customization information is in Versions on page 46.





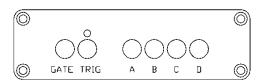
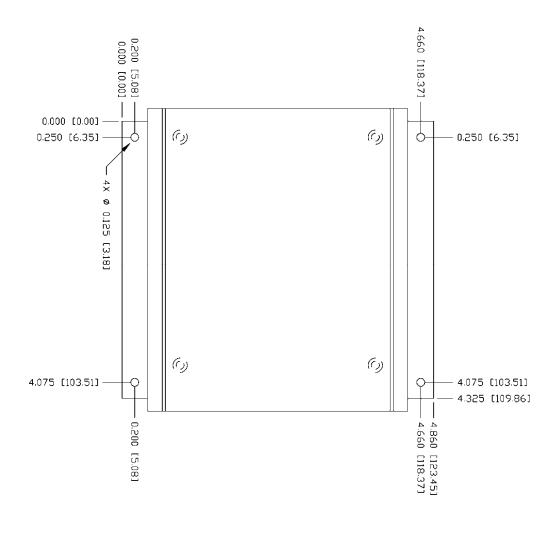


Figure 8-1 T560 Outline and Mounting



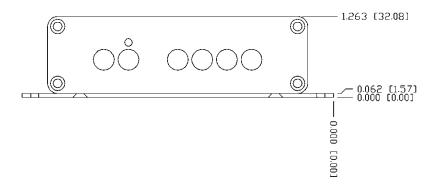


Figure 8-2 Flange Mounting Dimensions

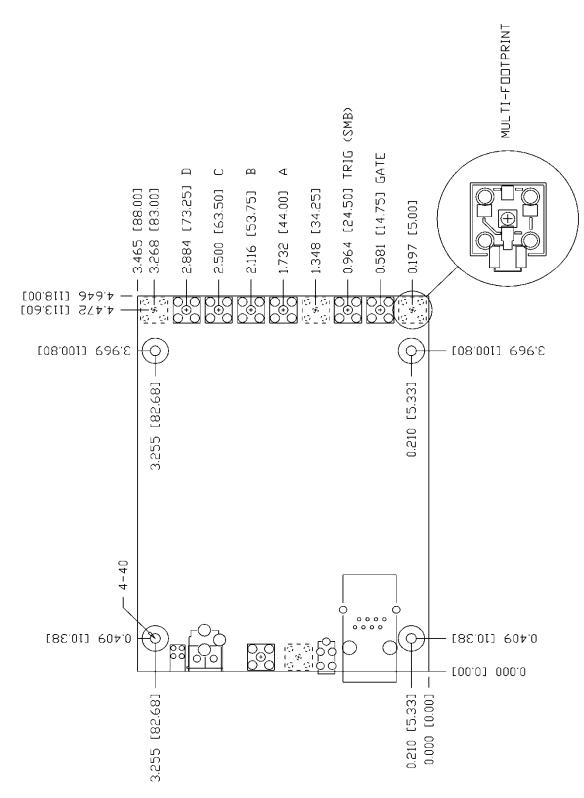


Figure 8-3 Printed-Circuit Board Dimensions

9. Demo Software

Win560.EXE is a Windows program that communicates with the T560 using serial commands. Device settings are displayed on screen and can be sent to the T560 all at once or refreshed all at once in the program. Communications access to the T560 is available via RS-232 or the Ethernet port.

Further information on running the program is available via the in-program Help screens. Win560 requires Windows 2000 or later.

10. Versions

T560-1: stand-alone 4-channel compact digital delay and pulse generator stand-alone 4-channel compact digital delay and pulse generator with Ethernet T560-2: interface board only 4-channel compact digital delay and pulse generator T560-3: (10 piece minimum order quantity) T560-4: board only 4-channel compact digital delay and pulse generator with Ethernet interface (10 piece minimum order quantity) T560-9: evaluation kit (includes T560-2 factory installed on mounting flange with Ethernet interface, power supply, two 3' SMB cables, and one RS-232 cable) T560-31: stand-alone 4-channel compact digital delay and pulse generator with OCXO option T560-32: stand-alone 4-channel compact digital delay and pulse generator with Ethernet interface and OCXO option

Consult factory for information about additional custom versions.

11. Revision History

11.1. Hardware Revisions

Revision L June 2021

Replaced obsolete parts. Improved manufacturability.

Functionally equivalent to Revision J

Revision K Sep 2014

Functionally equivalent to Revision J

Revision J Jan 2014

Replaced timing element with GaAs FETs to improve timing

accuracy and reduce crosstalk

Requires switch to 28A560 series firmware

Revision H Feb 2012

Improved manufacturability

Functionally equivalent to Revision C

Revision G Dec 2011

Improved manufacturability.

Functionally equivalent to Revision C

Revision F Dec 2010

Replaced obsolete regulator package Functionally equivalent to Revision C

Revision E Jul 2009

Improved manufacturability

Functionally equivalent to Revision C

Revision D Jan 2008

Improved manufacturability

Functionally equivalent to Revision C

Revision C Apr 2007

Reduced jitter to 50 ps RMS Reduced insertion delay to 20 ns Reduced minimum pulse width to 2 ns

Increased maximum trigger input rate to 125 MHz

Revision B Jan 2007

Initial production release. Worst case jitter of 80 ps RMS

Insertion delay 25 ns

Maximum trigger input rate 80 MHz

11.2. Firmware Revisions

28E560-E June 2021

For hardware revision L

Modified for revision L hardware

28E560-D February 2016

For hardware revisions J-K

Fixed TUNE error when powering up unit above room temperature. Fixed missing pulse in gate burst mode when the trigger is very

near the gate.

28E560-C January 2016

For hardware revisions J-K

Fixed bug with occasional loss of PLL lock during long delays.

28E560-B Aug 2015

For hardware revisions J-K

Fixed bug with T564 identification on some models

28E560-A Jan 2014

For hardware revision J

Improved timing calibration linearity

28E563-B Apr 2007

For hardware revision C-H

Modified for revision C hardware

28562-A Jan 2007

Hardware revision B

Initial release

12. Accessories

J12-1: 12 volt power supply (1 included with purchase)

J53-1: 3' SMB to BNC cable (2 included with evaluation kit purchase)

J53-2: 6" SMB to BNC cable

P10-1: 19" rack mount shelf (four t-boxes per rack)

T565-1: RS-232 cable (1 included with purchase)

T566-1: mounting flange (1 included with evaluation kit purchase)