



SHEETS

- 1 BLOCK DIAGRAM
- 2 CHANNELS 0-3
- 3 CHANNELS 4-7
- 4 CHANNELS 8-11
- 5 CHANNELS 12-15
- 6 CHANNELS 16-19
- 7 CHANNELS 20-23
- 8 DACS 0-23
- 9 ADCS 0-11
- 10 ADCS 12-23
- 11 ANALOG MULTIPLEXERS
- 12 CPU/FPGA POWER
- 13 CPU DATA & FLASH
- 14 CPU MEMORY BUS
- 15 FPGA
- 16 VME BUS 1
- 17 VME BUS 2
- 18 POWER SUPPLIES
- 19 D9 CONNECTOR

BLOCK DIAGRAM

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ENGINEER J LARKIN	DATE 6/12/17	HIGHLAND TECHNOLOGY INC.	
DRAWN B GLASS	6/12/17	SCHEMATIC, V545 SYNCHRO/LVDT SIMULATOR	
CHECKED			
APPROVED			
RELEASED		DRAWING NO: 22S545	REV: E
SHEET: 1 OF 19		FILENAME:22S545E.SCH	

UNMARKED PARTS ARE 0805