



- 1. BLOCK DIAGRAM
- 2. TRIGGER
- 3. GATED OSCILLATOR
- 4. DPLL
- 5. CLOCKS
- 6. ZYNQ 1
- 7. ZYNQ 2
- 8. ZYNQ 3
- 9. TRIGGER FPGA 1
- 10. TRIGGER FPGA 2
- 11. TO AND EOD DELAYS
- 12. VERNIER A
- 13. VERNIER B
- 14. VERNIER C
- 15. VERNIER D
- 16. OUTPUT TO
- 17. OUTPUT A
- 18. OUTPUT B
- 19. OUTPUT C
- 20. OUTPUT D
- 21. SERIAL DACS, +3REF
- 22. GATE/AUX
- 23. ETHERNET/USB/RS232
- 24. MEMORIES
- 25. BIST
- 26. POWER A
- 27. POWER B
- 28. POWER C, RESET
- 29. FRONT PANEL/OPTION
- 30. CLOCK I/O
- 31. HARDWARE

1\_BLOCK\_DIAGRAM

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ENGINEER JL/RG	DATE 10/12/2020	HIGHLAND TECHNOLOGY INC.	
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CHECKED			
APPROVED			
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