HIGHLAND TECHNOLOGY

V470

VME ANALOG OUTPUT & THERMOCOUPLE SIMULATOR MODULE

Technical Manual

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1. Introduction

This is the technical manual for the Highland Model V470 analog output/thermocouple simulator VME module.

The standard version is Highland Model V470-1. The version with optional Built-In Self-Test (BIST) facility is the V470-2.

Features of the V470 include:

- 16 independent, galvanically isolated analog output channels. Each channel is independently programmable for mode and output range.
- Voltage mode: provides 16-bit resolution with programmable output voltage ranges from ±25 millivolts to ±12.5 volts.
- Thermocouple simulation mode: simulates most common thermocouples: types J K E T R S B and N. NIST-standard lookup tables are included to allow direct entry of simulated temperatures.
- Four non-isolated precision RTD signal conditioners for reference junction temperature sensing, plus one on-board reference junction sensor. Any thermocouple simulation channel can be associated with any reference.
- Provision for open thermocouple simulation.
- No realtime handshaking is required; all settings may be written to module registers at VMEbus speed.
- Separate calibration connector allows in-crate calibration check.
- Field-wiring termination and module I/O cabling is included in the design architecture. Standard termination panels, thermocouple termination boxes, and cables are available.
- Support for one or two optional 8-channel J470 isothermal junction boxes, each with integral RTD reference junction sensor, or one or two J475 field-wiring interface boards.
- A version is available with an internal full-function BIST subsystem.
- True floating outputs: channels may be connected in series for higher output voltages.
- Clearly labeled DIP switches set VME address: no jumpers, headers, or trimpots.

2. Specifications: V470 Analog Output Module

FUNCTION	16-channel VME analog voltage output and thermocouple simulation module
DEVICE TYPE	16-bit VME register-based slave: A24:A16:D16; Implements 256 16-bit registers at switch selectable addresses in the VME 16 or 24 bit addressing spaces
CHANNELS	16, programmable functions, galvanically isolated
RANGES	Programmable per channel; 10 bipolar voltage ranges: ±25 mV, 50 mV, 80 mV, 125 mV, 250 mV, 500 mV, 1.25 V, 2.5 V, 5 V, 12.5 V; Thermocouples: Types J K E T R S B N
RESOLUTION	Voltage mode, 16 bits: 0.76 µV/LSB on 25 mV range; Temperature simulation mode, 0.0625°C
OUTPUT IMPEDANCE	0.25 Ω max
OUTPUT CURRENT	20 mA min into short circuit indefinitely
OUTPUT LOADING	Stable for capacitive loads up to 2 µF
OUTPUT PROTECTION	Differential, short or applied ±35 V DC or peak AC; Common-mode, ±750 V DC or peak AC; ESD to 15 KV, human body model
RTD INPUTS	Four non-isolated thermocouple reference junction inputs, 100 R or 1 K 4-wire Pt 385 RTD sensor
RTD ACCURACY	±250 PPM, equiv to 0.0625°C, range -65 to +150°C
INPUT PROTECTION	Shorts to ground, ESD
ONBOARD SENSOR	Semiconductor reference junction temperature sensor, ±2°C typical accuracy
OPERATING TEMPERATURE	0 to 60°C; extended MIL/COTS ranges available
CALIBRATION INTERVAL	One year

POWER	Standard VME supplies: +5 V, 0.6 A max +12 V, 1 A max -12 V, 5 mA max
CONNECTORS	2 D25 female for channels and RTDs; D9 male for test
INDICATORS	LEDs indicate VME access, CPU activity, error conditions; Additional user programmable LED
PACKAGING	6U single-wide VME module
CONFORMANCE	ANSI/VITA 1-1994 (R2002) VMEbus spec; does not support byte writes; Thermocouple tables based on NIST/ITS-90 RTD tables per IEC-751 for 385 curve RTDs

Output Accuracy:

Error	TYPICAL	LIMIT 15-35°C	LIMIT 0-60°C	LIMIT -40-80°C
Offset	±5uV ±30ppm of range	±20uV ±175ppm of range	±30uV ±300ppm of range	±40uV ±400ppm of range
Gain	±50ppm of output	±310ppm of output	±660ppm of output	±940ppm of output

3. Overview

The V470 includes sixteen independent, isolated output channels. Each channel has an isolated DC power supply, isolated data interface, D/A converter, range switching attenuator, output amplifier, and a calibration-bus switching relay.

Each channel may be user programmed to operate in either voltage-output or thermocouple simulation modes. In each mode, channel operating parameters and output level are set in per-channel, dedicated VME registers. Users may write temperature or voltage values at VMEbus speed, and the microprocessor will transparently do all necessary calculations and update the channel electronics. Available ranges are listed in section 5.3.12.

Four separate, non-isolated, 4-wire RTD signal conditioners are provided for reference junction sensing. A fifth internal reference-junction temperature sensor is provided on the printed circuit board adjacent to the two D25 output connectors.

An internal microprocessor manages all operations and communicates with the VME bus via a transparent VMEbus-speed dual-port memory.

The V470 includes lookup tables for all common thermocouple types so that users may write desired temperatures directly to VME registers. In thermocouple simulation mode, any channel can be associated with any of the reference junction sensors, located in the external field-wiring termination panels, or the on-board sensor. Cold-junction compensation is done via table lookup of thermocouple potential for the type currently selected. Reference junction temperatures are readable.

Two front-panel D-25 connectors are used to interface to external analog devices. Each connector provides eight differential outputs and connections for two 4-wire RTDs.

A front-panel D9 test connector is provided for in-crate calibration check. Each isolated channel incorporates a software-controlled DPDT relay which allows the channel output to be diverted to two pins of the test connector. This relay function can also be used for open thermocouple simulation. Other pins of the test connector allow verification of the accuracy of the reference-junction RTD measurement subsystem.

An optional BIST subsystem adds additional switching and an on-board ADC and firmware that allows the invocation of a full closed-loop test of all ranges of all 16 channels. BIST is available on module revision B and later.

Thermocouple linearization is based on NIST/ITS-90 polynomials; RTD data is per IEC-751 for 385 curve platinum RTDs. Units are calibrated against a Keithley digital voltmeter accurate to 20 PPM and traceable to NIST.

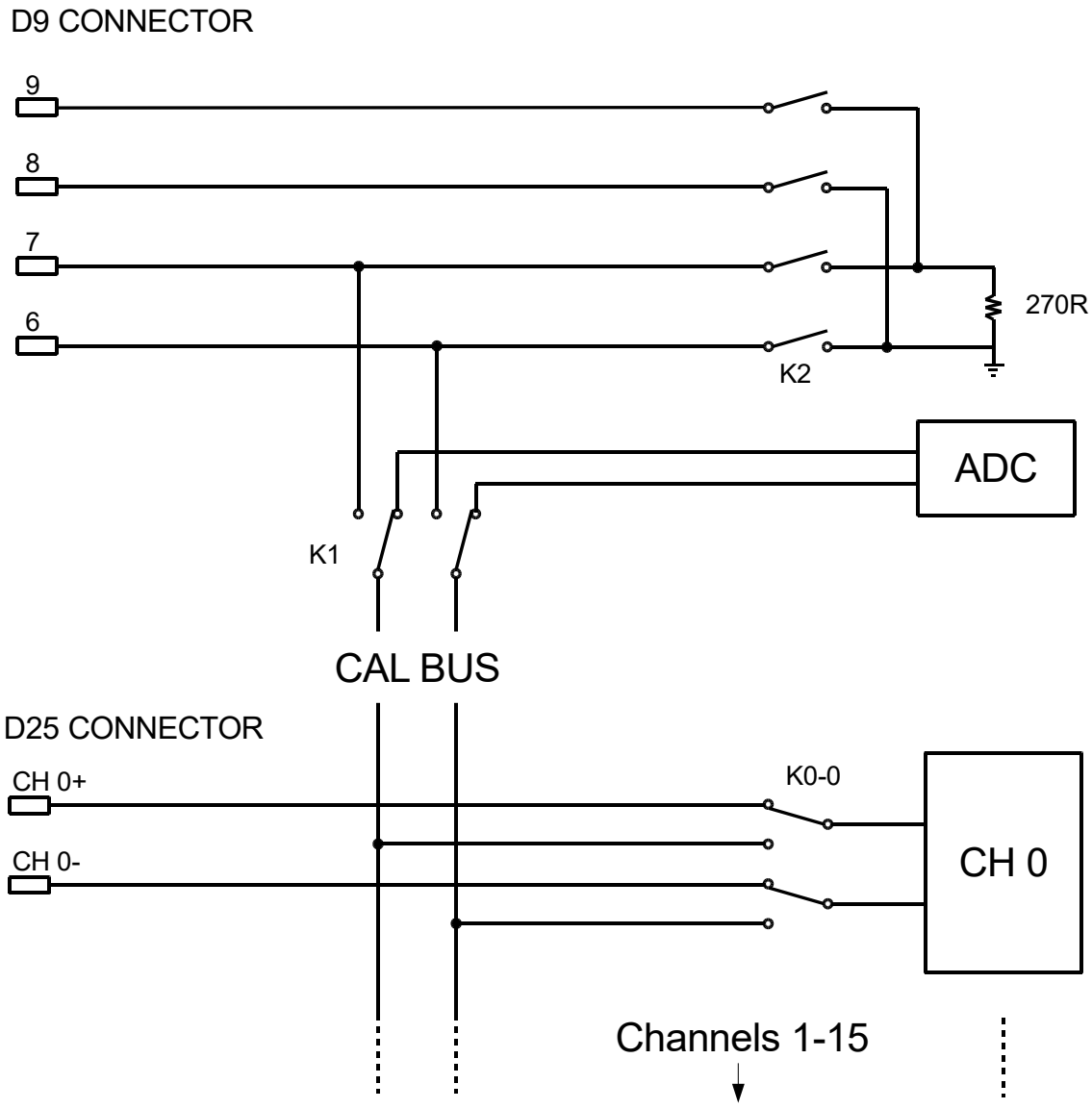


Figure 1. Functional diagram of the V470

4. Connectors and Installation

4.1 Address DIP Switches

The V470 appears as 256 16-bit registers in the VME 16 or 24-bit addressing spaces. The base address of the 256 registers is set by four 4-position rocker-type DIP switches, positioned near the top edge of the board. They are labeled, left to right, "A23" through "A9" and finally "A24M". Switches A23 through A9 set the base module address. This address is always a multiple of 512 bytes.

To set a switch to the logical 1 or ON position, press the side of the switch nearest its "Axx" lettering. Use a toothpick or paper clip, not a pen or pencil.

The A24M switch, when set, allows the board to operate in the VME 24-bit (A24) address space; in this case, all address switches are active and the board responds to VME address modifier codes 0x39 and 0x3D.

If the A24M switch is off, the module resides in the A16 space and responds to address modifiers 0x29 and 0x2D. In this case, only address switches A15 through A9 are active.

Units are shipped with switches A15 and A14 on, all others off, locating the register base at 0xC000 in the A16 space, as shown in the figure below:

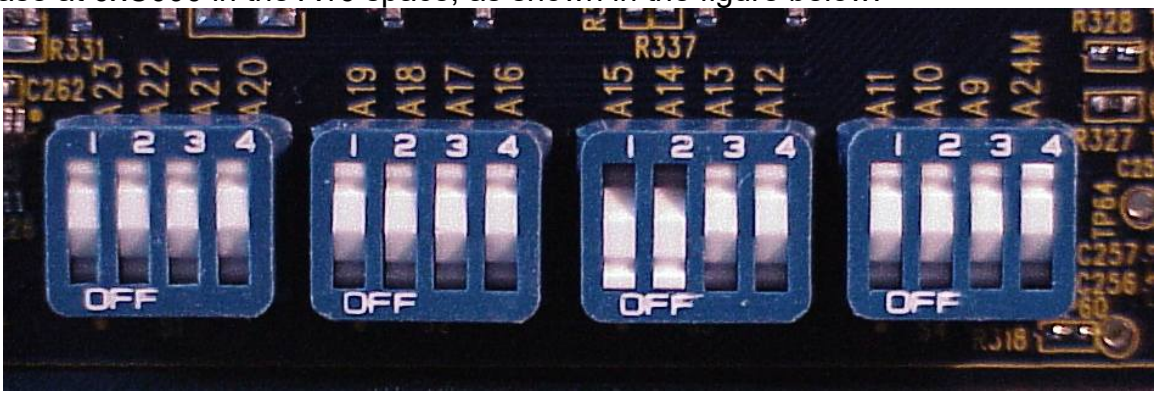


Figure 2. Address DIP switches

4.2 Installation

The V470 may be installed in any VME (IEEE 1014) crate, including VME64 variants. It uses only the P1 backplane connector and the +5 and +12 volt supplies.

The V470 passively passes all interrupt and bus grant signals, so may be used with backplane grant jumpers installed or not installed.

CAUTION: Do not install or remove the V470 with crate power on. VME modules are not hot-pluggable and will be damaged if hot-plugged.

Fully seat the module and secure front-panel screws before applying power.

Handle the V470 with proper ESD precautions to avoid static damage.

4.3 D25 Output Connectors

Two front-panel female D-25 connectors are provided to interface to external analog devices. Each connector accommodates eight differential outputs and two 4-wire RTD reference junction sensors.

The pinouts of the D25 connectors are as follows:

J1-1	ch 0+	J2-1	ch 8+		
J1-14	ch 0-	J2-14	ch 8-		
J1-2	ch 1+	J2-2	ch 9+		
J1-15	ch 1-	J2-15	ch 9-		
J1-3	ch 2+	J2-3	ch 10+		
J1-16	ch 2-	J2-16	ch 10-		
J1-4	ch 3+	J2-4	ch 11+		
J1-17	ch 3-	J2-17	ch 11-		
J1-5	ch 4+	J2-5	ch 12+		
J1-18	ch 4-	J2-18	ch 12-		
J1-6	ch 5+	J2-6	ch 13+		
J1-19	ch 5-	J2-19	ch 13-		
J1-7	ch 6+	J2-7	ch 14+		
J1-20	ch 6-	J2-20	ch 14-		
J1-8	ch 7+	J2-8	ch 15+		
J1-21	ch 7-	J2-21	ch 15-		
J1-9	RtdA E+	J2-9	RtdC E+	}	RTD excitation
J1-22	RtdA E-	J2-22	RtdC E-	}	
J1-10	RtdA S+	J2-10	RtdC S+	}	RTD sense
J1-23	RtdA S-	J2-23	RtdC S-	}	
J1-11	RtdB E+	J2-11	RtdD E+	}	RTD excitation
J1-24	RtdB E-	J2-24	RtdD E-	}	
J1-12	RtdB S+	J2-12	RtdD S+	}	RTD sense
J1-25	RtdB S-	J2-25	RtdD S-	}	
J1-13	VME GND	J2-13	VME GND		

The RTD E- pins are also VME ground.

Connector shells are bonded to the VME front panel, which connects to the crate frame through the module securing screws.

4.4 D9 Test Connector

A male test D9 connector is provided for connection to an external precision DVM. Each output channel incorporates a relay (K0) which allows it to be switched, using the RELAYS register, to the CAL bus. The MODE register can be used to connect the D9 connector to either the CAL bus (through K1) or the RTD subsystem check resistor (through K2). These modes make it possible to externally verify the channel output and reference junction accuracy.

Pinout of the D9 is

P3-7	CAL bus (+), test resistor source (+)	
P3-6	CAL bus (-), test resistor source (-)	
P3-9	test resistor sense (+)	
P3-8	test resistor sense (-)	
P3-1	VME GND	(Disconnected on rev. D and later)
P3-2	VME GND	(Disconnected on rev. D and later)
P3-3	VME GND	(Disconnected on rev. D and later)
P3-4	VME GND	(Disconnected on rev. D and later)

Activating a channel test relay will disconnect that channel from the D25 connector and reroute it to the D9 connector, thus simulating an open thermocouple.

Refer to section 6 of this manual for a discussion of module calibration verification.

4.5 Front-Panel LEDs

The blue VME LED will flash whenever the V470 is addressed from the VME bus.

The green CPU LED will blink about once every two seconds to indicate that the internal firmware is operating normally. If the MODE register is set to be nonzero, the CPU LED will blink twice as a warning that the module is in a maintenance mode.

The red ERROR LED will normally be off. Blink patterns are

One blink	Channel error detected
Two blinks	RTD acquisition error
Three blinks	RTD system self-check error
Four blinks	Calibration table error
Five blinks	FPGA configuration error

The last three blink patterns indicate fatal hardware problems.

The orange USER LED may be programmed from the VME bus, as described in section 5.3.6.

For modules with the BIST option, the green LED will blink rapidly while self-test sequences are active, and the red LED will come on solid if any error is detected. Both will resume normal operation about one second after all self-tests have finished.

5. Programming

5.1 General Considerations

All registers are implemented as true dual-port memory which is shared between the VME bus and the internal microprocessor.

Typical VME access time is under 500 ns, measured from DS* to DTACK*.

The V470 does not support single-byte writes from VME.

5.2 Quick Start Procedure

Basic operation of the V470 can be demonstrated by the following steps:

A 6U VME crate and computer interface are required. The crate must be compliant with the IEEE 1014 VME specification, or the equivalent ANSI/VITA 1-1994 (R2002) VMEbus spec. Any crate with the standard power supplies (+12, +5, -12) and the 16-bit P1 bus is adequate.

The computer interface must allow, as a minimum, reading and writing 16-bit registers in the A16 or A24 address spaces.

Pick an address space and module base address and set the V470 dip switches accordingly. See section 4.1. The as-shipped default is address 0xC000 in the 16-bit supervisory address space.

With crate power off, insert the V470 into any crate slot and firmly secure its mounting screws. **Do not hot-plug VME modules.**

Power up. The green CPU LED should blink, and the other LEDs should be off.

Now run software that can display the contents of VME registers.

Read the manufacturer ID register, the 16-bit VME register at the module base address. The default address would be 0xC000 in the A16 supervisory space. The blue VME LED should flash, and the register value should be 0xFEEE, identifying this as a Highland VME module.

Read the next register, offset address 0x02, default 0xC002. It should read 22470 decimal, 0x57C6, identifying the module as a V470.

By default, every channel is off and output is 0V. Write 0x0007 to the first CTL register, offset address 0x82, default 0xC082. This sets channel 0 to the 1.25V output range. Now write 0x6666 to the first VAL register, offset address 0x80, default 0xC080. This sets the output to 1V.

There should now be 1V output between pins 1 and 14 of the D25 connector, J1.

5.3 VME Registers

REG# below is the ordinal register number in decimal. OFFSET is the hex VMEbus offset from the module base address.

Read-only (RO) registers should not be written from VME; these registers are periodically refreshed by the microprocessor.

Read-write (RW) registers are normally written by VME and are not altered by the internal microprocessor. Only MACRO and the associated macro parameter registers are written by both VME and the microprocessor, and a macro handshake protocol is defined in section 5.3.9.

Registers flagged as "**" are active only with the BIST option. BIST registers are described in section 7.

REG Name	REG#	Offset	R/W	Function
VXI MFR	0	0x00	RO	VXI mfr ID: reads 65262, 0xFEEE
VXITYPE	1	0x02	RO	Module type, always 22470, 0x57C6
SERIAL	3	0x06	RO	Unit serial number
ROM ID	4	0x08	RO	Firmware ID, typically 22471 decimal
ROM REV	5	0x0A	RO	Firmware revision, typically ASCII "A"
MCOUNT	6	0x0C	RO	Microprocessor IRQ update counter
CFLAGS	8	0x10	RO	Channel error flags
RFLAGS	9	0x12	RO	RTD and misc. error flags

REG Name	REG#	Offset	R/W	Function
RELAYS	11	0x16	RW	Controls calibration-bus relays
ULED	12	0x18	RW	User LED control
MODE	13	0x1A	RW	Module operating mode
CALID	14	0x1C	RO	Calibration table status
BISS	15	0x1E	RO	BIST status register **
MACRO	16	0x20	RW	Macro command register
PARAM0	17	0x22	RW	Macro parameter
PARAM1	18	0x24	RW	Macro parameter
PARAM2	19	0x26	RW	Macro parameter
YCAL	24	0x30	RO	Calibration date: year
DCAL	25	0x32	RO	Calibration date: month/day
RTDA	32	0x40	RW	RTD A control
TMPA	33	0x42	RO	RTD A temperature
RTDB	34	0x44	RW	RTD B control
TMPB	35	0x46	RO	RTD B temperature
RTDC	36	0x48	RW	RTD C control
TMPC	37	0x4A	RO	RTD C temperature
RTDD	38	0x4C	RW	RTD D control
TMPD	39	0x4E	RO	RTD D temperature
TMPR	40	0x50	RO	Onboard ref junction (PCB) temperature
RAHI	44	0x58	RO	RTD A resistance, ohms
RALO	45	0x5A	RO	RTD A resistance, fractional ohms
RBHI	46	0x5C	RO	RTD B resistance, ohms
RBLO	47	0x5E	RO	RTD B resistance, fractional ohms
RCHI	48	0x60	RO	RTD C resistance, ohms

REG Name	REG#	Offset	R/W	Function
RCLO	49	0x62	RO	RTD C resistance, fractional ohms
RDHI	50	0x64	RO	RTD D resistance, ohms
RDLO	51	0x66	RO	RTD D resistance, fractional ohms
TRHI	52	0x68	RO	Test resistor resistance, ohms
TRLO	53	0x6A	RO	Test resistance, fractional ohms
BIVH	54	0x6C	RO	BIST loopback voltage, MS **
BIVL	55	0x6E	RO	BIST loopback voltage, LS **
FAKE1	60	0x78	RW	User-supplied fake reference temp
FAKE2	61	0x7A	RW	User-supplied fake reference temp
VAL0	64	0x80	RW	Channel 0 value
CTL0	65	0x82	RW	Channel 0 control
DVL0	66	0x84	RO	Channel 0 DAC level
VAL1	68	0x88	RW	Channel 1 value
CTL1	69	0x8A	RW	Channel 1 control
DVL1	70	0x8C	RO	Channel 1 DAC level
VAL2	72	0x90	RW	Channel 2 value
CTL2	73	0x92	RW	Channel 2 control
DVL2	74	0x94	RO	Channel 2 DAC level
VAL3	76	0x98	RW	Channel 3 value
CTL3	77	0x9A	RW	Channel 3 control
DVL3	78	0x9C	RO	Channel 3 DAC level
VAL4	80	0xA0	RW	Channel 4 value
CTL4	81	0xA2	RW	Channel 4 control
DVL4	82	0xA4	RO	Channel 4 DAC level

REG Name	REG#	Offset	R/W	Function
VAL5	84	0xA8	RW	Channel 5 value
CTL5	85	0xAA	RW	Channel 5 control
DVL5	86	0xAC	RO	Channel 5 DAC level
VAL6	88	0xB0	RW	Channel 6 value
CTL6	89	0xB2	RW	Channel 6 control
DVL6	90	0xB4	RO	Channel 6 DAC level
VAL7	92	0xB8	RW	Channel 7 value
CTL7	93	0xBA	RW	Channel 7 control
DVL7	94	0xBC	RO	Channel 7 DAC level
VAL8	96	0xC0	RW	Channel 8 value
CTL8	97	0xC2	RW	Channel 8 control
DVL8	98	0xC4	RO	Channel 8 DAC level
VAL9	100	0xC8	RW	Channel 9 value
CTL9	101	0xCA	RW	Channel 9 control
DVL9	102	0xCC	RO	Channel 9 DAC level
VAL10	104	0xD0	RW	Channel 10 value
CTL10	105	0xD2	RW	Channel 10 control
DVL10	106	0xD4	RO	Channel 10 DAC level
VAL11	108	0xD8	RW	Channel 11 value
CTL11	109	0xDA	RW	Channel 11 control
DVL11	110	0xDC	RO	Channel 11 DAC level
VAL12	112	0xE0	RW	Channel 12 value

REG Name	REG#	Offset	R/W	Function
CTL12	113	0xE2	RW	Channel 12 control
DVL12	114	0xE4	RO	Channel 12 DAC level
VAL13	116	0xE8	RW	Channel 13 value
CTL13	117	0xEA	RW	Channel 13 control
DVL13	118	0xEC	RO	Channel 13 DAC level
VAL14	120	0xF0	RW	Channel 14 value
CTL14	121	0xF2	RW	Channel 14 control
DVL14	122	0xF4	RO	Channel 14 DAC level
VAL15	124	0xF8	RW	Channel 15 value
CTL15	125	0xFA	RW	Channel 15 control
DVL15	126	0xFC	RO	Channel 15 DAC level

Registers 128-255 are reserved for BIST.

Note that Registers 44-55 report 32-bit values. Each value pair is atomically interlocked to avoid the possibility of a collision between a microprocessor update and a VME read, which could result in incoherent data. To guarantee coherent data, the VME user must read the first word of each pair and then read the second word of that same variable. If only the most significant (MS) word of the pair is of interest, it may be read alone at any time.

5.3.1 Module Overhead Registers

A group of read-only, fixed-value registers identify the module. They include

VXI MFR: always reads 0xFEEE, Highland's registered VXI ID code.

VXITYPE: always reads 22470 decimal for the V470-1

SERIAL: module serial number

ROM ID: firmware version, typically 22471 decimal

ROM REV: an ASCII code identifying the revision letter of the firmware, typically 0x41 for the letter "A"

5.3.2 MCOUNT Register

The read-only MCOUNT register is an unsigned 16-bit integer which is incremented every microprocessor interrupt, namely every 4.096 milliseconds, or at a rate of 244.14 Hz.

5.3.3 CFLAGS Channel Error Flags

The read-only CFLAGS register displays 16 channel error flags, with bits 0-15 corresponding to output channels 0-15.

15	14	13	12	11	10	9	8
E15	E14	E13	E12	E11	E10	E9	E8
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0

An error flag will be set if a channel is improperly programmed or if a channel is programmed as a thermocouple simulator and its corresponding RTD is disabled or in an error state. Error bits will self-clear if the channel returns to normal operation.

5.3.4 RFLAGS RTD Error Flags

This register displays error flags for the four external RTD reference-junction temperature sensors and several miscellaneous conditions.

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
LM71	FPGA	CERR	ERRT	ERRD	ERRC	ERRB	ERRA

Bits 0-3 flag errors in acquiring RTDs A-D, respectively. If an RTD is programmed as "unused" (RT code 0) its error bit will not be active. An RTD error can result from an RTD resistance being out of the legal range (-65 to +150°C equivalent), open or incorrectly wired excitation or sense connections, shorts between wires or to ground, or excessive (over about 25 ohms per leg) leadwire resistance.

The ERRT bit will be set if the onboard self-test resistor appears to be out of range, indicating that the RTD measurement subsystem is not operating normally.

The CERR bit will be set if the module calibration table is corrupted.

If the FPGA bit is set, either the Control or VME FPGAs has a configuration problem. If the VME FPGA does not configure properly, it is likely that no VME operations can be executed at all.

The LM71 bit will be set if the onboard semiconductor temperature sensor is defective or the board temperature is outside of the range -20 to +80°C.

5.3.5 RELAYS Register

The RELAYS register controls the sixteen channel test relays.

15	14	13	12	11	10	9	8
K0-15	K0-14	K0-13	K0-12	K0-11	K0-10	K0-9	K0-8
7	6	5	4	3	2	1	0
K0-7	K0-6	K0-5	K0-4	K0-3	K0-2	K0-1	K0-0

If the user sets any bit, the corresponding channel test relay will be actuated. The analog output of the associated channel will then be disconnected from the front-panel D25 connector and routed to the internal CAL bus, which may in turn be routed to pins 7 and 6 of the D9 test connector.

More than one relay may be operated at any time, resulting in the outputs of selected channels being connected in parallel. The resulting calibration signal will not be meaningful, but channels will not be damaged.

Actuating a channel relay will simulate an open thermocouple.

See section 6 for a discussion of using the D9 connector for verification of module accuracy. Section 7 discusses the use of the RELAYS register in BIST loopback mode.

5.3.6 ULED User LED Control

An orange LED is provided on the front panel for user application. The ULED register allows user flash patterns to be loaded. An internal shift register is periodically loaded from the contents of the ULED register, and the MS bit of this register operates the orange LED. The shift register is left-shifted every 250 milliseconds, and the register is reloaded every 16 shifts, namely every 4 seconds.

ULED pattern 0x0000 turns the user LED off. Pattern 0xFFFF turns it steady on. Pattern 0xF000 would result in a blink pattern, 1 second on and 3 seconds off.

5.3.7 MODE Register

15	14	13	12	11	10	9	8
							OFF
7	6	5	4	3	2	1	0
						M1	M0

Users may set the MODE bits M1:M0 to values 0, 1, or 2. Zero is the normal operating mode.

If mode = 1, relay K1 is actuated and the module's internal CAL bus is connected to the D9 connector pins 7 and 6, allowing an external DVM to monitor the output of any channel whose test relay is actuated. Any channels whose relays are not operated will continue to function normally.

If mode = 2, relay K2 is actuated and an external 4-lead digital voltmeter may be used to measure the value of the internal self-check resistor, nominally 270 ohms. Its measured value should agree with the value reported in the TRHI:TRLO registers to within 250 PPM. In this mode, external RTD reference junction scanning is suspended and the associated reference junction temperatures frozen.

Setting the OFF bit will disable the isolated power supplies to all 16 output channels, reducing module power consumption by about 8 watts.

5.3.8 CALID Register

The CALID register displays a value which reflects the currently installed calibration table. The normal value for the standard V470 module is 22470 decimal, 0x57C6. If the factory calibration table is corrupted, the firmware will install the default calibration table, the CALID register will display value 0xDEFC, the CERR bit will appear in the RFLAGS register, and the red LED will flash.

5.3.9 MACRO Register

Users may elect to write a 16-bit code into the MACRO register to initialize the module and/or set up all RTD and channel parameters to a common configuration. To do this

Verify that bit 15 of the MACRO register is clear, indicating that the microprocessor is ready to accept a command

Write a 16-bit macro code to MACRO

Wait until bit 15 clears. If any other MS byte bits are then set, an error has occurred.

Execution time will be no greater than the times noted below.

MACRO codes are as follows:

Code	Operation	Time
0x8400	no operation	5 ms
0x8401	All channels are type J thermocouple out, with all using the internal reference junction.	5 ms
0x8402	All channels are type K thermocouple out, with all using the internal reference.	5 ms
0x8403	All channels are type E thermocouple out, with all using the internal reference.	5 ms
0x8404	All channels are type T thermocouple out, with all using the internal reference.	5 ms
0x8405	All channels are ±12.5 volt output.	5 ms
0x8406	All channels are ±80 mV output.	5 ms
0x8407	All channels are ±25 mV output.	5 ms
0x8410	BIST: test all	80 s
0x8411	BIST: test one channel	5 s
0x8420	Hard reboot; reloads FPGAs, restarts code; disappears from VMEbus for about 4 seconds	5 s

0x8421	Soft reboot the module; remains on bus.	2 s

5.3.10 RTD Control Registers

There are four external RTD temperature sensor channels, each with an associated register block. The RTDs are called RTDA through RTDD, either customer supplied or within a J470 termination box. An internal semiconductor temperature sensor is also provided on the module, adjacent to the two D25 input connectors. Any of these sensors may be selected as the reference junction used by any of the 16 output channels when they are operated in thermocouple simulation mode.

The register, RTDn, associated with each RTD is arranged as follows:

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
						RT1	RT0

where the encoded RT bits declare the RTD type.

RT Code	RTD Type
0	RTD channel is unused
1	100 ohm platinum, ISO 385 curve
2	1K ohm platinum, ISO 385 curve

If any RTD is programmed to be active and the sensed temperature is out of acquisition range or a measurement error is detected, an RTD error flag will be reported in RFLAGS. Any analog output channel which references a failed or disabled RTD will also report a channel error in the CFLAGS register.

5.3.11 RTD Temperature Registers

Each RTD has a realtime temperature reporting register TMPn, which presents temperature in module-standard format, namely degrees C times 16. The V470 is capable of measuring RTD temperatures from -65 to +150°C.

If an RTD is programmed as unused, its temperature will be reported as zero, 0x0000 in the register. If an RTD is programmed as a 100 or 1K ohm type, and a measurement error is sensed in acquiring its temperature, its temperature will be reported as 0x8000, equivalent to -2048°C.

Any thermocouple simulation channel which references an unused RTD or one having an error will report a channel error flag in CFLAGS and output a signal as if using a 0°C reference.

The resistance of each RTD channel is also reported as a 32-bit value, with the MS word being resistance in ohms and the least significant (LS) word being a 16-bit fractional-ohm extension. The RnHI : RnLO register pair would thus contain 0x0064 : 0x8000 to indicate 100.5 ohms. A reported resistance of 0x8000 : 0x0000 indicates a resistance acquisition error.

The RTD resistance registers are interlocked to ensure atomic reads: so the microprocessor does not change the data in between VME reads of the two words. To ensure coherence, it is required that any pair of resistance registers be read in the order RnHI : RnLO.

5.3.12 Channel Control Registers and Ranges

Each of the 16 isolated output channels has an associated channel control register, CTL0 through CTL15. The control register arrangement is

15	14	13	12	11	10	9	8
					RS2	RS1	RS0
7	6	5	4	3	2	1	0
			RN4	RN3	RN2	RN1	RN0

The RN bits select the output type and range for this channel, with the five RN bits encoded 0 through 31, decimal. Ranges are

RN Code	Channel Type	Range	VALn reg LSB
0	off	0 volts out	
1	voltage	± 25 mV	0.763 uV
2	voltage	± 50 mV	1.526 uV
3	voltage	± 80 mV	2.441 uV
4	voltage	± 125 mV	3.815 uV
5	voltage	± 250 mV	7.629 uV

6	voltage	± 500 mV	15.26 uV
7	voltage	± 1.25v	38.15 uV
8	voltage	± 2.50v	76.29 uV
9	voltage	± 5.00v	152.6 uV
10	voltage	± 12.5v	381.5 uV
16	Type J TC	-210 to 1200°C	0.0625°C
17	Type K TC	-270 to 1372°C	0.0625°C
18	Type E TC	-270 to 1000°C	0.0625°C
19	Type T TC	-270 to 400°C	0.0625°C
20	Type R TC	-50 to 1768°C	0.0625°C
21	Type S TC	-50 to 1768°C	0.0625°C
22	Type B TC	0 to 1820°C	0.0625°C
23	Type N TC	-270 to 1300°C	0.0625°C

Selection of an undocumented range will result in zero volts out and will set a channel error flag.

The three RS bits select which sensor is used for reference junction compensation for this channel. These bits apply to thermocouple modes only, and are ignored in voltage output modes.

RS Code	**RTD Used**	**Connector Pins**	**Notes**
0	RTD A	J1 9 10 22 23	External RTD
1	RTD B	J1 11 12 24 25	External RTD
2	RTD C	J2 9 10 22 23	External RTD
3	RTD D	J2 11 12 24 25	External RTD
4	internal	n/a	Internal reference
5	FAKE1	n/a	User-supplied ref temp
6	FAKE2	n/a	User-supplied ref temp
7	none	n/a	0°C equivalent

In the case of RS code 4, thermocouple-alloy extension leads should be wired directly to the D25 male connectors which plug into the V470 front panel. Because the front panel and connectors are not a well-controlled isothermal environment, this mode can be expected to be less accurate than using an external isothermal reference junction box with associated RTD sensor.

RS selections 5 or 6 use a temperature specified by the user in the FAKE1 or FAKE2 registers as the effective reference junction temperature, with temperature specified in module-standard format of °C times 16. This allows other data acquisition systems to acquire and furnish reference junction temperature. These programmed values must be in the range of -65 to +150°C.

Selection 7 simulates using a reference junction at 0°C (ice point).

A channel error will result if the selected RTD is disabled or presents a resistance that is out of range.

5.3.13 Channel Value Registers

Channel output levels are set by the user writing to the sixteen channel value registers VAL0 through VAL15. The 16-bit numerical values express either voltages in range-fractional form or temperatures in module-standard form, as described in section 5.4. Channel control and value registers may be written in any order at any time.

5.3.14 DAC Level Registers

Each output channel has a read-only DAC level register, named DVL0 through DVL15. Each displays the last fractional value which was loaded into the channel DAC hardware. If a channel is programmed to be a voltage type, the value, after the channel is updated, will be identical to the VALn programmed value.

If the channel is a thermocouple type, the value is derived from the programmed temperature in VALn, adjusted by any reference-junction compensation offset. The full-scale signed fractional value is ±80 millivolts for thermocouple types J, K, and E; ±50 mV for type N; and ±25 mV for types T, R, S, and B.

5.3.15 Calibration Date

The YCAL and DCAL registers display the date of last factory calibration. YCAL is the year, with year 2005 presented as integer 2005, 0x07D5. DCAL presents the month in its MS byte and day in its LS byte; March 15 would then be 0x030F.

5.4 Voltage and Temperature Scaling

If a channel is selected to be a voltage output, the channel value register, VALn, is scaled as a signed, 16-bit fractional value spanning the selected range. For example, if the channel control RN field were set to 10 decimal, selecting the ±12.5 volt range, scaling of the VALn register would be:

DECIMAL	HEX	FRACTIONAL	VOLTAGE OUT
+32767	0x7FFF	+0.999969	+12.49996
+16384	0x4000	+0.500000	+6.250000
+00001	0x0001	+0.000031	+0.000381
00000	0x0000	+0.000000	0.000000
-00001	0xFFFF	-0.000031	-0.000381
-16384	0xC000	-0.500000	-6.250000
-32768	0x8000	-1.000000	-12.50000

Temperatures are always scaled as a signed integer representing temperature in °C times 16. The full-scale range is thus ±2048°C. Examples are

DECIMAL	HEX	TEMP, °C
+32767	0x7FFF	+2047.93
+16384	0x4000	+1024.00
+00001	0x0001	+0.06250
00000	0x0000	0.00000
-03200	0xF380	-200.000

If a temperature is loaded which is beyond the range defined for that thermocouple type, a channel error will be declared and the actual simulated temperature will clamp at the appropriate high or low defined limit.

Resolution is thus 1/16 (0.0625) °C, equivalent to 0.1125 ºF. The same format is used to report RTD temperatures. If an RTD is disabled or a measurement error is sensed, its temperature will be reported as 0x8000, equivalent to -2048°C.

6. Calibration Verification

The calibration of one or more V470 modules may be verified in their operating VME crate.

The V470 module or modules should be connected to a precision digital voltmeter, such as a Keithley 2000 or equivalent. The required connections are

D9 PIN	DVM CONNECTION	FUNCTION
P3-7	INPUT HI	channel output (+), test resistor source (+)
P3-6	INPUT LO	channel output (-), test resistor source (-)
P3-9	SENSE HI	test resistor sense (+)
P3-8	SENSE LO	test resistor sense (-)

To verify a channel output, set the MODE register to 1 and set the bit in the RELAYS register corresponding to that channel. Now the channel output will be diverted into the DVM voltage input leads. Users may then program the channel and verify accuracy using DVM measurements.

Note that the channel ±25 mV range is used for thermocouple types T, R, S, and B, and the ±80 mV range is used for types J, K, and E. Type N uses the ±50 mV range.

To verify the accuracy of the RTD measurement subsystem, operate the module normally (MODE = 0) and note the resistance reported in the TRHI:TRLO 32-bit register pair. Then set the MODE register to 2 and use the DVM to make a 4-wire resistance measurement of the module's internal test resistor. The reading of the DVM should be 270 ohms ±0.25% and should agree with the reported TRHI:TRLO value to within 250 PPM, equivalent to an RTD temperature measurement error of 0.0625°C. Clear the MODE register to resume normal operation.

If the voltage-mode outputs and RTD subsystem are accurate, then thermocouple simulation will be correct.

The D9 connector pins of multiple V470 modules may be bussed in parallel to a single precision DVM, provided that only one module is operating in a non-zero MODE at any one time.

Highland can furnish a suitable multi-station cable assembly if desired.

7. Built-in Self-Test (BIST)

The V470-2 version is equipped with a BIST facility. This allows module functionality and accuracy to be verified with a high degree of confidence. Note that BIST cannot allow absolute verification of module accuracy, as external NIST-traceable standards are required for formal calibration.

When BIST is available, the registers which are flagged “**” in section 5.3 are active, and the corresponding BIST macros are available, as noted in section 5.3.9.

BIST adds an analog-to-digital converter (ADC) path that allows the module firmware to access the internal calibration bus. When a channel's test relay is activated, connecting the channel output to the CAL bus, the ADC can measure and report the channel output.

Although the BIST operations can detect most module failures, certain errors can be missed. They include

Failure of a channel test relay.

Failure of a connector pin or associated printed-circuit traces.

Failure of certain RTD multiplexer paths; such failures will, however, probably cause an RTD measurement error to be reported.

Two self-test facilities are provided for modules having the BIST option: Loopback Mode and Automatic BIST mode.

7.1 Loopback Mode

Loopback mode is a non-automatic BIST function in which the module internally reads a channel output voltage.

To perform loopback mode BIST, MODE must be set to 0. The RELAYS bit corresponding to the channel to be read should be set. The channel output voltage will appear in the BIVH:BIVL register pair, scaled as a signed 32-bit fractional value having range ±16 volts. All other module operations, including normal service of all 16 output channels, will continue. Loopback mode is not associated with the BISS register except that the BAV bit must be up. The loopback measurement may take up to 2 seconds.

For example, one could set the RELAYS register to 0x0010, actuating the test relay of output Channel 4. Then any analog output programmed for Channel 4 would be readable in BIVH:BIVL. If Channel 4 were then programmed for +10 volts output, the loopback data would appear as fractional value 10/16 = 0.625, with the hex register pair displaying 0x5000 : 0x0000. The 32-bit value in BIVH:BIVL may then be viewed as a signed 32-bit integer having an LSB value of 7.45058 nV.

The loopback ADC accuracy is input-voltage dependent. For voltages above 0.470 volts, accuracy is ±250 PPM of reading ±100 uV; for voltages below 0.470, accuracy is ±250 PPM ±10 uV.

Like all other 32-bit values, the MS word (BIVH) should be read before the LS word (BIVL) to ensure coherent data. BIVH may also be used alone as a 16-bit signed fractional. These registers read zero if the BIST option is not present.

7.2 BISS Register

Automatic self-tests are invoked as module macros and use the dedicated BISS register to indicate status.

15	14	13	12	11	10	9	8
BCH	BCS	ISO	RTF	TSF			
7	6	5	4	3	2	1	0
BSY							BAV

The BAV bit will be set if the BIST option is available. If it is not available, the entire BISS register will be cleared.

BSY will be set while automatic self-tests are running.

BCS will be set if automatic BIST tests discover a "soft" channel error and BCH will be set if they discover a "hard" error. A soft error is defined as an output channel error above ±1000 PPM, and a hard error is a channel error beyond ±2%.

The ISO bit will be set if electrical leakage is detected from a channel common to module ground. The threshold is about 450K ohms.

The RTF bit will be set if an error is detected in the RTD acquisition subsystem.

The TSF will be set if an error is detected in the local reference junction temperature sensor.

7.3 Automatic BIST Mode

Automatic self-tests are provided by means of BIST macro operations, using the MACRO register and associated parameters. Its status and results are reported in the BISS register.

Loading the MACRO register with 0x8410 performs a full module test. The RTD subsystem and the internal reference temperature sensor are checked, then each of the 16 channels is tested on each of its ten electrical output ranges, using three points per range. Channel isolation is checked, and the RTD measurement subsystem is verified for accuracy. Total test time is about 80 seconds. The test may be aborted by clearing the MACRO register. At the end of the test, the BIST register will indicate if any errors were detected.

Macro 0x8411 allows an individual channel to be tested. Load the PARM0 register with channel number 0-15 before executing the macro. The RTD subsystem and internal temperature sensor are not tested.

Test time is about 5 seconds per channel. Again, the BIST register will summarize test results. While any channel is being tested, the channel test relay is operated, disconnecting the output channel from the front-panel D25 connector. When a channel test is finished, the channel output is restored to its normal programmed level and the relay de-energized to restore normal operation.

The green CPU LED will blink rapidly during automatic BIST operations. The red LED will go on solid if any error is detected, and will resume normal operation after the BIST sequence.

If any errors are reported in the BIST register, users may elect to review each error in detail. The block of registers from 128 to 255 are reserved for BIST error reports and are all cleared at the start of execution of either of the BIST macros. If any errors are detected during the automatic BIST operation, each error will generate a 6-word error report in this block of registers, with the first report posted to registers 128-133 and additional errors posted to sequential 6-word blocks, for a maximum of 21 errors. The six words in each error report block are arranged

0 Error summary word
1 null
2 MS word of expected value
3 LS word of expected value
4 MS word of actual value
5 LS word of actual value

The error summary word is

15	14	13	12	11	10	9	8
BCH	BCS	ISO	RTF	TSF			
7	6	5	4	3	2	1	0
ER3	ER2	ER1	ER0	EC3	EC2	EC1	EC0

EC3-EC0 specify a channel, 0-15. ER3-ER0 specify a range and are encoded

1	25	mV
2	50	mV
3	80	mV
4	125	mV
5	250	mV
6	500	mV
7	1.25	V
8	2.5	V
9	5.0	V
10	12.5	V

The BCH-TSF bits specify an error condition; they are defined the same as their corresponding bits in the BISS register and are described in section 7.2.

An error summary word that is all zeroes indicates that no more errors have been posted.

A nonzero error summary word is followed by a zero word then four value words. The first two words are the expected value, as a 32-bit fractional, and the last two are the actual (measured) value. These fractional values are channel voltages scaled to ±16 volts.

For isolation errors, the fractional value is voltage drop across a current sense resistor, with the expected value being zero. The error limit is ±1 millivolt, equivalent to about 450 Kohms to ground.

If an RTF error is reported, the expected value is 270 ohms, and the actual value is the measured value of the on-board precision test resistor. Both are expressed as an MS word of integer ohms and LS word of fractional ohms.

If the TSF error is posted, the expected value is 25°C and the actual value is the internal reference junction sensor temperature These are expressed in the LS word only, in degrees C times 16.

When the full test macro is executed, a maximum of four errors are reported per channel. For either of the BIST macros, a maximum of 21 errors are posted in the reporting space, VME words 128-253. In either case, all programmed tests are actually performed and the appropriate error flags are set in the BISS register.

VME register 254 displays the currently-under-test range and channel (as 0x00RC where R is range and C is channel) and location 255 displays the total number of errors detected, with a possible maximum of 498.

8. Realtime Considerations

The V470 firmware execution includes an inner loop which scans all 16 channels looking for changes in the VALn registers. If any VAL register has changed from the previous scan, the new value is processed and loaded into the channel DAC hardware.

After each channel VAL scan, one overhead sub-task, called a "snippet", is executed. There are about 35 such snippets, and they are executed in rotation, one after each VAL scan. The snippets include updating VME overhead registers, reading/posting RTD setups and data, managing relays, and servicing channel control registers.

When no new channel value data is loaded, the full 16-channel VAL scan takes place about every 225 microseconds, but is occasionally extended to as much as 350 microseconds worst-case when snippet code and interrupt processing peaks. Each changed voltage-mode value adds about 4 microseconds of processing time, and each new thermocouple-mode value adds about 40 microseconds.

If the output value of a single voltage-type channel is altered, it may take up to 350 microseconds before the channel DAC hardware is loaded with the appropriately scaled and calibrated data.

Once a DAC is loaded, the analog outputs have a nominal 10-90% risetime of about 500 microseconds and will settle to 0.1% within 2 milliseconds.

The entire snippet chain is executed about every 6.5 milliseconds.
If a channel control register is altered, the V470 may take as much as 7 milliseconds to reconfigure the channel.

A periodic interrupt service routine runs every 4 milliseconds. It services the front-panel LEDs, scans the RTDs, drives the relays, and services the watchdog timer. Execution time is typically about 50 microseconds but occasionally peaks at about 75 microseconds.

If all channels are operating in voltage mode and channel configurations are stable, and as many as 16 channel value registers are rapidly loaded, all outputs will begin to slew within 420 microseconds and be settled to 90% within 1 millisecond and 0.1% within 2.4 milliseconds.

If the RELAYS register is altered, it may take up to 18 milliseconds before all relay contact changes have settled.

Loopback-mode BIST data may take up to two seconds to accurately reflect a change in channel output voltage.

Automatic BIST takes about 5 seconds per channel, 80 seconds for the full 16-channel test sequence.

9. Accessories

The J470 is an enclosed 8-channel isothermal termination box with integral RTD reference-junction sensor. It may be located up to 300 feet from the V470, and can be connected using standard RS232 type shielded 25-pin copper-wire cable assemblies. One or two J470's may be connected to each V470.

The J475 is simple 8-channel PC-board termination panel that transitions from a D25 connector to screw terminals. One or two may be connected to a V470.

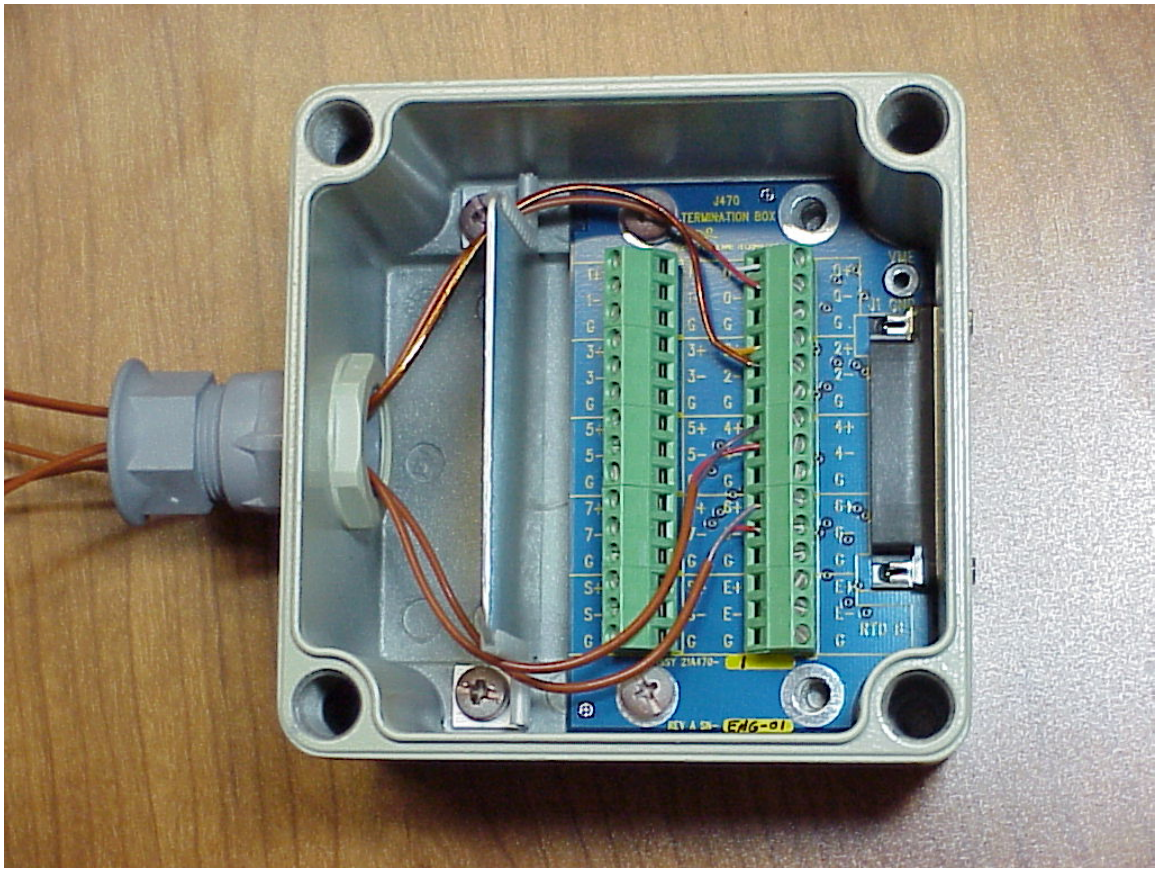


Figure 3. Model J470 8-Channel Isothermal Termination Box

10. Versions

The standard V470 versions are:

V470-1	16-channel VME analog output and thermocouple simulator module
V470-2	16-channel VME analog output and thermocouple simulator module with BIST
V470-11	16-channel VME analog output and thermocouple simulator module with conformal coating
V470-12	16-channel VME analog output and thermocouple simulator module with BIST and conformal coating

11. Customization

Consult factory for information about additional custom versions.

12. Hardware and Firmware Revision History

12.1 Hardware Revision History

Revision G	April 2019 PCB changes to improve manufacturability.
Revision F	Aug 2012 Replaces channel fuses with Poly fuses, reduces noise on internal RTD check resistor measurement
Revision E	Apr 2008 Adds LC filtering to +12V rail to prevent shooting noise back onto VME power rail
Revision D	Oct 2006 Adds PCB features for easier assembly Disconnects pins 1-4 of D9 connector from GND
Revision C	May 2006 Improves clock terminations for use with high-speed crate controllers
Revision B	Nov 2005 Reduces dc/dc noise feedthrough Adds BIST hardware
Revision A	Aug 2005 Initial PCB release, BIST not supported

12.2 Firmware Revision History

22471 Revision E	Mar 2008 Fixes communication problem to channels causing timing failures
22471 Revision D	Apr 2006 Fixes timing ambiguity in VME FPGA
22471 Revision C	Mar 2006 Adds clock de-glitching to channel FPGA
22471 Revision B	Feb 2006 Corrects glitch in type B TC table

	Fixes pullup of A24- DIP switch
22471 Revision A	Dec 2005 Adds BIST support for Rev B and above hardware
22470 Revision A	Oct 2005 Initial firmware release, Rev A hardware only

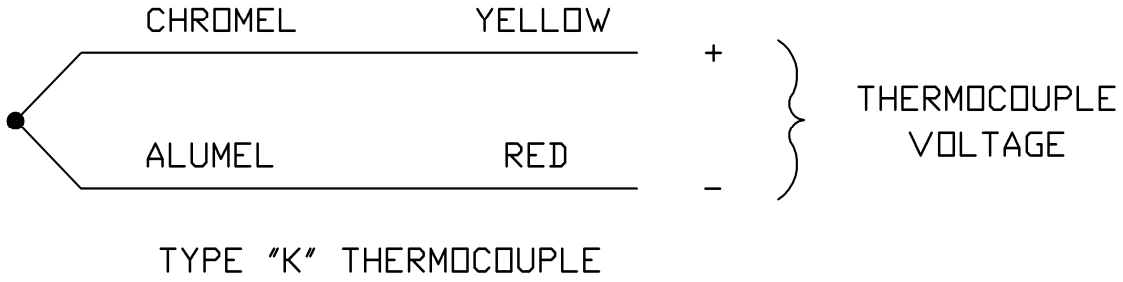
13. Accessories

J55-1	6' shielded D25 male to D25 male cable
J56-1	10' shielded D25 male to D25 male cable
J71-1	Dual D9 female to Agilent 34104A cable
J75-1	D9 female to two (2) dual banana plug cable
J76-1	D9 OpenCVA busing cable
J470-1	8-channel D25 female isothermal termination box
J475-1	8-channel D25 female Din rail termination panel
J475-2	8-channel D25 female Din rail termination panel w/ reference junction sensor

14. Appendix A: Thermocouple Theory and Notes

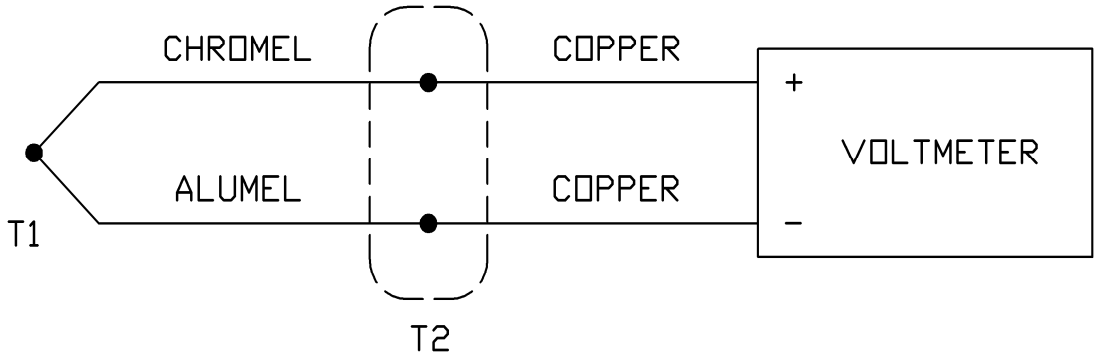
A thermocouple is a pair of dissimilar-alloy wires used to measure temperature. Any metallic alloy can be thought of as having an intrinsic energy level or voltage that is a nonlinear function of temperature. This voltage is usually in the range of about 5 to 40 microvolts per degree C.

The figure below illustrates a Type K thermocouple. Since the chromel and alumel alloys have different thermocouple voltage versus temperature functions, a voltage appears at the ends of the leads that depends on the temperature gradients along the wires



TYPE "K" THERMOCOUPLE

If we want to measure the junction temperature, we connect a voltmeter to the ends of the thermocouple leads

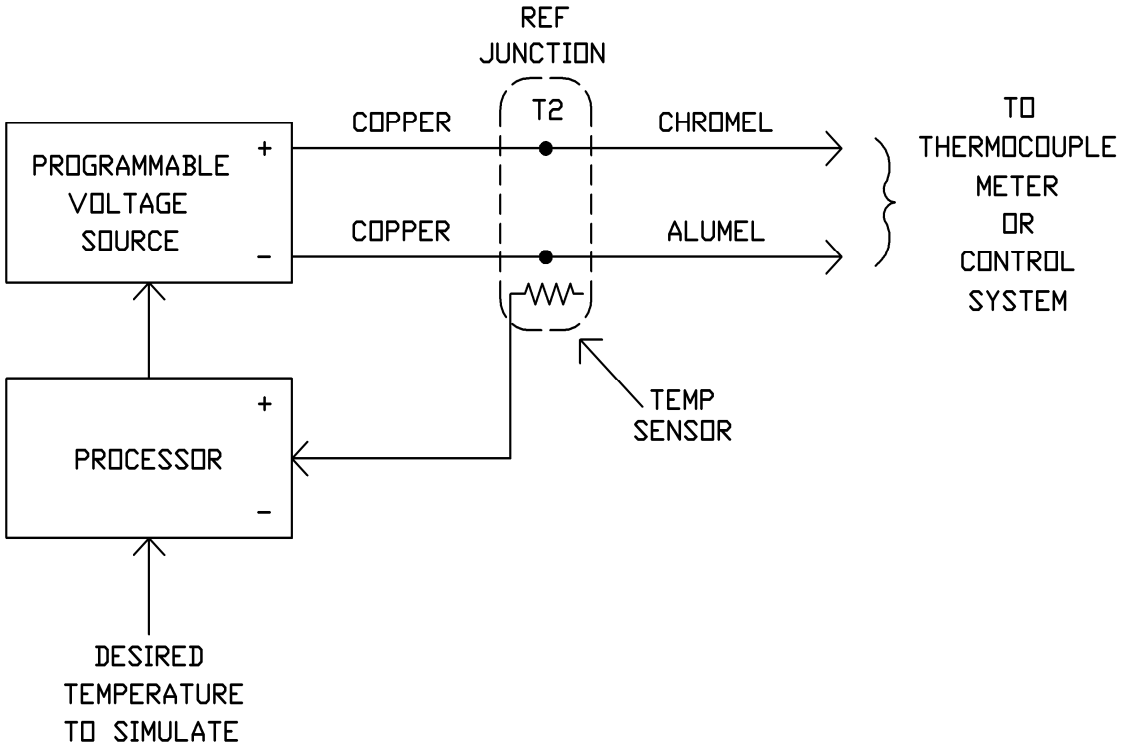


In this case, T1 is the temperature to be measured and T2 is the reference junction temperature. NIST publishes thermocouple temperature/voltage tables which assume that the reference junction is kept at ice point, 0°C.
If the reference junction cannot be maintained at 0°C, its temperature can be measured and a correction factor applied to the indicated voltmeter reading, so the

ice-point-based lookup tables can then be used. Note that, because the thermocouple effect is nonlinear, the voltmeter reading is ***not*** an accurate function of the temperature difference between T1 and T2: it is more correctly a function of the difference in ***thermocouple potentials*** at T1 and T2.

Many thermocouple instruments apply a linear correction to the measured voltage, as a function of reference junction temperature, but this is only an approximation. Ideal thermocouple reference junction compensation corrects the voltmeter reading by the actual, nonlinear thermocouple potential at point T2, which is the technique used in the V470.

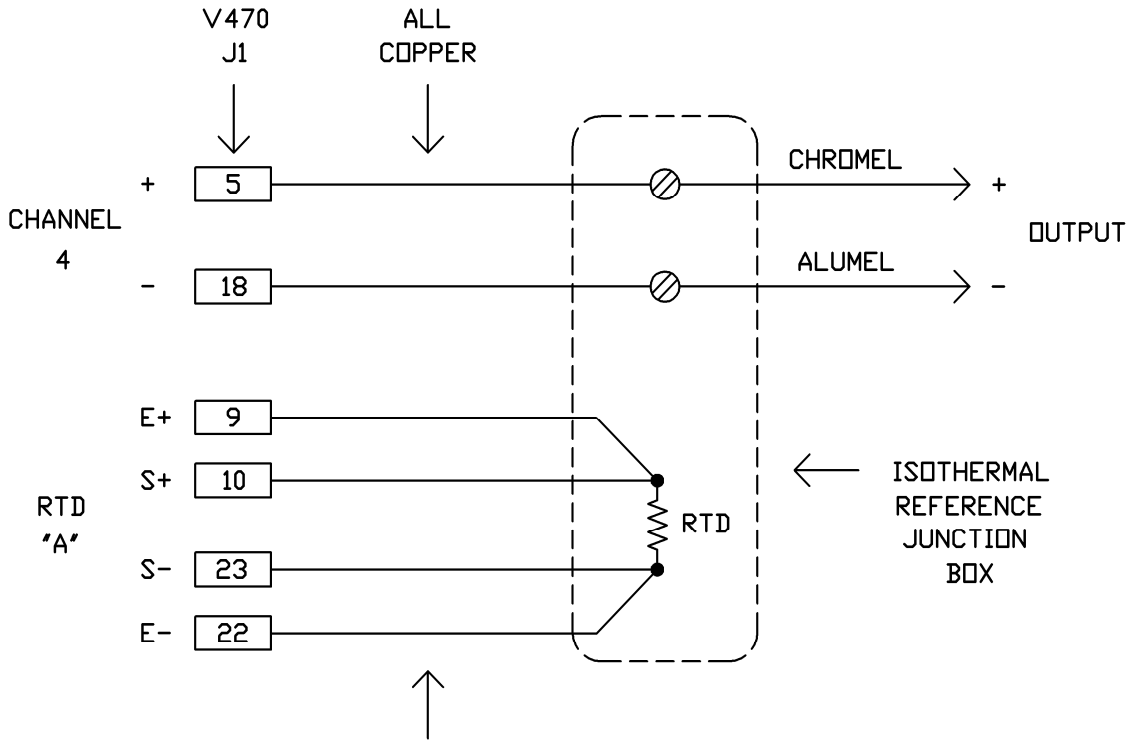
A thermocouple simulator, like the V470, is configured



Here, a microprocessor is given a thermocouple type and a temperature to simulate. It looks up the proper microvolt level for the specified temperature, and also reads the temperature sensor at the reference junction temperature T2, and applies the appropriate nonlinear offset voltage to compensate for reference junction temperature. Within the reference junction box are screw terminals where the transition is made from copper-copper leads to the actual thermocouple alloys. It is important that both screw terminals and the temperature sensor be at the same temperature in order for the compensation to be accurate.
Note that the device being driven, a thermocouple meter or control system, generally has its own reference junction and associated compensation.

The V470 includes the capability to measure up to four platinum RTD temperature sensors to perform the reference junction math. Any of the 16 output channels may be assigned to use any one desired reference junction sensor. The module assumes that the RTDs are calibrated to 100 or 1000 ohms at zero degrees C, and that they follow the standard ISO 385 nonlinearity curve. RTDs are connected as 4-wire devices to eliminate errors caused by the resistance of connection wires from the V470 to the reference junction.

A typical V470 channel setup might be



where channel 4 is to be used to simulate a Type K thermocouple.

To program the module for this case, after powerup

Write 0x0001 to the RTDA register to enable RTD A as a 100 ohm sensor.

Write 0x0011 to the CTL4 register to select RTD A as its reference (RS code 0) and Type K as its sensor (RN code 17.)

Write the desired temperature to the VAL4 register, as a 16-bit 2's complement value, degrees C multiplied by 16, for example 0x640 for +100°C.

The cabling from the front panel of the V470 to the reference junction can be ordinary connectors and copper wiring. Appropriate connector shells should be in place to ensure that all pins within the mating connector are reasonably isothermal and protected against air currents and thermal transients. Shielded wiring is preferred, with the shield bonded to the connector shell, which is VME front-panel and chassis frame ground.

If the internal temperature sensor of the V470 is to be used, the thermocouple wires should be extended all the way to the front panel of the module, soldered or crimped into the pins of the mate to J1 or J2. Program the channel control register to specify the internal sensor, RS code 4. Because the sensor is on the printed-circuit board but the reference junction is effectively within the mating connector, isothermal conditions will be poor and errors on the order of several degrees C may be expected.

There are many potential sources of error in thermocouple simulation:

Imperfection in the V470 programmable voltage source.

Imperfection in the reference-sensing RTD and the V470 RTD acquisition subsystem.

Non-isothermal reference junction.

Voltage drop in thermocouple wires.

Imperfect thermocouple wire chemistry.

A V470 using the J470 termination box will typically have errors below ±0.2°C over the full Type K range. Type K thermocouples are available with standard accuracy limits of ±2.2°C or 0.75% of temperature, whichever is greater; "Special limit" thermocouples are available with errors of about half that. So the V470 will usually not be a significant error contributor compared to inherent thermocouple accuracy.

Thermocouple wire generally has high resistance compared to copper. For example, a Type J pair, #24 wire, is about 0.9 ohms per foot, and Type K is about 1.5 ohms/foot, as compared to 0.05 ohms/foot for a pair of #24 copper wires – a 30:1 ratio. Thermocouple wire resistance can be a significant source of error. For example, 200 feet of #24 Type K has about 300 ohms resistance. If a measurement device had a low input impedance of, say, 100K ohms, the resulting error would be about 0.3%, 3°C at 1000°C. If a measuring device applied a constant +1 microampere DC current in order to detect an open thermocouple, the voltage drop in the leadwire would be about 300 microvolts, equivalent to an error of +14 degrees C.

Finer-gage wire has correspondingly higher resistance. Type K extension wire is available in #30 (6 ohms/foot) and #40 (63 ohms/foot.)

15. Appendix B: Thermocouple Types

Type	+/- Alloys	Range °C	uV/°C nom	USA Colors	IEC Colors
J	Iron/Constantan	210 to 1200	50	white/red	black/white
K	Chromel/Alumel	-270 to 1372	39	yellow/red	green/white
E	Chromel/Constantan	-270 to 1000	59	violet/red	violet/white
T	Copper/Constantan	-270 to 400	39	blue/red	brown/white
R	Pt-13Rh/Platinum	-50 to 1768	5	black/red	orange/white
S	Pt-10Rh/Platinum	-50 to 1768	5	black/red	orange/white
B	Pt-30Rh/Pt-6Rh	0 to 1820	10	grey/red	grey/white
N	Nicrosil/Nisil	70 to 1300	26	orange/red	pink/white

Note that the negative wire is always red in the USA/ANSI color code, and always white for the IEC colors.

Type B has a near-zero thermal coefficient at room temperature, so is often used without a reference junction sensor, namely programmed to use a simulated ice point reference.