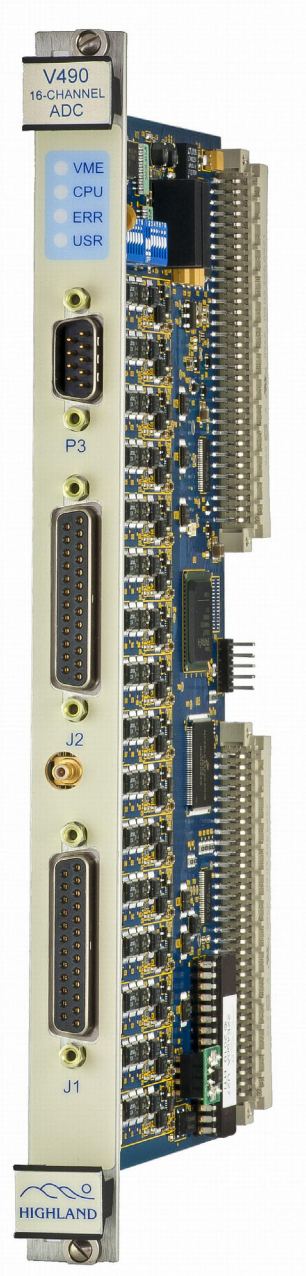
HIGHLAND TECHNOLOGY



V490
16-CHANNEL
VME
MULTI-RANGE
DIGITIZER

Technical Manual

October 9, 2023

650 Potrero Avenue San Francisco, CA 94110 www.highlandtechnology.com tel: 415 551-1700 fax: 415 551-5129

650 Potrero Avenue, San Francisco, CA 94110
Phone 415-551-1700 • Fax 415-551-5129
www.highlandtechnology.com

NOTICE

HIGHLAND TECHNOLOGY, INC. PROVIDES THIS PUBLICATION “AS IS” WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

(Disclaimer of expressed or implied warranties in certain transactions is not allowed in some states. Therefore, the above statement may not apply to you.)

This manual may contain technical inaccuracies and/or typographical errors. Changes are periodically made to this manual which are incorporated in later editions. Highland Technology, Inc. may make changes and improvements to the product(s) and/or programs described in this publication at any time without notice.

The V490 has finite failure rates associated with its hardware, firmware, design, and documentation. Do not use the product in applications where a failure or defect in the instrument may result in injury, loss of life, or property damage.

IN NO EVENT WILL HIGHLAND TECHNOLOGY, INC. BE LIABLE FOR DAMAGES, INCLUDING LOST PROFITS, LOST SAVINGS OR OTHER INCIDENTAL OR CONSEQUENTIAL DAMAGES ARISING OUT OF THE USE OF OR INABILITY TO USE SUCH PRODUCT, EVEN IF HIGHLAND TECHNOLOGY, INC. OR AN APPROVED RESELLER HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, OR FOR ANY CLAIM BY ANY OTHER PARTY.

Table of Contents

1. Introduction

This is the manual for the V490, a 16-channel fast analog-to-digital converter VME module.

Features of the V490 include:

- 16 channels of differential analog input acquisition
- Each channel is independently programmable for input range, sample rate, operating modes, and digital lowpass filtering
- Provides continuous, realtime measurement and simultaneously emulates classic filtered, triggered ADC modes
- Input ranges from ± 10.24 mV to ± 40.96 volts with 16-bit resolution
- Common-mode rejection 100 dB typical, ±10 V common-mode range
- Overload protected to ± 250 volts on all ranges
- ADC per channel with 500 Ks/s sample rate
- Programmable lowpass filter per channel from 1 Hz to 100 KHz
- 4K sample FIFO and trigger interpolator per channel provide nanosecond external-trigger accuracy
- FIFO input sample rate is programmable with internal, VME, or external triggering
- Simultaneous sampling, extendable across unlimited number of modules
- Realtime and FIFO-buffered data simultaneously available
- No realtime handshaking is required: once channel parameters are set up, measurements appear in dual-port memory registers with VMEbus-speed access
- In-crate calibration check via dedicated test connector
- Clearly labeled dipswitches set VME address; no jumpers, headers, or trimpots
- Optional built-in self-test (BIST)

2. Specifications: V490 Analog Input Module

FUNCTION	16-channel differential analog-to-digital converter
DEVICE TYPE	16-bit VME register-based slave: A24:A16:D16:D32; Implements 256 16-bit registers at switch selectable addresses in the VME 16 or 24 bit addressing spaces
RANGES	Programmable per channel ±10.24 mV ± 40.96 mV ± 160 mV ± 640 mV ± 2.56 V ± 10.24 V ± 40.96 V
RESOLUTION	16 bits, 0.313 µV on 10.24 mV range
INPUT IMPEDANCE	> 500 K to ground, each differential input
ACCURACY	± 0.05% of range ± 20 µV ± 5 µV/°C
CMRR	100 dB typical on 10 mV range to 60 dB typical on 40 V range CM range ± 10 V, ± 140 V on 10 and 40 V ranges
SAMPLE RATE	500 Ks/s FIFO path has programmable trigger rate
FILTERING	Analog, 80 KHz 5-pole pre-ADC lowpass Digital, 1 Hz to 50 KHz, 8-pole Bessel or Butterworth
PROTECTION	± 250 volts either input to ground
OPERATING TEMPERATURE	0 to 60°C; extended MIL/COTS ranges available
CALIBRATION INTERVAL	One year
POWER	Standard VME supplies: + 5 volts, 0.8 amp max +12 volts, 250 mA max -12 volts, 250 mA max

CONNECTORS	Two D25 female, each 8 channels One D9 male analog test One SMB trigger i/o
INDICATORS	LEDs indicate VME access, CPU activity, error conditions Additional LED is user programmable
PACKAGING	6U single-wide VME module
CONFORMANCE	ANSI/VITA 1-1994 (R2002) VME bus spec; does not support byte writes

Bandwidth Specifications:

RN Code	Range	Bandwidth (-3dB)	Slew Rate Limit
0	± 10.24 mV	9 KHz	0.58 V/ms
1	± 40.96 mV	30 KHz	7.8 V/ms
2	± 160 mV	80 KHz	71 V/ms
3	± 640 mV	80 KHz	330 V/ms
4	± 2.56 V	80 KHz	900 V/ms
5	± 10.24 V	80 KHz	5.2 V/us
6	± 40.96 V	80 KHz	14 V/us

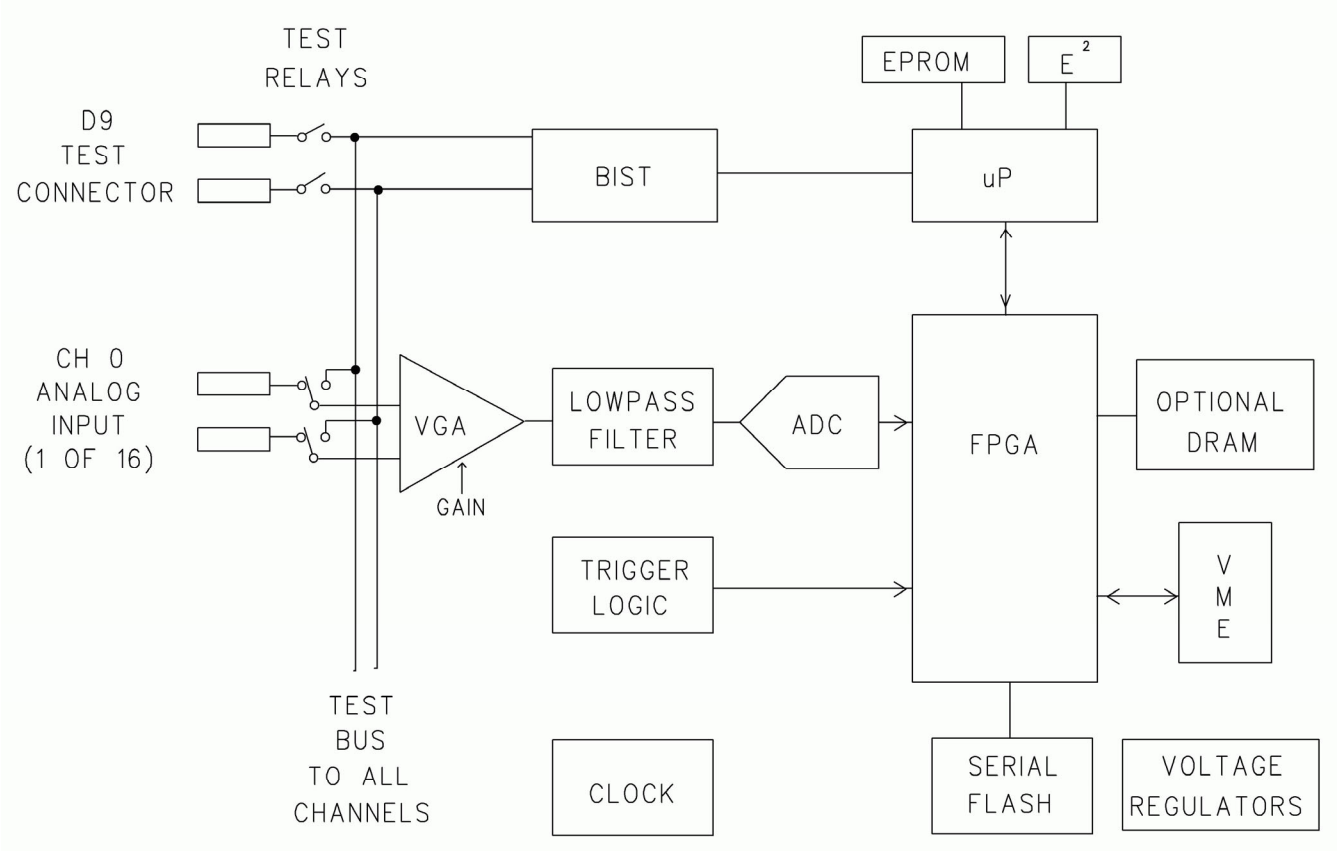
3. Overview

The V490 includes 16 independent differential-input analog-to-digital converters.

3.1 Channel Circuits

Each channel includes

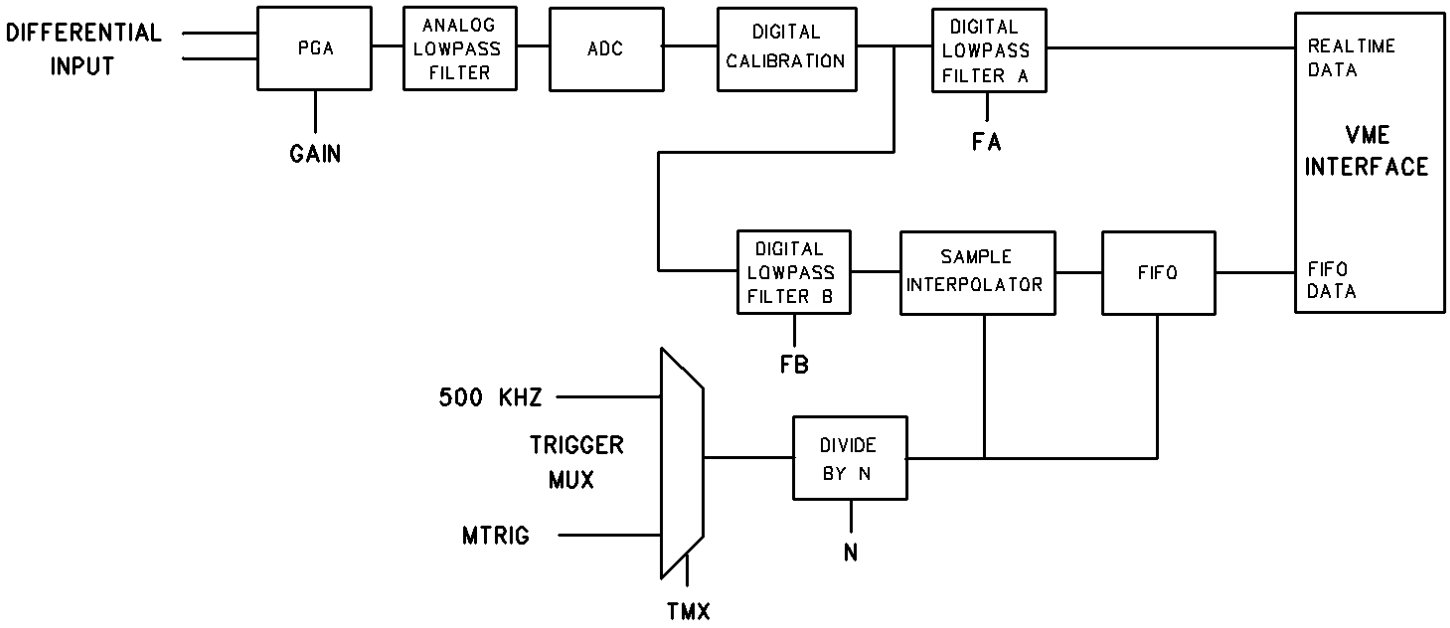
BIST/CAL relay
Input protection
Input attenuator
Variable-gain differential amplifier
100 KHz analog anti-aliasing lowpass filter
16-bit A/D converter
Digital signal processing



3.2 Signal Processing

In the standard V490, all sixteen ADCs are triggered at a constant 500 KHz rate. Each resulting data stream is digitally lowpass filtered and the result posted to a "realtime" VME register at the 500 KHz rate. Users may read this register at any time.

An alternate path for ADC data provides a separate digital lowpass filter, a programmable sample rate clock, trigger interpolator, and a 4K sample FIFO memory with its own VME interface.



Signal Processing

Filter types and bandwidths are programmable on a per-channel basis, with filter responses available from 1 Hz to 100 KHz. The combination of pre-ADC analog filtering, constant 500 KHz digitizing, and programmable digital filtering allows essentially alias-free data acquisition.

The output of Filter A is immediately available to the VME interface, simulating an ADC that receives a lowpass filtered analog input and is triggered the instant that it is read by VME.

A separate lowpass Filter B feeds the digital interpolator and FIFO memory. When triggered, the interpolator delivers a sample to the FIFO that simulates a sample-and-hold and ADC whose input is the filtered analog signal. The resulting sample is not quantized to the 500 KHz ADC sample rate but accurately represents the filtered analog value at the instant the trigger is received. Effective aperture jitter is typically below 5 nanoseconds RMS.

The MTRIG global trigger signal can come from a variety of internal and external sources; see section 8.

CAUTION: V490 differential inputs have approximately 500 K ohms impedance to ground. If connected to floating sources, users should provide a DC path to ground to prevent leakage currents and hum from producing excess common-mode voltages.

4. Connectors and Installation

4.1 Address DIP Switches

The V490 appears as 256 16-bit registers in the VME 16 or 24-bit addressing spaces. The base address of the 256 registers is set by dip switches.

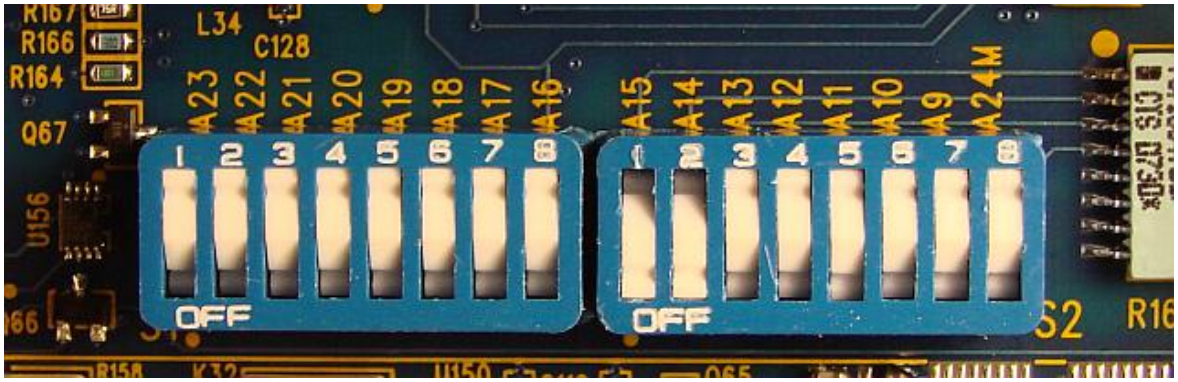
Four 4-position rocker-type dipswitches are provided near the top edge of the board. They are labeled, left to right, "A23" through "A9" and finally "A24M".

To set a switch to the logical "1" or "ON" position, press the side of the switch nearest its "Axx" lettering. Use a toothpick or paper clip, not a pen or pencil.

The A24M switch, when set, allows the board to operate in the VME 24-bit (A24) address space; in this case, all address switches are active and the board responds to VME address modifier codes 0x39 and 0x3D.

If the A24M switch is off, the module resides in the A16 space and responds to address modifiers 0x29 and 0x2D. In this case, only address switches A15 through A9 are active.

Units are shipped with switches A15 and A14 on, all others off, locating the register base at 0xC000 in the A16 space, as shown below.



Address DIP Switch

4.2 Installation

The V490 may be installed in any standard 6U VME crate, including VME64 variants. It supports 32-bit data transfers using the P1 and P2 connectors, or may be used in 16-bit mode using only the P1 backplane connector.

The V490 passes all interrupt and bus grant signals, so may be used with backplane grant jumpers installed or not installed.

CAUTION: Do not install or remove the V490 with crate power on. VME modules are not hot-pluggable. The V490 will be damaged if hot-plugged.

CAUTION: Fully seat the module and secure front-panel screws before applying power.

CAUTION: Handle the V490 with proper ESD precautions to avoid static damage.

CAUTION: V490 differential inputs are high impedance. If connected to floating sources, users should provide a DC path to ground to prevent leakage currents and hum from producing excess common-mode voltages.

4.3 D25 Input Connectors

Two front-panel female D-25 connectors are provided. Pinout is as follows:

J1 Pin	Function	J2 Pin	Function
J1-1	ch 0+	J2-1	ch 8+
J1-14	ch 0-	J2-14	ch 8-
J1-2	ch 1+	J2-2	ch 9+
J1-15	ch 1-	J2-15	ch 9-
J1-3	ch 2+	J2-3	ch 10+
J1-16	ch 2-	J2-16	ch 10-
J1-4	ch 3+	J2-4	ch 11+
J1-17	ch 3-	J2-17	ch 11-
J1-5	ch 4+	J2-5	ch 12+
J1-18	ch 4-	J2-18	ch 12-
J1-6	ch 5+	J2-6	ch 13+
J1-19	ch 5-	J2-19	ch 13-
J1-7	ch 6+	J2-7	ch 14+
J1-20	ch 6-	J2-20	ch 14-
J1-8	ch 7+	J2-8	ch 15+
J1-21	ch 7-	J2-21	ch 15-
J1-22	VME GROUND	J2-22	VME GROUND
J1-24	VME GROUND	J2-24	VME GROUND

Connector shells are bonded to the VME front panel, which connects to the crate frame through the module securing screws.

4.4 D9 Calibration Connector

A male D9 connector is provided for connection to an external precision voltage source, allowing verification of module calibration without removing field-wiring connectors. Each input channel incorporates a relay which allows it to be switched, under software control, to this test connector.

Pinout of the D9 is:

```
P3-7      CalSig+

P3-6      CalSig-

P3-5      VME GROUND
```

An external voltage source may be connected to Pins 7 and 6, and one or more channel relays activated to allow channels to measure the test source instead of its normal input. If no other path exists from the test supply to ground, it is recommended that its low side be connected to P3-5 in order to establish a solid common-mode reference.

The RELAYS register is used to control the channel test relays and the MODE register controls access to the cal bus. For example, writing value 4 to RELAYS and 1 to MODE will connect the external source to the input of channel 2.

V490-2 modules, equipped with BIST, can internally generate test voltages that can be applied simultaneously to the D9 test connector and to the internal cal bus. This allows channel calibration verification using an external DVM.

See sections 6.3, 6.5, and 7.3 for details of channel test switching.

4.5 SMB Trigger Connector

An SMB trigger connector is located on the front panel between the D25 signal connectors. It can serve as a trigger input or output. It is compatible with TTL, 3.3 volt CMOS, or 5-volt CMOS levels. As an output, it provides 3.3 volt CMOS trigger pulses. See section 8.

The V490 is capable of accepting external triggers, or of operating multiple modules in master/slave trigger modes, emulating asynchronously triggered, ADC-per-channel architectures.

Highland can furnish SMB-BNC cables, multi-station trigger connector bussing assemblies, and electrical or fiberoptic trigger fanouts.

5. Operation

5.1 LEDs

There are four front-panel LED indicators.

The blue VME led flashes whenever the module is accessed from the VME bus.

The green CPU led flashes about once a second to indicate CPU activity

The red ERR led will flash to indicate errors:

Two blinks	Channel Configuration Error
Three blinks	Calibration table error; default calibrations are in use
Four blinks	FPGA error; module may not respond to the VME bus

The orange USR led displays a user-defined blink pattern. See section 6.4

There is an additional LED on the PCB surface which illuminates green when the FPGA is properly configured.

5.2 Powerup Defaults

At powerup or following a reboot macro, the module setup will be:

All channels on ± 10.24 volt ranges

All filters set to 1 KHz Bessel

All FIFO load rates 500 KHz; channel trigger divisors set to zero.

RELAYS, MODE, and BMUX registers clear

TRIGGER, BOUNCE, and M registers clear

ULED led control register clear

Users can immediately read input voltages in the sixteen RDAT0 through RDAT15 (signed, 16 bit) realtime data registers.

Powerup or reboot takes about 5 seconds.

5.3 Quick Start

Basic operation of the V490 can be demonstrated by the following steps:

A 6U VME crate and computer interface are required. The crate must be compliant with the IEEE 1014 VME specification, or the equivalent ANSI/VITA 1-1994 (R2002) VMEbus spec. Any crate with the standard power supplies (+12, +5, -12) and the 16-bit "P1" bus is adequate.

The computer interface must allow, as a minimum, reading and writing 16-bit registers in the A16 or A24 address spaces.

Pick an address space and module base address and set the V490 dip switches accordingly. See section 4.1. The as-shipped default is address 0xC000 in the 16-bit address space.

With crate power off, insert the V490 into any crate slot and firmly secure its mounting screws. Do not hot-plug VME modules.

Power up. After a few seconds, the V490 green "CPU" LED should flash, and the other LEDs should be off.

Now run software that can display the contents of VME registers.

Read the manufacturer ID register, the16-bit VME register at the module base address. The default address would be 0xC000. The blue "VME" LED should flash, and the register value should be 0xFEEE, identifying this as a Highland VME module.

Read the next register, offset address 2, default 0xC002. It should read 22490 decimal, 0x57DA, identifying the module as a V490.

The module powers up digitizing all 16 analog inputs, all on their ± 10.24 volt range with 1 KHz Bessel lowpass filtering.

Read the RDAT0 register, offset address 0x48, default 0xC048. This represents the differential voltage applied to channel 0 at J1 pins 1 and 14. If the register value is "N", and is interpreted as a signed 16-bit value from -32768 (0x8000) to +32767 (0x7FFF), the voltage is

```
V = N * 10.24 / 32768
```

The other channel voltages can be read in the RDAT1 through RDAT15 realtime data registers, as mapped in section 6.1.

Channel ranges and filter settings can be changed by writing to the channel control and filter control registers; see section 6.13.

6. VME Registers

The V490 implements 256 16-bit VME registers. REG# below is the ordinal register number in decimal; OFFSET is the hex VMEbus offset from the module base address.

Registers identified as "RO" should be treated as read-only and should not be written from VME; these registers are periodically refreshed by the internal microprocessor.

Read-write (RW) registers are written by VME and are not altered by the internal microprocessor.

Read-write + macro registers (RWM) can be written by the user, but may also be changed by the V490 in response to a user executed MACRO command. A macro handshake protocol is defined in Section 6.8.

VMEbus response time (DS0* to DTACK*) averages about 125 ns.

Registers tagged # are serviced by FPGA logic at VMEbus speed.

Other VME registers are dual-port memory serviced by the uP. The microprocessor normally services these registers about every 2.5 milliseconds.

Range changes, filtering changes, and relay actuation may take up to 25 milliseconds. See section 6.14 for comments on realtime issues.

6.1 VME Register Map

Reg Name	REG#	Offset	R/W	Function	#
VXI MFR	0	0x00	RO	Highland ID: reads 65262, 0xFEEE	
VXI TYPE	1	0x02	RO	V490 module ID, 22490, 0x57DA	
SERIAL	3	0x06	RO	unit serial number	
ROM ID	4	0x08	RO	firmware ID, typically 22490 decimal	
ROM REV	5	0x0A	RO	firmware revision, typically ASCII "B"	
MCOUNT	6	0x0C	RO	microprocessor IRQ update counter	
DASH	7	0x0E	RO	module version (dash) number	
FPGA ID	8	0x10	RO	FPGA code ID, typ 22491 decimal	#
FPGA REV	9	0x12	RO	FPGA revision, typ ASCII "B"	#
RELAYS	11	0x16	RW	controls calibration-bus relays	
ULED	12	0x18	RW	user LED control	
MODE	13	0x1A	RW	module operating mode	
CALID	14	0x1C	RO	calibration table status	
CHER	15	0x1E	RO	channel configuration error flags	
MACRO	16	0x20	RWM	macro command register	
PARAM0	17	0x22	RWM	macro parameter	
PARAM1	18	0x24	RWM	macro parameter	
PARAM2	19	0x26	RWM	macro parameter	
YCAL	20	0x28	RO	calibration date, year	
DCAL	21	0x2A	RO	calibration date, month/day	
BERN	22	0x2C	RO	BIST error count	
BMUX	23	0x2e	RW	BIST mux control	
FZAP	24	0x30	RW	FIFO clear register	#
VMETRIG	25	0x32	RW	VME trigger	#
TRIGGER	26	0x34	RW	master/slave global trigger control	#

Reg Name	REG#	Offset	R/W	Function	#
BOUNCE	27	0x36	RW	trigger debounce control	#
M	28	0x38	RW	500 KHz trigger divisor	#
CTL0	32	0x40	RW	channel 0 control	
FILT0	33	0x42	RW	channel 0 filtering	
FIFO0	34	0x44	RO	channel 0 FIFO status	#
FDIV0	35	0x46	RW	channel 0 FIFO rate divisor	#
RDAT0	36	0x48	RO	channel 0 realtime data	#
	37	0x4A		reserved	
FDAT0A	38	0x4C	RO	channel 0 FIFO data A	#
FDAT0B	39	0x4E	RO	channel 0 FIFO data B	#
CTL1	40	0x50	RW	channel 1 control	
FILT1	41	0x52	RW	channel 1 filtering	
FIFO1	42	0x54	RO	channel 1 FIFO status	#
FDIV1	43	0x56	RW	channel 1 FIFO rate divisor	#
RDAT1	44	0x58	RO	channel 1 realtime data	#
	45	0x5A		reserved	
FDAT1A	46	0x5C	RO	channel 1 FIFO data A	#
FDAT1B	47	0x5E	RO	channel 1 FIFO data B	#
CTL2	48	0x60	RW	channel 2 control	
FILT2	49	0x62	RW	channel 2 filtering	
FIFO2	50	0x64	RO	channel 2 FIFO status	#
FDIV2	51	0x66	RW	channel 2 FIFO rate divisor	#
RDAT2	52	0x68	RO	channel 2 realtime data	#
	53	0x6A		reserved	
FDAT2A	54	0x6C	RO	channel 2 FIFO data A	#
FDAT2B	55	0x6E	RO	channel 2 FIFO data B	#
CTL3	56	0x70	RW	channel 3 control	
FILT3	57	0x72	RW	channel 3 filtering	
FIFO3	58	0x74	RO	channel 3 FIFO status	#

Reg Name	REG#	Offset	R/W	Function	#
FDIV3	59	0x76	RW	channel 3 FIFO rate divisor	#
RDAT3	60	0x78	RO	channel 3 realtime data	#
	61	0x7A		reserved	
FDAT3A	62	0x7C	RO	channel 3 FIFO data A	#
FDAT3B	63	0x7E	RO	channel 3 FIFO data B	#
CTL4	64	0x80	RW	channel 4 control	
FILT4	65	0x82	RW	channel 4 filtering	
FIFO4	66	0x84	RO	channel 4 FIFO status	#
FDIV4	67	0x86	RW	channel 4 FIFO rate divisor	#
RDAT4	68	0x88	RO	channel 4 realtime data	#
	69	0x8A		reserved	
FDAT4A	70	0x8C	RO	channel 4 FIFO data A	#
FDAT0B	71	0x8E	RO	channel 4 FIFO data B	#
CTL5	72	0x90	RW	channel 5 control	
FILT5	73	0x92	RW	channel 5 filtering	
FIFO5	74	0x94	RO	channel 5 FIFO status	#
FDIV5	75	0x96	RW	channel 5 FIFO rate divisor	#
RDAT5	76	0x98	RO	channel 5 realtime data	#
	77	0x9A		reserved	
FDAT5A	78	0x9C	RO	channel 5 FIFO data A	#
FDAT5B	79	0x9E	RO	channel 5 FIFO data B	#
					#
CTL6	80	0xA0	RW	channel 6 control	
FILT6	81	0xA2	RW	channel 6 filtering	
FIFO6	82	0xA4	RO	channel 6 FIFO status	#
FDIV6	83	0xA6	RW	channel 6 FIFO rate divisor	#
RDAT6	84	0xA8	RO	channel 6 realtime data	#
	85	0xAA		reserved	
FDAT6A	86	0xAC	RO	channel 6 FIFO data A	#
FDAT6B	87	0xAE	RO	channel 6 FIFO data B	#

Reg Name	REG#	Offset	R/W	Function	#
CTL7	88	0xB0	RW	channel 7 control	
FILT7	89	0xB2	RW	channel 7 filtering	
FIFO7	90	0xB4	RO	channel 7 FIFO status	#
FDIV7	91	0xB6	RW	channel 7 FIFO rate divisor	#
RDAT7	92	0xB8	RO	channel 7 realtime data	#
	93	0xBA		reserved	
FDAT7A	94	0xBC	RO	channel 7 FIFO data A	#
FDAT7B	95	0xBE	RO	channel 7 FIFO data B	#
CTL8	96	0xC0	RW	channel 8 control	
FILT8	97	0xC2	RW	channel 8 filtering	
FIFO8	98	0xC4	RO	channel 8 FIFO status	#
FDIV8	99	0xC6	RW	channel 8 FIFO rate divisor	#
RDAT8	100	0xC8	RO	channel 8 realtime data	#
	101	0xCA		reserved	
FDAT8A	102	0xCC	RO	channel 8 FIFO data A	#
FDAT8B	103	0xCE	RO	channel 8 FIFO data B	#
CTL9	104	0xD0	RW	channel 9 control	
FILT9	105	0xD2	RW	channel 9 filtering	
FIFO9	106	0xD4	RO	channel 9 FIFO status	#
FDIV9	107	0xD6	RW	channel 9 FIFO rate divisor	#
RDAT9	108	0xD8	RO	channel 9 realtime data	#
	109	0xDA		reserved	
FDAT9A	110	0xDC	RO	channel 9 FIFO data A	#
FDAT9B	111	0xDE	RO	channel 9 FIFO data B	#
CTL10	112	0xE0	RW	channel 10 control	
FILT10	113	0xE2	RW	channel 10 filtering	
FIFO10	114	0xE4	RO	channel 10 FIFO status	#
FDIV10	115	0xE6	RW	channel 10 FIFO rate divisor	#
RDAT10	116	0xE8	RO	channel 10 realtime data	#
	117	0xEA		reserved	

Reg Name	REG#	Offset	R/W	Function	#
FDAT10A	118	0xEC	RO	channel 10 FIFO data A	#
FDAT10B	119	0xEE	RO	channel 10 FIFO data B	#
CTL11	120	0xF0	RW	channel 11 control	
FILT11	121	0xF2	RW	channel 11 filtering	
FIFO11	122	0xF4	RO	channel 11 FIFO status	#
FDIV11	123	0xF6	RW	channel 11 FIFO rate divisor	#
RDAT11	124	0xF8	RO	channel 11 realtime data	#
	125	0xFA		reserved	
FDAT11A	126	0xFC	RO	channel 11 FIFO data A	#
FDAT11B	127	0xFE	RO	channel 11 FIFO data B	#
CTL12	128	0x100	RW	channel 12 control	
FILT12	129	0x102	RW	channel 12 filtering	
FIFO12	130	0x104	RO	channel 12 FIFO status	#
FDIV12	131	0x106	RO	channel 12 FIFO rate divisor	#
RDAT12	132	0x108	RO	channel 12 realtime data	#
	133	0x10A		reserved	
FDAT12A	134	0x10C	RO	channel 12 FIFO data A	#
FDAT12B	135	0x10E	RO	channel 12 FIFO data B	#
CTL13	136	0x110	RW	channel 13 control	
FILT13	137	0x112	RW	channel 13 filtering	
FIFO13	138	0x114	RO	channel 13 FIFO status	#
FDIV13	139	0x116	RW	channel 13 FIFO rate divisor	#
RDAT13	140	0x118	RO	channel 13 realtime data	#
	141	0x11A		reserved	
FDAT13A	142	0x11C	RO	channel 13 FIFO data A	#
FDAT13B	143	0x11E	RO	channel 13 FIFO data B	#
CTL14	144	0x120	RW	channel 14 control	
FILT14	145	0x122	RW	channel 14 filtering	
FIFO14	146	0x124	RO	channel 14 FIFO status	#

Reg Name	REG#	Offset	R/W	Function	#
FDIV14	147	0x126	RW	channel 14 FIFO rate divisor	#
RDAT14	148	0x128	RO	channel 14 realtime data	#
	149	0x12A		reserved	
FDAT14A	150	0x12C	RO	channel 14 FIFO data A	#
FDAT14B	151	0x12E	RO	channel 14 FIFO data B	#
CTL15	152	0x130	RW	channel 15 control	
FILT15	153	0x132	RW	channel 15 filtering	
FIFO15	154	0x134	RO	channel 15 FIFO status	#
FDIV15	155	0x136	RW	channel 15 FIFO rate divisor	#
RDAT15	156	0x138	RO	channel 15 realtime data	#
	157	0x13A		reserved	
FDAT15A	158	0x13C	RO	channel 15 FIFO data A	#
FDAT15B	159	0x13E	RO	channel 15 FIFO data B	#
BFLAG0	192	0x180	RO	channel 0 BIST flags	
BFLAG1	193	0x182	RO	channel 1 BIST flags	
BFLAG2	194	0x184	RO	channel 2 BIST flags	
BFLAG3	195	0x186	RO	channel 3 BIST flags	
BFLAG4	196	0x188	RO	channel 4 BIST flags	
BFLAG5	197	0x18A	RO	channel 5 BIST flags	
BFLAG6	198	0x18C	RO	channel 6 BIST flags	
BFLAG7	199	0x18E	RO	channel 7 BIST flags	
BFLAG8	200	0x190	RO	channel 8 BIST flags	
BFLAG9	201	0x192	RO	channel 9 BIST flags	
BFLAG10	202	0x194	RO	channel 10 BIST flags	
BFLAG11	203	0x196	RO	channel 11 BIST flags	
BFLAG12	204	0x198	RO	channel 12 BIST flags	
BFLAG13	205	0x19A	RO	channel 13 BIST flags	
BFLAG14	206	0x19C	RO	channel 14 BIST flags	
BFLAG15	207	0x19E	RO	channel 15 BIST flags	
TONE0	208	0x1A0	RO	single-channel BIST data	

Reg Name	REG#	Offset	R/W	Function	#
...	...	...	RO	...	
TONE27	235	0x1D6	RO	single-channel BIST data	
PERR	240	0x1E0	RO	power supply error flags	
EP17	241	0x1E2	RO	+17 power supply voltage	
EP8	242	0x1E4	RO	+8.8	
EP5	243	0x1E6	RO	+5	
EP3	244	0x1E8	RO	+3.3	
EP2	245	0x1EA	RO	+2.048	
EP1	246	0x1EC	RO	+1.25	
EM5	247	0x1EE	RO	-5	
EM17	248	0x1F0	RO	-17	
UTEST	254	0x1FC	RW	user read/write test register	
HTEST	255	0x1FE	RO	always reads 0xABCD	

6.2 Module Overhead Registers

A number of read-only overhead registers are provided.

```
VXI MFR: always reads 0xFEEE, Highland's registered VXI
         module ID code.

VXITYPE: always reads 22490 decimal to identify a V490
         module

SERIAL:  module serial number.

DASH:    module version (dash) number.

ROM ID:  firmware version, typically 22490 decimal

ROM REV: ASCII code identifying the revision letter of
         the firmware, typically 0x0042, ascii "B"

FPGA ID  Identifies the FPGA version, typically 22491
         decimal

FPGA REV  FPGA revision, typically 0x0042, ascii "B"

MCOUNT:  a 16-bit counter that is incremented by the
         internal microprocessor at about 200 Hz.
```

6.3 RELAYS Registers

The RELAYS register controls actuation of the sixteen channel test relays.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
K15	K14	K13	K12	K11	K10	K9	K8	K7	K6	K5	K4	K3	K2	K1	K0

If the user sets any bit ON, the corresponding channel test relay will be actuated. The analog input of the associated channel will then be disconnected from the front-panel D25 connector and connected to the internal cal bus, which may in turn be driven from the internal BIST voltage generator or from the CALSIG+ and CALSIG- Pins (Pins 7 and 6) of the D9 test connector. See sections 4.4, 6.5 and 7.3.

More than one relay may be operated at any time, resulting in the inputs of selected channels being connected in parallel to the cal bus. For highest precision measurements, only one channel test relay should be activated at a time.

Note that channels are provided with overload current limiters which limit input current to about 1.5 mA in over-range conditions. Overdriving channels beyond their programmed voltage range regions can cause these 1.5 mA currents to be drawn from the calibration bus and external cal sources or BIST multiplexers, which could cause unexpected readings on other channels.

Upon altering the RELAYS register it may take up to 25 milliseconds before all relay contact changes have settled.

6.4 ULED - User LED Control

An orange LED is provided on the front panel for user application. The ULED register allows user flash patterns to be loaded. An internal shift register is periodically loaded from the contents of the ULED register, and the MS bit of this register operates the orange LED. The shift register is left-shifted every 125 milliseconds, and the register is reloaded every 16 shifts, namely every 2 seconds.

ULED pattern 0x0000 turns the user LED off. Pattern 0xFFFF turns it steady on.

6.5 MODE - Calibration Bus Control

The V490 includes an internal calibration bus and the optional BIST test voltage generator. The MODE register controls routing of signals between the front-panel D9 connector, the cal bus, and the BIST source.

The mapping of MODE values is...

0	Off	D9 and BIST are disconnected
1	Channel Test	The D9 connector drives the cal bus
2	BIST drive	The BIST voltage generator drives the cal bus, with voltage set by the BMUX register
3	Both	Both the D9 connector and the BIST source are connected to the cal bus.

In mode 1, users may apply an external voltage to the D9 connector pins 7 and 6, and those signals are connected to cal bus lines CAL+ and CAL- respectively. Now any channel whose test relay is activated will digitize the test voltage.

Modes 2 and 3 are available on modules with the BIST option.

Mode 2 will apply an internally-generated test voltage to the cal bus, as selected by the BMUX register. See section 7.

In mode 3, the BIST voltage is applied to the cal bus and the D9 path is enabled. This outputs the BIST test voltage to the D9, so that an external, traceable DVM may be used to verify channel calibrations without the need for an external voltage source. See section 7.

A mode change may take up to 25 milliseconds.

6.6 CALID, YCAL, DCAL - Calibration Status Registers

The CALID register displays a value which reflects the currently installed calibration table. The normal value for the V450-1 and V450-2 modules is 22490 decimal, 0x57DA. If the factory calibration table is corrupted, the firmware will install the default calibration table, the CALID register will display value 0xDEFC and the red LED will flash three times every few seconds..

YCAL and DCAL display the last date of module calibration. YCAL is the year, as an integer, such as 2010 decimal. The high byte of DCAL is month 1-12, and the low byte is day 1-31. The recommended factory recalibration interval for the V490 is one year.

6.7 BIST Registers

See section 7 for description of the various BIST registers.

6.8 MACRO, PARAMx - Macro Controls

The macro control register allows the execution of microprocessor routines which perform calibration and test tasks. Some macros also take a parameter in the PARAM0 register. PARAM1 and PARAM2 are currently unused.

To execute a macro, verify that the MS bit (bit 15) of the MACRO register is clear, then write any required parameter into PARAM0 and then write a macro code to the MACRO register. Wait until the MS bit of MACRO self-clears.

The MACRO codes are...

```
0x8400    no-op dummy macro

0x8401    run full BIST; see section 7.1

0x8407    Reboot. The module will disappear from
          the VME bus for about 5 seconds.

0x8408    self-test one channel. PARAM0 is channel
          number. See section 7.2.

0x8409    power supply test. See 7.4.
```

6.9 FZAP - FIFO Clear Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Z15	Z14	Z13	Z12	Z11	Z10	Z9	Z8	Z7	Z6	Z5	Z4	Z3	Z2	Z1	Z0

The FZAP register allows clearing the 16 FIFO buffers and their associated rate divisor counters synchronously. Writing bit "Zn" clears channel "n". Writing 0xFFFF to this register will clear and synchronize sampling on all 16 channels. All channels must have identical FDIV values and trigger sources to subsequently remain in sync.

Channel FIFOs are cleared at the instant the FZAP register is written. Readback will display the last-written bit pattern.

6.10 VMETRIG - VME Trigger Register

Writing anything to the VMETRIG register creates a module internal VME Trigger pulse. This register always reads back all zeroes. See section 8.

6.11 TRIGGER, BOUNCE, M - Global Trigger Controls

The TRIGGER register selects the module operating modes that control simultaneous triggering of ADC data in a single module or across multiple modules. The BOUNCE register controls trigger debouncing. The M registers is the global trigger divisor. See section 8

6.12 CHER - Channel Setup Error Flags

Bits 0..15 of the CHER register are channel setup error flags for the 16 channels respectively. If a channel control register or filter setting register are set to illegal patterns, the corresponding CHER bit will be set. If CHER is nonzero, the red ERR front-panel LED will flash twice every few seconds.

6.13 Channel Registers

Each of the 16 A/D channels has a block of 7 associated registers.

6.13.1 Channel Control Register

Each of the 16 input channels has a channel control register, CTL0 through CTL15.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
											TMX		RN2	RN1	RN0

The RN bits select the input range for this channel, with the three RN bits encoded 0 through 6 decimal. Ranges are:

RN Code	Range	Approx LSB Resolution
0	± 10.24 mV	312.5 nV
1	± 40.96 mV	1.25 uV
2	± 160 mV	4.88 uV
3	± 640 mV	19.53 uV
4	± 2.56 V	78.13 uV
5	± 10.24 V	312.5 uV
6	± 40.96 V	1.25 mV

The powerup default is 5, selecting the ± 10.24 volt range.

The TMX bit controls the trigger multiplexer for sampling FIFO data. If the TMX bit is low, FIFO loading is clocked from the local 500 KHz ADC clock. If TMX is high, the FIFO is triggered by the module's MTRIG signal, which itself has selectable internal and external sources. Either source can be divided as noted in section 6.13.4. See section 8 for more discussion of triggering.

6.13.2 Filter Control Register

Each of the 16 input channels has a user-writable filter control register, FILT0 through FILT15.

The low byte controls the digital lowpass filter in the realtime data path, the path from the ADC to the RDATn realtime data register. The high byte controls the filter from the ADC into the FIFO, data from which appears at the FDATnA and FDATnB registers.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FB		FF4	FF3	FF2	FF1	FF0		RB		RF4	RF3	RF2	RF1	RF0

The five encoded RF or FF bits select the digital lowpass filter cutoff frequency, as follows:

F Code	Cutoff Frequency
0	1 Hz
1	1.6 Hz
2	2 Hz
3	4 Hz
4	5 Hz
5	8 Hz
6	10 Hz
7	16 Hz
8	20 Hz
9	40 Hz
10	50 Hz
11	80 Hz
12	100 Hz
13	160 Hz
14	200 Hz
15	400 Hz
16	500 Hz

F Code	Cutoff Frequency
17	800 Hz
18	1 KHz
19	1.6 KHz
20	2 KHz
21	4 KHz
22	5 KHz
23	8 KHz
24	10 KHz
25	16 KHz
26	20 KHz
27	40 KHz
28	50 KHz
29	reserved
30	reserved
31	100 KHz

Selection 31, 100 KHz, disables digital filtering and uses only the 100 KHz 5-pole analog filter ahead of the ADC.

If the RB bit is set, the realtime data path filter response is Butterworth; if clear, it is Bessel. If the FB bit is set, the FIFO data path filter response is Butterworth; if clear, it is Bessel.

Powerup default is 0x1212, 1 KHz Bessel filtering for both signal paths.

The contents of the realtime data register RDATn is updated 500,000 times per second regardless of the filter selection.

In the FIFO data path, ADC data is processed through the digital filter and data interpolator before being loaded into the FIFO. If the TMX control bit is low, sample interpolation is irrelevant, since triggers are synchronous to the 500 KHz clock.

In external trigger FIFO mode, the interpolator removes the 500 KHz ADC clock time quantization and makes the system behave as if the ADC were triggered by the external trigger. Interpolation is active at all filter settings.

For the triggered FIFO path, using Butterworth filters, excellent anti-aliasing is accomplished if the filter cutoff frequency is 0.4 of the sample rate or less, for

example a 4 KHz or lower filter for a 10 KHz sample rate. For Bessel filters, a filter cutoff frequency of 0.25 or less of the sample rate is appropriate.

6.13.3 FIFO Status Register

Each of the 16 ADC channels has a FIFOn register which reports the state of the channel FIFO buffer. The register arrangement is...

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FERR				FC11	FC10	FC9	FC8	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0

The low 11 bits indicate how many samples are currently stored in the FIFO, range 0 (empty) to 4095 (full). When this value is nonzero, valid data may be read from the FIFO. The FERR bit will be set if the FIFO overflows, namely if data is attempted to be transferred from the lowpass filter into the FIFO when no room is available. FERR will remain up until the FIFO is reset using the FZAP register.

The FIFO is unloaded by reading the FDATnA and FDATnB registers.

The unique FDAT analog data value -32768 (0x8000) is reserved for "FIFO empty." Actual analog inputs will rail at +32767 and -32767.

Multiple channel FIFOs may be cleared and synchronized using the FZAP register.

6.13.4 FIFO Divisor Register

Each of the 16 input channels has an FDIVn register which controls the rate at which data is loaded into the channel FIFO buffer. The register can be interpreted as an unsigned 16-bit integer D, where the FIFO data rate is TR/(D+1).

If the channel control register TMX bit is low, the trigger source TR is the local 500 KHz clock, which allows the FIFO to be loaded at rates from 500 KHz (D=0) to 7.6294 Hz (D=65535). Powerup default is 0, for a 500 KHz FIFO fill rate.

If the channel control TMX bit is high, the channel is triggered from the MTRIG master trigger signal, and FDIVn divides that rate, with value D=0 using the MTRIG signal undivided. See section 8.

An FZAP operation resets the divide hardware.

6.13.5 Channel Realtime Data Registers

Each of the 16 input channels has a realtime data register RDATn. This register is loaded with lowpass-filtered data sampled at the 500 KHz ADC sample rate, and may be read at any time. The value is interpreted as a signed 16-bit integer which spans the full bipolar range of the current ADC range. If one reads signed 16-bit integer N from this register, the actual voltage is

```
V = Range * N / 32768
```

where Range can vary from 10.24e-3 to 40.96.

For example, on the ±10.24 volt range,

```
 32767     0x7FFF    is   +10.239688  volts
     1     0x0001    is    +0.0003125 volts
     0     0x0000    is     0         volts
    -1     0xFFFF    is    -0.0003125 volts
-32767     0x8001    is   -10.239688  volts
```

6.13.6 Channel FIFO Data Registers

Each of the 16 input channels has a pair of read-only FIFO data registers FDATnA and FDATnB. Scaling of the FIFO data is identical to the realtime data noted above.

These registers can be accessed in three different ways:

16 bit word mode: in this mode, users read only the FDATnA register. Each read provides one FIFO output sample and decrements the FIFO count in the FIFOn register.

16 bit longword mode: in this mode, users operate in D16 bus mode but read longwords, as in a MOVE.L assembly instruction or a C-language assignment from a 32-bit volatile. This executes two VME bus cycles, the first a 16-bit read of the "A" register and the second a 16-bit read of the "B" register. The two reads unload successive FIFO data words and decrement the FIFO fill count by two.

32 bit mode: a single VME D32-type read at the FDATnA address can be used to read the "A" and "B" registers in a single bus transaction. Assuming a big-endian convention, the resulting 32 bit value will have the first-in-time ADC sample in bits 31..16, and the next sample in 15..0. The FIFO fill count is decremented by two.

In all cases, an attempt to read an empty FIFO sample will return data 0x8000; the FERR error flag will not be set.

Users should be careful to ensure that endian conventions do not reverse sample order when reading in either of the longword modes.

6.14 Realtime Considerations

When programming the V490, some VME register writes are serviced in FPGA hardware and some are processed through the on-board microprocessor. Registers tagged # in the register listing are hardware processed and their functions take place immediately when a register is written.

Because of microprocessor execution times and settling times of analog hardware and relays, some operations should be allowed to settle before other actions are performed. Some specifics are...

Changes in channel ranges or the RELAYS or MODE registers may involve relay switching, which may take up to 25 milliseconds to settle.

Changes to a FILTn filter settings register may take 2.5 milliseconds plus one full cycle of the cutoff frequency to settle. So after, for example, changing a filter to 100 Hz cutoff, wait at least 12.5 milliseconds before acquiring data.

If the TMX bit in a channel control register is changed, wait at least 2.5 milliseconds and then execute an FZAP operation on the channel to ensure that the trigger logic is initialized and that multiple channels will operate coherently.

If global triggering parameters are changed, by writing to the TRIGGER, BOUNCE, or M registers, or to a channel FDIV divisor, one should wait at least 2.5 milliseconds and then use FZAP to initialize the trigger logic of any affected channels.

7. BIST

All V490 units are capable of connecting one or more channel inputs to the front-panel D9 test connector. This allows users to apply known voltages to the channels and verify calibration. This facility is controlled by the MODE and RELAYS registers, as noted in sections 6.3 and 6.5.

The V490-2 version is furnished with a built-in-self-test facility, where an internal voltage generator is provided to drive the calibration bus. BIST verifies basic functionality of all ranges of all channels, but is not sufficiently accurate to verify calibration.

Internal BIST verifies reasonable channel performance for all ranges of all channels. Tests measure offset at zero input, gain near positive full scale and negative full scale, and verify common-mode rejection .

Formal calibration verification requires that an external, NIST-traceable precision voltage source be connected to the D9 test connector or to individual channel inputs. The MODE register also allows the internal BIST voltage generator to drive the internal cal bus and, if desired, also drive the D9 test connector. This allows the V490-2 to internally generate channel test voltages which can be measured with an NIST-traceable digital voltmeter.

7.1 Full BIST

To invoke the full automated BIST sequence, verify that the MS bit of the MACRO register is clear, then write 0x8401 to MACRO. Wait until the MS bit of MACRO clears, then read the BIST error counter register BERN. Execution time will be about 16 seconds.

If any errors are reported in the BERN register, read the channel BIST status registers BFLAG0 through BFLAG15, corresponding to channels 0 through 15. A zero value indicates no channel errors. The BFLAGn register format is....

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				CER	NER	PER	ZER		RA6	RA5	RA4	RA3	RA2	RA1	RA0

The RA0 through RA6 bits flag errors detected on gain ranges 0 through 6 respectively.

ZER is set if there was excessive zero offset on any range.

PER flags a gain error on any range with the input near positive full-scale.

NER flags a gain error on any range with the input near negative full-scale.

CER indicates insufficient common-mode rejection on any range.
Full BIST also runs the power supply self-test, reporting supply voltages, updating the VPERR error flags register, and counting any supply errors in BERN. See 7.4.

7.2 Single-channel Self-Test

To test a single channel, verify that the MS bit of the MACRO register is clear, then write the channel number (0..15) to the PARAM0 register, then write 0x8408 to the MACRO register. Wait until the MS bit of MACRO clears, then read the BIST error counter register BERN. Execution time will be about 1 second.

The BFLAGn register will summarize the test results of the named channel, as noted in section 7.1. The sequence involves 28 measurements, and the results of each measurement are recorded in the TONE0 through TONE27 registers. The TONE register values are as follows:

Reg	Range	Parameter	nom value
TONE0	0	zero offset	0
TONE1	0	positive input	31834
TONE2	0	negative input	-31834
TONE3	0	CMRR	0
TONE4	1	zero offset	0
TONE5	1	positive input	31834
TONE6	1	negative input	-31834
TONE7	1	CMRR	0
TONE8	2	zero offset	0
TONE9	2	positive input	20455
TONE10	2	negative input	-20455
TONE11	2	CMRR	0
TONE12	3	zero offset	0
TONE13	3	positive input	25079
TONE14	3	negative input	-25079
TONE15	3	CMRR	0
TONE16	4	zero offset	0
TONE17	4	positive input	25370
TONE18	4	negative input	-25370
TONE19	4	CMRR	0
TONE20	5	zero offset	0
TONE21	5	positive input	32000
TONE22	5	negative input	-32000
TONE23	5	CMRR	0
TONE24	6	zero offset	0

```
TONE25   6  positive input   8000
TONE26   6  negative input  -8000
TONE27   6  CMRR               0
```

7.3 Background BIST MUX function

On V490-2 modules, when a BIST macro operation is not active, users may control the BIST voltage generator, which allows a selection of signals to be applied to the internal calibration bus. The MODE register controls signal routing when an automatic BIST sequence is not active; see section 6.5.

To route the BIST voltage generator test signal to one or more channels, set the MODE register to 2 or 3 and use the RELAYS register to switch one or more channel test relays to the cal bus. Mode 2 connects the BIST voltage generator to the internal cal bus. In mode 3, the BIST source drives both the cal bus and the front-panel D9 test connector.

The BMUX VME register controls the signal applied to the cal bus. Load it with an integer between 0 and 31. Selections 0 through 15 are as follows:

BMUX	CAL VOLTAGE	NOM ADC CODE	on RANGE
0	zero volts	0	all
1	+ 9.948 V	+31834	0
2	- 9.948 mV	+31834	0
3	+39.791 mV	+31834	1
4	-39.791 mV	-31834	1
5	+99.877 mV	+20455	2
6	-99.877 mV	-20455	2
7	+489.83 mV	+25079	3
8	-489.83 mV	-25079	3
9	+1.982 V	+25370	4
10	-1.982 V	-25370	4
11	+10.000 V	+32000	5
12	-10.000 V	-32000	5
11	+10.000 V	+8000	6
12	-10.000 V	-8000	6
13	+99.877 mV CMRR	0	all
14	+1.982 V CMRR	0	all
15	+10 V CMRR	0	all

The selected test bus voltages will be accurate to about ±0.25%.

Selections 0, 13, 14, and 15 apply the same voltage to the differential CAL+ and CAL- bus lines and short the lines to one another with a low-offset solid-state relay.

If bit 4 of BMUX is set (ie, codes 16...31) the selected output is alternated with zero volts at a 200 Hz rate. For example, code 27 will result in a 100 Hz square wave on the cal bus, alternating between zero and +10 volts. Code 31 applies a 10 volt p-p square-wave common-mode signal. The signal alternation is synchronous to the LSB of the MCOUNT register.

There is some small channel loading of these signals, so best accuracy results when only one channel is selected. The "zero" and CMRR selections activate a solid-state relay which shorts the cal bus CAL+ and CAL- lines, ensuring a very low potential difference across the bus.

More than one channel test relay may be operated at any time, resulting in the inputs of selected channels being connected in parallel to the cal bus. For highest precision measurements, only one channel test relay should be activated at a time.

Note that channels are provided with protective devices which limit input current to about 1.5 mA in over-range conditions. Overdriving channels beyond their programmed voltage range regions can cause these 1.5 mA currents to be drawn from the calibration bus and external cal sources or BIST multiplexers, which could cause unexpected readings on other channels.

7.4 Power Supply BIST

The V490 has provision for monitoring its internal power supply voltages. The power supplies are checked when the full BIST test (macro 0x8401) is executed. These tests can also be invoked with the 0x8409 macro.

The PERR register flags power supply voltage errors, and the EP17..EM17 registers report actual supply voltages. BERN counts any errors.

The PERR register layout is...

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								M17	M5	P1	P2	P3	P5	P9	P17

Each bit has a corresponding voltage reporting register. The LSB value is 1 millivolt.

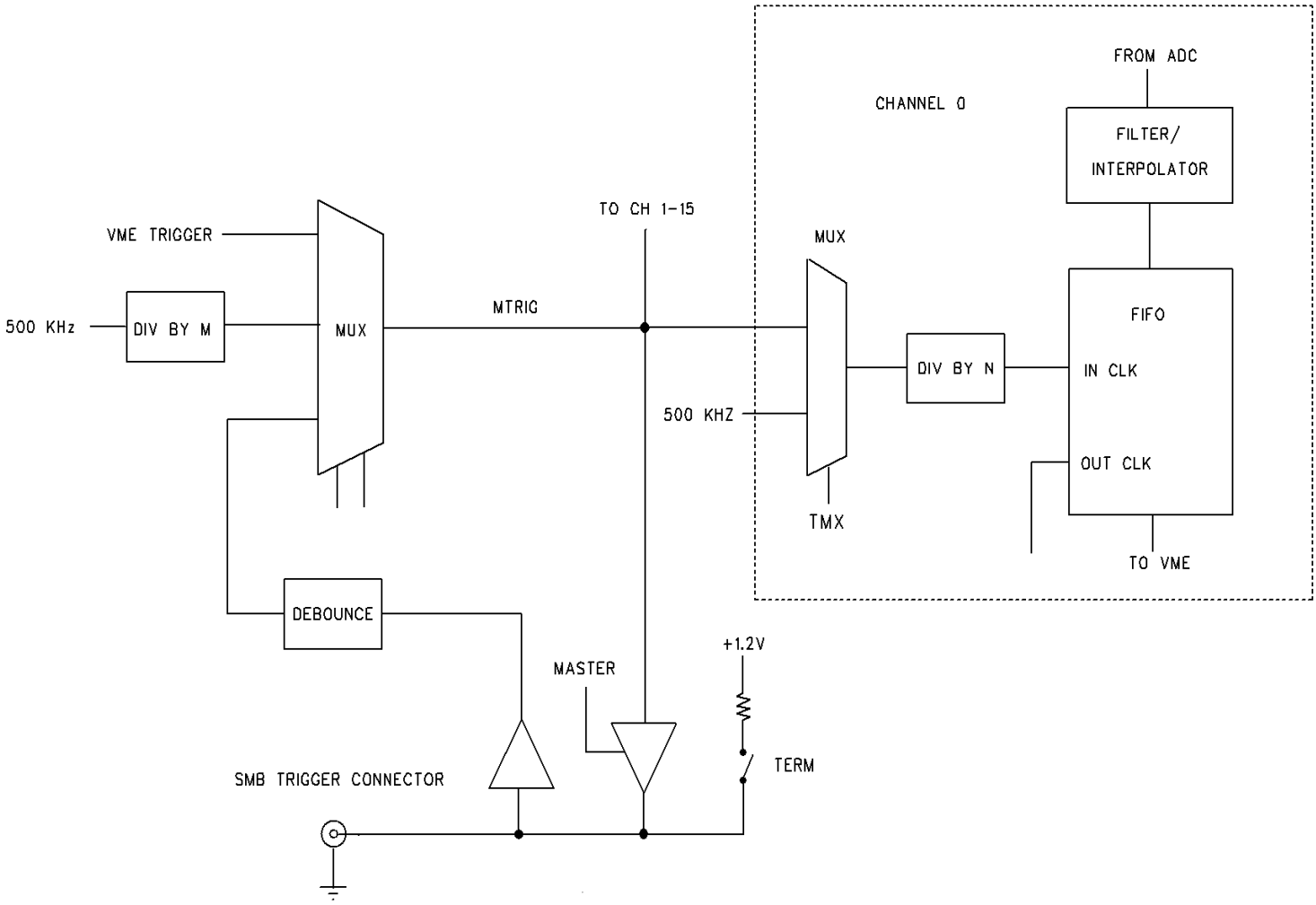
BIT	VOLTAGE	REGISTER
P17	+17	EP17
P9	+8.8	EP9
P5	+5	EP5
P3	+3.3	EP3
P2	+2.048	EP2
P1	+1.25	EP1
M5	-5	EM5
M17	-17	EM17

8. Local and Global Triggering

Each V490 channel is capable of emulating a classic ADC architecture: preamp, lowpass filter, triggered ADC, FIFO. The actual implementation uses a 16-bit ADC that runs continuously at 500 KHz, a digital filter, and a digital interpolator, with FIFO data sampled at the instant a trigger is received. The result is a signal-theory equivalent of the classic architecture but with superior noise performance and continuous availability of realtime data even when triggers are not present.

Only FIFO data is triggered. The RDATn realtime data registers always reflect the instantaneous output of the realtime path lowpass filters.

The trigger logic of the V490 is depicted below.



The TMX bit in each channel control register selects whether this channel uses the local 500 KHz clock and divide-by-N counter as the FIFO trigger, or whether it uses the shared MTRIG signal.

The front-panel SMB trigger connector can be used to input or output shared triggers.

The module's TRIGGER register selects the overall module trigger mode. The selections are...

0	OFF	MTRIG is inactive. The SMB connector is ignored.
1	LOCAL VME	MTRIG is fired by writing to the VMETRIG register of this module. The SMB is ignored.
2	LOCAL DIVN	MTRIG is driven by the 500 KHz clock, divided by integer M. The SMB is ignored.
3	MASTER VME	MTRIG is fired by writing to the VMETRIG register of this module. MTRIG also drives the SMB connector as the master trigger source.
4	MASTER DIVN	MTRIG is driven by the 500 KHz clock divided by integer M. This module also drives the SMB as the master trigger source.
5	SLAVE	MTRIG is received from the SMB trigger connector, from a user trigger pulse or from another V490 which is in master mode.
6	SLAVE TERM	Like 5 above, but the SMB trigger input signal is also electrically terminated, 50 ohms to 1.6 volts.

The BOUNCE register allows digital debouncing to be added to the external trigger path. This may prove useful in many-channel systems with imperfectly controlled trigger distribution. Loading BOUNCE with an integer D, in the range of 0 to 255, adds a trigger debounce time of 7.8 nanoseconds times D. The debounce time will add to trigger latency, and restrict the trigger rate to no higher than the reciprocal of twice the debounce time.

The "M" register allows the internal 500 KHz clock to be divided and used as the MTRIG source in trigger modes 2 and 4. The resulting trigger frequency is 500K/(M+1).

In configuring a master/slave system, the V490 modules are preferentially physically contiguous in the VME crate, with the master on the left and the terminating slave in the rightmost slot.

When a module drives the trigger bus as master, it generates 1 microsecond wide positive trigger pulses at 3.3 volt CMOS level.

All modules may be configured as slaves, with samples taken at the rising edge of a user-furnished trigger pulse. The user-furnished trigger would drive the trigger string from the left, and the rightmost module would be programmed as the terminating slave.

Slave modules have an input threshold of about 1.5 volts and trigger on a received rising edge. The inputs are 5-volt tolerant. Terminating slaves terminate to 1.6 volts at 50 ohms.

See section 6.14 for some realtime considerations.

Highland can furnish SMB-BNC cables and SMB connector bussing assemblies that properly distribute the trigger and analog calibration signals present on module trigger connectors. Electrical and fiberoptic fanouts are also available.

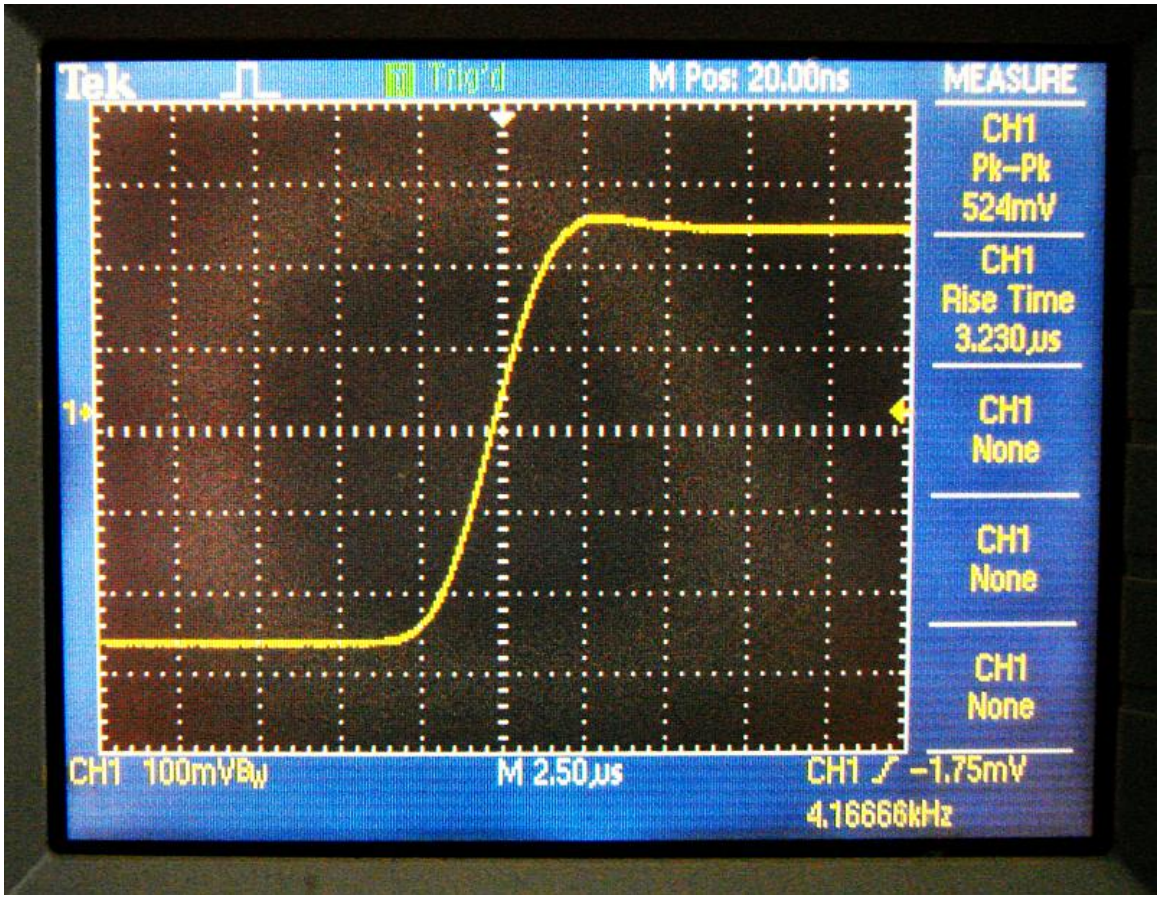
Model J346-3 3-position Trigger Bussing Strip

9. Typical Performance

9.1 Analog Filter

The analog anti-aliasing filter before the A/D converter is a 5-pole transitional Gaussian lowpass with a 3 dB point of 100 KHz. It is down about 60 dB at 400 KHz, the first major alias. The combination of pre-ADC analog filtering and post-ADC digital filtering is basically alias free.

The analog filter step response is shown below.



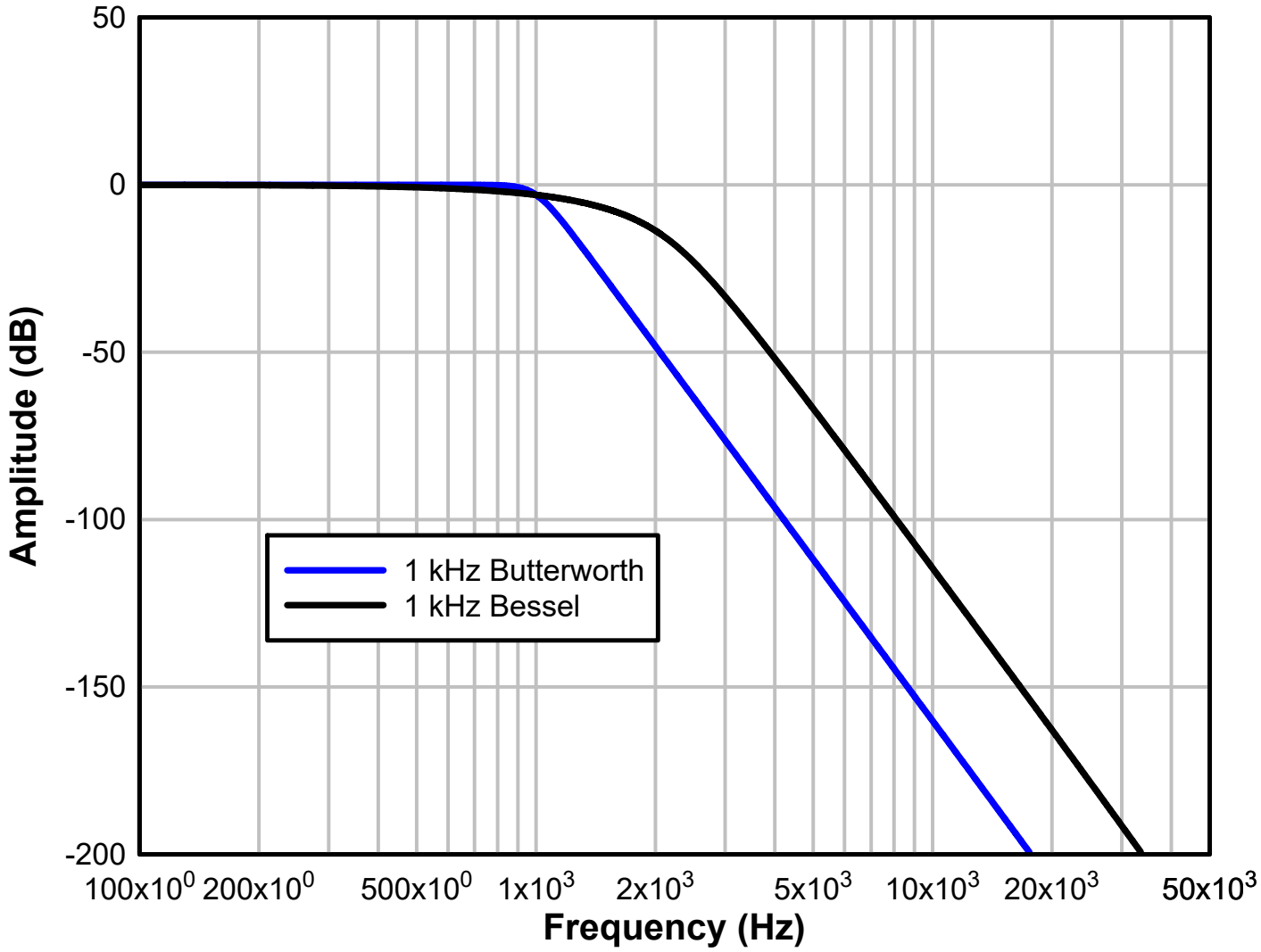
The 10 millivolt range of the input differential amplifier has a reduced bandwidth of about 50 KHz, with a risetime of about 7 microseconds.

9.2 Digital Filters

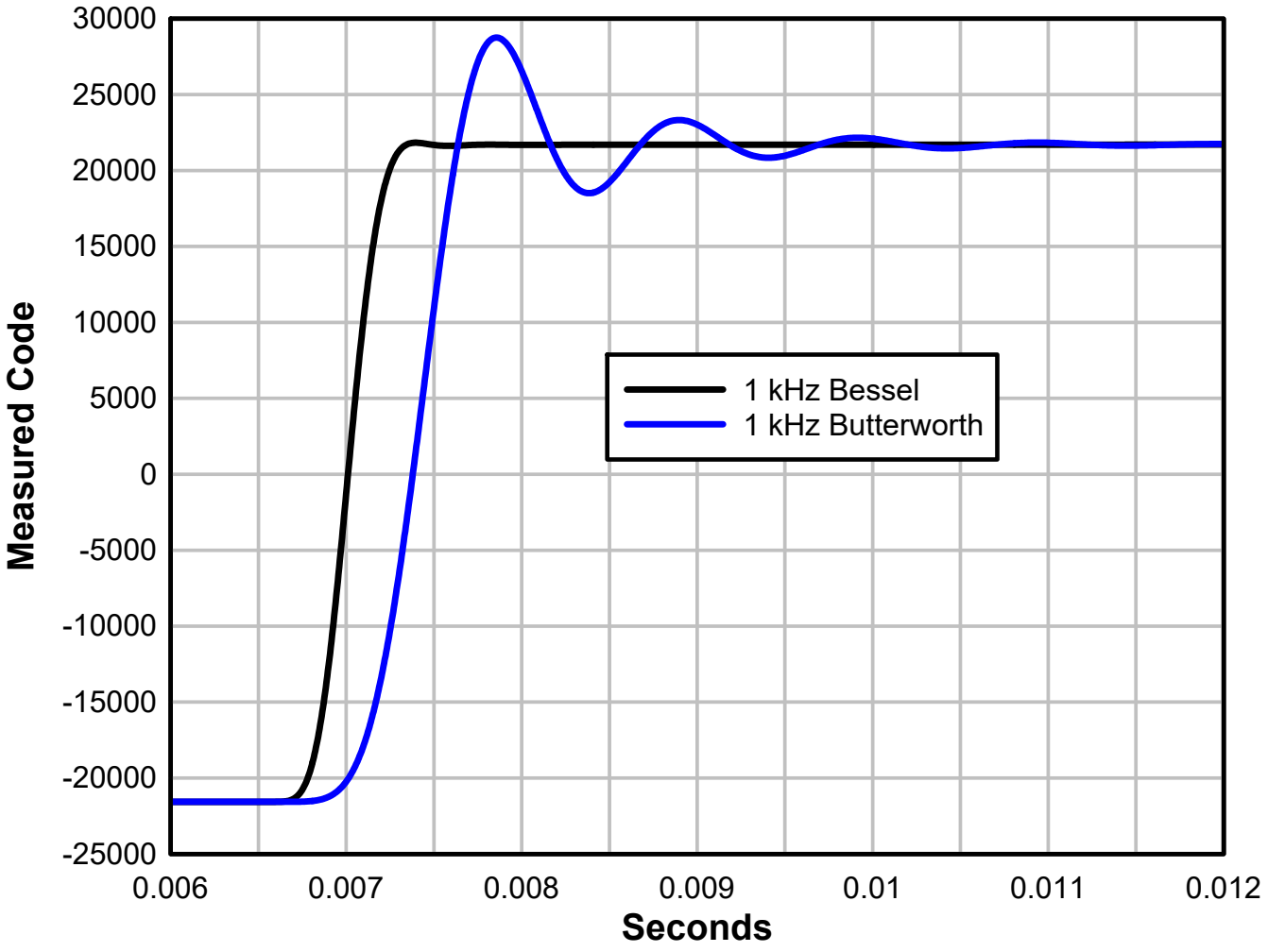
Each channel has two independent 8-pole programmable digital filters, one for the realtime data path and one for the FIFO data path. Each is selectable to have Bessel (best phase response) or Butterworth (best frequency rolloff) response, and each is programmable in steps from 1 Hz to 50 KHz. A "filter off" selection allows 100 KHz response, using just the front-end analog filter.

The digital filters always operate at the 500 KHZ ADC sample rate, so they do not introduce aliasing that might be associated with filtering schemes which decimate sample rates to simplify the internal math.

The graph below compares the frequency responses of 1 KHz Bessel and Butterworth filters. Other filter frequencies have similar scaled rolloffs.



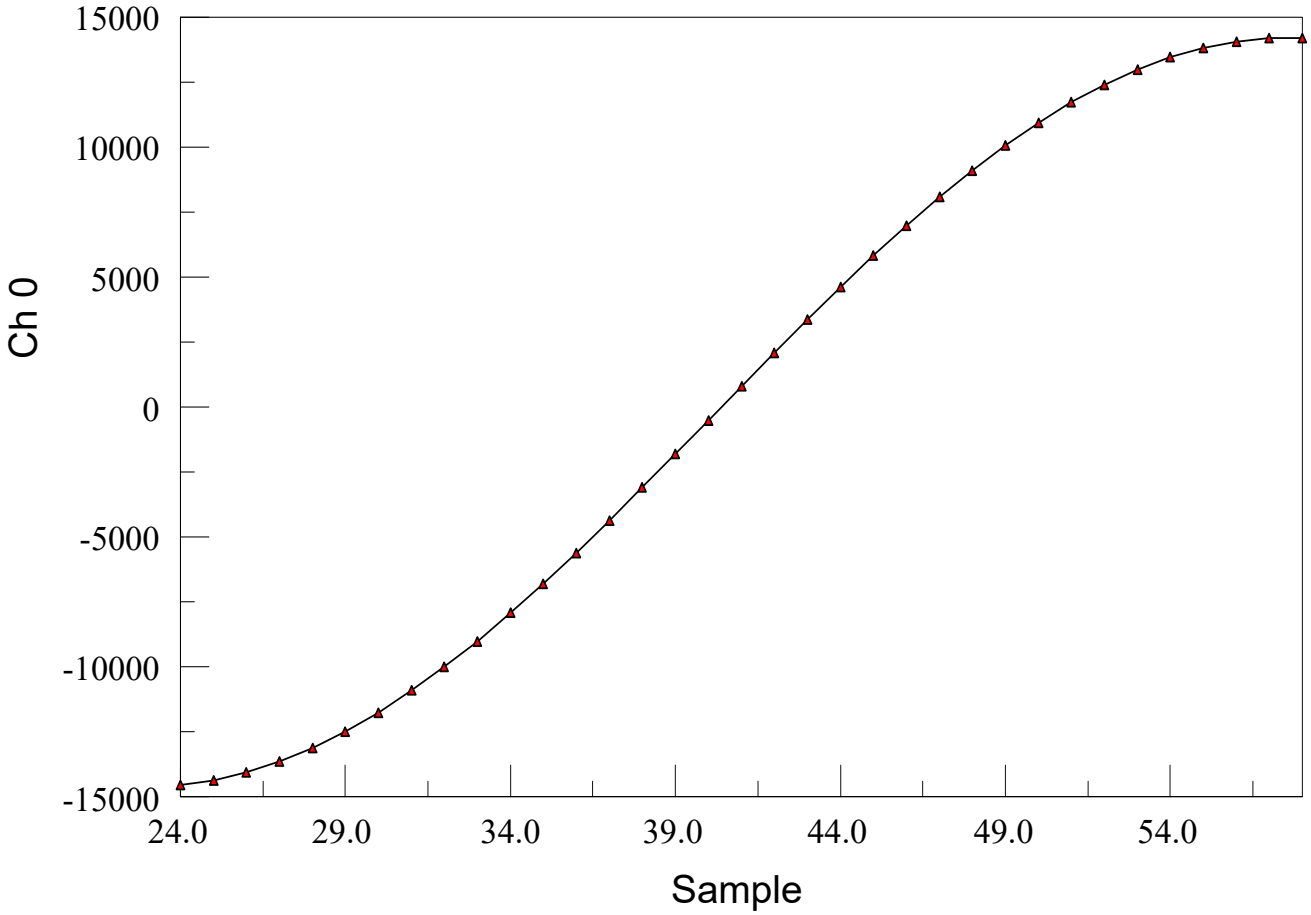
The graph below compares the step responses of 1KHz Bessel and Butterworth filters, as digitized and FIFO buffered by a V490. The Butterworth has superior frequency rolloff at the expense of time-domain overshoot. The Butterworth is actually a closer approximation of a mathematically ideal "brickwall" lowpass filter.



9.3 Interpolation

The waveform below is a portion of a 10 KHz sine wave, externally triggered at a sample rate of 700 KHz, above and asynchronous to the 500 KHz sample rate of the channel ADC. Note that the data points are smoothly positioned along the sine wave and are not quantized to the 500 KHz sample rate.

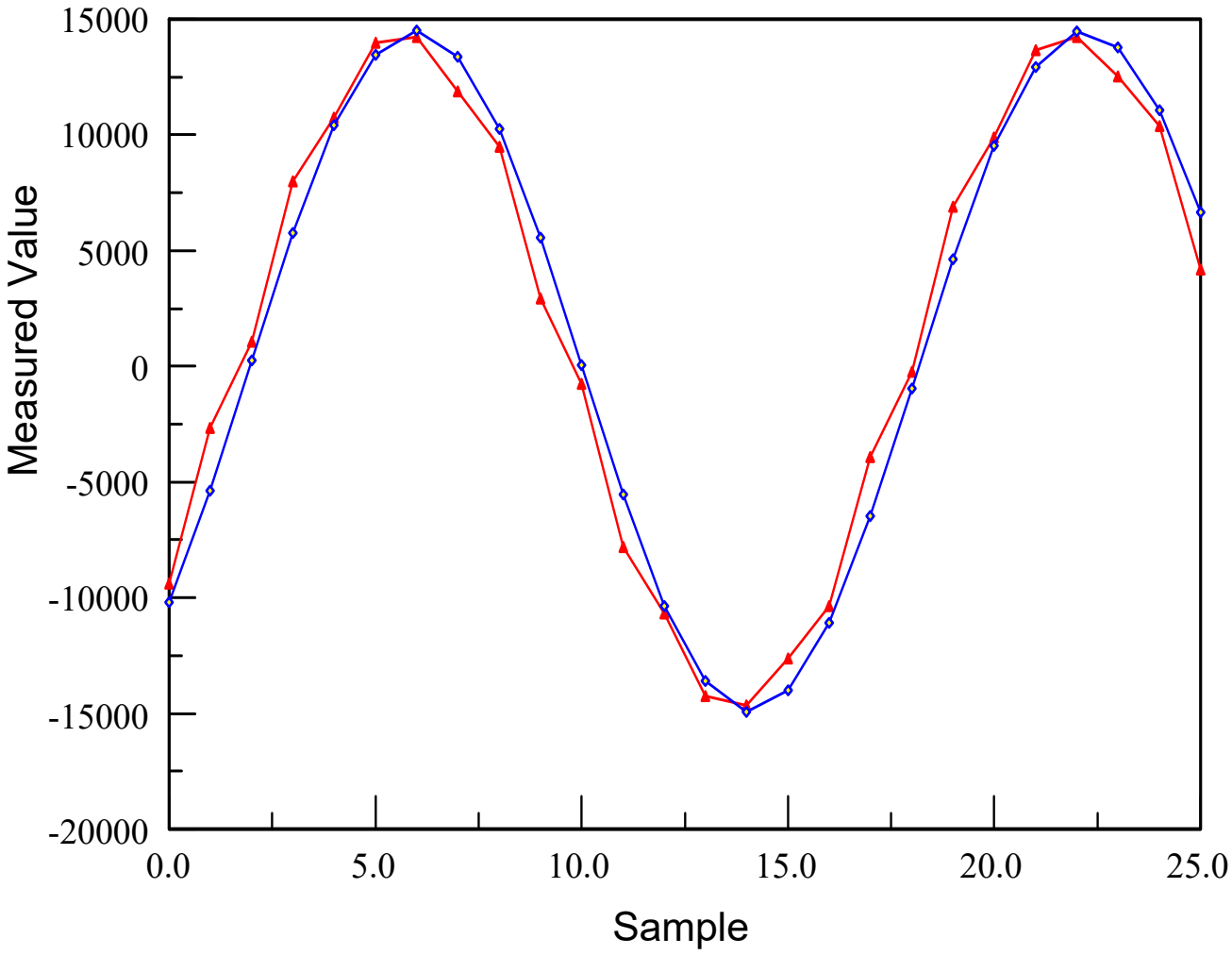
The FIFO data interpolator allows the V490 to sample the signal accurately at the 700 KHz external trigger rate.



From an external, asynchronous trigger, the equivalent ADC sample-and-hold aperture jitter typically measures about 4.1 nanoseconds RMS. This represents the statistical timing error of the V490 from an external trigger, as compared to an ideal triggered sample-and-hold and ADC.

The graph below shows two channels with the same signal applied. The blue curve is normal operating mode, and the red curve was taken with interpolation disabled.

The V490 was externally triggered at 333 KHz, and the analog input to both channels was a 20 KHz sine wave. Again, the interpolation algorithm allows the input signal to be accurately sampled at external trigger times. Without interpolation, the 500 KHz ADC sampling rate adds time quantization jitter to external trigger times.

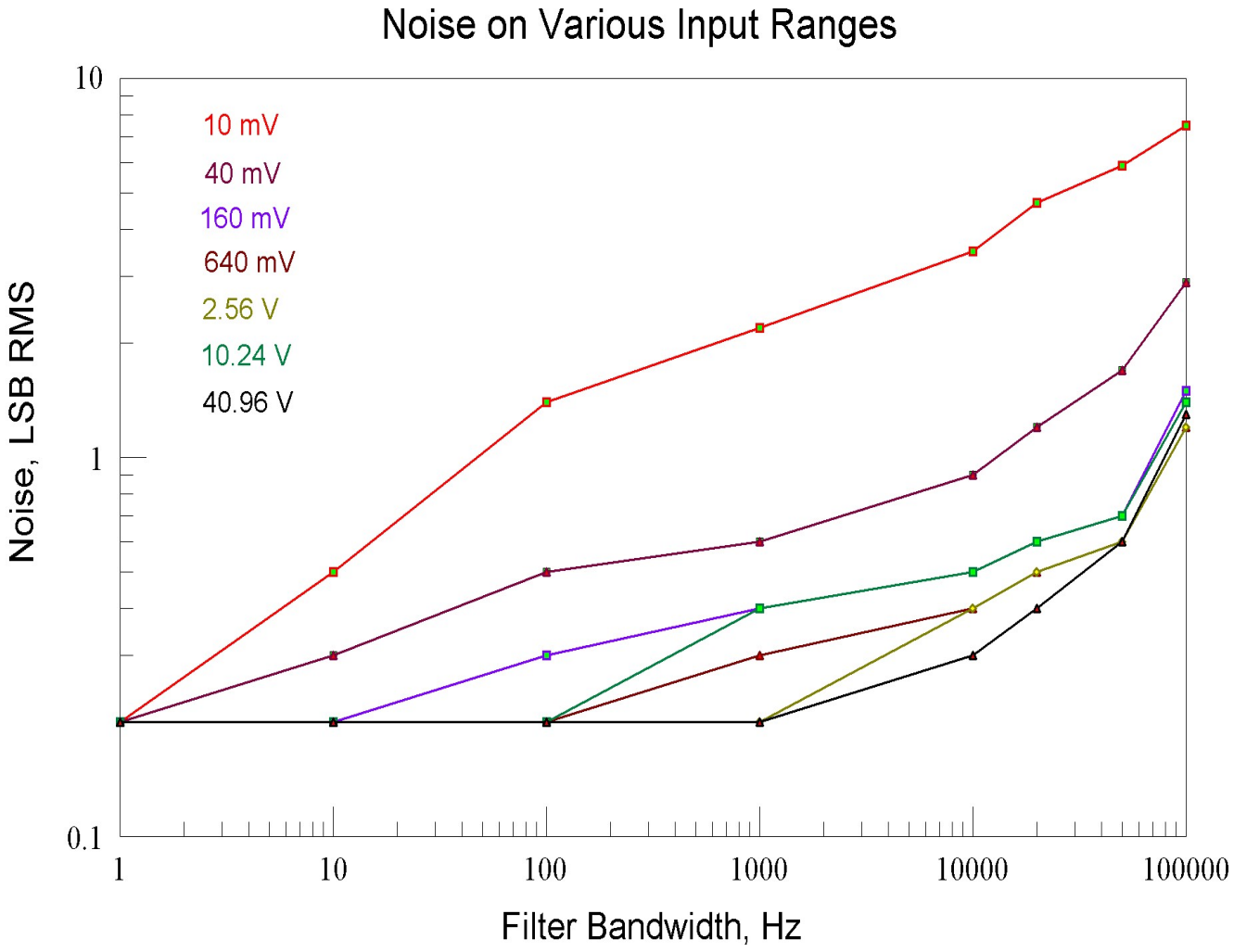


9.4 Noise Performance

The following graph shows equivalent shorted-input RMS noise, expressed in realtime register LSBs, as a function of channel range and filter bandwidth.

To convert these values to volts, multiply by the specified range full-scale value and divide by 32768. For example, on the 40 millivolt range, with 1 KHz filtering selected, noise is 0.6 bits, or 0.75 microvolts RMS.

The worst noise is on the 10 mV range with 100 KHz filtering, which is 7.5 LSBs, equivalent to 2.3 microvolts RMS. This represents a noise density of about 10.5 nV/rootHz.



10. Versions

The following are the standard V490 versions:

V490-1 16-channel VME multi-range digitizer

V490-2 16-channel VME multi-range digitizer with BIST

11. Customization

Consult factory for information about additional custom versions.

12. Hardware and Firmware Revision History

12.1 Hardware Revision History

Revision E	Aug 2022 Improved manufacturability. Functionally equivalent to Revision D
Revision D	Feb 2019 Modified PCB layout to improve noise rejection
Revision C	Jun 2010 Allows CAL voltage to be output from D9 Brings out Trig as I/O on SMB connector located between D-sub connectors
Revision B	Apr 2010 First production release
Revision A	Jan 2010 Initial PCB release

12.2 Firmware Revision History

Revision C	May 2014 Improves alignment of BIST limits to module specifications
Revision B	Jul 2010 For Rev B and C Hardware

	Uses FPGA 22C491B **I**ncludes 32 filter frequency selections, 1 1.6 2 etc. order
Revision A	May 2010 For Rev B Hardware (Interim release of the firmware for the V490 rev B) Uses FPGA 22C491A Partially functional: no filtering/FIFO, no power supply BIST

The firmware is provided as a plug-in EPROM chip which can be field upgraded. This chip is labeled "22E490-C".

The FPGA configuration is provided on a plug-in serial flash chip which can also be replaced in the field. It is labeled "22C491C"

13. Accessories

J55-1	6' shielded D25 male to D25 male cable
J56-1	10' shielded D25 male to D25 male cable
J71-1	Dual D9 female to Agilent 34104A cable
J75-1	D9 female to two(2) dual banana plug cable
J75-2	D9 female to dual banana plug cable
J76-X	D9 OpenCVA busing cable
J346-X	SMB trigger bus cable
J475-1	8-channel D25 female Din rail termination panel