



SCHEMATIC SHEETS

- 1. BLOCK DIAGRAM
- 2. OC3 & CLOCK
- 3. CONTROL FPGA
- 4. TIMING FPGA
- 5. CH 0 VERNIER
- 6. CH 1 VERNIER
- 7. CH 2 VERNIER
- 8. CH 3 VERNIER
- 9. CH 4 VERNIER
- 10. CH 5 VERNIER
- 11. CH 6 VERNIER
- 12. CH 7 VERNIER
- 13. MICROPROCESSOR
- 14. ADC
- 15. PULSE MONITOR OUTPUT
- 16. VME
- 17. POWER CONDITIONING
- 18. REFERENCE OUTPUT, TEST, LED'S

BLOCK DIAGRAM

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ENGINEER J LARKIN	DATE 4/10/01	HIGHLAND TECHNOLOGY INC.	
DRAWN M SALAZAR	11/20/03	SCHEMATIC TIMING MODULE	
CHECKED			
APPROVED			
RELEASED		DRAWING NO: 22S880	REV: D
		SHEET: 1 OF 18	FILENAME:22S880D.SCH