





SHEETS

1 BLOCK DIAGRAM

2 I/O 0...7

3 I/O 8...15

4 I/O 16...23

5 I/O 24...31

6 I/O 32...39

7 I/O 40...47

8 I/O 48...55

9 I/O 56...63

10 OUTPUT DRIVERS

11 DACS/AMPS

12 VME 1

13 VME 2

14 POWER

15 FPGA 1

16 FPGA 2/CLOCK/FLASH

1_BLOCK_DIAGRAM

CONFIDENTIAL PROPRIETARY INFORMATION COPYRIGHT HIGHLAND TECHNOLOGY ENGINEERING CHANGE ORDERS MAY APPLY

C DEVEZE DATE 12/18/2019 HIGH	HLAND TECHNOLOGY INC.
DRAWN CD/BG 12/18/2019	SCHEMATIC, V250
	IGITAL INPUT/OUTPUT
IPPROVED DRAWING N	NO: 22S250 REV: B
RELEASED	OF 16 FILE: 22S250B.sch