



SHEETS

1. BLOCK DIAGRAM
2. CH 0 SIGNAL CONDITIONING
3. CH 1 SIGNAL CONDITIONING
4. CH 2 SIGNAL CONDITIONING
5. CH 3 SIGNAL CONDITIONING
6. CH 4 SIGNAL CONDITIONING
7. CH 5 SIGNAL CONDITIONING
8. CH 6 SIGNAL CONDITIONING
9. CH 7 SIGNAL CONDITIONING
10. POWER REGULATORS & DACS
11. TIMER FPGA
12. MICROPROCESSOR
13. VME INTERFACE
14. TEST CIRCUITS & CLOCK
15. OVERSPEED RELAYS

BLOCK DIAGRAM

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ENGINEER J LARKIN	DATE 6/21/06	HIGHLAND TECHNOLOGY INC.	
DRAWN M SALAZAR	6/21/06	SCHEMATIC, V365 TACH/OVERSPEED MODULE	
CHECKED			
APPROVED		DRAWING NO: 22S365 SHEET: 1 OF 15	
RELEASED			
		REV: B	FILENAME: 22S365B.SCH