

## Notes: Unless Otherwise Stated

### Scheme Spec:

FLASH: MLC, 3V  
DRAM: DDR3, 1.5V  
Key: Vol+, Vol-, MENU, SEARCH, HOME, ESC, ENTER  
Power: DCIN, 5V, 2A; BAT, 4.2V  
USB0: OTG  
USB2: WIFI  
WIFI: USB WIFI&SDIO WIFI+BT  
Card: TFcard  
Other: Headphone, MIC, G-Sensor, Camera


### Power Supply:

Name	Vout	Imax	Use
AXP209 DCDC2	1.25V	1600mA	CPU
AXP209 DCDC3	1.2V	1200mA	CORE
AXP209 LDO1	1.3V	30mA	RTC
AXP209 LDO2	3V	200mA	AVCC
AXP209 LDO3	2.8V	400mA	CSI0-IO
AXP209 LDO4	2.8V	200mA	CSI1-IO
AP2125 LDO	1.8V	300mA	CSI-DVDD
AP3410 DCDC	1.5V	1200mA	DRAM
AP3410 DCDC	3V	1200mA	VCC/LCD/NAND//WIFI
SY7208	5V	1000mA	HDMI/USB
AP2125 LDO	3.3V	300mA	WIFI
AP3032 DCDC		1400mA	LCD
AP3032 DCDC		1400mA	LCD
AP3032 DCDC		1400mA	LCD MIPI

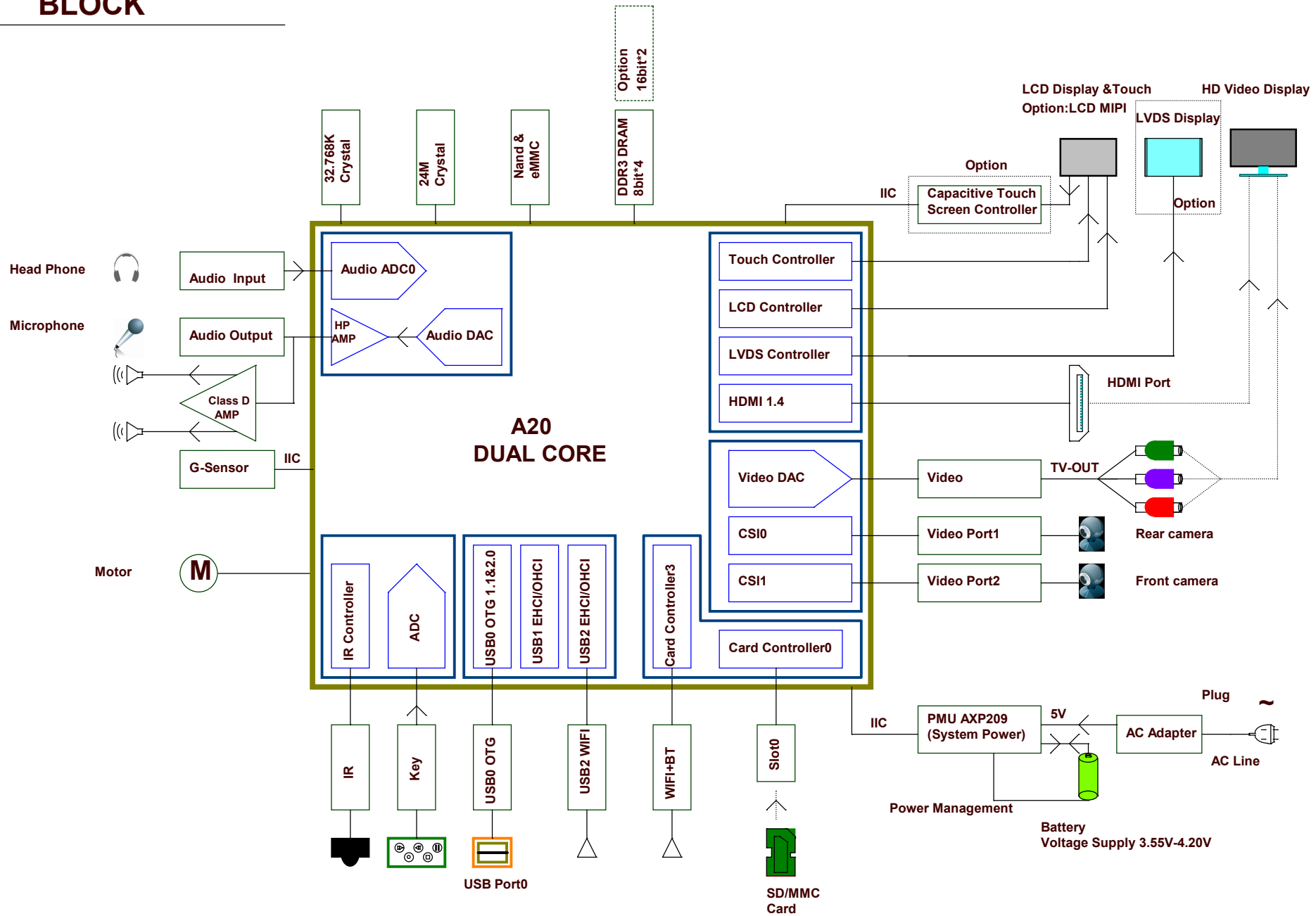
### Schematics Index:

P01: COVER  
P02: BLOCK  
P03: PIO ASSIGNMENT  
P04: POWER TREE  
P05: CPU1  
P06: CPU2  
P07: DDR3 8bit x 4pcs  
P08: DDR3 16bit x 2pcs  
P09: BESIDE CPU  
P10: POWER1  
P11: POWER2  
P12: NAND&eMMC  
P13: HDMI-CSI  
P14: KEY-IR-TVOUT-MT  
P15: CARD-DEBUG-GS  
P16: LCD  
P17: WIFI+BT  
P18: USB  
P19: HP-MIC-SPK  
P20: LCD MIPI 7"85

Rev	Description	Date	Drawn	Checked	Approved
A20_PAD_STD_V1.0		2013-01-30			
A20_PAD_STD_V1.1		2013-04-01	Dennislo		

 AllWinner Technology Co.,Ltd			
Title A20_PAD_STD			
Size A3	Document Number COVER		Rev
Date: Monday, April 01, 2013	Sheet 1 of 20		

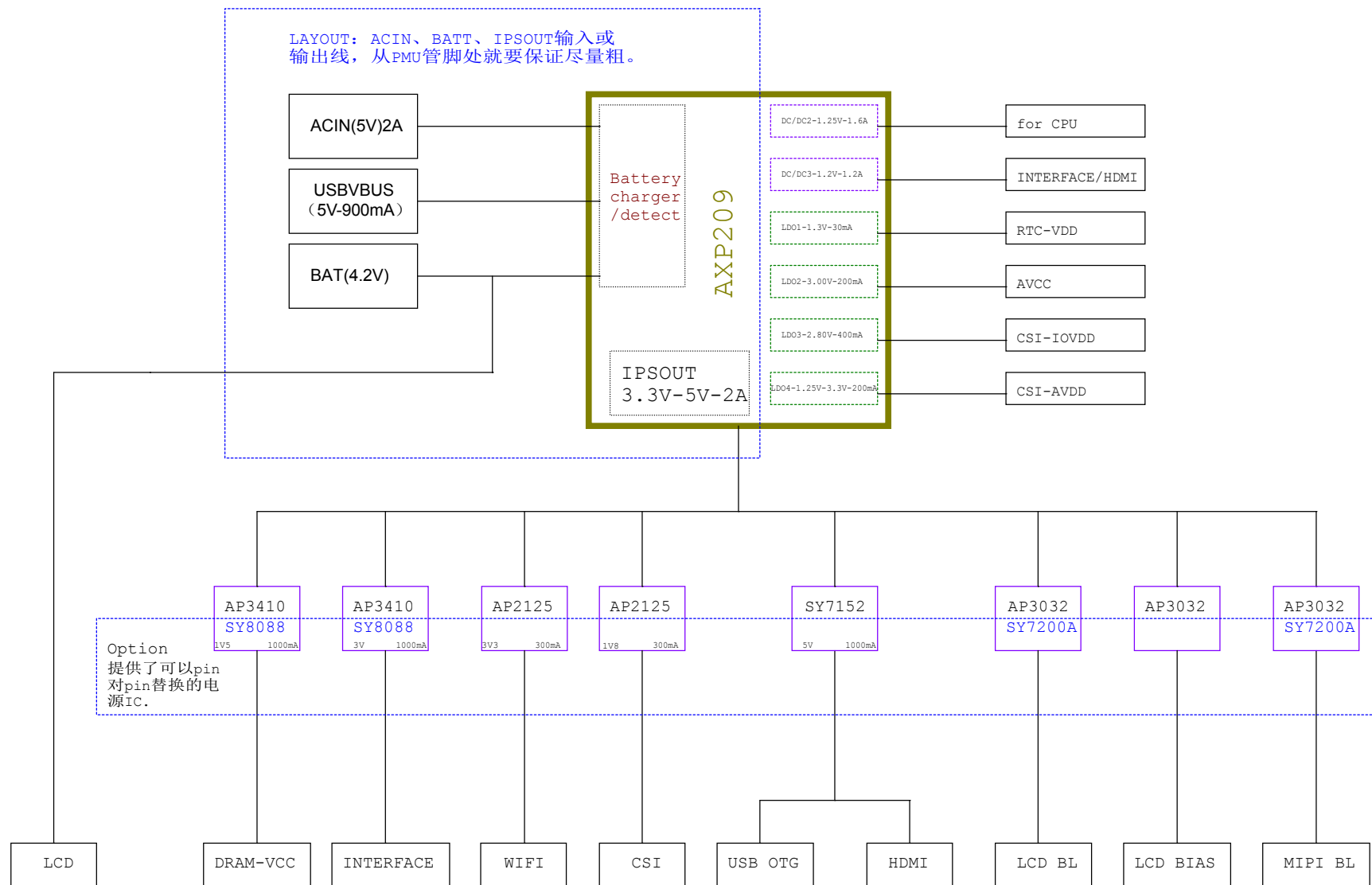
# BLOCK



PIO ASSIGNMENT

Pin Group	Pin Name	Define	Function	Pin Group	Pin Name	Define	Function	Pin Group	Pin Name	Define	Function	Pin Group	Pin Name	Define	Function	Pin Group	Pin Name	Define	Function		
PA (18)	PA0	GPIO	LCD-CSX	PC (25)	PC0	NWE#	NAND	PD (28)	PD18	LCD0_D18	LCD	PH (28)	PH0	EINT0	USB-ICTRL	PI (22)	PI15	GPIO			
	PA1	GPIO			PC1	NALE			PD19	LCD0_D19			PH1	GPIO_IN	SD0-DET		PI16	GPIO			
	PA2	GPIO			PC2	NCLE			PD20	LCD0_D20			PH2	GPIO_IN			PI17	GPIO			
	PA3	GPIO			PC3	NCE1			PD21	LCD0_D21			PH3	GPIO_OUT	USB2-DRV		PI18	GPIO			
	PA4	ETXD3			PC4	NCE0			PD22	LCD0_D22			PH4	GPIO_IN	USB0-IDDET		PI19	GPIO			
	PA5	SPI3-CS0			PC5	NRE#			PD23	LCD0_D23			PH5	GPIO_IN	ACIN-EN		PI20	GPIO_OUT	BT-WAKE		
	PA6	SPI3-CLK			PC6	NRB0			PD24	LCD0_CLK			PH6	GPIO_OUT	LCD-RST		PI21	GPIO_OUT	BT-HOST-WAKE		
	PA7	SPI3-MOSI			PC7	NRB1			PD25	LCD0_DE			PH7	GPIO_OUT	LCD-BL-EN						
	PA8	SPI3-MISO			PC8	NDQ0			PD26	LCD0_HSYNC			PH8	GPIO_OUT	LCD-FWR						
	PA9	GPIO			PC9	NDQ1			PD27	LCD0_VSYNC			PH9	GPIO_OUT	WIFI-SHDN						
	PA10	GPIO			PC10	NDQ2		PE (12)	PE0	CSIO_PCLK	CSIO		PH10	GPIO_IN	WIFI-HOST-WAKE						
	PA11	GPIO			PC11	NDQ3			PE1	CSIO_MCLK			PH11	GPIO							
	PA12	GPIO			PC12	NDQ4			PE2	CSIO_HSYNC			PH12	GPIO							
	PA13	GPIO			PC13	NDQ5			PE3	CSIO_VSYNC			PH13	GPIO_OUT	CAM-R-RESET#						
	PA14	GPIO			PC14	NDQ6			PE4	CSIO_D0			PH14	GPIO_OUT	CAM-F-RESET#						
	PA15	GPIO			PC15	NDQ7			PE5	CSIO_D1			PH15	GPIO_OUT	PA-SHDN#						
	PA16	GPIO			PC16	NWP			PE6	CSIO_D2			PH16	GPIO_OUT	CAM-PWR-EN						
PA17	GPIO	PC17	NCE2		PE7	CSIO_D3			PH17	GPIO											
PB (24)	PB0	TWIO_SCK	PMU		PC18	NCE3			PF (6)	PF0	SDC0_D1		SDC0	PI (22)	PI0		GPIO	WIFI			
	PB1	TWIO_SDA			PC19	GPIO				PF1	SDC0_D0				PI1		GPIO				
	PB2	PWM0			PC20	GPIO				PF2	SDC0_CLK				PI2		GPIO				
	PB3	GPIO_OUT			PC21	GPIO				PF3	SDC0_CMD				PI3		GPIO				
	PB4	IR0_RX	IR		PC22	GPIO		PF4		SDC0_D3	PI4				SDC3_CMD						
	PB5	GPIO_OUT	BT-RST		PC23	GPIO		PF5		SDC0_D2	PI5				SDC3_CLK						
	PB6	I2S_BCLK	BT-PCM-CLK	PD (28)	PC24	NDQS	LCD	PG (12)	PG0	CSII_PCLK	CSII		PI6		SDC3_D0						
	PB7	I2S_LRCK	BT-PCM-SYNC		PD0	LCD0_D0			PG1	CSII_MCLK			PI7		SDC3_D1						
	PB8	I2S_DO0	BT-PCM-OUT		PD1	LCD0_D1			PG2	CSII_HSYNC			PI8		SDC3_D2						
	PB9	GPIO_OUT	USB0-DRV		PD2	LCD0_D2			PG3	CSII_VSYNC			PI9		SDC3_D3						
	PB10	GPIO	BT-PCM-IN		PD3	LCD0_D3			PG4	CSII_D0			PI10		GPIO						
	PB11	GPIO			PD4	LCD0_D4			PG5	CSII_D1			PI11		GPIO	CLK-32K					
	PB12	I2S_DI			PD5	LCD0_D5			PG6	CSII_D2			PI12		SPI0_MOSI						
	PB13	GPIO_OUT			PD6	LCD0_D6			PG7	CSII_D3			PI13		GPIO						
	PB14	JTAG_MS0	JTAG		PD7	LCD0_D7			PG8	CSII_D4			PI14		GPIO						
	PB15	JTAG_CK0			PD8	LCD0_D8			PG9	CSII_D5											
	PB16	JTAG_DO0			PD9	LCD0_D9			PG10	CSII_D6											
	PB17	JTAG_DI0			PD10	LCD0_D10			PG11	CSII_D7											
	PB18	TWI1_SCK	TWI1		PD11	LCD0_D11		PG (12)	PG0	CSII_PCLK	CSII										
	PB19	TWI1_SDA			PD12	LCD0_D12			PG1	CSII_MCLK											
	PB20	TWI2_SCK	TWI2		PD13	LCD0_D13			PG2	CSII_HSYNC											
	PB21	TWI2_SDA			PD14	LCD0_D14			PG3	CSII_VSYNC											
	PB22	UART0_TX	UART (DEBUG)		PD15	LCD0_D15			PG4	CSII_D0											
PB23	UART0_RX	PD16			LCD0_D16	PG5			CSII_D1												
			PD17		LCD0_D17	PG6			CSII_D2												
						PG7			CSII_D3												
						PG8			CSII_D4												
						PG9			CSII_D5												
						PG10			CSII_D6												
						PG11			CSII_D7												

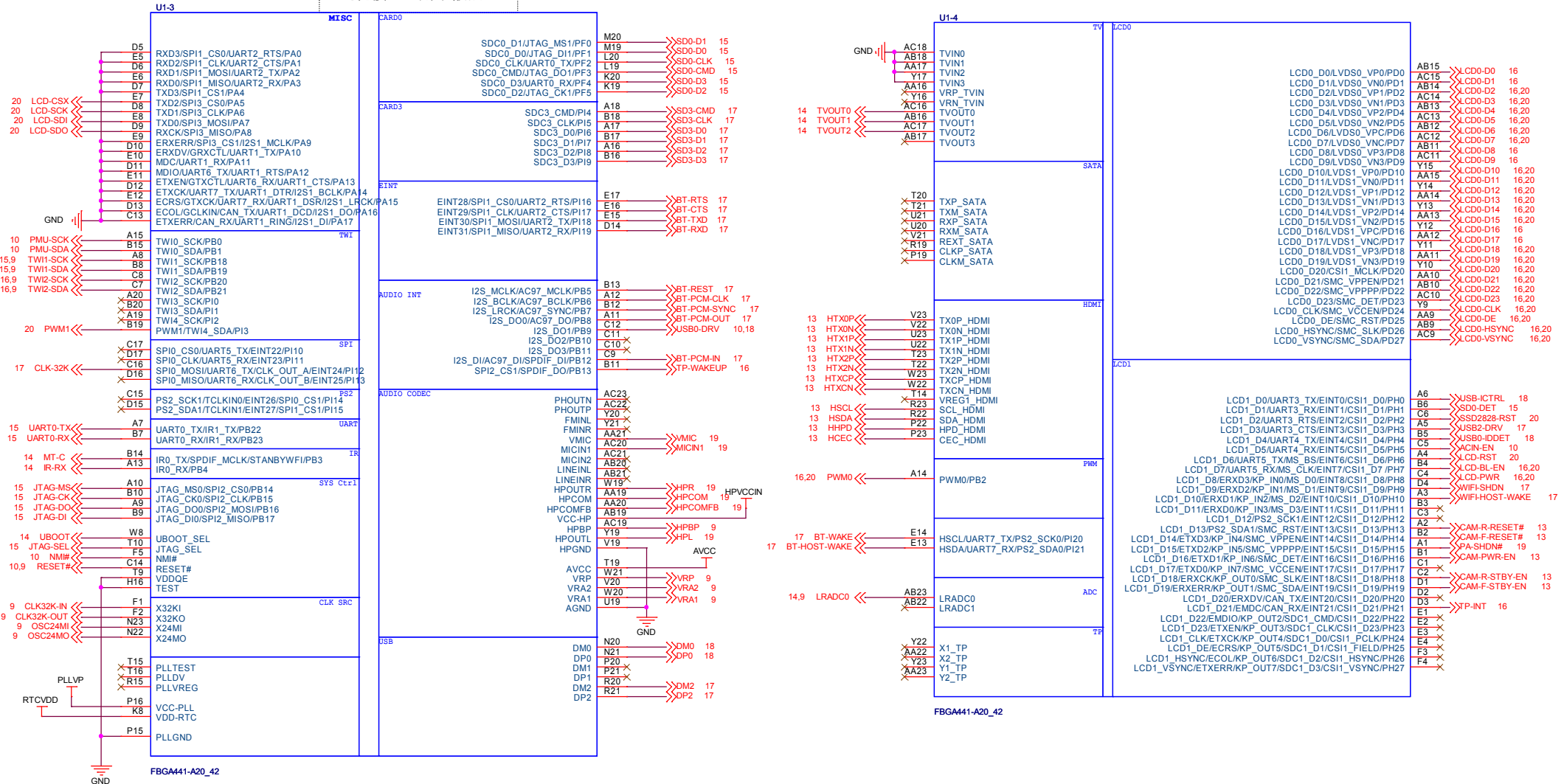
# POWER TREE





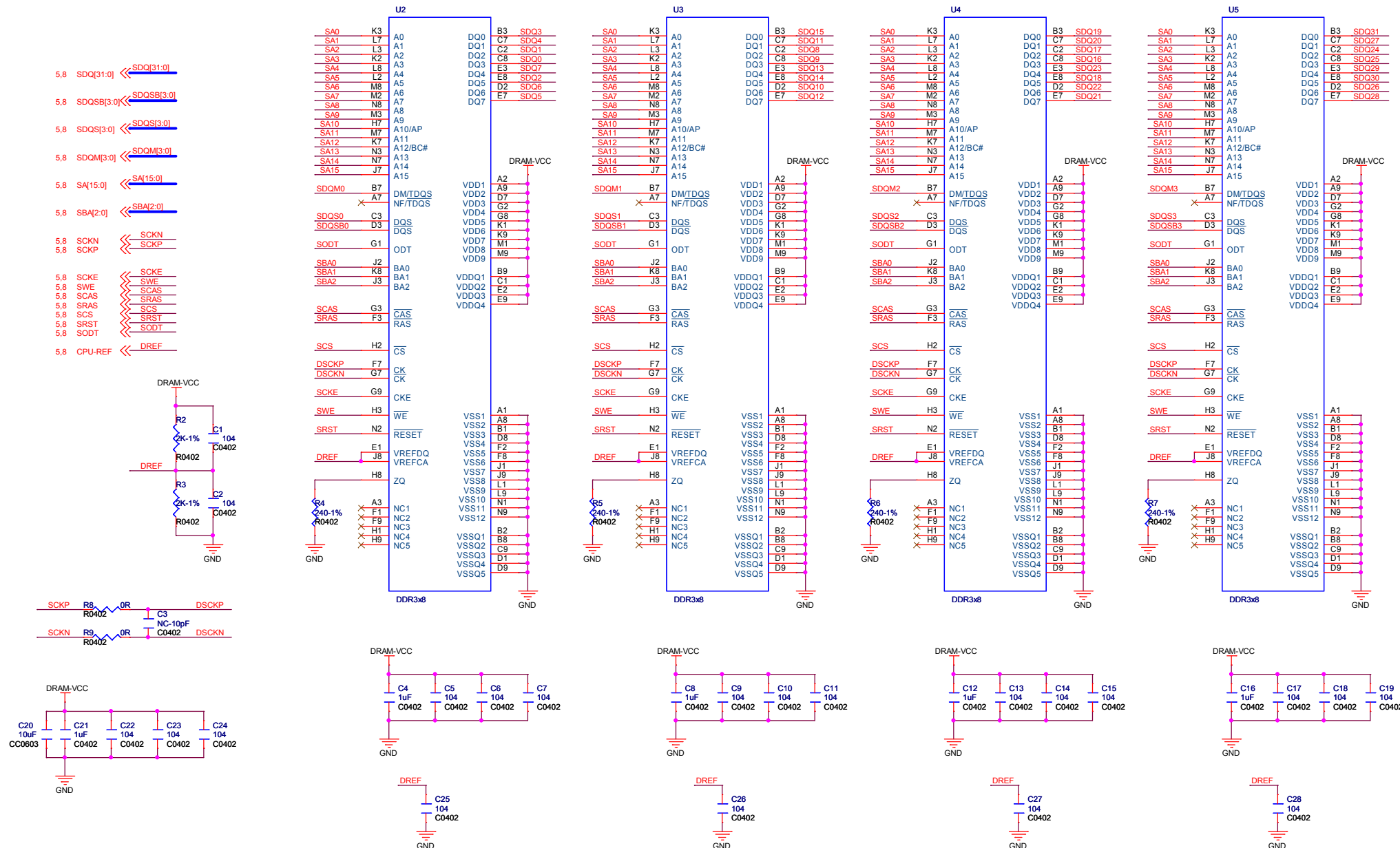
## CPU2

注意：PA剩余口全部过孔接地，用于散热。



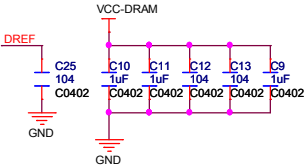
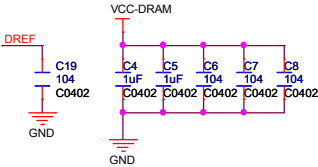
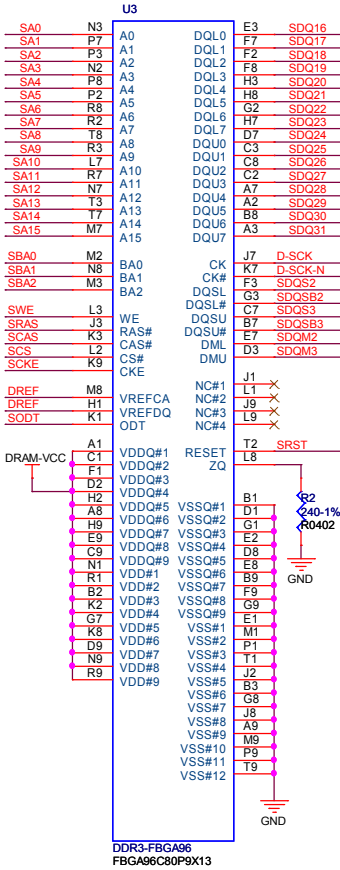
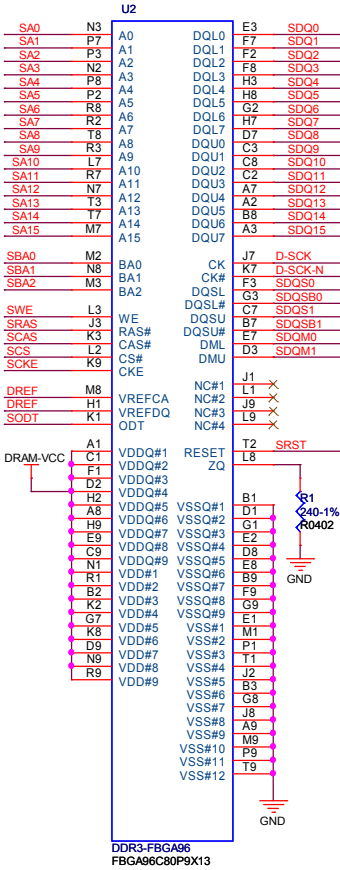
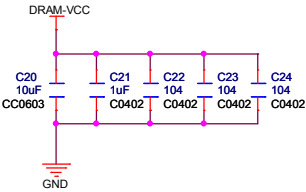
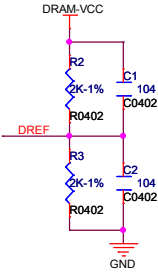
# DDR3-8BITX4

Please directly copy the referred DRAM layout and follow the PCB layout guide. This circuit is only for single-side PCB layout.



DDR3-16BITX2

- 5.7 SDQ[31:0] << SDQ[31:0]
- 5.7 SDQS[31:0] << SDQS[31:0]
- 5.7 SDQS[3:0] << SDQS[3:0]
- 5.7 SDQM[3:0] << SDQM[3:0]
- 5.7 SA[15:0] << SA[15:0]
- 5.7 SBA[2:0] << SBA[2:0]
- 5.7 SCKN <<
- 5.7 SCKP <<
- 5.7 SCKE <<
- 5.7 SWE <<
- 5.7 SCAS <<
- 5.7 SRAS <<
- 5.7 SCS <<
- 5.7 SRST <<
- 5.7 SODT <<
- 5.7 CPU-REF << DREF



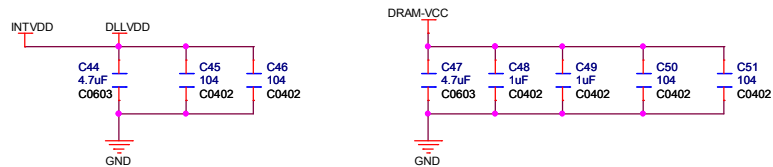
AllWinner Technology Co.,Ltd

Title			A20_PAD_STD
Size	Document Number	Rev	
A3	DDR3 16bit x 2pcs		
Date:	Monday, April 01, 2013	Sheet	8 of 20

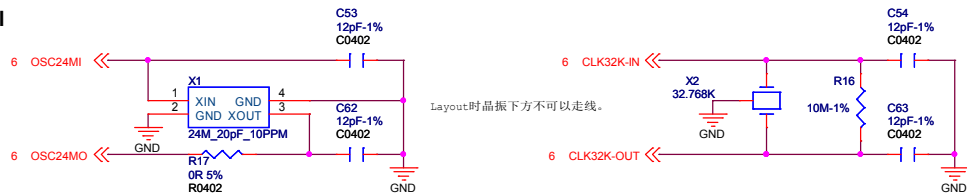


# BESIDE CPU

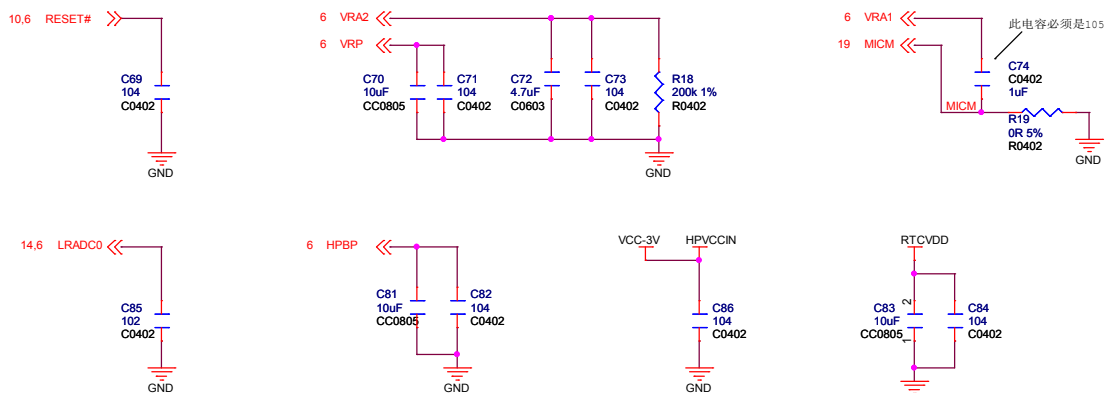
## DRAM



## Crystal



## AUDIO&SYS&TP



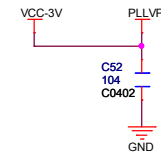
## USB



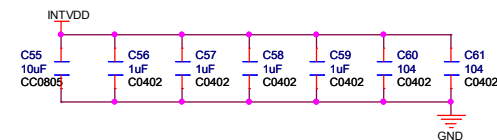
## HDMI



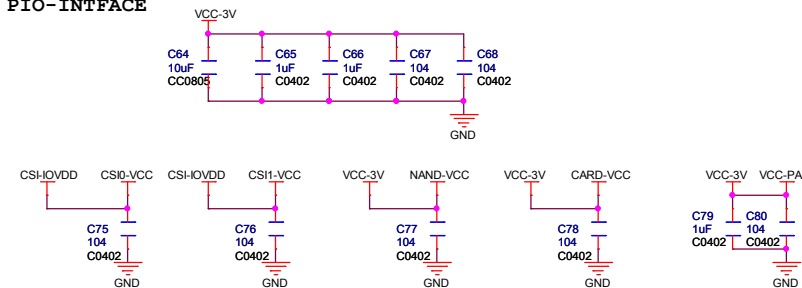
## PLL



## CORE

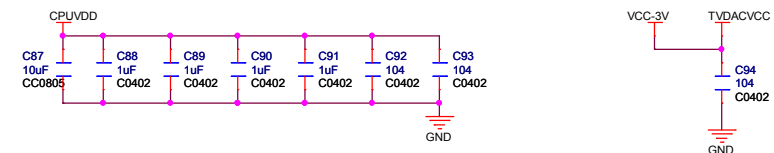


## PIO-INTERFACE

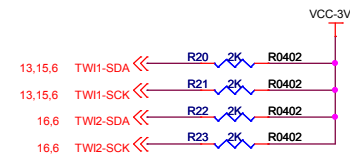


## CPU&TV

LAYOUT: 按照一个PIN, 放一个电容, 并且尽量靠近PIN摆放。



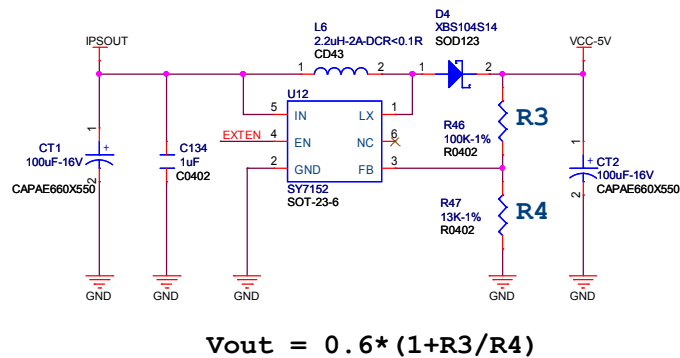
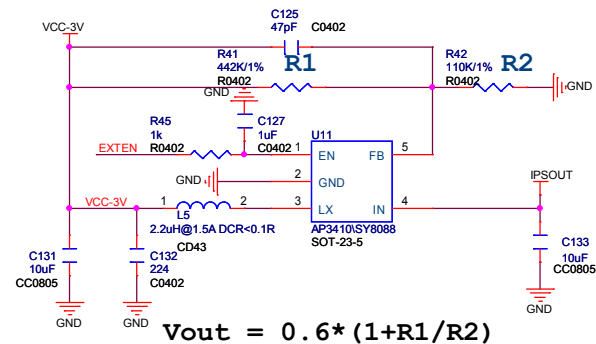
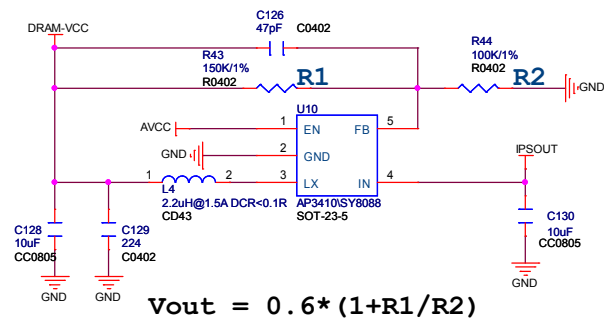
## TWI-PULLUP





# POWER-DC/DC

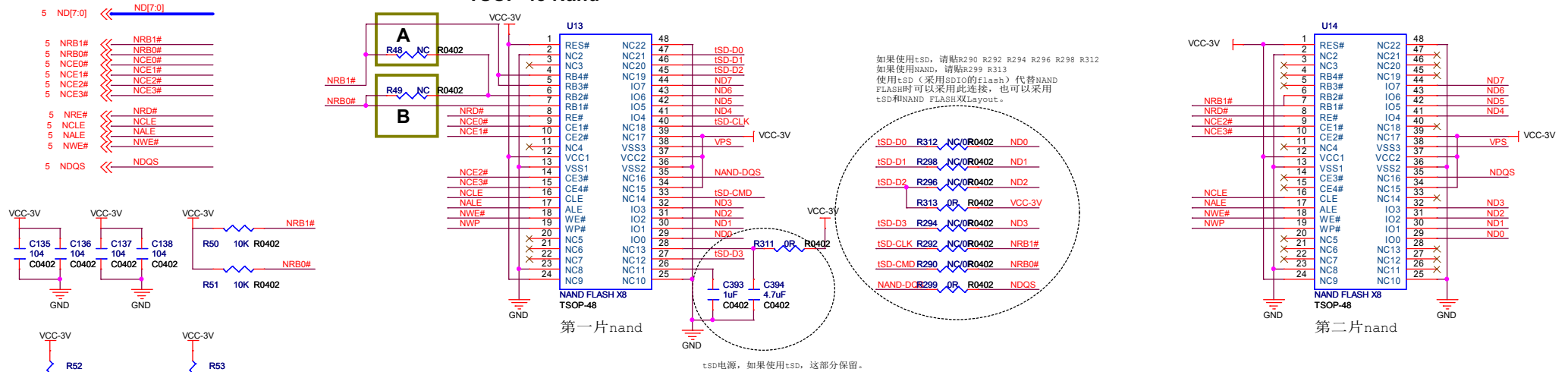
10 EXTEN >> EXTEN



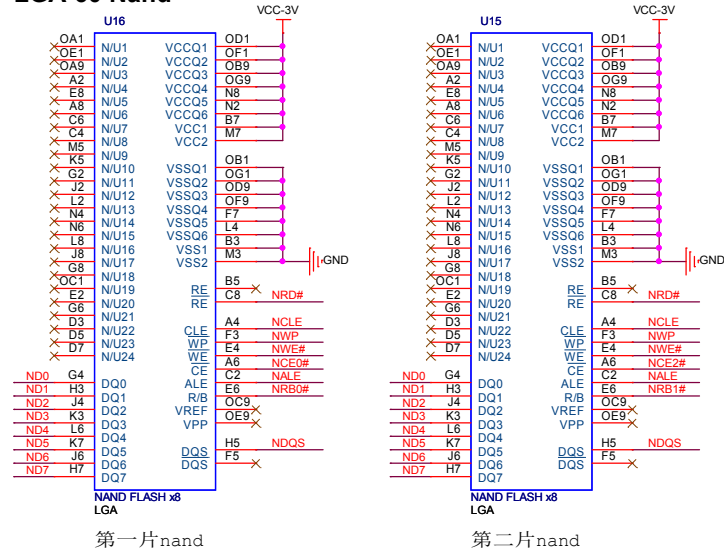
# NAND Flash

- (1) 接1片单片选Nand 时, 电阻A, B全断开
- (2) 接1片双片选Nand 时, 连接电阻A, 断开电阻B
- (3) 接1片四片选Nand 时, 连接电阻B, 断开电阻A
- (4) 接2片单片选或接2片双片选Nand 时, 连接电阻A, 断开电阻B

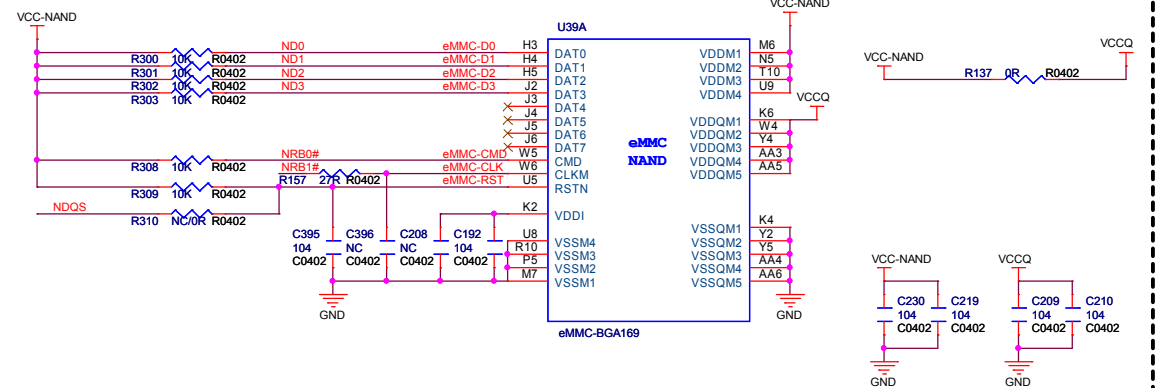
## TSOP-48 Nand



## LGA-60 Nand

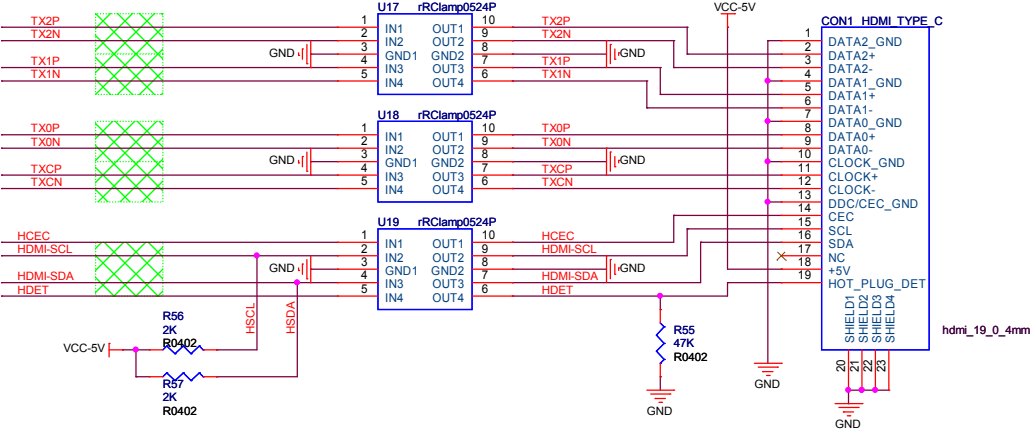
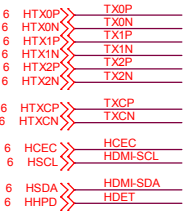


## eMMC FLASH

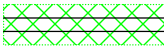


# HDMI-CSI

## HDMI



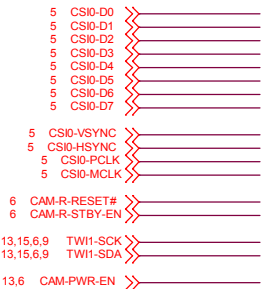
Differential pairs  
Z0= 100 ohm



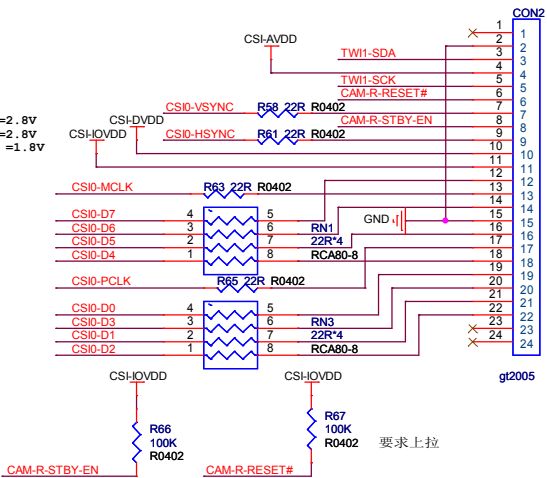
LAYOUT差分走线过孔不能超过2个，有完整铺地。

## CSI0-BACK

200W-后置高分辨率

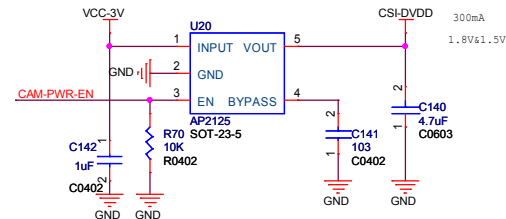
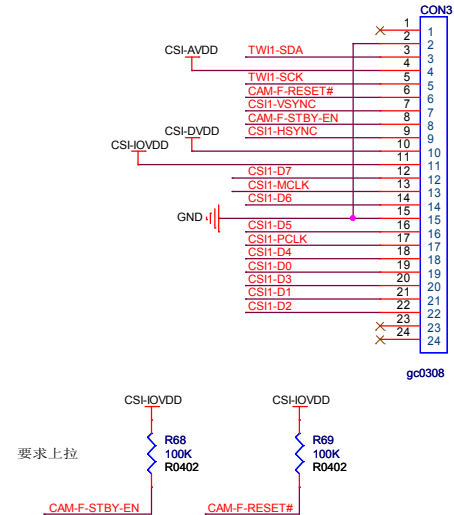
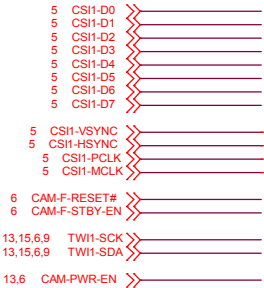


CSI-IOVDD =2.8V  
CSI-AVDD =2.8V  
CSI-DVDD =1.8V



## CSI1-FRONT

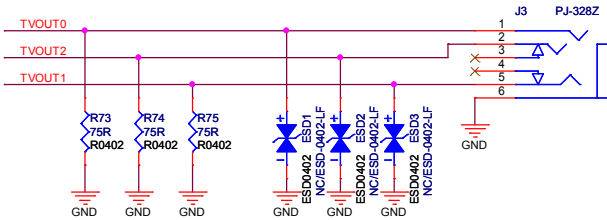
30W-前置低分辨率



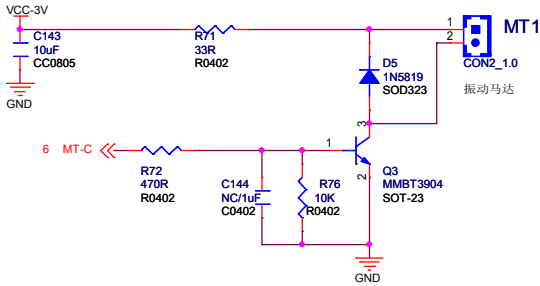
- 1、LAYOUT时，请保证摄像头成像方向与LCD显示一致；
- 2、LAYOUT时，请尽量保证两个摄像头的连接器不要分开太远，保证电源以及信号到达CSI的一致性；
- 3、若选用其他模组，请检查CSI-IOVDD, CSI-AVDD, CSI-DVDD的具体电压值以及负载能力能够满足。

KEY-IR-TVOUT-MT

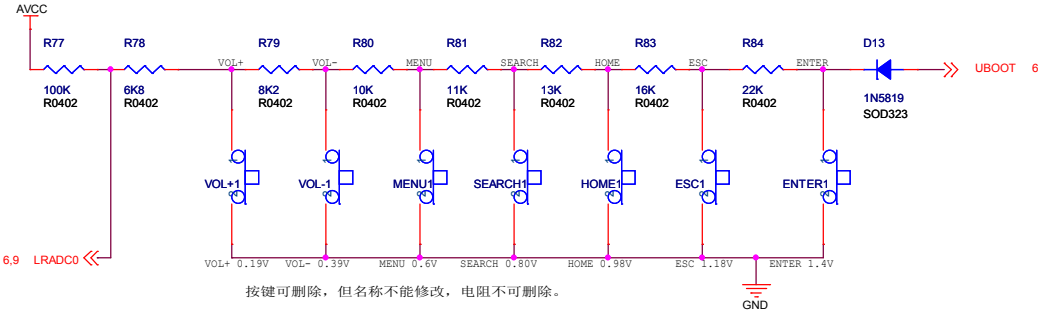
TVOUT



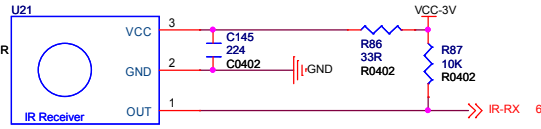
Motor



KEY

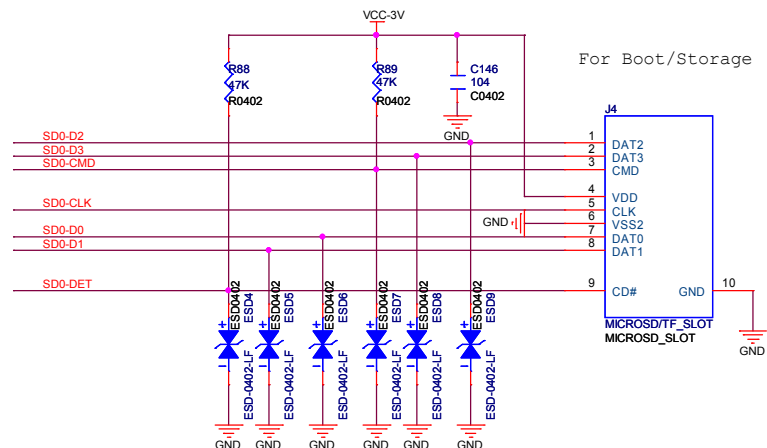


IR MODULE

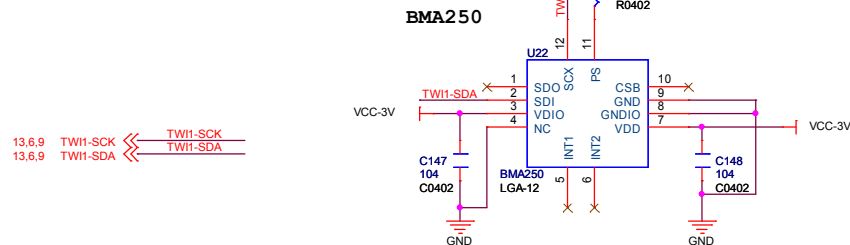


# CARD-DEBUG-GS

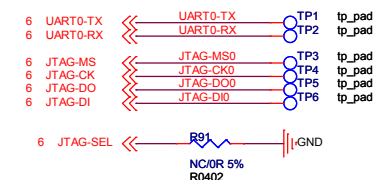
## CARD0



## G-SENSOR



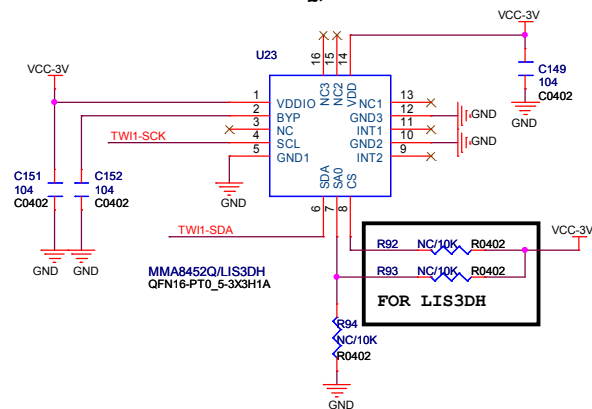
## DEBUG



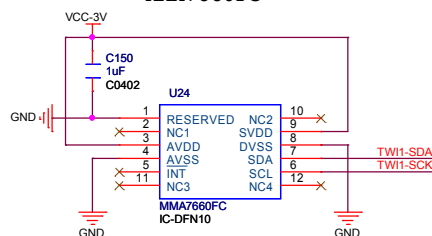
预留JTAG、UART测试点，并要保证测试点方便焊接排列整齐，以备调试使用。

## Option

### MMA8452Q/LIS3DH



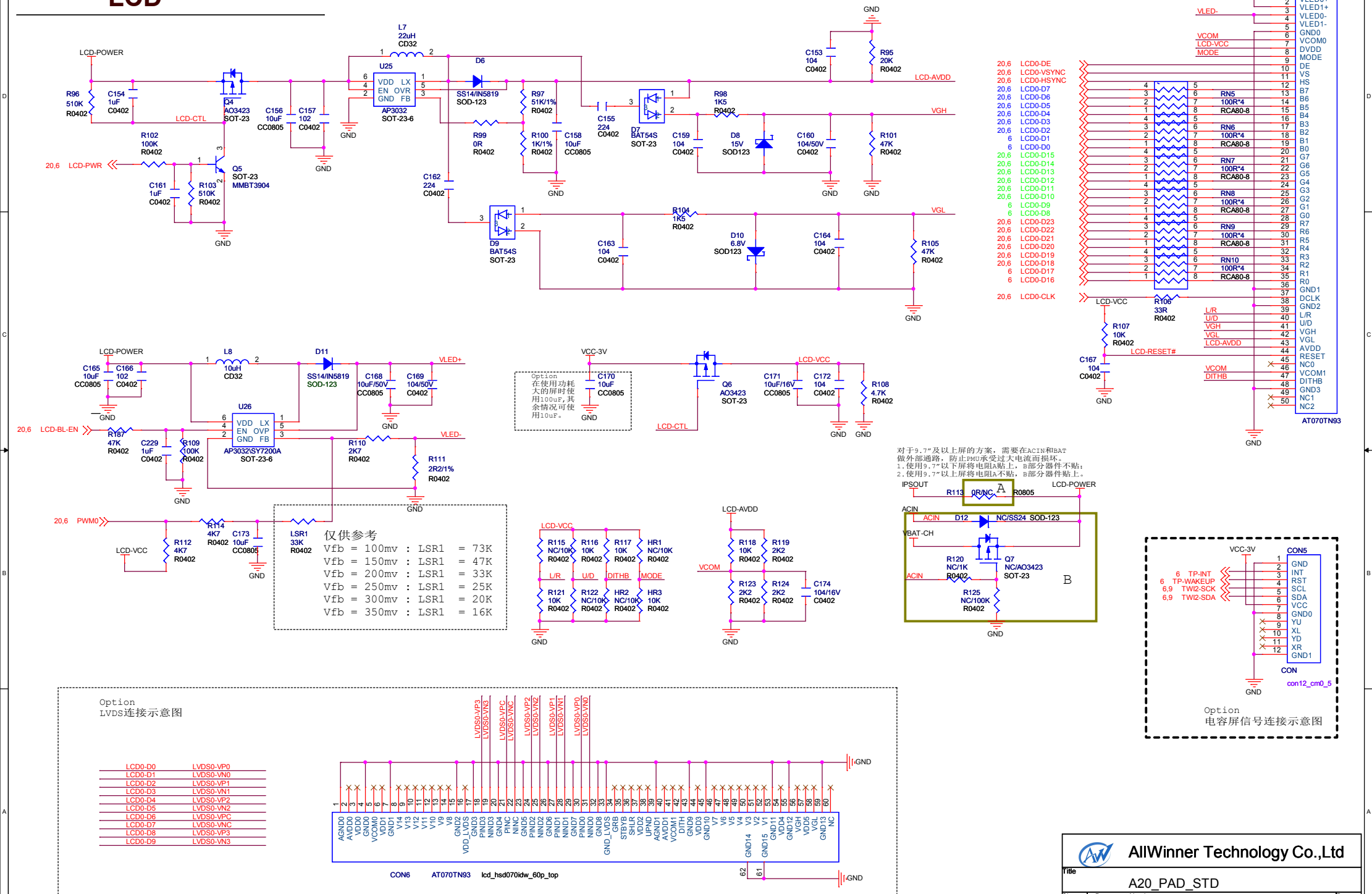
### MMA7660FC



AllWinner Technology Co.,Ltd

Title			A20_PAD_STD
Size	Document Number	Rev	
A3	CARD-DEBUG-GS		
Date:	Monday, April 01, 2013	Sheet	15 of 20

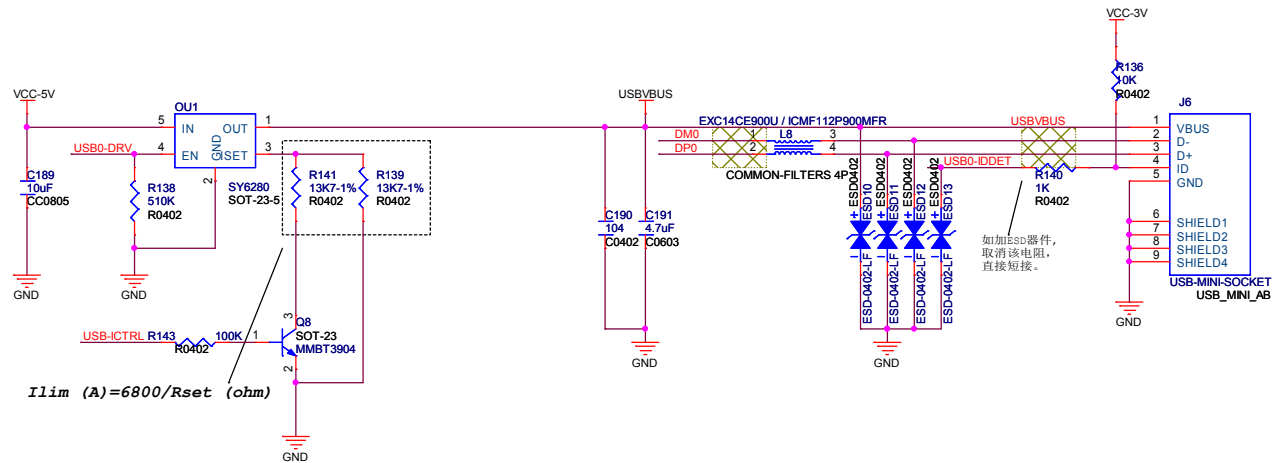
## LCD





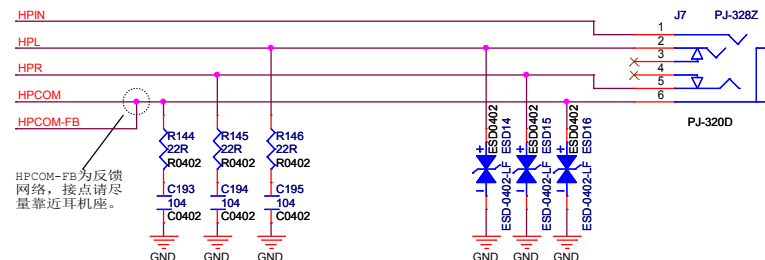


6	DM0	DM0
6	DP0	DP0
6	USB0-IDDET	USB0-IDDET
10,6	USB0-DRV	USB0-DRV
10	USBVBUS	USBVBUS
6	USB-ICTRL	USB-ICTRL

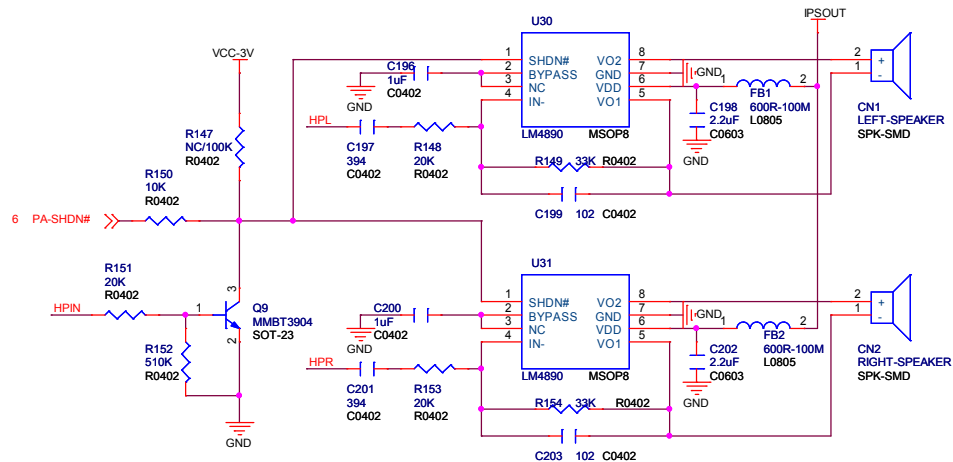


# HP-MIC-SPK

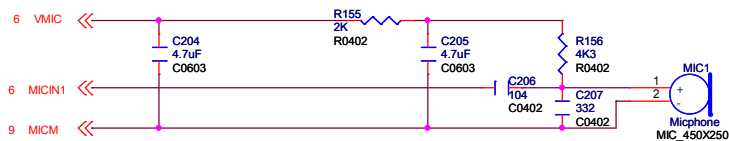
## Head Phone



## Speaker



## Microphone



AllWinner Technology Co.,Ltd

Title A20\_PAD\_STD

Size A3 Document Number HP-MIC-SPK

Date: Monday, April 01, 2013

Sheet 19 of 20

## LCD MIPI

