Ayudantía UART

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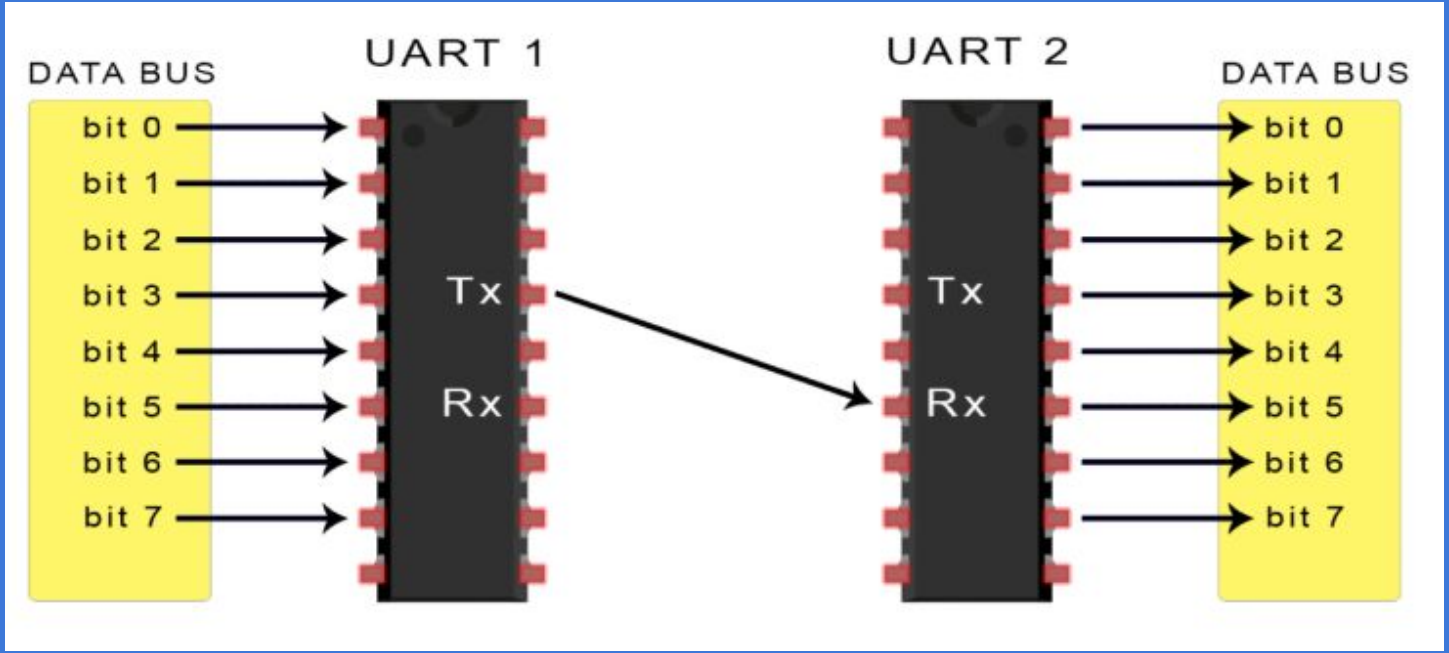
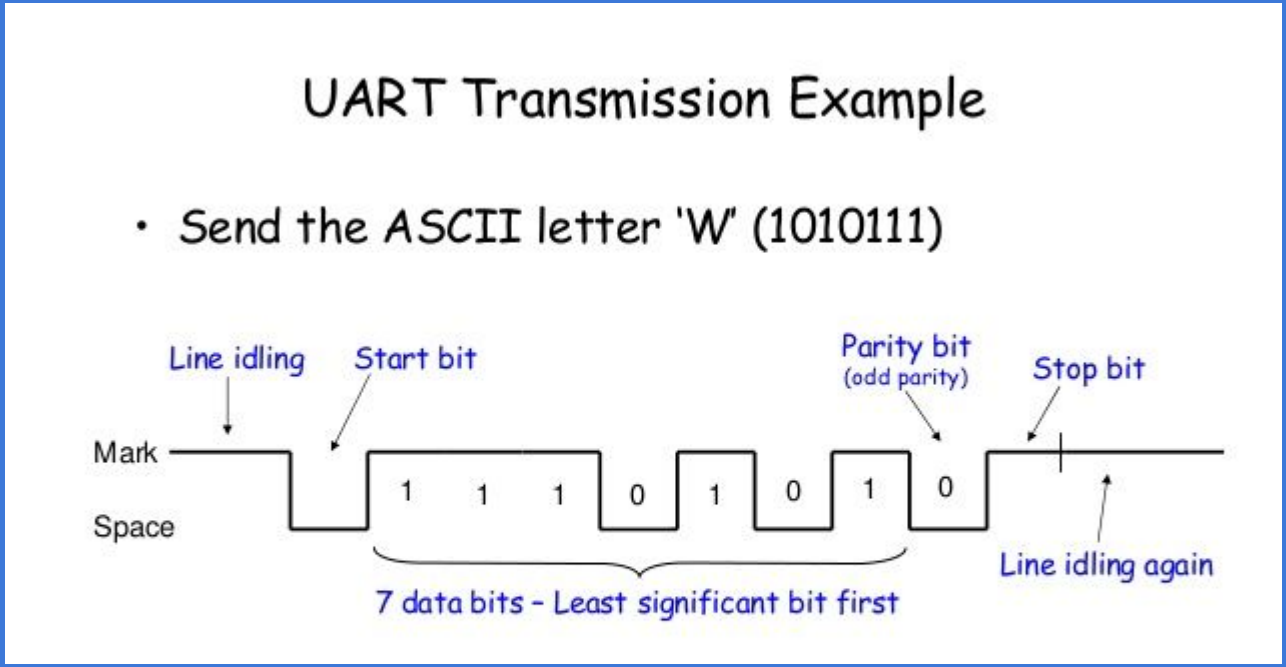
Funcionamiento de Protocolo



Fuente: www. circuitbasics.com

Estructura de Protocolo

Packet:
-Start bit: Es un 0 lógico. Cuando no hay comunicación la línea de transmisión se encuentra en 1 lógico.
-Data frame: 5 a 8 bits.
-Parity bit: para detectar errores.
-Stop bit: puede ser 1 o 2 bits.



Fuente: BYU Electrical and Computer Engineering

Registros MSP430

Selección modo puertos Rx y Tx:

12.4.14 PxSEL Register

Port x Port Select Register

Figure 12-14. PxSEL Register

7	6	5	4	3	2	1	0
PxSEL							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 12-16. PxSEL Register Description

Bit	Field	Type	Reset	Description
7-0	PxSEL	RW	0h	Port x function selection 0b = I/O function is selected 1b = Peripheral module function is selected

P4.4/PM_UCA1TXD/ PM_UCA1SIMO	51	45	H3	D7	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Transmit data – USCI_A1 UART mode Default mapping: Slave in, master out – USCI_A1 SPI mode
P4.5/PM_UCA1RXD/ PM_UCA1SOMI	52	46	G3	C9	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Receive data – USCI_A1 UART mode Default mapping: Slave out, master in – USCI_A1 SPI mode

Registros MSP430

Selección de baud rate:

Description
USCI clock source select. These bits select the BRCLK s 00b = UCAxCLK (external USCI clock) 01b = ACLK 10b = SMCLK 11b = SMCLK

Frecuencia de clocks:
ACLK: 01b (UCSSEL_1): 32 768 Hz
SMCLK: 10b (UCSSEL_2): 1 048 576 Hz

Table 36-4. Commonly Used Baud Rates, Settings, and Errors, UCOS16 = 0

BRCLK Frequency (Hz)	Baud Rate (baud)	UCBRx	UCBRSx	UCBRFx	Maximum TX Error (%)		Maximum RX Error (%)	
32 768	1200	27	2	0	-2.8	1.4	-5.9	2.0
32 768	2400	13	6	0	-4.8	6.0	-9.7	8.3
32 768	4800	6	7	0	-12.1	5.7	-13.4	19.0
32 768	9600	3	3	0	-21.1	15.2	-44.3	21.3
1 000 000	9600	104	1	0	-0.5	0.6	-0.9	1.2
1 000 000	19200	52	0	0	-1.8	0	-2.6	0.9
1 000 000	38400	26	0	0	-1.8	0	-3.6	1.8
1 000 000	57600	17	3	0	-2.1	4.8	-6.8	5.8
1 000 000	115200	8	6	0	-7.8	6.4	-9.7	16.1
1 048 576	9600	109	2	0	-0.2	0.7	-1.0	0.8
1 048 576	19200	54	5	0	-1.1	1.0	-1.5	2.5
1 048 576	38400	27	2	0	-2.8	1.4	-5.9	2.0
1 048 576	57600	18	1	0	-4.6	3.3	-6.8	6.6
1 048 576	115200	9	1	0	-1.1	10.7	-11.5	11.3
4 000 000	9600	416	6	0	-0.2	0.2	-0.2	0.4
4 000 000	19200	208	3	0	-0.2	0.5	-0.3	0.8
4 000 000	38400	104	1	0	-0.5	0.6	-0.9	1.2
4 000 000	57600	69	4	0	-0.6	0.8	-1.8	1.1
4 000 000	115200	34	6	0	-2.1	0.6	-2.5	3.1
4 000 000	230400	17	3	0	-2.1	4.8	-6.8	5.8
4 194 304	9600	436	7	0	-0.3	0	-0.3	0.2

Registros MSP430

Selección de baud rate:

36.4.3 UCAxBR0 Register

USCI_Ax Baud Rate Control Register 0

Figure 36-14. UCAxBR0 Register

7	6	5	4	3	2	1	0
UCBRx							
rw	rw	rw	rw	rw	rw	rw	rw

Can be modified only when UCSWRST = 1.

Table 36-9. UCAxBR0 Register Description

Bit	Field	Type	Reset	Description
7-0	UCBRx	RW	undefined	Low byte of clock prescaler setting of the baud-rate generator. The 16-bit value of (UCAxBR0 + UCAxBR1 × 256) forms the prescaler value UCBRx.

36.4.4 UCAxBR1 Register

USCI_Ax Baud Rate Control Register 1

Figure 36-15. UCAxBR1 Register

7	6	5	4	3	2	1	0
UCBRx							
rw	rw	rw	rw	rw	rw	rw	rw

Can be modified only when UCSWRST = 1.

Table 36-10. UCAxBR1 Register Description

Bit	Field	Type	Reset	Description
7-0	UCBRx	RW	undefined	High byte of clock prescaler setting of the baud-rate generator. The 16-bit value of (UCAxBR0 + UCAxBR1 × 256) forms the prescaler value UCBRx.

36.4.5 UCAxMCTL Register

USCI_Ax Modulation Control Register

Figure 36-16. UCAxMCTL Register

7	6	5	4	3	2	1	0
UCBRFx				UCBRSx			UCOS16
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Can be modified only when UCSWRST = 1.

Registros MSP430

Configuración Packet:

36.4.1 UCAxCTL0 Register

USCI_Ax Control Register 0

Figure 36-12. UCAxCTL0 Register

7	6	5	4	3	2	1	0
UCPEN	UCPAR	UCMSB	UC7BIT	UCSPB	UCMODEx		UCSYNC
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Can be modified only when UCSWRST = 1.

-bit 0: Synchronous mode enable. Por defecto en modo Asíncrono.

-bit 3: Stop bit select

-bit 4: Character length. 7 u 8 bits de largo

-bit 6: Parity select

-bit 7: Parity enable

Registros MSP430

Configuración Packet:

36.4.2 UCAxCTL1 Register

USCI_Ax Control Register 1

Figure 36-13. UCAxCTL1 Register

7	6	5	4	3	2	1	0
UCSSELx		UCRXEIE	UCBRKIE	UCDORM	UCTXADDR	UCTXBRK	UCSWRST
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-1

Can be modified only when UCSWRST = 1.

-bit 0: Software reset enable. Para configurar el módulo UART, este bit debe estar en 1 lógico

-bit 6 & 7: USCI clock source select. Para configurar el clock

Description
USCI clock source select. These bits select the BRCLK s 00b = UCAxCLK (external USCI clock) 01b = ACLK 10b = SMCLK 11b = SMCLK

Frecuencia de clocks:
ACLK: 32 768 Hz
SMCLK: 1 048 576 Hz

Registros MSP430

Registro de señalización y estado:

36.4.13 UCAxIFG Register

USCI_Ax Interrupt Flag Register

Figure 36-24. UCAxIFG Register

7	6	5	4	3	2	1	0
Reserved						UCTXIFG	UCRXIFG
r-0	r-0	r-0	r-0	r-0	r-0	rw-1	rw-0

Table 36-19. UCAxIFG Register Description

Bit	Field	Type	Reset	Description
7-2	Reserved	R	0h	Reserved. Always reads as 0.
1	UCTXIFG	RW	1h	Transmit interrupt flag. UCTXIFG is set when UCAxTXBUF empty. 0b = No interrupt pending 1b = Interrupt pending
0	UCRXIFG	RW	0h	Receive interrupt flag. UCRXIFG is set when UCAxRXBUF has received a complete character. 0b = No interrupt pending 1b = Interrupt pending

-bit 0: UCRXIFG: Receive interrupt flag. Cuando se recibe un carácter, el bit toma el valor de 1 lógico.

-bit 1: UCTXIFG: Transmit interrupt flag. Cuando el buffer está vacío, el bit toma el valor de 1 lógico.

Registros MSP430

Buffer de datos:

Para transmisión: entregamos el dato que queremos transmitir al registro UCAxTXBUF.

Para recepción: leemos el dato que se encuentra en el registro UCAxRXBUF.

A diferencia de la ATmega328P, la MSP430 posee dos registros buffer, uno para transmisión y otro para recepción de datos.

36.4.7 UCAxRXBUF Register

USCI_Ax Receive Buffer Register

Figure 36-18. UCAxRXBUF Register

7	6	5	4	3	2	1	0
UCRXBUFx							
r	r	r	r	r	r	r	r

Table 36-13. UCAxRXBUF Register Description

Bit	Field	Type	Reset	Description
7-0	UCRXBUFx	R	undefined	The receive-data buffer is user accessible and contains the last received character from the receive shift register. Reading UCAxRXBUF resets the receive-error bits, the UCADDR or UCIDLE bit, and UCRXIFG. In 7-bit data mode, UCAxRXBUF is LSB justified and the MSB is always reset.

36.4.8 UCAxTXBUF Register

USCI_Ax Transmit Buffer Register

Figure 36-19. UCAxTXBUF Register

7	6	5	4	3	2	1	0
UCTXBUFx							
rw	rw	rw	rw	rw	rw	rw	rw

Table 36-14. UCAxTXBUF Register Description

Bit	Field	Type	Reset	Description
7-0	UCTXBUFx	RW	undefined	The transmit data buffer is user accessible and holds the data waiting to be moved into the transmit shift register and transmitted on UCAxTXD. Writing to the transmit data buffer clears UCTXIFG. The MSB of UCAxTXBUF is not used for 7-bit data and is reset.

Registros MSP430

Para trabajar con interrupciones:

36.4.12 UCAxIE Register

USCI_Ax Interrupt Enable Register

Figure 36-23. UCAxIE Register

7	6	5	4	3	2	1	0
Reserved						UCTXIE	UCRXIE
r-0	r-0	r-0	r-0	r-0	r-0	rw-0	rw-0

Table 36-18. UCAxIE Register Description

Bit	Field	Type	Reset	Description
7-2	Reserved	R	0h	Reserved. Always reads as 0.
1	UCTXIE	RW	0h	Transmit interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
0	UCRXIE	RW	0h	Receive interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled

*Utilizar el vector de interrupción adecuado

Presentación Código

Registros ATmega328P

Selección de baud rate:

Table 19-1. Equations for Calculating Baud Rate Register Setting

Operating Mode	Equation for Calculating Baud Rate[1]	Equation for Calculating UBRRn Value
Asynchronous normal mode (U2Xn = 0)	$BAUD = \frac{f_{OSC}}{16(UBRRn + 1)}$	$UBRRn = \frac{f_{OSC}}{16BAUD} - 1$
Asynchronous double speed mode (U2Xn = 1)	$BAUD = \frac{f_{OSC}}{8(UBRRn + 1)}$	$UBRRn = \frac{f_{OSC}}{8BAUD} - 1$
Synchronous master mode	$BAUD = \frac{f_{OSC}}{8(UBRRn + 1)}$	$UBRRn = \frac{f_{OSC}}{2BAUD} - 1$

Note: 1. The baud rate is defined to be the transfer rate in bit per second (bps)

BAUD	Baud rate (in bits per second, bps)
f_{osc}	System oscillator clock frequency
UBRRn	Contents of the UBRRnH and UBRRnL registers, (0-4095)

Registros ATmega328P

Selección de baud rate:

19.10.5 UBRRnL and UBRRnH – USART Baud Rate Registers

Bit	15	14	13	12	11	10	9	8	
	–	–	–	–	UBRRn[11:8]				UBRRnH
	UBRRn[7:0]								UBRRnL
	7	6	5	4	3	2	1	0	
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

- **Bit 15:12 – Reserved Bits**

These bits are reserved for future use. For compatibility with future devices, these bit must be written to zero when UBRRnH is written.

- **Bit 11:0 – UBRR11:0: USART Baud Rate Register**

This is a 12-bit register which contains the USART baud rate. The UBRRnH contains the four most significant bits, and the UBRRnL contains the eight least significant bits of the USART baud rate. Ongoing transmissions by the transmitter and receiver will be corrupted if the baud rate is changed. Writing UBRRnL will trigger an immediate update of the baud rate prescaler.

Registros ATmega328P

Configuración Packet:

19.10.4 UCSRnC – USART Control and Status Register n C

Bit	7	6	5	4	3	2	1	0	
	UMSELn1	UMSELn0	UPMn1	UPMn0	USBSn	UCSZn1	UCSZn0	UCPOLn	UCSRnC
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	1	1	0	

-bits 1 & 2: Character Size (Data frame)

-bit 3: Stop Bit Select

-bits 4 & 5: Parity Mode

-bits 6 & 7: USART Mode Select. Por defecto configuración en modo asíncrono

Registros ATmega328P

Inicio comunicación:

19.10.3 UCSRnB – USART Control and Status Register n B

Bit	7	6	5	4	3	2	1	0	
	RXCIEn	TXCIEn	UDRIEn	RXENn	TXENn	UCSZn2	RXB8n	TXB8n	UCSRnB
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	
Initial Value	0	0	0	0	0	0	0	0	

-bit 3: TXENn: Transmitter Enable n
Configurando este bit en 1 lógico **habilitamos la transmisión** de datos del periférico UART.

-bit 4: RXENn: Receiver Enable n
Configurando este bit en 1 lógico **habitamos la recepción** de datos del periférico UART.

Registros ATmega328P

Registro de señalización y estado:

19.10.2 UCSRnA – USART Control and Status Register n A

Bit	7	6	5	4	3	2	1	0	
	RXCn	TXCn	UDREn	FEn	DORn	UPEn	U2Xn	MPCMn	UCSRnA
Read/Write	R	R/W	R	R	R	R	R/W	R/W	
Initial Value	0	0	1	0	0	0	0	0	

-bit 7: Flag que indica que la la recepción ha terminado.

-bit 6: Flag que indica que la la transmisión ha terminado.

-bit 5: Flag que indica que el registro UDRn está desocupado y disponible.

Registros ATmega328P

Buffer de datos:

19.10.1 UDRn – USART I/O Data Register n

Bit	7	6	5	4	3	2	1	0	
	RXB[7:0]								UDRn (Read)
	TXB[7:0]								UDRn (Write)
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

The USART transmit data buffer register and USART receive data buffer registers ***share the same I/O address referred to as USART data register or UDRn.*** *The transmit data buffer register (TXB) will be the destination for data written to the UDRn register location. Reading the UDRn register location will return the contents of the receive data buffer register (RXB).*

Para transmisión: entregamos el dato que queremos transmitir a este registro.
Para recepción: leemos el dato que se encuentra en este registro.

Registros ATmega328P

Para trabajar con interrupciones:

19.10.3 UCSRnB – USART Control and Status Register n B

Bit	7	6	5	4	3	2	1	0	
	RXCIEn	TXCIEn	UDRIEn	RXENn	TXENn	UCSZn2	RXB8n	TXB8n	UCSRnB
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	
Initial Value	0	0	0	0	0	0	0	0	

En el mismo registro B mostrado anteriormente para habilitar transmisión y recepción encontramos los bits que habilitan las interrupciones de UART. Estos son:

-bit 5: UDRIEn. *Writing this bit to one enables interrupt on the UDREn flag.*

-bit 6: TXCIEn. *Writing this bit to one enables interrupt on the TXCn flag.*

-bit 7: RXCIEn. *Writing this bit to one enables interrupt on the RXCn flag.*

Presentación Código