**Laboratory Grade**

Lab demonstration grade: \_\_\_\_\_\_\_ of 100

Lab report grade: \_\_\_\_\_\_\_ of 100

Student comments:

Grader comments:

**Astable and Monostable Multivibators Using the 555 Timer**

1. Introduction

This lab experiment will explore the procedures for designing a monostable and astable multivibrators. The 555 timer IC will be used to create these multivibrators [1]. The 555 timer is an IC that can be used to make quick output signal pulse with just two resistors and a capacitor [4]. This device allows the output pulse to be independent of the input voltage that may be applie and its design also allows it to be stable over different temperatures [3]. A monostable configuration on the 555 timer is a timing device that will only output a predetermined pulse signal when an input signal triggers It [3]. This is useful in order to only output a pulse signal when needed. On the other hand, an astable configuration will continuously send a pulse signal during operation [3]. These two configurations will be built and analyzed through an oscilloscope. A pulse width for the monostable configuration will be setup, and five load resistances will be connected to the output to test the output voltage and current effects from the different load resistances. Next, a frequency and duty cycle will be set for the astable configuration. The same five load resistances will be connected the output and the output voltage and current will be tested as well. Finally, the oscilloscope will be used to measure the magnitude of the Fourier components of the circuit.

1. Theory

Two resistors, R1 and R2, and a capacitor in series are the only components that are needed to configure the 555 timer in stable mode. The on time of the output is pulse is given by equation 1:

|  |  |
| --- | --- |
|  | (1) |

The off time of the output pulse is given by equation 2:

|  |  |
| --- | --- |
|  | (2) |

Because the on time is decided by the same values of the off time but includes the resistor R1, the on time will always be higher than the off time. This can be seen with the duty cycle by equation 3:

|  |  |
| --- | --- |
| . | (3) |

Taking the limit as R1 reaches zero, shows that the lowest duty cycle that can be achieved from a standard 555 astable configuration is 50 percent. In order to circumvent this, a diode can be added in parallel with the second resistor. This allows the current to skip R2 and therefore R2 is not included when calculating the on time of the output. The frequency at which the output is pulsing is defined by equation 4:

|  |  |
| --- | --- |
| . | (4) |

A current is sent through R1 and R2 to the capacitor to charge. Inside the 555 timer, there are three resistors of the same value in series from Vcc to ground. The current between the first two resistors is connected to the inverting and non-inverting inputs of two op-amps. With three resistors in series and connected to the other inputs of the op-amps, this creates one op-amp that is on and the other that is off [2]. A low is fed into the input of a NOR gate which causes it to output a high voltage. The voltage is fed back into another NOR gate input along with the second op-amp that is on and outputs a high as well. This causes the second NOR gate to output a low and is fed back into the first NOR gate [2].

After the external capacitor has charged, it releases the voltage and raises the inverting input of the second op-amp [2]. This causes the second op-amp to be on instead of off. This outputs a high on the second NOR gate and causes it to loop back into the first NOR gate, essentially turning it off. This feedback into the NOR gates is the main operation behind the switching of off and on in the circuit [2]. The first NOR gate is outputted to the resistor load. The second NOR gate is connected to a MOSFET and is used to trigger the charge and discharge of the external capacitor. The voltage across the capacitor is modeled by equation 5:

|  |  |
| --- | --- |
|  | (5) |

Once the capacitor voltage reaches 2/3 of the Vcc voltage, the voltage is high enough to trigger the timer and start the capacitor discharge [3]. The capacitor discharges until it is 1/3 the voltage of Vcc and triggers the 555 timer again to start charging [3]. Setting Vc(0) = 2/3Vcc and Vc(∞) = 0, the final equation for the capacitor voltage of the external capacitor is equation 6:

|  |  |
| --- | --- |
|  | (6) |

The monostable configuration works mostly the same way but only involves one capacitor. Thus, the on time of the single pulse output is given by equation 7:

|  |  |
| --- | --- |
| . | (7) |

The output pulse is triggered by a low then high pulse in the trigger input [4]. This pulse must be shorter than the time it takes for the capacitor to charge or the trigger will continually trigger the output pulse. This is because once the capacitor is charged to 2/3Vcc, the high pulse of the output is set low [2]. One thing to watch is the trigger voltage must get higher than 1/3Vcc or the voltage will not be higher enough to trigger the 555 monostable timer [2].

1. Experimental

The astable configuration will be the first circuit to be discussed. The astable configuration with the internals of the 555 timer can be seen in Fig. 1:

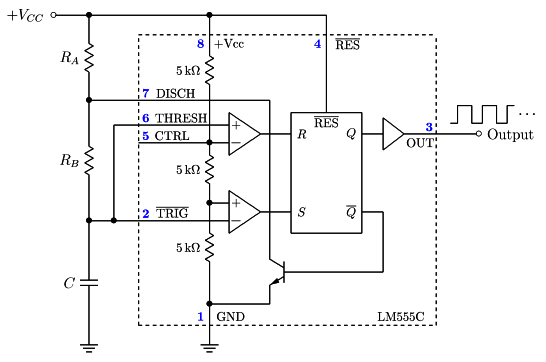


Fig. 1 The circuit for an astable 555 timer circuit.

Output pin five of the 555 timer was connected to a capacitor of 10nF then connected to ground. The frequency and duty cycle given in lab to configure the astable circuit was 2.53 kHz and 88.5% respectively. This came out for the two external resistors, Ra = 1000 Ω and Rb = 150 Ω. A 1k Ω resistor is standard and in order to get the 150 Ω, a 100 Ω and two 100 Ω resistors in parallel were used. The external capacitance value needed was 0.47 µF. This came out to be a frequency and duty cycle of 2.36 kHz and 88.46% respectively. According to the datasheet, the maximum output current is 100mA. The output voltage over five different resistance values was measured. After which, the magnitude of the Fourier components of the astable circuit was measured. This was measured with three different duty cycle to how the duty effects the Fourier output. Lastly, a duty cycle as a function of the resistor value Rb was plotted.

Next, the monostable configuration of the 555 timer was built. This configuration can be seen in Fig. 2:

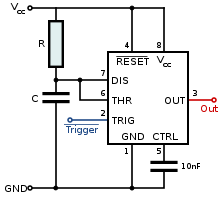


Fig. 2 The configuration for a monostable 555 timer circuit.

The pulse input signal used was a square wave at a duty cycle of about 88% and at a frequency of 234 Hz. This ensures the low pulse is shorter than the capacitor charging time but the high time pulse is longer than the capacitor charging time. The on time given in lab was 3.30 ms. This came out to be a resistor R value of 300k Ω and a capacitor value C = 10nF. The output voltage was measured over five resistance loads as well. The five resistor values chosen for the load were 100 Ω, 1k Ω, 10k Ω, 100k Ω, and 1M Ω resistors.

1. Results

Simulations for the monostable and astable 555 timer configurations can be seen in Fig. 3 and Fig. 4. The top of Fig. 3 is the input trigger pin of the 555 timer. As can be seen, the low time pulse is shorter than the capacitor charging (graph in the middle of Fig. 3). The high voltage time is also longer than the charge time of the capacitor. In the third graph at the bottom of Fig. 3, the output pin three can be seen. The high voltage time starts when the capacitor starts charging and goes low when the capacitor discharges. The trigger of the output pulse is caused by the quick low then high voltage time of the trigger pin.

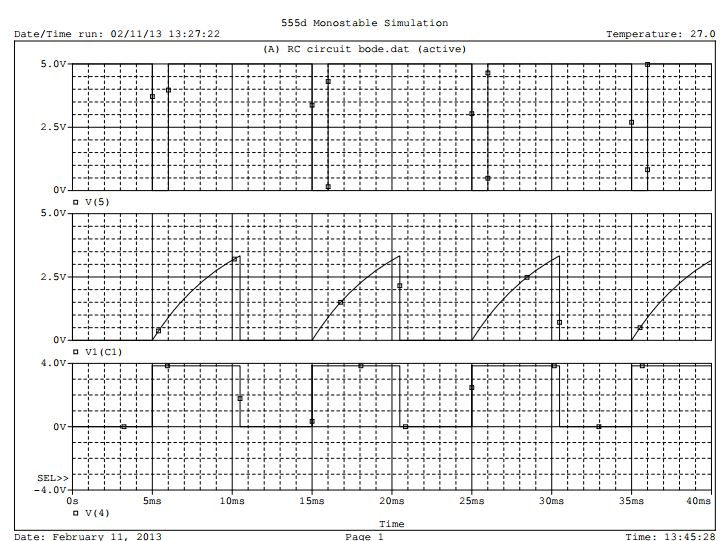


Fig. 3 Monostable 555 timer simulation.

The value of the resistor for the monostable 555 timer circuit is 500k Ω and the capacitor value is 10nF. This makes the high voltage time of the output at 5.49 ms.

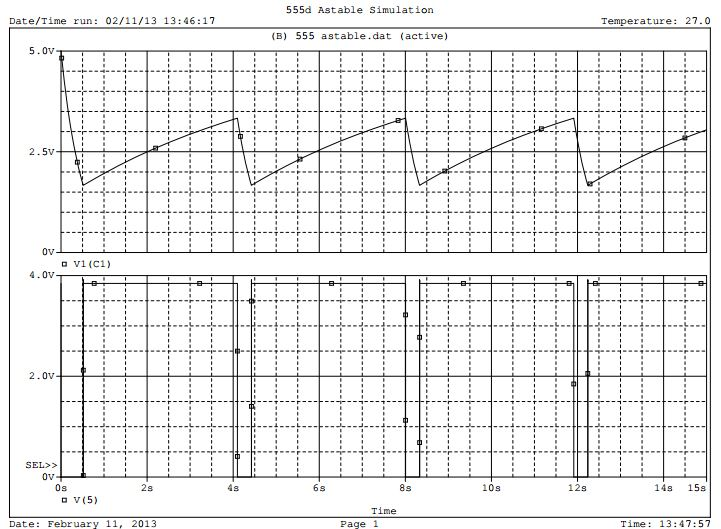


Fig. 4 Astable 555 timer simulation.

The astable configuration output and capacitor voltage is in Fig. 4. The top graph is the capacitor voltage and is alternating from 1/3Vcc to 2/3Vcc. The output, seen on the lower graph in Fig. 4, shows how the output triggers high when the capacitor starts charging and goes back low when the capacitor starts the discharge. Resistors R1 and R2 are 100k Ω and 10k Ω respectively while capacitor C equals 47 µF. This makes the high voltage time 3.29 ms and the low voltage time 0.033 ms. The frequency of the output is 0.3009 Hz.

In the lab, the astable circuit was tested first. In Fig. 5, channel 2 is the capacitor voltage and channel 1 is the output of the timer. As can be seen, just like the simulation, the output voltage goes high when the capacitor starts charging and goes low when the capacitor starts discharging. The voltage at the output with respect to ground is at 9.8v. A 0.2 drop in voltage from the 10v set at Vcc.

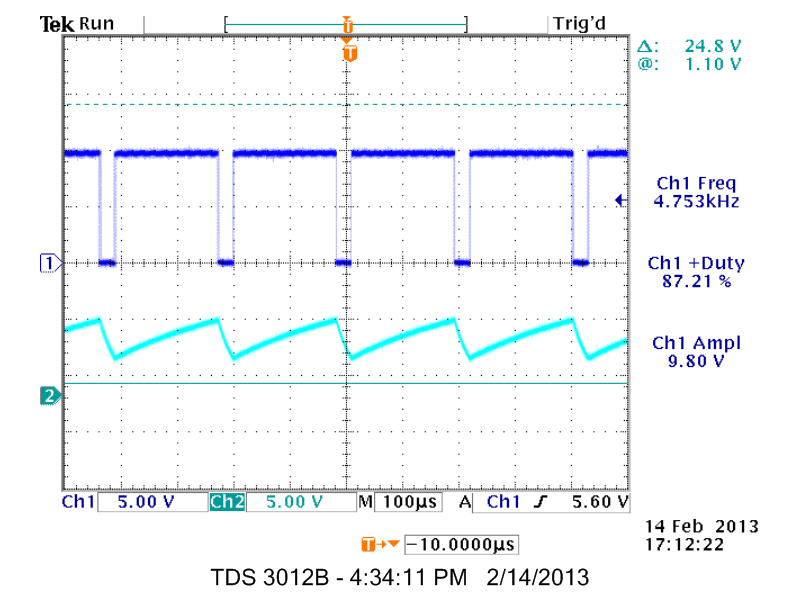


Fig. 5 Capacitor voltage bottom and 555 timer output top.

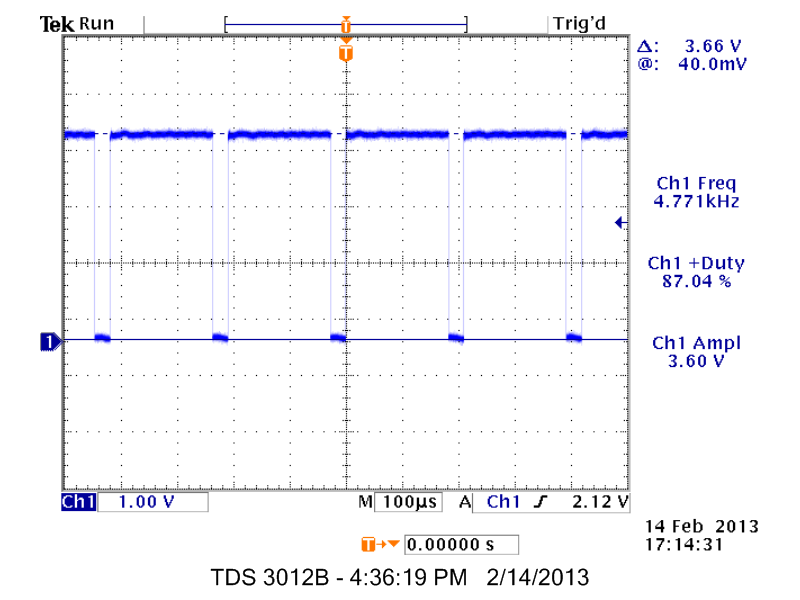


Fig. 6 Output of astable 555 time with 100 Ω load.

In Fig. 6, this is the output of the 555 timer with a load of 100 ohms. With the maximum output current of 100mA, the voltage across the resistor has dropped to 3.60v. In Fig. 7, a 1k Ω resistance was connect to the load. The voltage here can be seen to be 8.76v. This is still lower than the 9.80 voltage when there is no load. In Fig. 8, the load resistance is 10k and the voltage is at 9.60v. This is close enough to show that a resistance between 1k and 10k is needed to keep the input voltage of ten volts. In Fig. 9, the load resistance is 100k Ω and the voltage goes up slightly to 9.72v. In Fig. 10, the load resistance is set to 1M Ω, and the voltage is still at 9.72v. This shows that the highest voltage that can be obtained with a 10v input is 9.72v. The output load resistance required for minimum voltage drop is upwards of about 100k Ω. This is a high resistance needed to keep the voltage and an op-amp is recommended to boost this limitation.

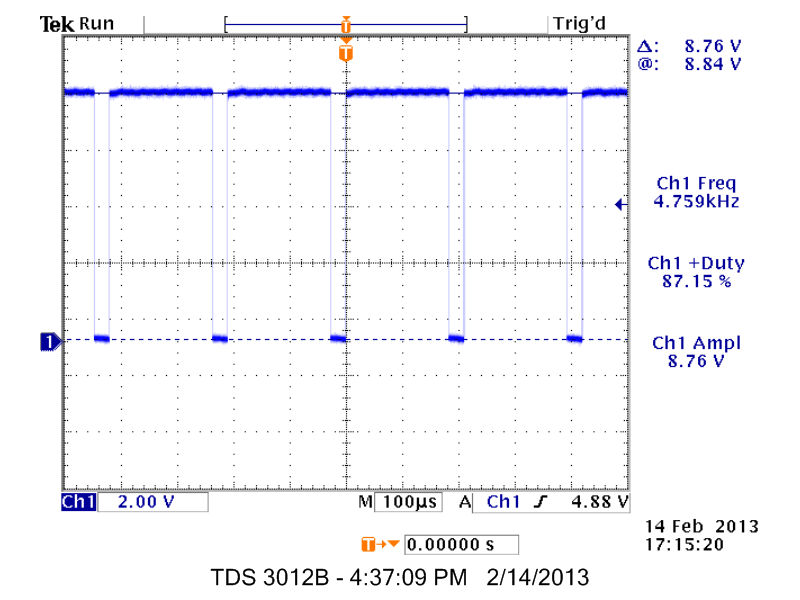


Fig. 7 Output of astable 55 timer with 1k Ω load.

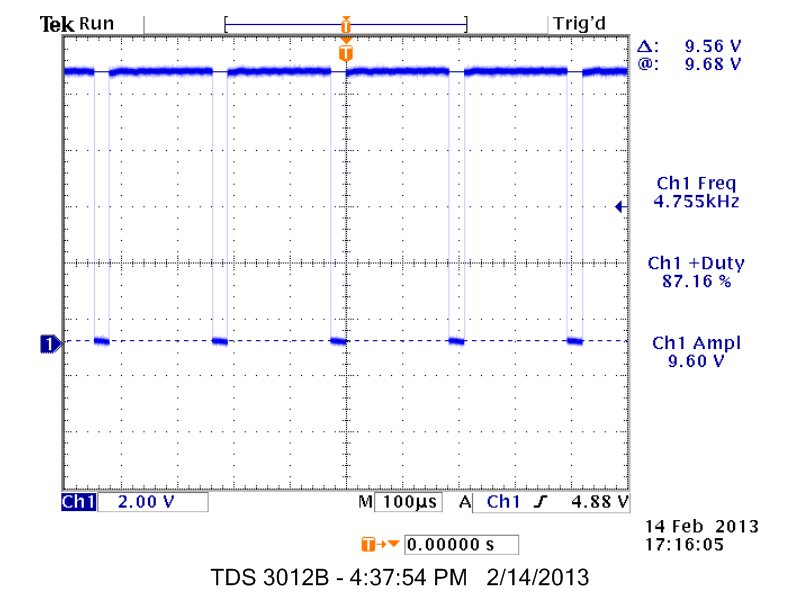


Fig. 8 Output of astable 555 timer with 10k Ω load.

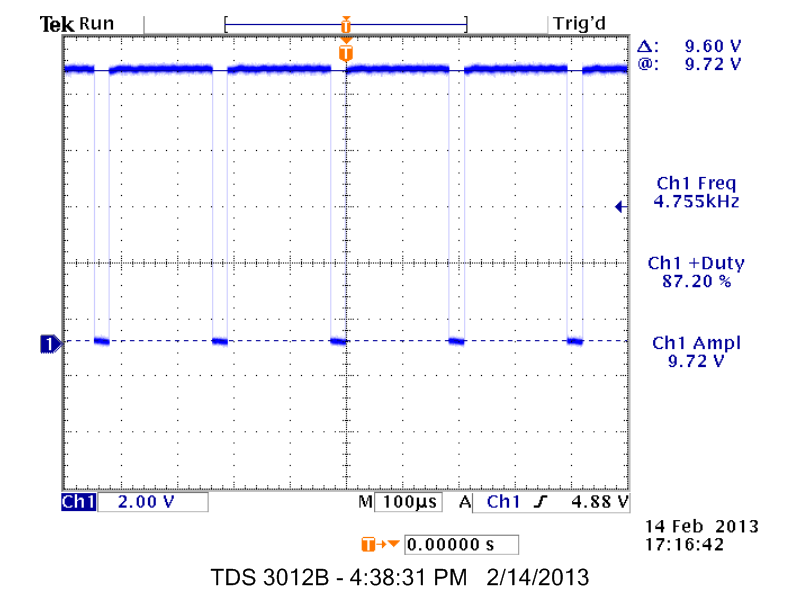


Fig. 9 Output of astable 555 timer with 100k Ω load.

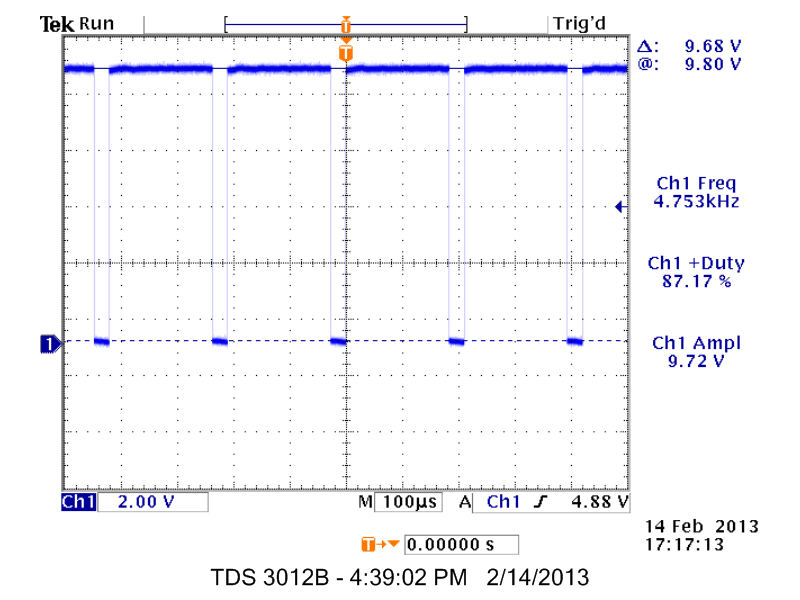


Fig. 10 Output of astable 555 timer with 1M Ω load.

Next, the monostable 555 timer configuration is built and the input trigger pulse, the capacitor voltage, and the output voltage can be seen in Fig. 11 respectively.

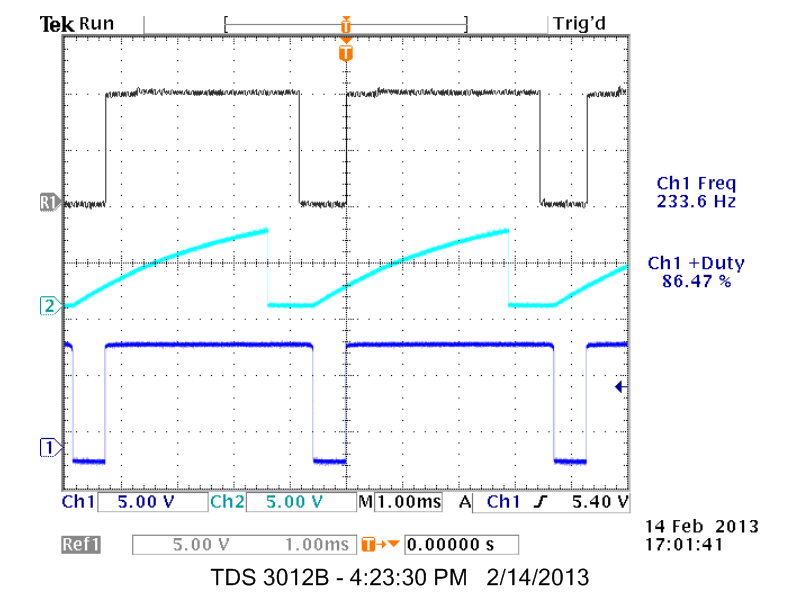


Fig. 11 Monostable 55 timer top trigger input, middle capacitor voltage, bottom, output voltage.

Five load resistances were also placed on the output of the 555 timer and the same drop in voltage can be seen at lower resistances. The voltage for a 100 ohm load is in Fig. 12 and the voltage is 3.52v. In Fig. 13, the load resistance is 1k-ohm and the output voltage is at 9.00v.

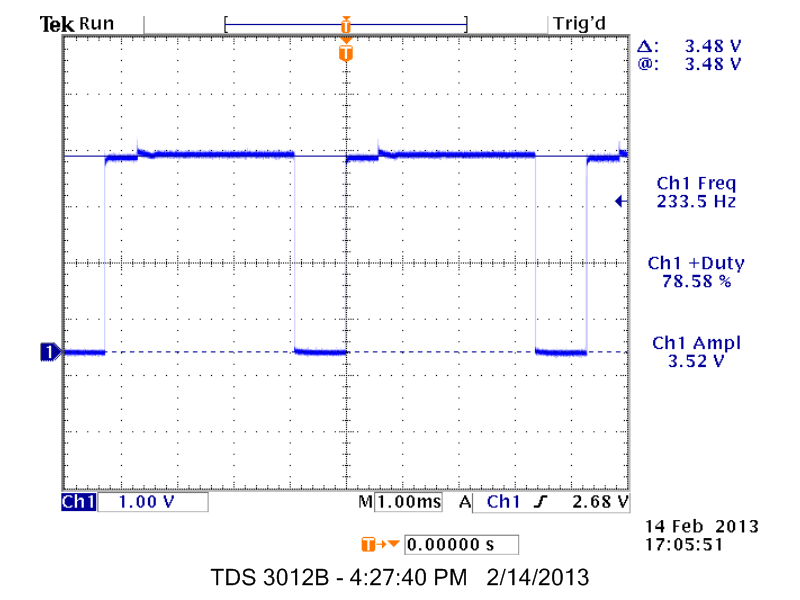


Fig. 12 Monostable 555 timer with 100 Ω load.

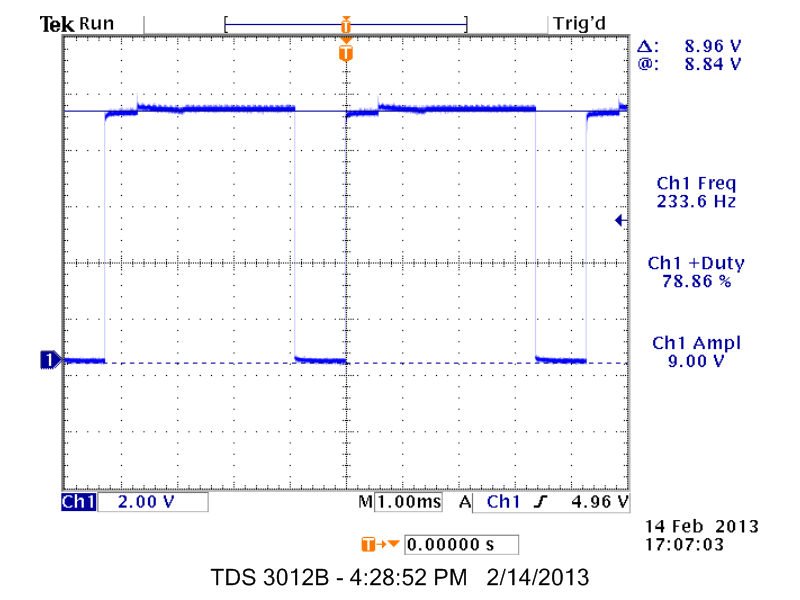


Fig. 13 Monostable 555 time with 1k Ω load.

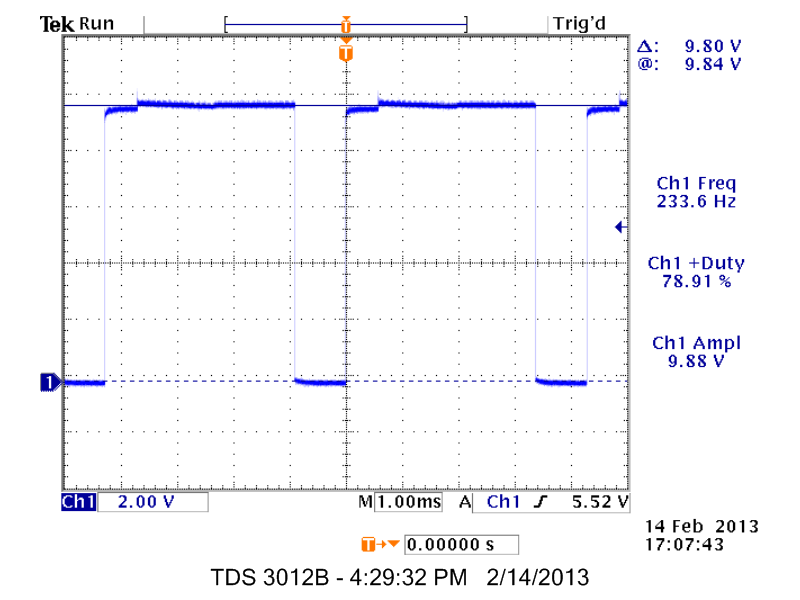


Fig. 14 Monostabel 555 timer with 10k Ω load.

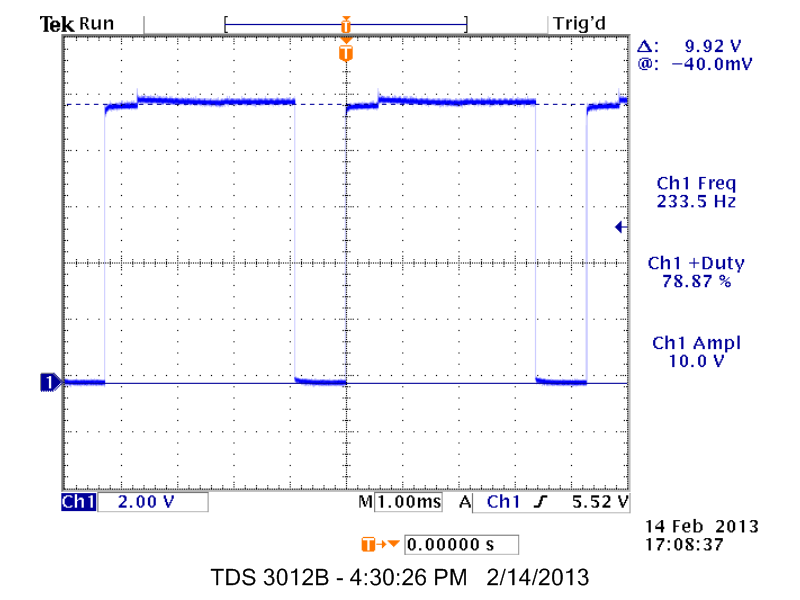


Fig. 15 Monostable 555 timer with 100k Ω load.

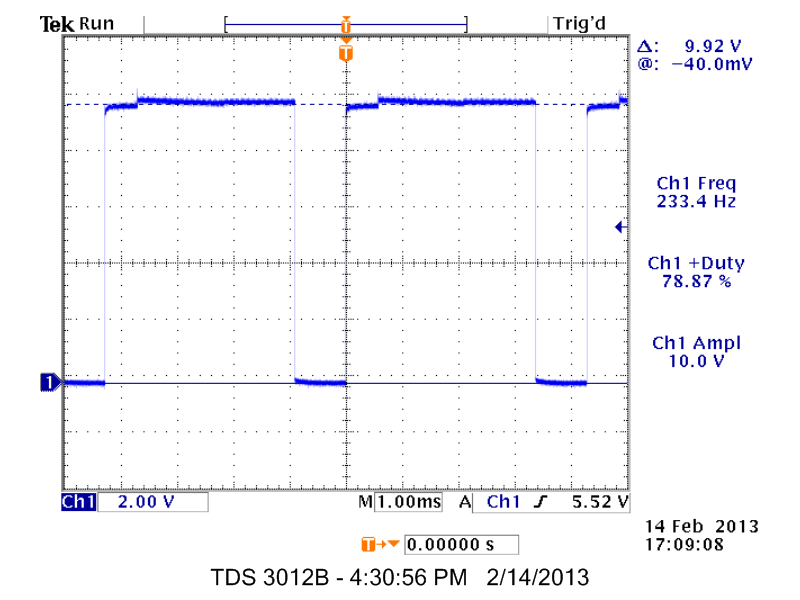


Fig. 16 Monostable 555 timer with 1M Ω load.

In Fig. 14, the load resistance is 10k Ω and the voltage is 9.88 volts. In Fig. 15, the load resistance is 100k Ω and the voltage is at 10v. Finally, in Fig. 16, the load resistance is at 1M Ω and the voltage is also, 10v. In the monostable configuration, the load resistance still needs to be high in order to get no voltage drop from the current limit of the 555 timer.

Lastly, for the astable configuration of the 555 timer, the magnitude of the Fourier components of the circuit were tested. Three different duty cycles were set and are shown in Fig. 17, 18, and 19, with a duty cycle of 98.39%, 87.2%, and 51.78% respectively. Analyzing the   
Fourier graphs, when the duty cycle is lowered, the even numbered harmonics are seen dropping and the odd numbered harmonics are staying.

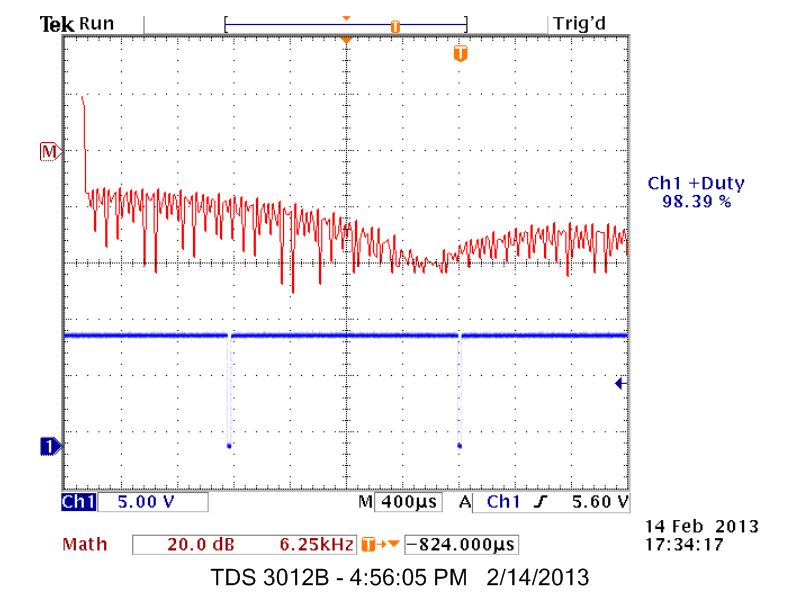


Fig. 17 Fourier components of astable 555 timer with 98.39% duty cycle.

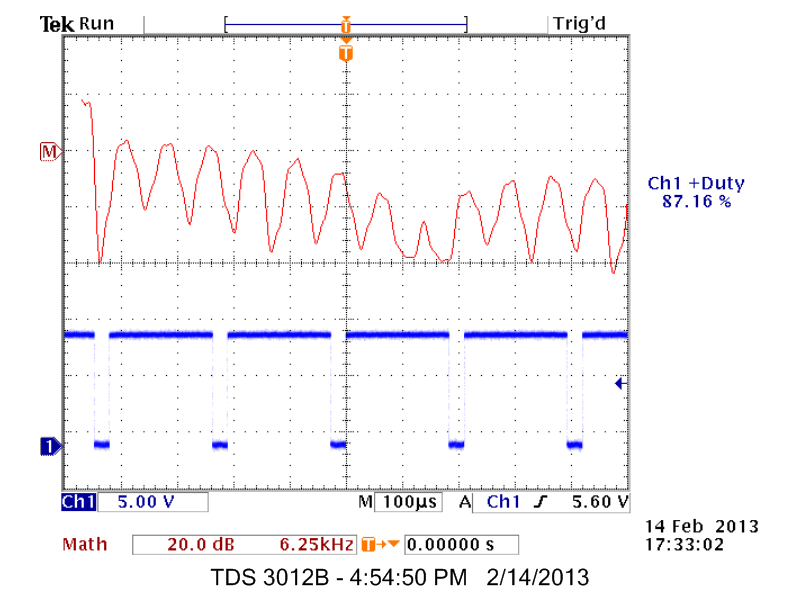


Fig. 18 Fourier components of astable 555 timer with 87.16% duty cycle.

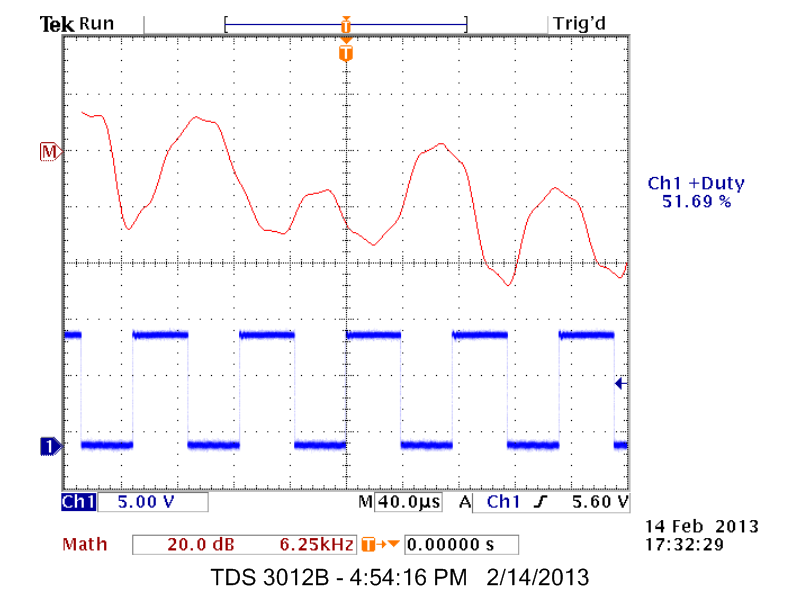


Fig. 19 Fourier components of astable 555 timer with 51.69% duty cycle

1. Conclusions

In this lab, we explored the monostable and astable configurations of the 555 timer IC. Five load resistances were connected to the output and the voltage across them was measured. It was shown that a high resistance load of 100k is needed in order to keep the output voltage the same as the input voltage. This limitation is from the 555 timer’s maximum output current of 100mA. For the astable configuration, the frequency was at a 6.72% error and the duty cycle at a 0.06% error.

References

[1] Adams, Johnathan. “The 555 Timer,” 555 Timer Electronic Circuit, 21, Feb. 2013.

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[2] Phillips, W.D. “Inside the 555”, Doctronics, 21, Feb. 2013. < http://www.doctronics.co.uk/555.htm#inside >

[3] Sedra, Adel, Smith, Kenneth. Microelectronic Circuits. New York: Oxford. 2010. Print.

[4] Surtell, Tim. “The 555 Timer,” Eleinmec, 21, Feb. 2013. <http://www.eleinmec.com/article.asp?1 >