University of Central Florida

Department of Computer Science

CDA 5106: Fall 2021

Machine Problem 1: Cache Design, Memory Hierarchy Design

by

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Honor Pledge: "I have neither given nor received unauthorized aid on this test or assignment."

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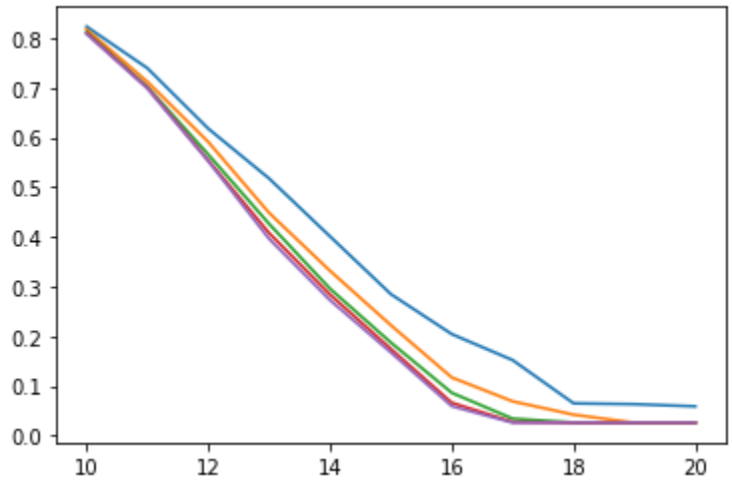
(sign by typing your name)

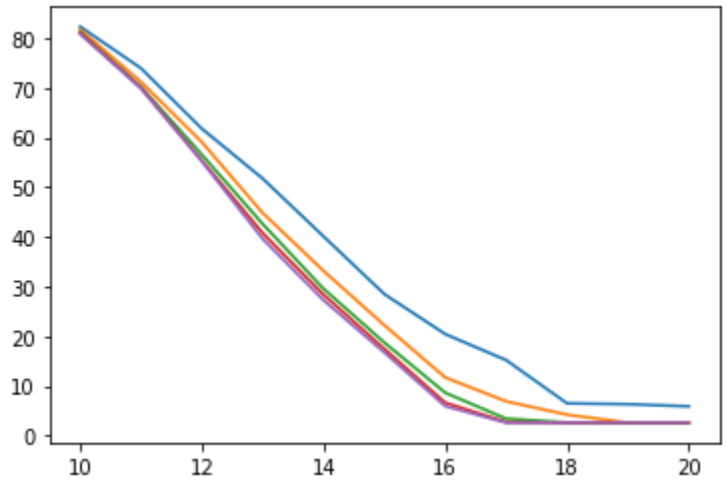
8.1

Graph 1



1. The graph steadily decreases and plateaus at a very low miss rate, near 0.0. This is common amongst all associativities tested, which shows that increasing cache size decreases the miss rate consistently up to a certain point, in this case around the 128KB mark. For a given cache size, increasing associativity tends to slightly lower the miss rate as well.
2. Given the way the absolute miss rates trend toward 0, we can assume the compulsory miss rate is *very* low, near 0.
3. Conflict Miss rate definition from *Reducing Compulsory and Capacity misses* by Norman P. Jouppi: “Conflict misses are misses that would not occur if the cache were fully associative with LRU replacement.” Since we ran the same simulation for each associativity, we can compare the miss rates between associativity x and full, where the gap between them correlates to the number of conflict misses. As associativity increases, the gap narrows, i.e. the number of conflict misses decreases, until they are nearly zero in 8-way associativity, considering the miss rates almost overlap with fully associative.

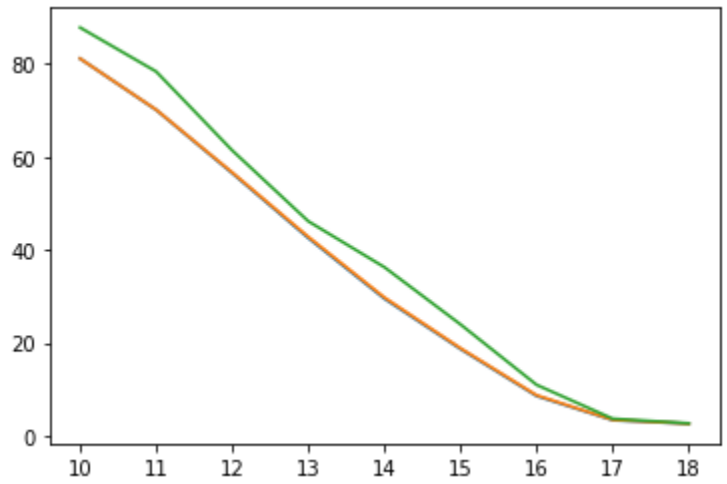
Graph 2



1. Full and 8 way associativies yield about the same AAT, each bottoming out above a 128KB Cache size configuration.

8.2

Graph 3

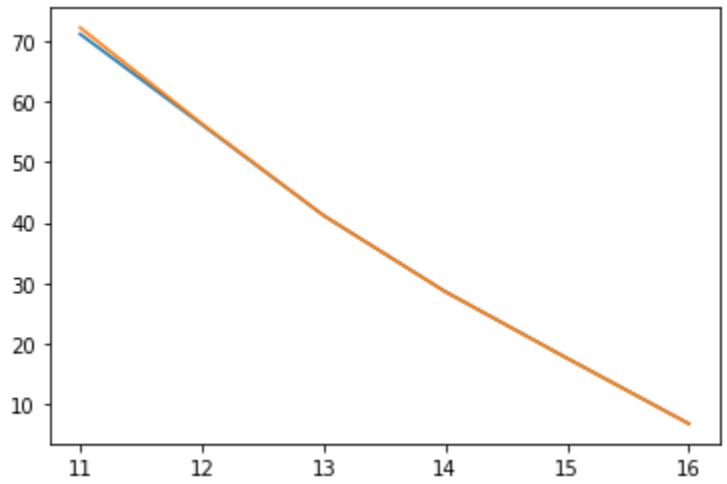


1. Each replacement policy trends towards 0 AAT with increased cache size. LRU and PLRU yield nearly identical results, to the point where the lines completely overlap each other in the graph (in orange). Considering how similar they are, we

can conclude that both LRU and PLRU yield the best (lowest) AAT, while Optimal yields a slightly higher AAT at each simulated cache size.

8.3

Graph 4



1. Both inclusion policies trend linearly towards 0 with increasing L2 Cache sizes. Non-inclusive and inclusive yield quite similar AAT results, with Non-inclusive producing slightly better (lower) AAT at lower L2 Cache sizes (2KB-4KB) before they even out.