S5K4ECGX

1/4" 5Mp CMOS Image Sensor SoC with an Embedded Image Signal Processor

Revision 0.07
October 2010

Technical Data Sheet

SAMSUNG ELECTRONICS

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S5K4ECGX 1/4" 5Mp CMOS Image Senor SoC
Technical Data Sheet, Revision 0.05

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List of Acronyms

Acronyms	Descriptions
APS	Active Pixel Sensor
ADC	Analog to Digital Convertor
CDS	Correlated Double Sampling
AE	Auto Exposure
AWB	Auto White Balance
AF	Auto Focus
PVI	Parallel Video Interface
GTG	Generic Timing Generator

1 FEATURE

1.1 IMAGE SENSOR

- Optical Format : 1/4 inch
- Unit Pixel Size : 1/4um
- Effective Resolution : 2608(H) x 1960(V)
- Active Resolution : 2592(H) x 1944(V)
- Color filter : RGB Bayer pattern
- Shutter type : Electronic rolling shutter
- Max. Capture frame rate : 15fps @full resolution
- Max. Video frame rate : 120fps @QVGA
- Max. Pixel clock frequency : 92MHz(JPEG)
- ADC accuracy : 10bit
- Progressive scan readout
- Window panning & cropping
- Vertical flip and horizontal mirror mode
- Continuous and single frame capture mode
- Frame rate control

1.2 IMAGE SIGNAL PROCESSOR

- Color interpolation and correction
- False color suppression
- Lens shading correction
- Noise removal
- Edge enhancement
- Scaler for preview and capture (3M and smaller at step 2)
- Programmable gamma correction
- Auto defect correction
- Auto dark level compensation
- Auto anti flicker correction(50/60Hz)

- Auto exposure (AE)
- Auto white balance (AWB)
- Auto focus (AF)
- Built-in test image generation
- Special effects
- 10bit parallel video interface, 8bit ITU-R.656/601
- MIPI CSI2 (dual lane)
- Output formats: YUV422, RGB565, RGB888, RAW8, RAW10, JPEG, Interleaved JPEG8 (SOSI, EOSI, SOEI, EOEI), Interleaved JPEG/Video (by data type).
- Integrated JPEG encoder and embedded SpeedTag for Fast JPEG management by Scalado SpeedView
- JPEG can be output in YUV422 format and support image rotation in JPEG.
- JPEG on-the-fly compression with embedded JPEG file size control.
- Standard frame spoof mode for JPEG8. Status and Pointers to interleaved video lines embedded in frame footer.

1.3 DEVICE

- Host control interface : I2C bus
- Internal PLL (24MHz to 100MHz input frequency)
- Operating temperature: -20℃ to +60℃
- Supply voltage : 2.8V for analog, 1.2V for digital core(with internal regulator), 1.8V ~ 2.8V for I/O
- 1.8V to 1.2V internal regulator
- VDD 1.8V regulated mode, hardware standby mode support.
- VDD 1.2V direct mode(VDD_MAIN and VDD_ALIVE direct connect to 1.2V), hardware standby mode cannot be supported.

2 GENERAL DESCRIPTION

2.1 GENERAL DESCRIPTION

The S5K4ECGX is a highly integrated 5Mp camera chip which includes a CMOS image sensor and an image signal processor with 8-bit ITU-R.656/601 parallel and MIPI CSI2 compliant serial interfaces. It is fabricated by SAMSUNG 0.09um CMOS image sensor process targeted for high-efficiency and low-power image sensors.

The CMOS image sensor consists of a 2608x1960 active pixel sensor (APS) array in 1/4 inch optical format. It has an on-chip 10-bit ADC array, and correlated double sampling (CDS) which reduce fixed pattern noise (FPN) significantly.

The image signal processor performs sophisticated image processing functions including color recovery and correction, false color suppression, lens shading correction, noise removal, edge enhancement, programmable gamma correction, image down scaling, auto defect correction, auto dark level compensation, auto flicker correction (50/60Hz), auto exposure (AE), auto white balance (AWB) and auto focus (AF). The auto functions are preformed by F/W on an embedded RISC processor. The host controller is able to access and control this devices via a general I2C bus.

2.2 LOGICAL SYMBOL DIAGRAM

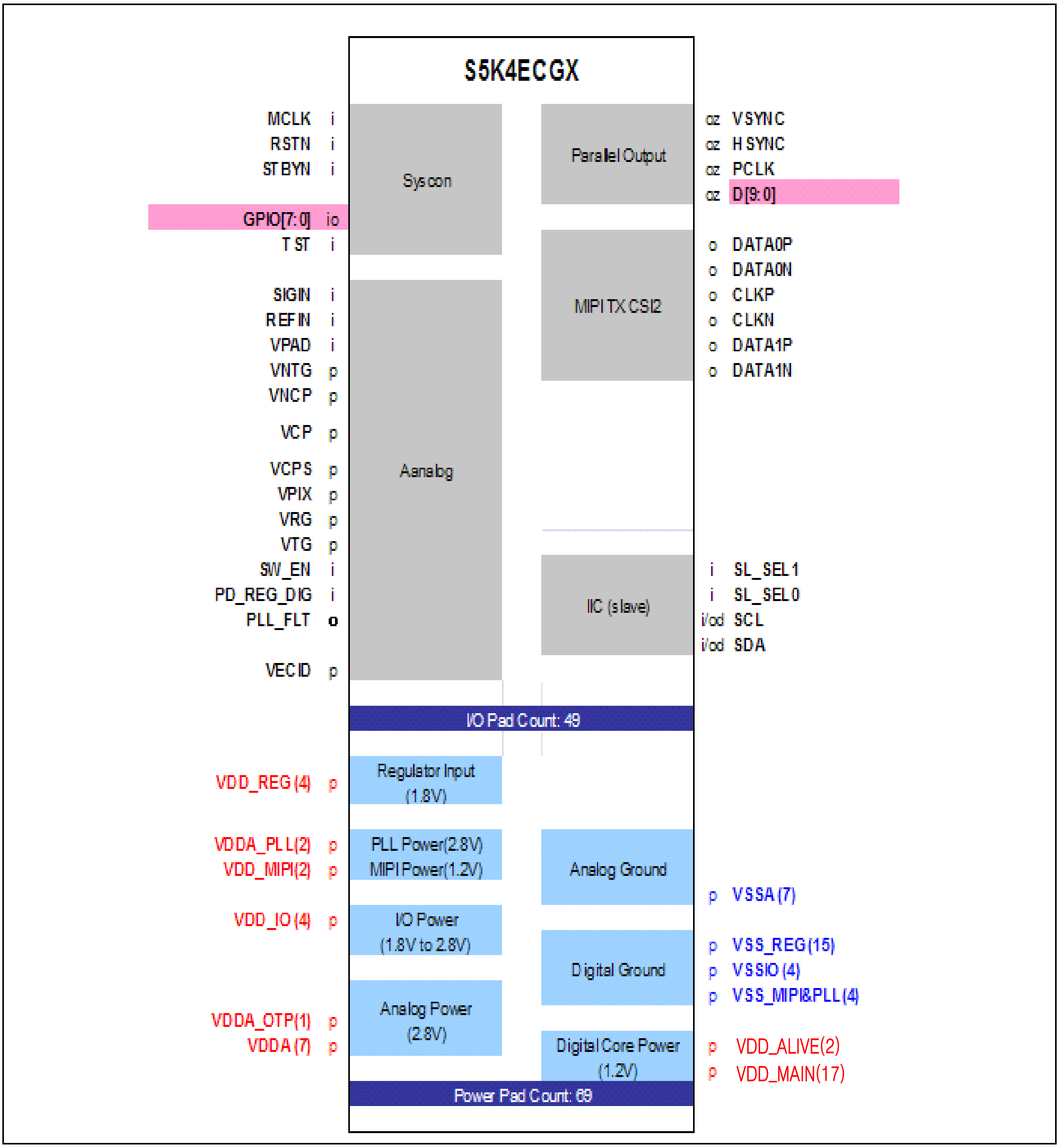


Figure 1 Logical symbol diagram

2.3 PIN CONFIGURATION

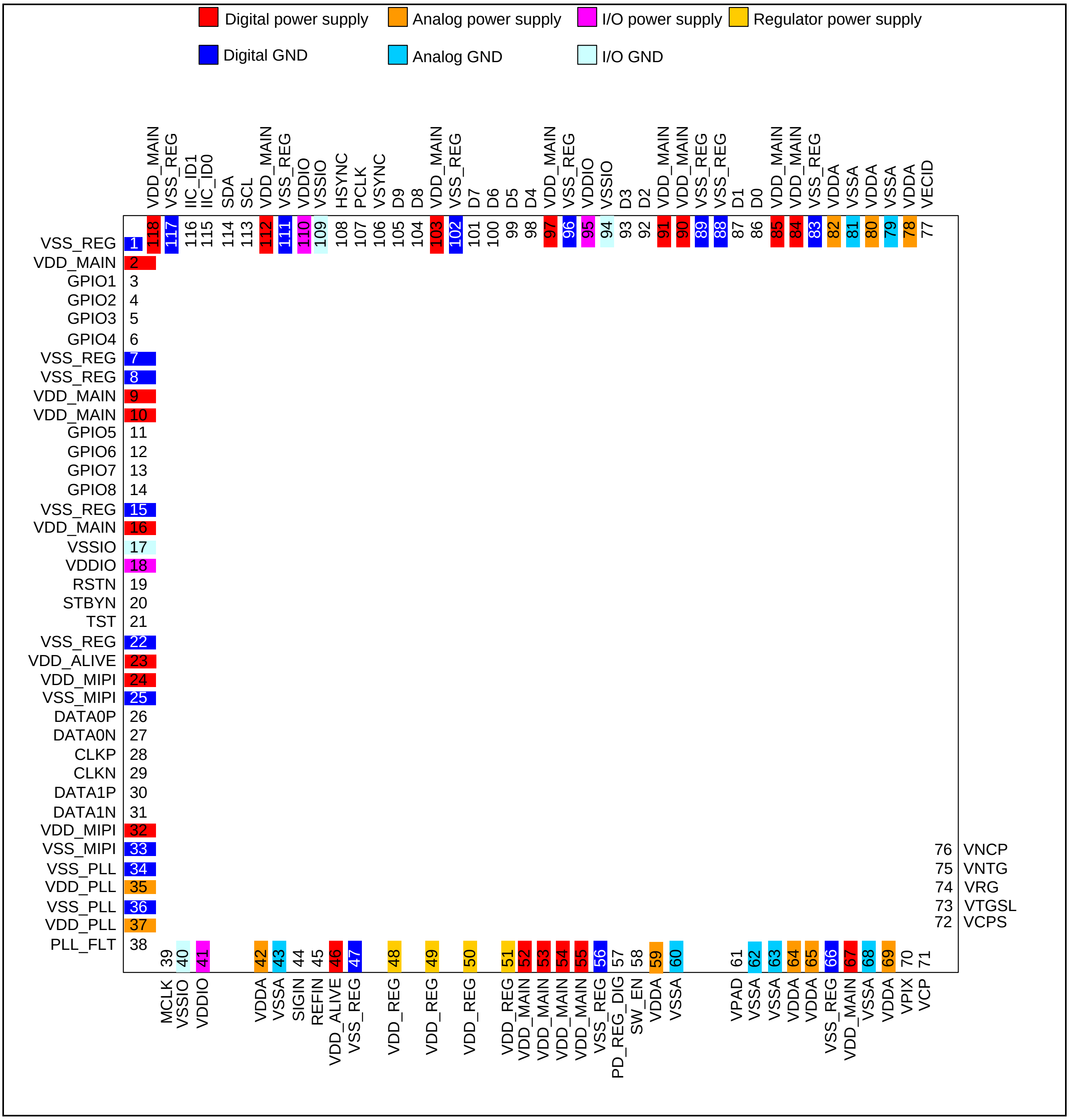


Figure 2 Pin Configuration

2.4 PIN DESCRIPTION

Table 2-1 Pin description

Pin No.	Name	I/O	A/D	Description
1	VSS_REG	GND	D	Digital ground
2	VDD_MAIN	Power	D	1.2V digital power supply
3	GPIO1	I/O	D	General purpose I/Os
4	GPIO2	I/O	D	
5	GPIO3	I/O	D	
6	GPIO4	I/O	D	
7	VSS_REG	GND	D	Digital ground
8	VSS_REG	GND	D	
9	VDD_MAIN	Power	D	1.2V digital power supply
10	VDD_MAIN	Power	D	
11	GPIO5	I/O	D	General purpose I/Os
12	GPIO6	I/O	D	
13	GPIO7	I/O	D	
14	GPIO8	I/O	D	
15	VSS_REG	GND	D	Digital ground
16	VDD_MAIN	Power	D	1.2V digital power supply
17	VSSIO	GND	D	I/O ground
18	VDDIO	Power	D	I/O power supply(1.8V ~ 2.8V)
19	RSTN	I	D	Master reset(Active low)
20	STBYN	I	D	Hardware standby mode (Active low)
21	TST	I	D	Test pin. NC
22	VSS_REG	GND	D	Digital ground
23	VDD_ALIVE	Power	D	1.2V digital power supply
24	VDD_MIPI	Power	D	1.2V digital power supply
25	VSS_MIPI	GND	D	Digital ground
26	DATA0P	O	A	CSI-2 Tx data lane 0 positive.
27	DATA0N	O	A	CSI-2 Tx data lane 0 negative.
28	CLKP	O	A	CSI-2 Tx clock positive
29	CLKN	O	A	CSI-2 Tx clock negative
30	DATA1P	O	A	CSI-2 Tx data lane 1 positive
31	DATA1N	O	A	CSI-2 Tx data lane 1 negative
32	VDD_MIPI	Power	D	1.2V digital power supply
33	VSS_MIPI	GND	D	Digital ground

34	VSS_PLL	GND	D	Digital ground
35	VDD_PLL	Power	A	2.8V analog power supply
36	VSS_PLL	GND	D	Digital ground
37	VDD_PLL	Power	A	2.8V analog power supply
38	PLL_FLT	O	A	Analog test. NC
39	MCLK	I	D	External clock.
40	VSSIO	GND	D	I/O ground
41	VDDIO	Power	D	I/O power supply(1.8V ~ 2.8V)
42	VDDA	Power	A	2.8V analog power supply
43	VSSA	GND	A	Analog ground
44	SIGIN	I	A	Analog test. NC
45	REFIN	I	A	Analog test. NC
46	VDD_ALIVE	Power	D	1.2V digital power supply
47	VSS_REG	GND	D	Digital ground
48	VDD_REG	Power	D	1.8V Regulator power supply
49	VDD_REG	Power	D	
50	VDD_REG	Power	D	
51	VDD_REG	Power	D	
52	VDD_MAIN	Power	D	1.2V digital power supply
53	VDD_MAIN	Power	D	
54	VDD_MAIN	Power	D	
55	VDD_MAIN	Power	D	
56	VSS_REG	GND	D	Digital ground
57	PD_REG_DIG	I	A	Regulator power down.(Active high)
58	SW_EN	I	A	Regulator switch enable.(Active high)
59	VDDA	Power	A	2.8V analog power supply
60	VSSA	GND	A	Analog ground
61	VPAD	I	A	Analog test. NC
62	VSSA	GND	A	Analog ground
63	VSSA	GND	A	
64	VDDA	Power	A	2.8V analog power supply
65	VDDA	Power	A	
66	VSS_REG	GND	D	Digital ground
67	VDD_MAIN	Power	D	1.2V digital power supply
68	VSSA	GND	A	Analog ground
69	VDDA	Power	A	2.8V analog power supply
70	VPIX	O	A	Connect to 2.8V analog power
71	VCP	O	A	Analog test. External cap 0.1uF

72	VCPS	O	A	Analog test. NC
73	VTGSL	O	A	Analog test. NC
74	VRG	O	A	Analog test. NC
75	VNTG	O	A	Analog test. NC
76	VNCP	O	A	Analog test. NC
77	VECID	I	A	Analog test (High voltage input for OTP memory write). NC
78	VDDA	Power	A	2.8V analog power supply
79	VSSA	GND	A	Analog ground
80	VDDA	Power	A	2.8V analog power supply
81	VSSA	GND	A	Analog ground
82	VDDA	Power	A	2.8V analog power supply
83	VSS_REG	GND	D	Analog ground
84	VDD_MAIN	Power	D	1.2V digital power supply
85	VDD_MAIN	Power	D	
86	D0	O	D	Pixel data output
87	D1	O	D	Pixel data output
88	VSS_REG	GND	D	Digital ground
89	VSS_REG	GND	D	
90	VDD_MAIN	Power	D	1.2V digital power supply
91	VDD_MAIN	Power	D	
92	D2	O	D	Pixel data output
93	D3	O	D	Pixel data output
94	VSSIO	GND	D	I/O ground
95	VDDIO	Power	D	I/O power supply(1.8V ~ 2.8V)
96	VSS_REG	GND	D	Digital ground
97	VDD_MAIN	Power	D	1.2V digital power supply
98	D4	O	D	Pixel data output
99	D5	O	D	Pixel data output
100	D6	O	D	Pixel data output
101	D7	O	D	Pixel data output
102	VSS_REG	GND	D	Digital ground
103	VDD_MAIN	Power	D	1.2V digital power supply
104	D8	O	D	Pixel data output
105	D9	O	D	Pixel data output (D9 ~ D0 : 10bit data, D9 ~ D2 : 8bit data)
106	VSYNC	O	D	Vertical sync for parallel interface
107	PCLK	O	D	Pixel clock output for parallel interface
108	HSYNC	O	D	Horizontal sync for parallel interface
109	VSSIO	GND	D	I/O ground

110	VDDIO	Power	D	I/O power supply(1.8V ~ 2.8V)
111	VSS_REG	GND	D	Digital ground
112	VDD_MAIN	Power	D	1.2V digital power supply
113	SCL	I/O	D	I2C slave clock
114	SDA	I/O	D	I2C slave data
115	IIC_ID0	I	D	I2C slave address selection. [IIC_ID1,IIC_ID0] = 00 : 0x78, 01 : 0x7A, 10 : 0x5A(default), 11 : 0xAC
116	IIC_ID1	I	D	
117	VSS_REG	GND	D	Digital ground
118	VDD_MAIN	Power	D	1.2V digital power supply

2.5 PIXEL ARRAY INFORMATION

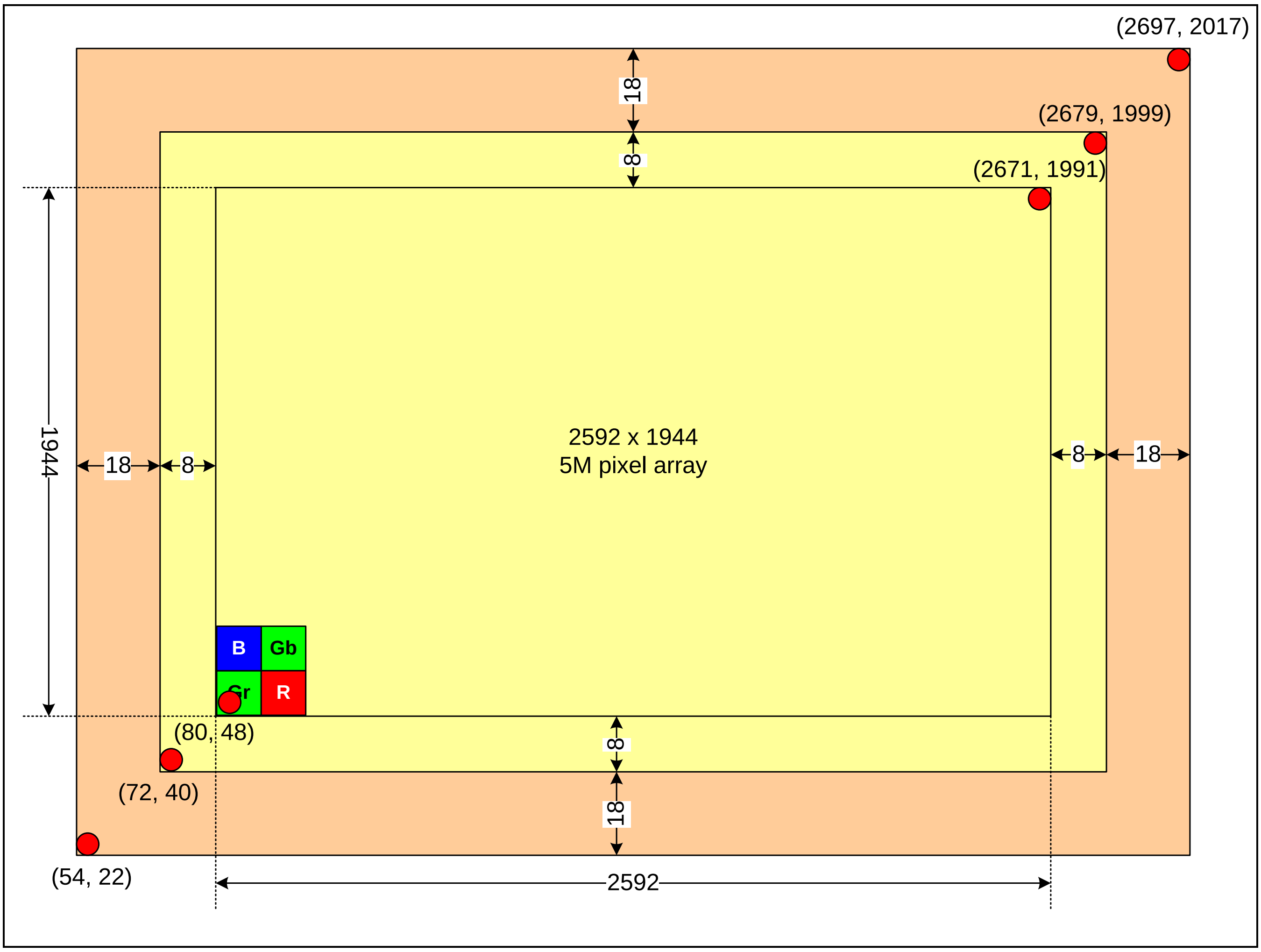


Figure 3 Pixel array information

2.6 CHIP CENTER, OPTICAL CENTER AND PIN ASSIGNMENT

2.6.1 CHIP CENTER, OPTICAL CENTER AND PIN ASSIGNMENT

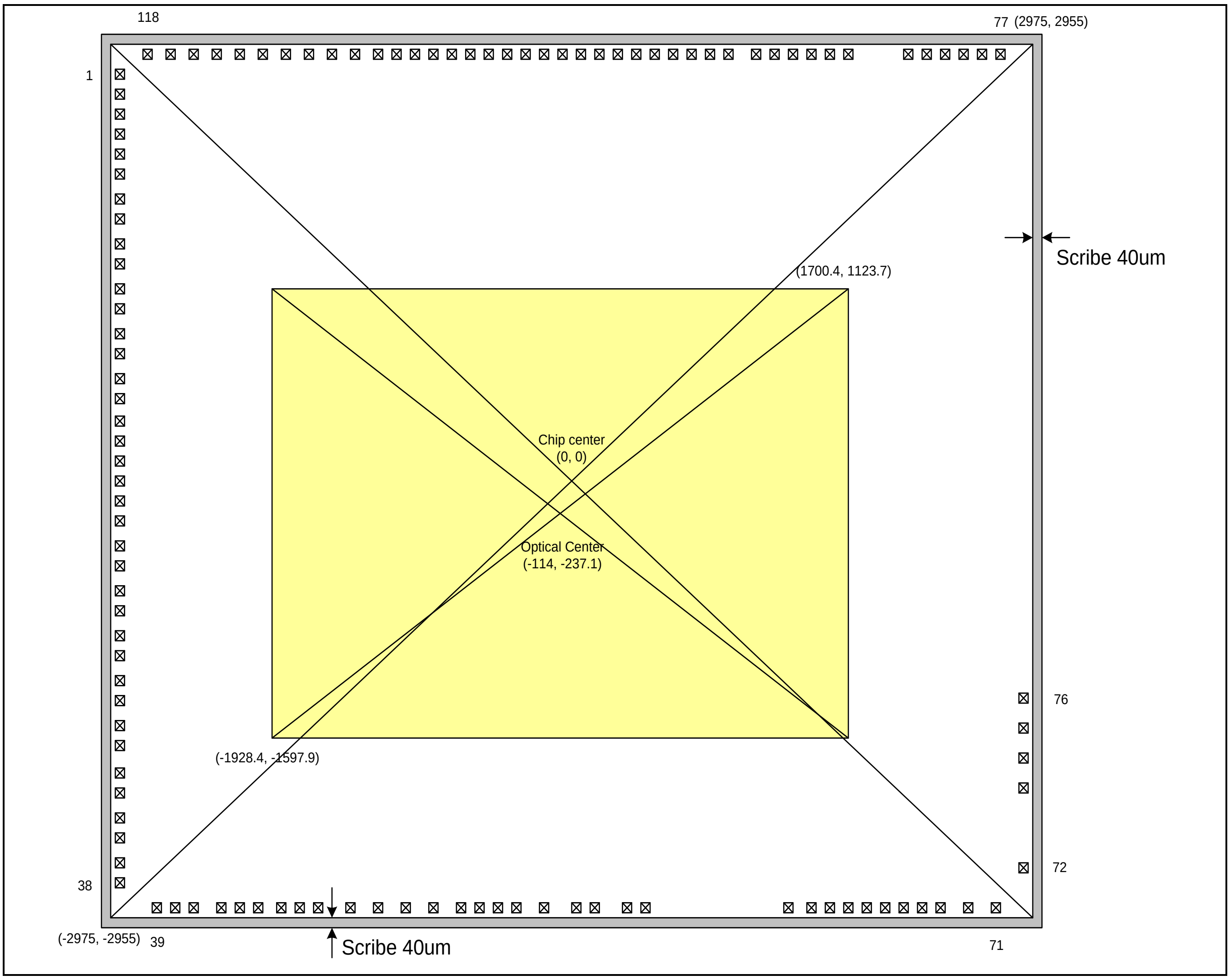


Figure 4 Chip center, Optical center and Pin assignment

2.6.2 PIN COORDINATES

Table 2-2 Pin Coordinates

	X	Y
Chip Center	0	0

No	Pin Name	X[um]	Y[um]		No	Pin Name	X[um]	Y[um]
1	VSS_REG	-2869.80	2735.12		60	VSSA	430.22	-2849.80
2	VDD_MAIN	-2869.80	2618.12		61	VPAD	1471.52	-2849.80
3	GPIO1	-2869.80	2501.12		62	VSSA	1588.52	-2849.80
4	GPIO2	-2869.80	2384.12		63	VSSA	1705.52	-2849.80
5	GPIO3	-2869.80	2267.12		64	VDDA	1822.52	-2849.80
6	GPIO4	-2869.80	2150.12		65	VDDA	1939.52	-2849.80
7	VSS_REG	-2869.80	2033.12		66	VSS_REG	2056.52	-2849.80
8	VSS_REG	-2869.80	1916.12		67	VDD_MAIN	2173.52	-2849.80
9	VDD_MAIN	-2869.80	1799.12		68	VSSA	2290.52	-2849.80
10	VDD_MAIN	-2869.80	1682.12		69	VDDA	2407.52	-2849.80
11	GPIO5	-2869.80	1565.12		70	NC	2524.52	-2849.80
12	GPIO6	-2869.80	1448.12		71	VCP	2690.52	-2849.80
13	GPIO7	-2869.80	1331.12		72	NC	2869.80	-2682.82
14	GPIO8	-2869.80	1214.12		73	NC	2869.80	-2159.58
15	VSS_REG	-2869.80	1097.12		74	NC	2869.80	-1993.58
16	VDD_MAIN	-2869.80	980.12		75	NC	2869.80	-1827.58
17	VSSIO	-2869.80	764.32		76	NC	2869.80	-1596.58
18	VDDIO	-2869.80	647.32		77	NC	2781.98	2849.80
19	RSTN	-2869.80	490.32		78	VDDA	2601.62	2849.80
20	STBYN	-2869.80	353.32		79	VSSA	2449.66	2849.80
21	TST	-2869.80	236.32		80	VDDA	2332.66	2849.80
22	VSS_REG	-2869.80	119.30		81	VSSA	2215.66	2849.80
23	VDD_ALIVE	-2869.80	2.30		82	VDDA	2098.66	2849.80
24	VDD_MIPI	-2869.80	-655.94		83	VSS_REG	1849.96	2849.80
25	VSS_MIPI	-2869.80	-775.58		84	VDD_MAIN	1718.62	2849.80
26	DATA0P	-2869.80	-1037.60		85	VDD_MAIN	1587.28	2849.80
27	DATA0N	-2869.80	-1156.40		86	NC	1455.94	2849.80
28	CLKP	-2869.80	-1275.22		87	NC	1324.60	2849.80
29	CLKN	-2869.80	-1394.02		88	VSS_REG	1193.26	2849.80
30	DATA1P	-2869.80	-1512.82		89	VSS_REG	1061.90	2849.80
31	DATA1N	-2869.80	-1631.62		90	VDD_MAIN	930.56	2849.80

32	VDD_MIPI	-2869.80	-1748.62		91	VDD_MAIN	799.22	2849.80
33	VSS_MIPI	-2869.80	-1868.26		92	D2	667.88	2849.80
34	VSS_PLL	-2869.80	-1987.90		93	D3	536.54	2849.80
35	VDD_PLL	-2869.80	-2107.54		94	VSSIO	405.20	2849.80
36	VSS_PLL	-2869.80	-2320.18		95	VDDIO	273.86	2849.80
37	VDD_PLL	-2869.80	-2439.82		96	VSS_REG	142.52	2849.80
38	PLL_FLT	-2869.80	-2654.26		97	VDD_MAIN	11.16	2849.80
39	MCLK	-2660.16	-2849.80		98	D4	-120.16	2849.80
40	VSSIO	-2520.14	-2849.80		99	D5	-251.52	2849.80
41	VDDIO	-2380.12	-2849.80		100	D6	-382.86	2849.80
42	VDDA	-2146.58	-2849.80		101	D7	-514.20	2849.80
43	VSSA	-2029.58	-2849.80		102	VSS_REG	-645.54	2849.80
44	NC	-1912.58	-2849.80		103	VDD_MAIN	-776.88	2849.80
45	NC	-1795.58	-2849.80		104	D8	-908.22	2849.80
46	VDD_ALIVE	-1678.58	-2849.80		105	D9	-1039.56	2849.80
47	VSS_REG	-1561.58	-2849.80		106	VSYNC	-1170.90	2849.80
48	VDD_REG	-1345.78	-2849.80		107	PCLK	-1302.26	2849.80
49	VDD_REG	-1135.78	-2849.80		108	HSYNC	-1433.60	2849.80
50	VDD_REG	-925.78	-2849.80		109	VSSIO	-1564.94	2849.80
51	VDD_REG	-715.78	-2849.80		110	VDDIO	-1696.28	2849.80
52	VDD_MAIN	-505.78	-2849.80		111	VSS_REG	-1827.62	2849.80
53	VDD_MAIN	-388.78	-2849.80		112	VDD_MAIN	-1958.96	2849.80
54	VDD_MAIN	-271.78	-2849.80		113	SCL	-2090.32	2849.80
55	VDD_MAIN	-154.78	-2849.80		114	SDA	-2221.66	2849.80
56	VSS_REG	-37.78	-2849.80		115	NC	-2353.00	2849.80
57	PD_REG_DIG	79.22	-2849.80		116	NC	-2484.34	2849.80
58	SW_EN	196.22	-2849.80		117	VSS_REG	-2615.68	2849.80
59	VDDA	313.22	-2849.80		118	VDD_MAIN	-2747.02	2849.80

2.7 VIDEO OUTPUT INTERFACE DESCRIPTION

The Video output interface is based on two interfaces - PVI (Parallel Video Interface) and MIPI (operating non-concurrently). The Video Output Interface defines an interface between a peripheral device (camera) and a host processor (base-band, application engine). The MIPI interface (CSI-2 + D-PHY) provides robust, scalable, low-power, high-speed, cost-effective standard interface for mobile devices. The Parallel Video Interface (PVI) is the output interface of most Camera devices. The PVI interface can be configured to operate as a camera interface. The Special Interleave unit collects data from Application Layer data streams and feeds it toward one of the interfaces.

2.7.1 MODES OF OPERATION

2.7.1.1 Video (Preview)

Full resolution, downscaled to VGA and sub VGA size @30fps.

Minimal power, as this is the most common operational mode.

2.7.1.2 Video (Capture)

Up to full resolution of 2592 x 1944 output for single or multiple frames @15fps.

2.7.1.3 JPEG (Preview)

Full resolution image, downscaled to VGA and sub VGA size, compressed @30fps.

Optional uncompressed video embedded in JPEG for display.

Optional JPEG file size control and rotation support.

2.7.1.4 JPEG (Capture)

Up to full resolution of 2592 x 1944 compressed output for single or multiple frames at 15fps.

Optional uncompressed thumbnail embedded in JPEG for display.

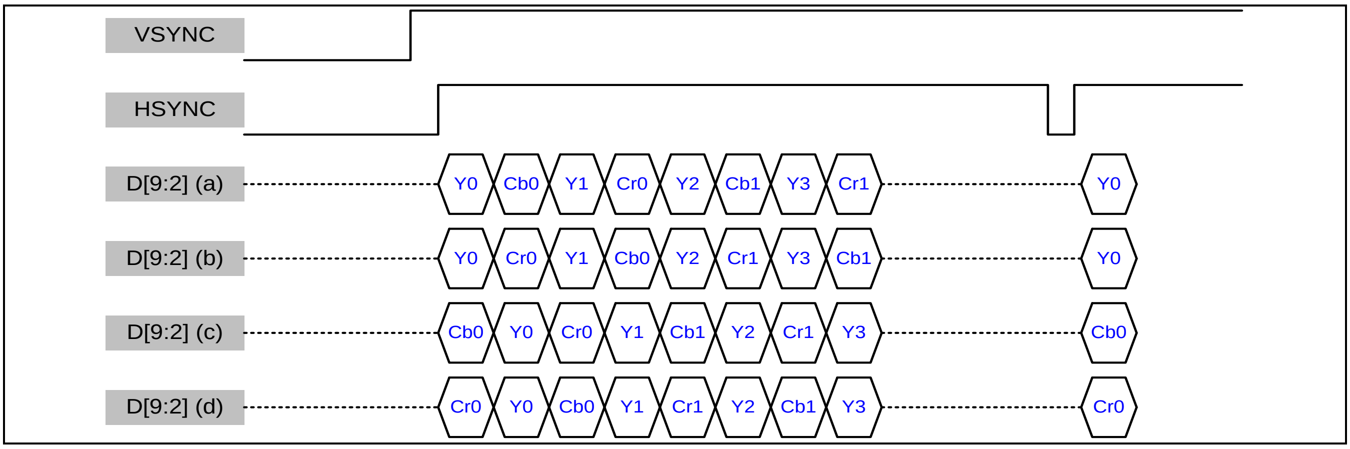
Optional JPEG file size control and rotation support.

2.7.2 PARALLEL VIDEO INTERFACE

There are two output formats: ITU-R.601 and ITU-R.656 formats. ITU-R.601 possible data format is all (RGB888/RGB565/YUV422/YUV420/JPEG/Embedded/Bayer8) and ITU-R.656 possible data format is YUV422 (Y:16-235,UV:16-240), Bayer8, RGB888, RGB565. Embedded, JPEG and Bayer 10 are not supported in 656 format.

2.7.2.1 ITU-R.601 Data output format

ITU-R.601 output data can be output parallel interface. In the parallel output interface, ITU-R.601 output data is output on the 8-bit parallel bus D[9:2], with VSYNC, HSYNC, and PCLK. ITU-R.601 output data is valid when VSYNC and HSYNC are asserted. When the ITU-R.601 data output for the frame completes, VSYNC and HSYNC are de-asserted.



NOTE: The data output sequence, (a) to (d) can be selected by register setting.

Figure 5 ITU-R.601 YCbCr(YUV422) Data output timing

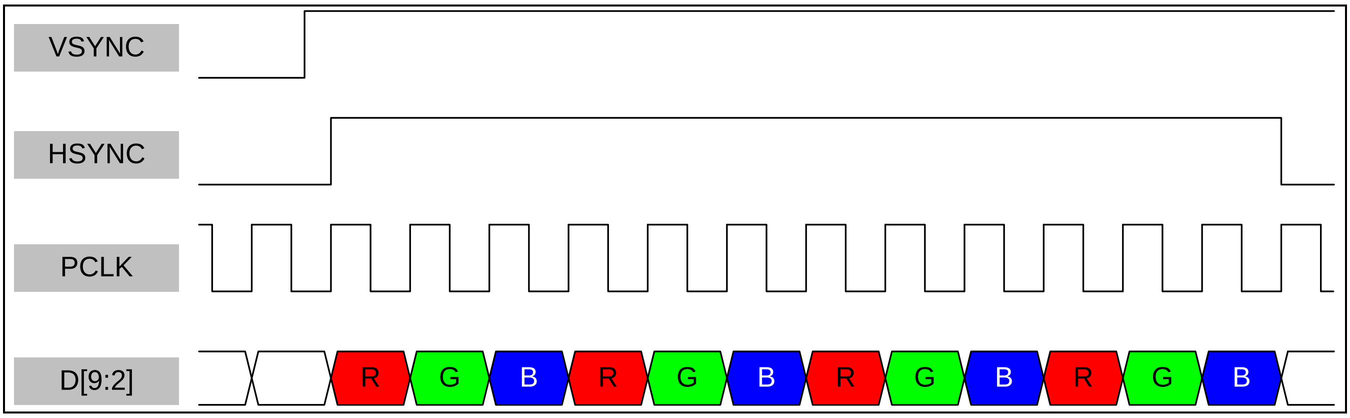


Figure 6 RGB888 Data output timing in ITU-R.601 format

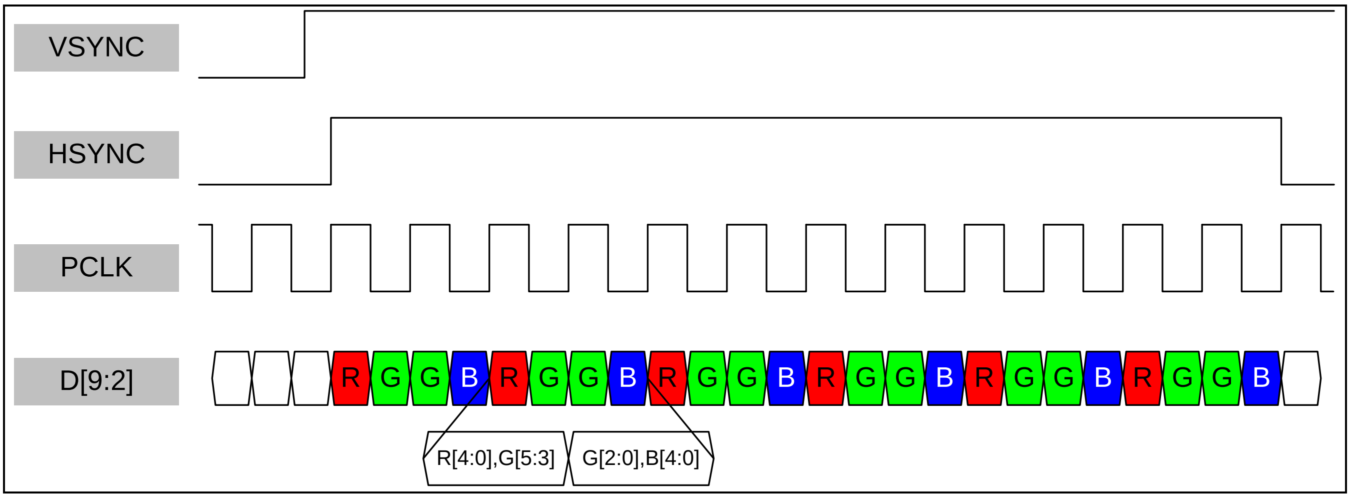


Figure 7 RGB565 Data output timing in ITU-R.601 format

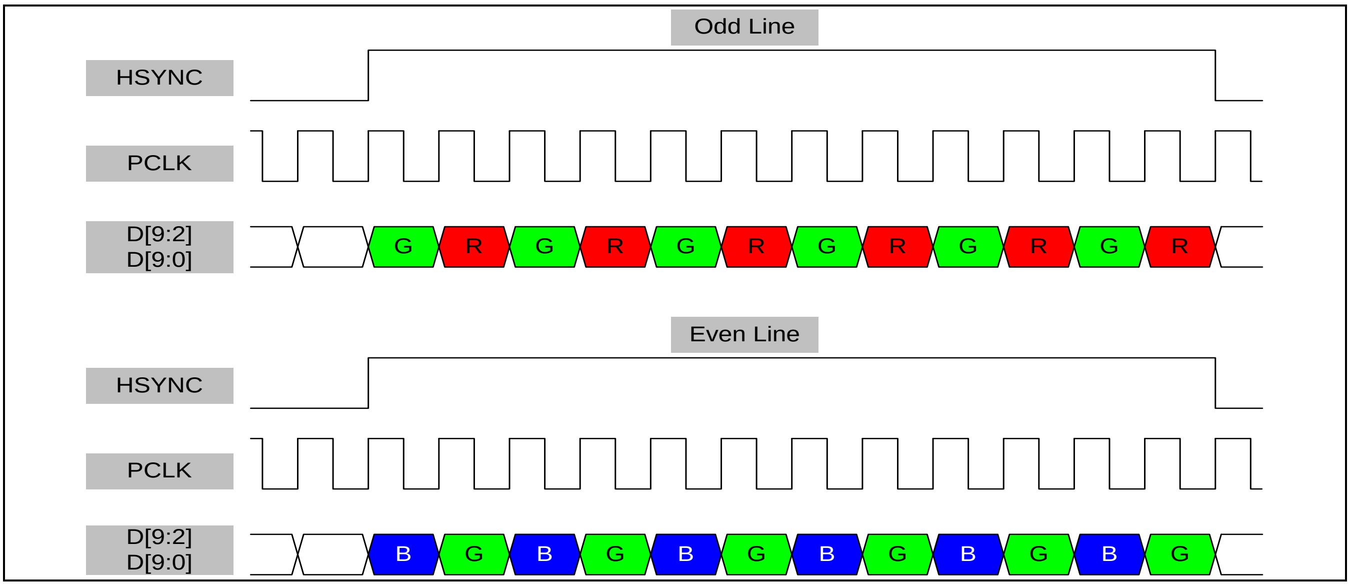


Figure 8 Bayer8 or Bayer10 Data output timing in ITU-R.601 format

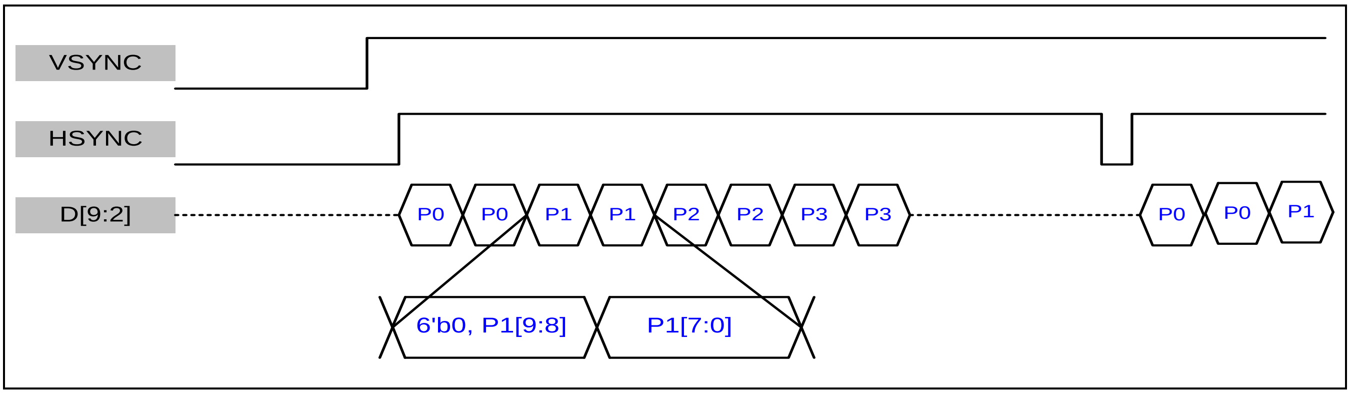


Figure 9 Bayer10-(2+8) Data output timing in ITU-R.601 format

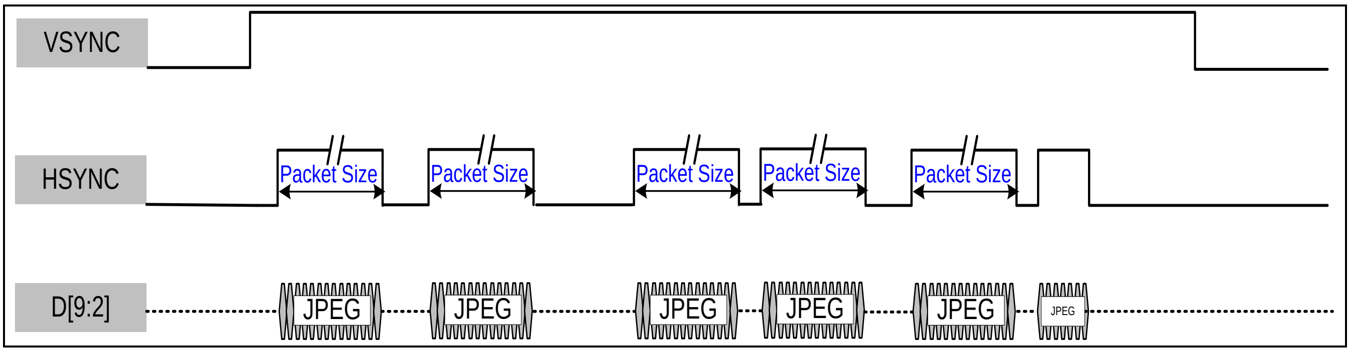


Figure 10 JPEG Compressed video timing in ITU-R.601 format

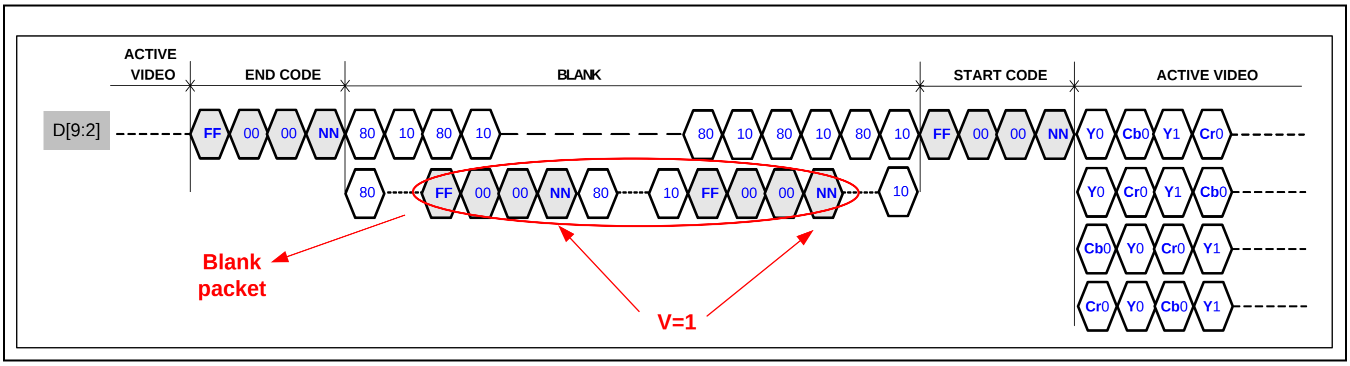
2.7.2.2 ITU-R.656 Data output format

Embedded, JPEG and Bayer10 are not supported. Since 656 commit data manipulation (The data words 0 and 255 (00 and FF in hex notation) are reserved for data identification purposes and consequently only 254 of the possible 256 words may be used to express a signal value).

Frame – distinguishing between frames can be done by two options:
Using F field- F = 0 during frame 1, F=1 during frame 2, F=0 during frame 3…
Blank packet – blank packet is sent between frames.

ITU-R.656 markers: FF, 00, 00, NN, according to field.
Field0: start active - 80, end active - 9D, start blank - AB, end blank - B6
Field1: start active - C7, end active - DA, start blank - EC, end blank - F1

In YUV422, Bayer8, RGB888 – ff value is replaced by fe value and 00 value is replaced by 01 value.
In RGB565 – if switch register is set, even columns: ff -> f7, 00 -> 08 odd columns: ff -> fe, 00 -> 01. If switch register is clear the opposite is true.



NOTE:

(1) The video data is in compliance with recommendation 656.
(2) The data words 0 and 255 (00 and FF in hex notation) are reserved for data identification purposes and consequently only 254 of the possible 256 words may be used to express signal values.
(3) Each timing reference code consists of a four word sequence in the following format : FF 00 00 NN.
(4) The fourth word (NN) contains information about the state of field blanking, and the state of line blanking.
(5) NN consist of 1(MSB, fixed), F, V, H, P3, P2, P1, P0(LSB) bits
(F=0 during field 1, 1 during field 2; V=0 elsewhere, 1 during field blanking; H=0 in SAV(Start of Active Video), 1 in EAV(End of Active Video); P3, P2, P1, P0 : protection bits)

Figure 11 ITU-R.656 YCbCr Data output timing

The following Figure 12 shows output of RGB888 in 656 interface format:

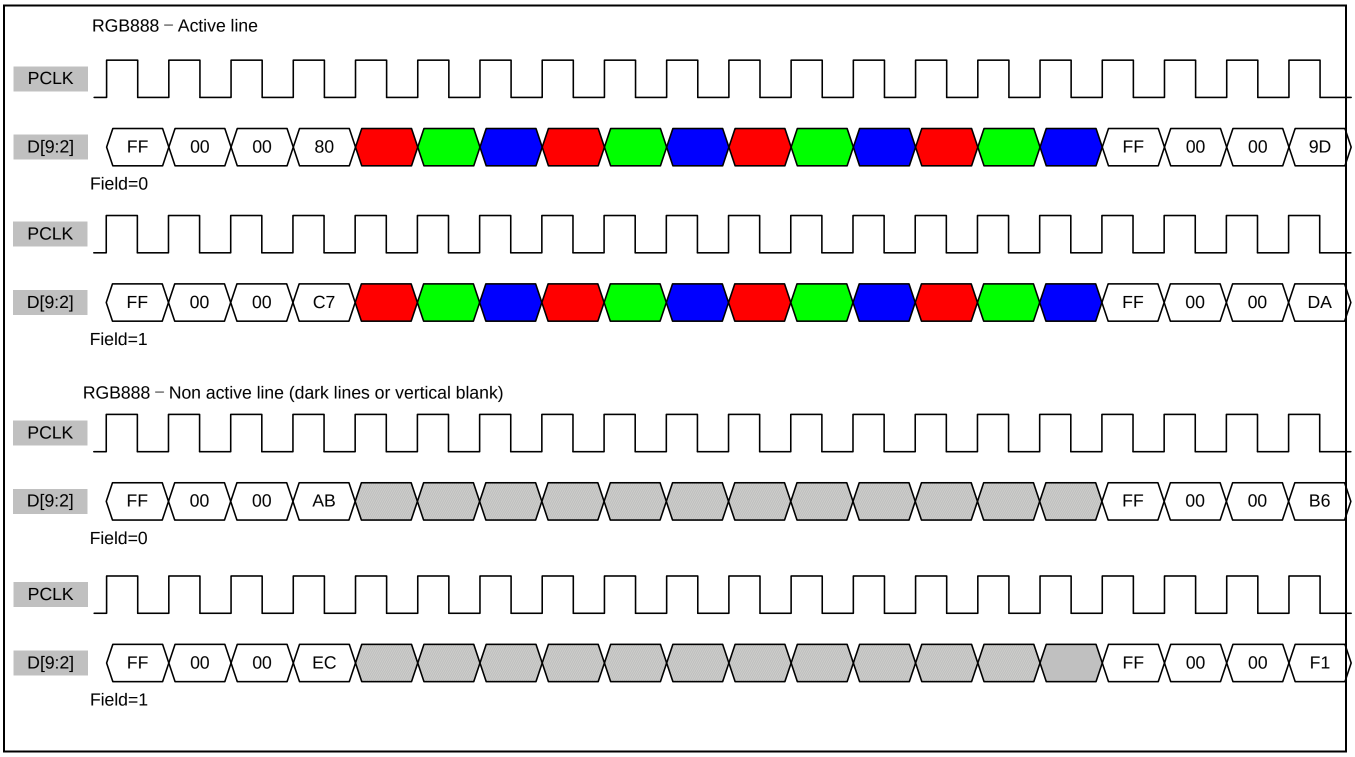


Figure 12 ITU-R.656 RGB888 Data output timing

NOTE: In 656 Standard interface, there is a need to distinguish between two consecutive frames (filled with active lines). This can be done by toggling the field bit (see the above figure) or by inserting a non-active line (and keep field = 0). Both options are supported according to the register setup. The insertion of blank line is done by register setting. The blank line length is set by blank line with register.

2.7.2.3 Interleaving without Data Type Markers

2.7.2.3.1 JPEG with Video

A JPEG packet is sent before any Video packet (Jpeg Header is sent as separate packet). JPEG packet size is determined by outregs_jpeg_packet_length register.
Video packets are attached with start marker generated by PVI (Video Markers) and are driven to the IO block.
Video packet size is determined by outregs_video_packet_length register.
Start Marker - Start_val is set by dedicated registers.
(Outregs_pvi_jpg_start_mrker_h[15:0] and Outregs_pvi_jpg_start_mrker_l[15:0]).
JPEG packets are sent to the IO with no change.

2.7.2.3.2 JPEG with Embedded

Embedded data is transmitted last in each frame.
Embedded packets are sent to the IO with no change.

2.7.2.3.3 Video with Embedded

Embedded data is transmitted last in each frame.
Embedded packets are sent to the IO with no change.

2.7.2.3.4 Video with JPEG with Embedded

See JPEG with Video and JPEG with Embedded.

The following Figure 13 shows schematically the PVI output of a frame (without data type markers). The PVI added markers (Video during JPEG) are shown in orange. Packets widths are same for Video, JPEG, and Embedded to simplify the figure.

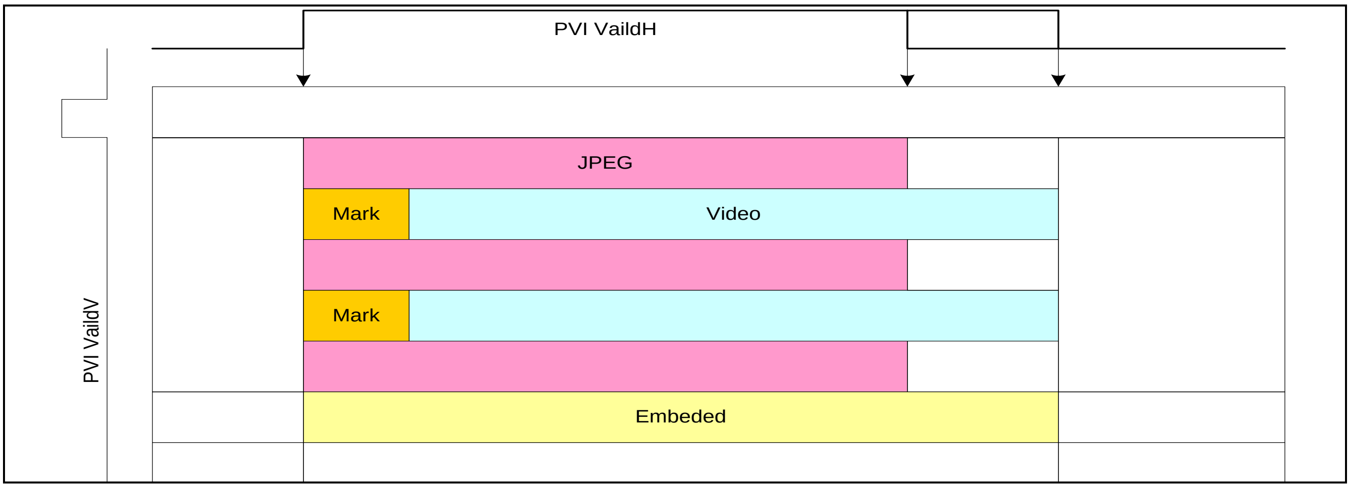


Figure 13 Interleave data transfer without data type markers

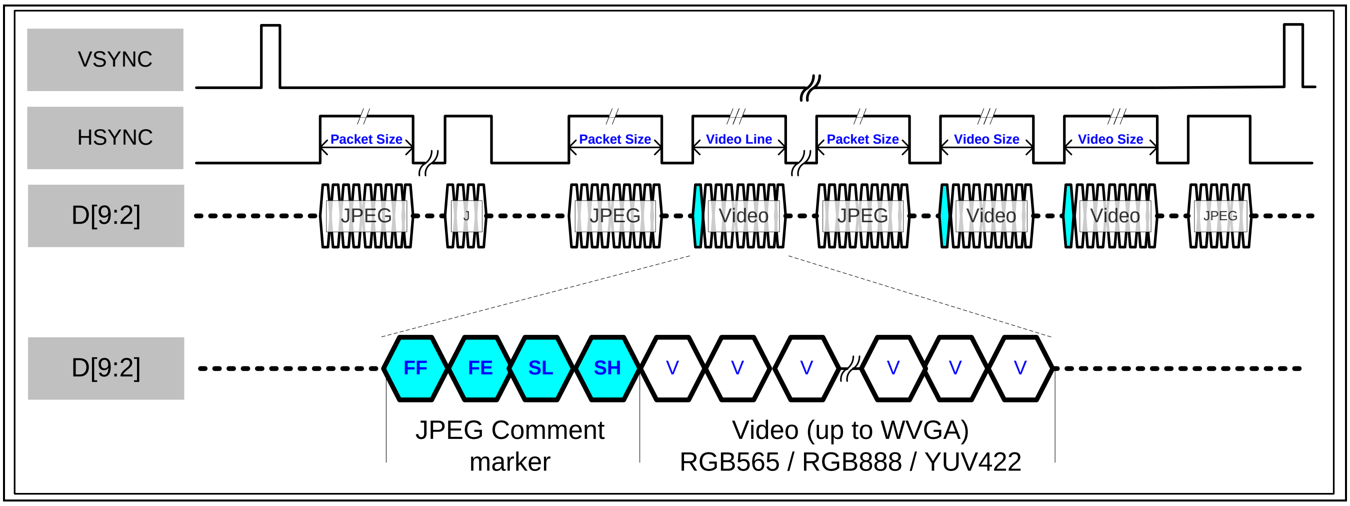


Figure 14 Interleave data transfer without data type markers

The following Figure 15 shows schematically the PVI output of a frame (with data type markers).

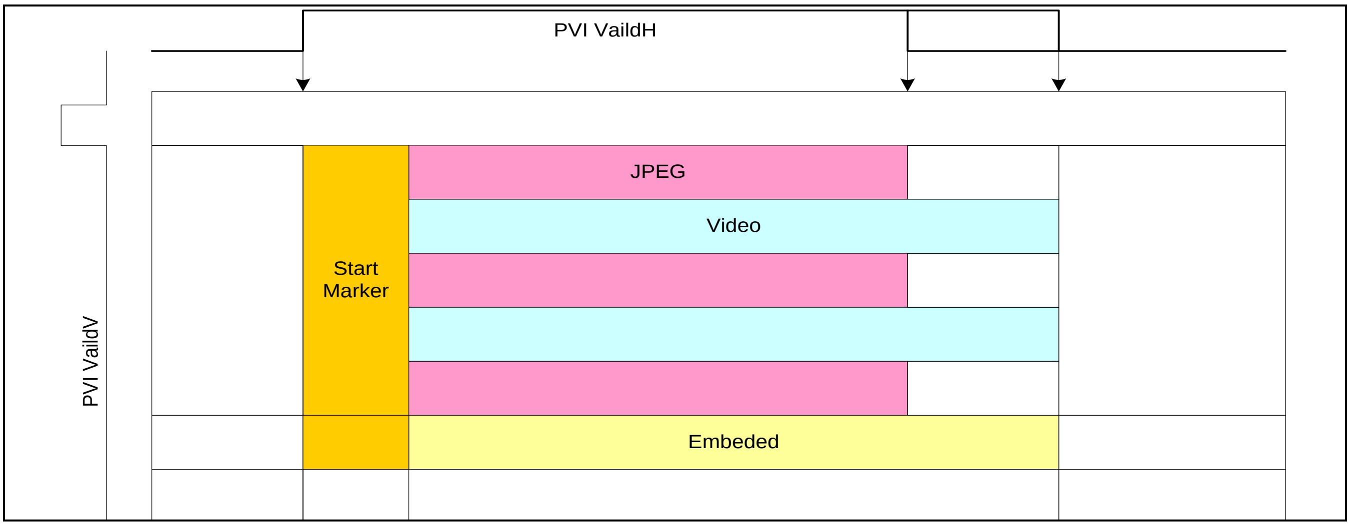
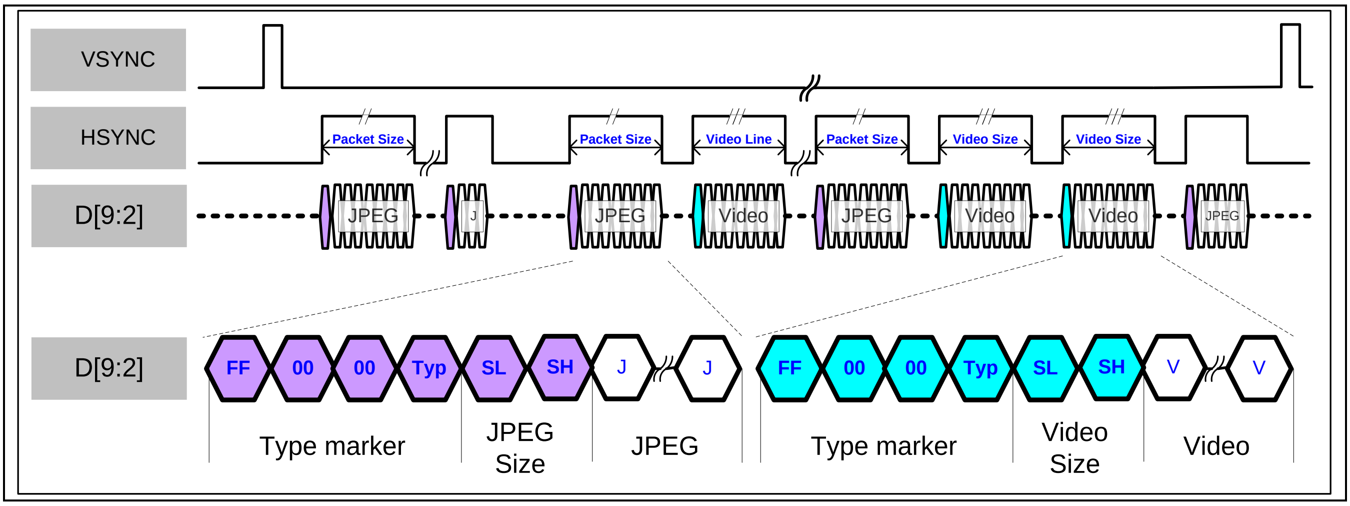


Figure 15 Interleave data transfer with data type markers



NOTE: Used for preview during MJPEG capture and for thumbnail of captured image.

All transmission is preceeded by FF 00 00 and type marker, then followed by data size.

TC header is supported in interleaved mode only.

Figure 16 JPEG-Video Interleaving with Data Type Markers

2.7.2.4 PVI fixed frame size mode (Spoof, ITU 601 only)

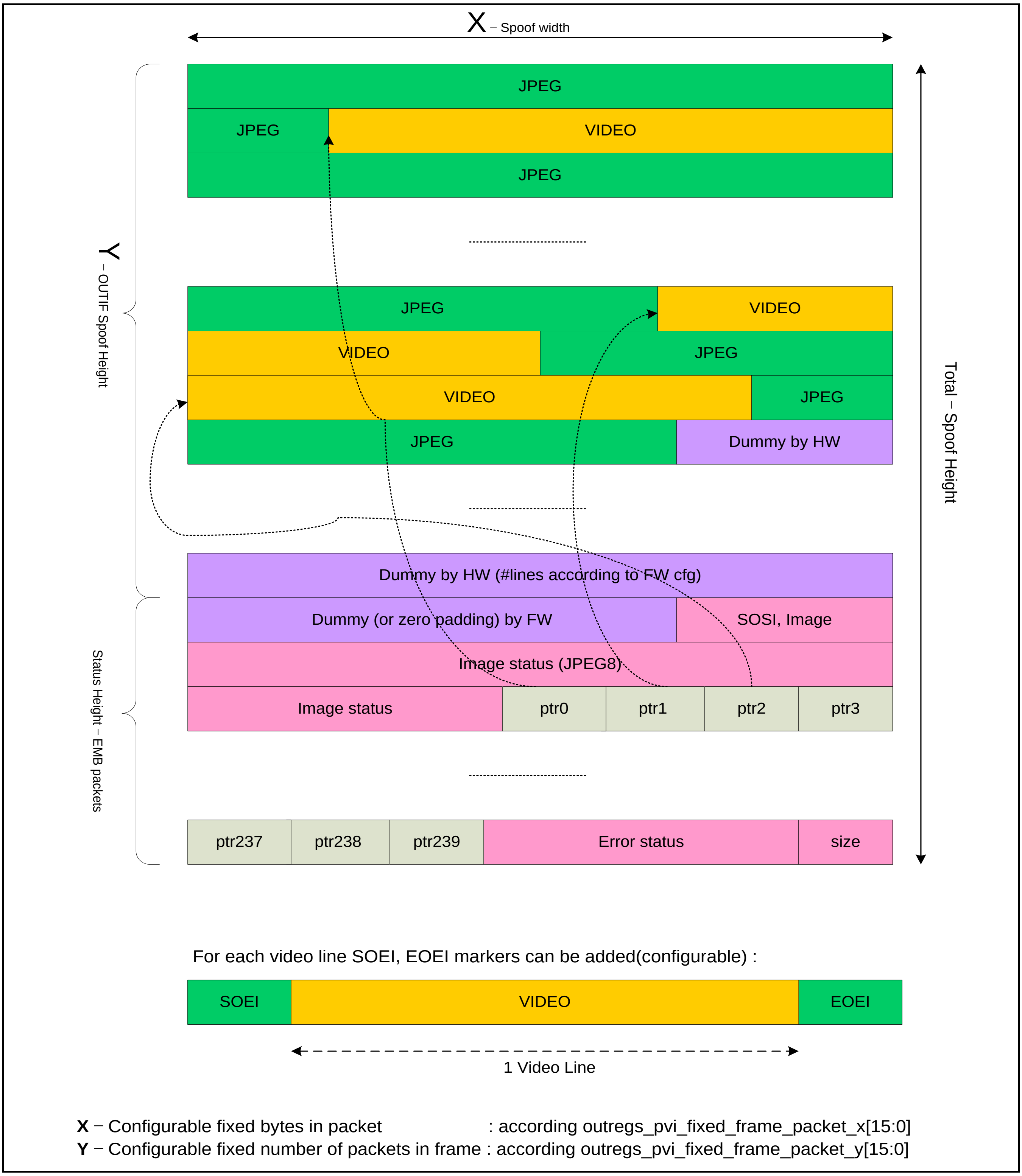


Figure 17 Fixed frame size

NOTE:

Supports PVI ITU 601 only
Supports all Video stream excluding Bayer
All PVI interleaved Data type markers are not supported
The Y configured for the OUTIF do not contains the SPOOF status packets which are transmitted as EMB packets therefore it is not the total spoof height. FW should calculate the number of Y by decrementing the number of Spoof EMB packets from the requested SPOOF Height.

DEFINITION:

Frame size (X * Y) is fixed. OUTIF will transmit the exact number of bytes according frame size.

JPEG8 - Each video field can be separated by the SOEI/EOEI markers, and JPEG8 status information can be added with SOSI/EOSI markers.

JPEG8 Additional Marker Symbol	Marker Data Code
SOSI (Start Of Status Information)	0xFF 0xBC
EOSI (End Of Status Information)	0xFF 0xBD
SOEI (Start Of Embedded Image)	0xFF 0xBE
EOEI (Start Of Embedded Image)	0xFF 0xBF

Underflow - If frame size (X * Y) is larger than Video+JPEG payload data sum of bytes, the remaining bytes will be padded with blank bytes (programmable value).

Overflow - If frame size (X * Y) is smaller than Video+JPEG payload data sum of bytes, the payload data transmission will stop after the X * Y byte were transmitted and error indication will be set in the status information.

Status packets will be transmitted at end of each frame containing:

- Video pointers
- Frame status information

Spoof status information description:

Name / Description		Size in bytes (*)	Units
Dummy (or padding)		X size dependant	
SOSI (Start Of Status Information) - JPEG8 marker 0xFFBC		2*	
JPEG8 status information size in bytes		2	
JPEG8 Status Information	Info Version - Used by the receiver to validate supported info version	2	
	CHIP ID - e.g. 04EC	2	
	EVT number - e.g. 0000 for EVT0	2	
	Image Width	2	
	Image Height	2	
	Thumbnail Width	2	
	Thumbnail Height	2	
	Exposure time in usec	4	usec

	Frame time in msec (1/fps)	2	msec
	Analog gain	2	8:8
	Digital gain	2	8:8
	White balance gains - R (2 bytes), G (2 bytes), B (2 bytes)	6	8:8
	User brightness setting	2	
	User contrast setting	2	
	AF current lens position (when applicable)	2	
JPEG8 status information size in bytes		2	
EOSI (End Of Status Information) - JPEG8 marker 0xFFBD		2*	
Video line pointers (when applicable) - 3 bytes each pointer		3*(Thumb line size)	
Error status : 0 - Frame O.K Else - Frame Error, Frame should be ignored		2*	
JPEG size - Number of JPEG bytes in frame		3*	

NOTE: (*) Byte size is without JPEG8 byte data padding (1010,1010)

2.7.2.5 Sync hold function

The VSYNC/HSYNC should be held and re-operated by host commands as shown in the Figure 18.

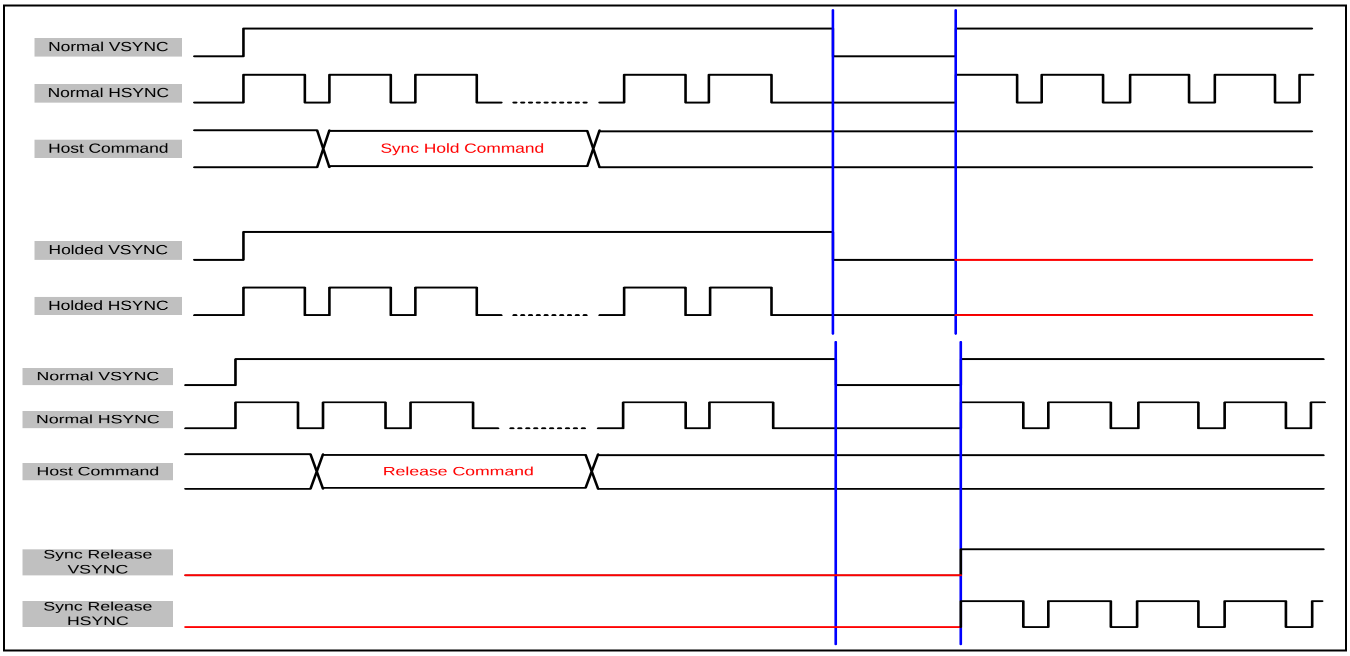
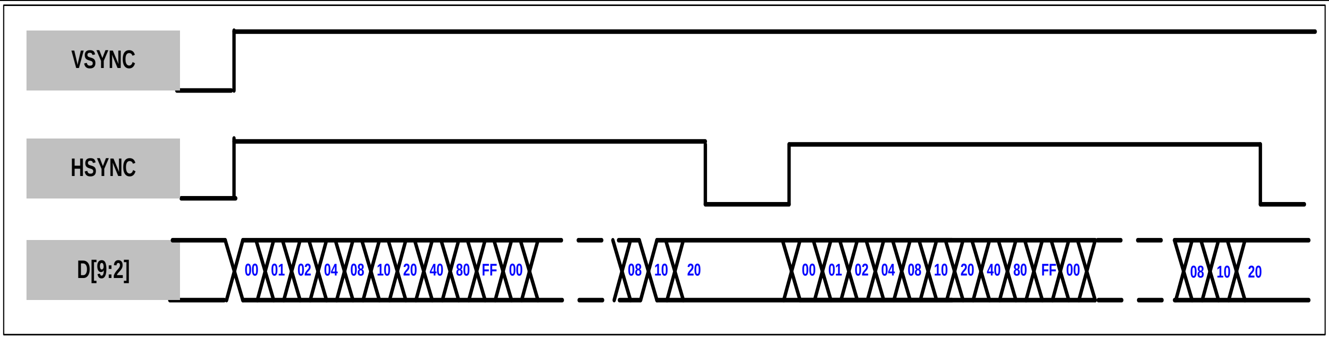


Figure 18 Sync Hold Function

2.7.2.6 Rolling test pattern

- The rolling test pattern sequence is like the Figure 19, and it must be supported for valid connectivity test in factory.

- The pattern sequence should be repeated every HSYNC period.
- The previous pattern should be held while blank period.
- There are 2 rolling pattern modes which selected by register (Add: xxx Field: xxx) - 10bit mode & 8bit mode.



(10-bit mode)

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	1	0
0	0	0	0	0	0	0	1	0	0
0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	1	0	0	0	0
0	0	0	0	1	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	1	1
0	0	0	0	0	0	0	0	0	0

.

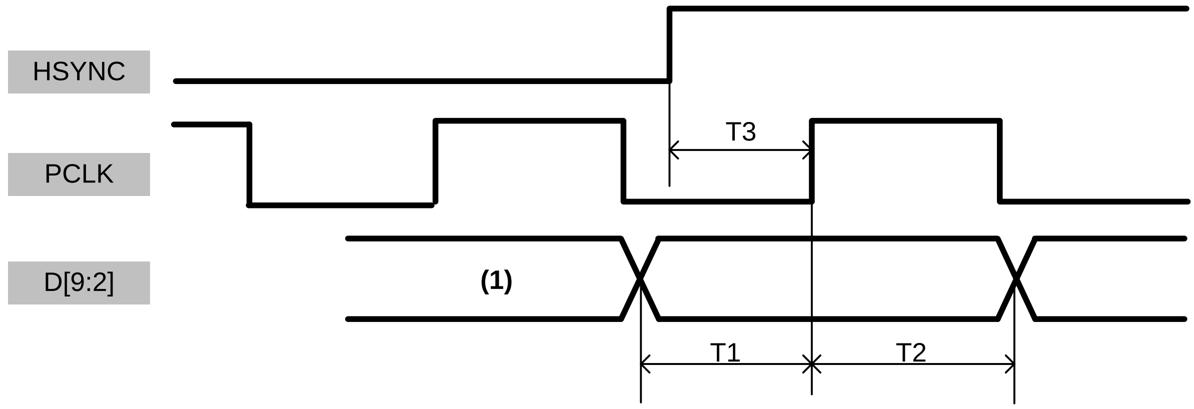
(8-bit mode)

D9	D8	D7	D6	D5	D4	D3	D2
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1
0	0	0	0	0	0	1	0
0	0	0	0	0	1	0	0
0	0	0	0	1	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	1	0	0	0	0	0	0
1	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1
0	0	0	0	0	0	0	0

.

Figure 19 Rolling test pattern generation

2.7.2.7 Pixel clock and data timing



[NOTE] (1): blank & start code, otherwise ‘0’ for ITU-R.656 output format:

SYMBOL	PARAMETER	MIN	MAX	UNIT
T1	Data Setup Time to PLCK↑	4	-	ns
T2	Data Hold Time to PLCK↑	4	-	ns
T3	HSYNC↑ to PLCK↑ Delay	4	-	ns

Figure 20 Output data and pixel clock timing

2.7.3 SERIAL OUTPUT INTERFACE (MIPI CSI-2)

Below is a description the relevant info from the MIPI protocol.

2.7.3.1 Multi-Lane Distribution and Merging

CSI-2 is a Lane-scalable specification. Applications requiring more bandwidth than that provided by one data Lane, or those trying to avoid high clock rates, can expand the data path to two, three, or four Lanes wide and obtain approximately linear increases in peak bus bandwidth. The mapping between data at higher layers and the serial bit stream is explicitly defined to ensure compatibility between host processors and peripherals that make use of multiple data Lanes.

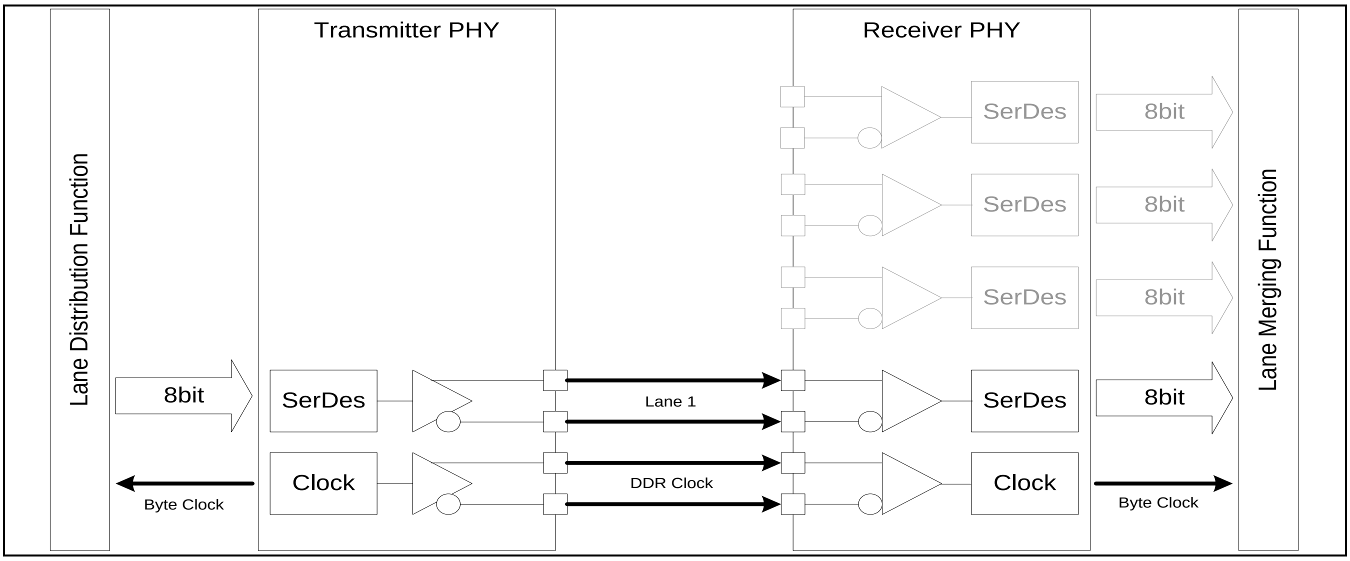


Figure 21 One Lane Transmitter and Four Lane Receiver Example

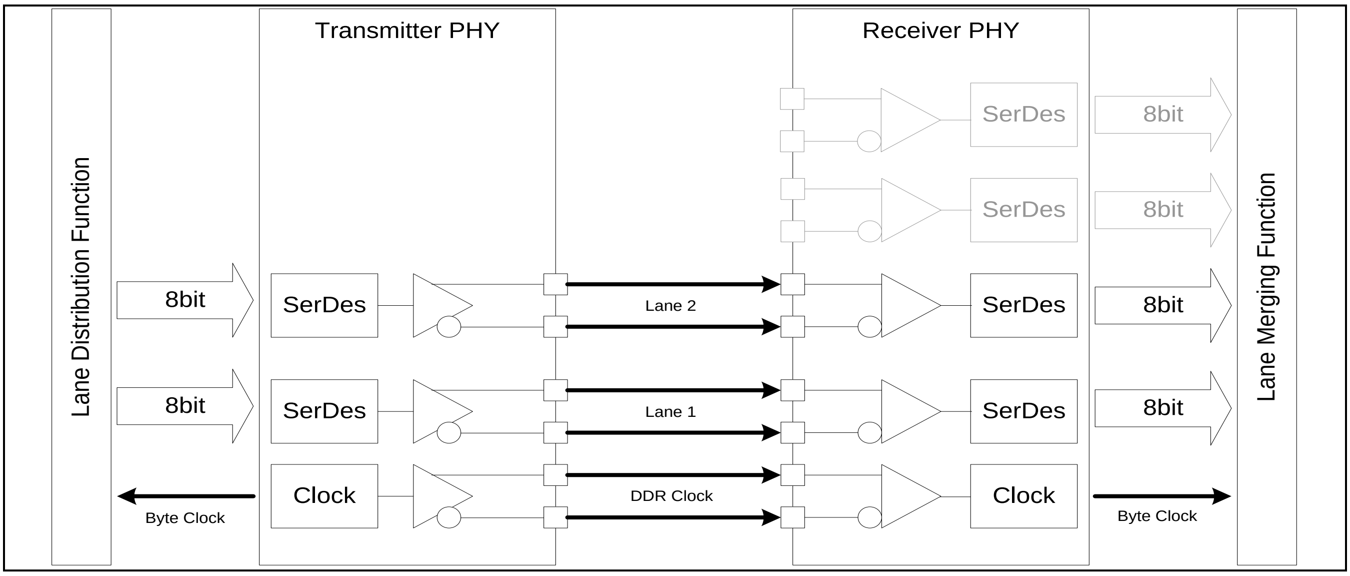


Figure 22 Two Lane Transmitter and Four Lane Receiver Example

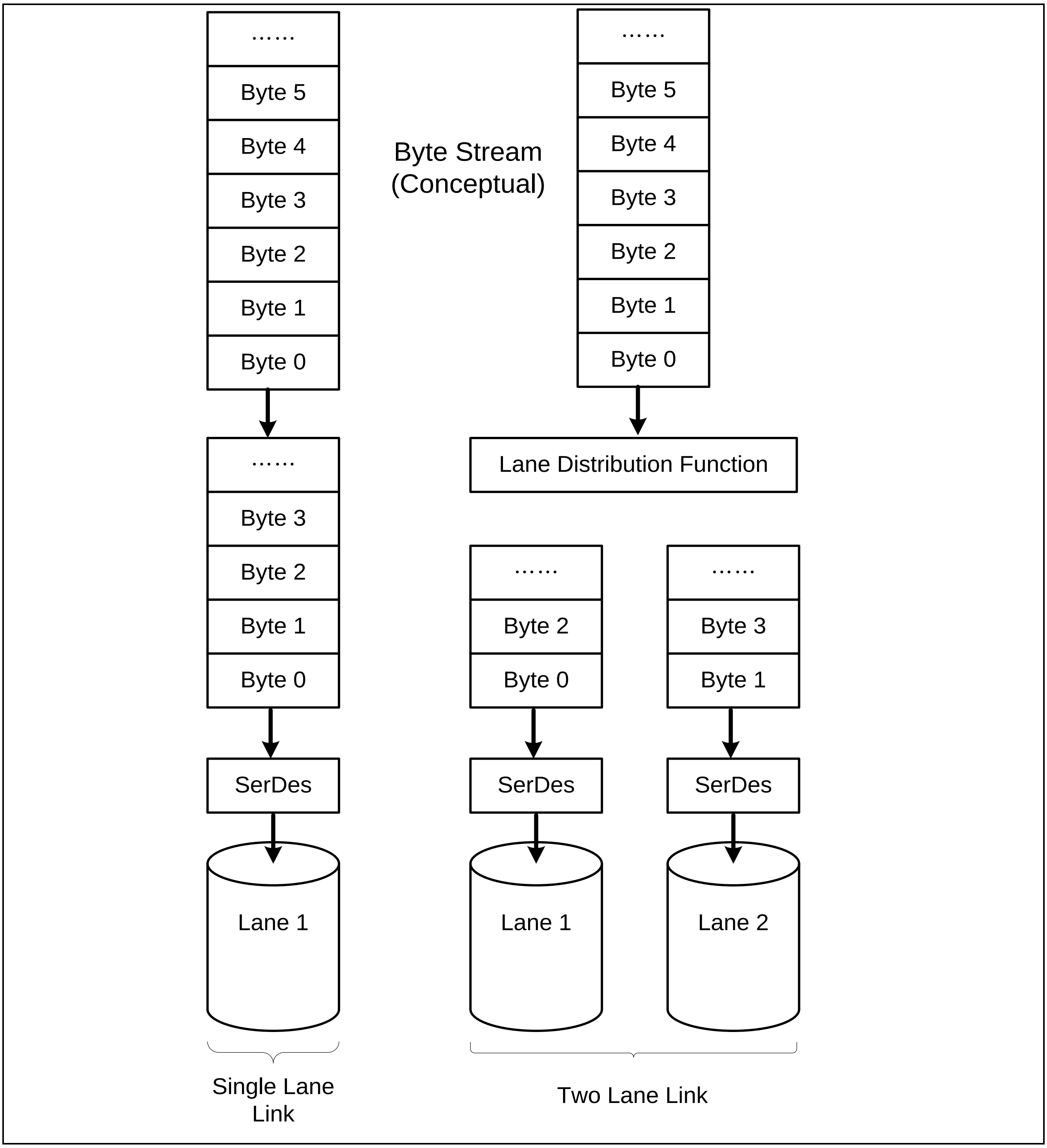


Figure 23 Conceptual Overview of the Lane Merging Function

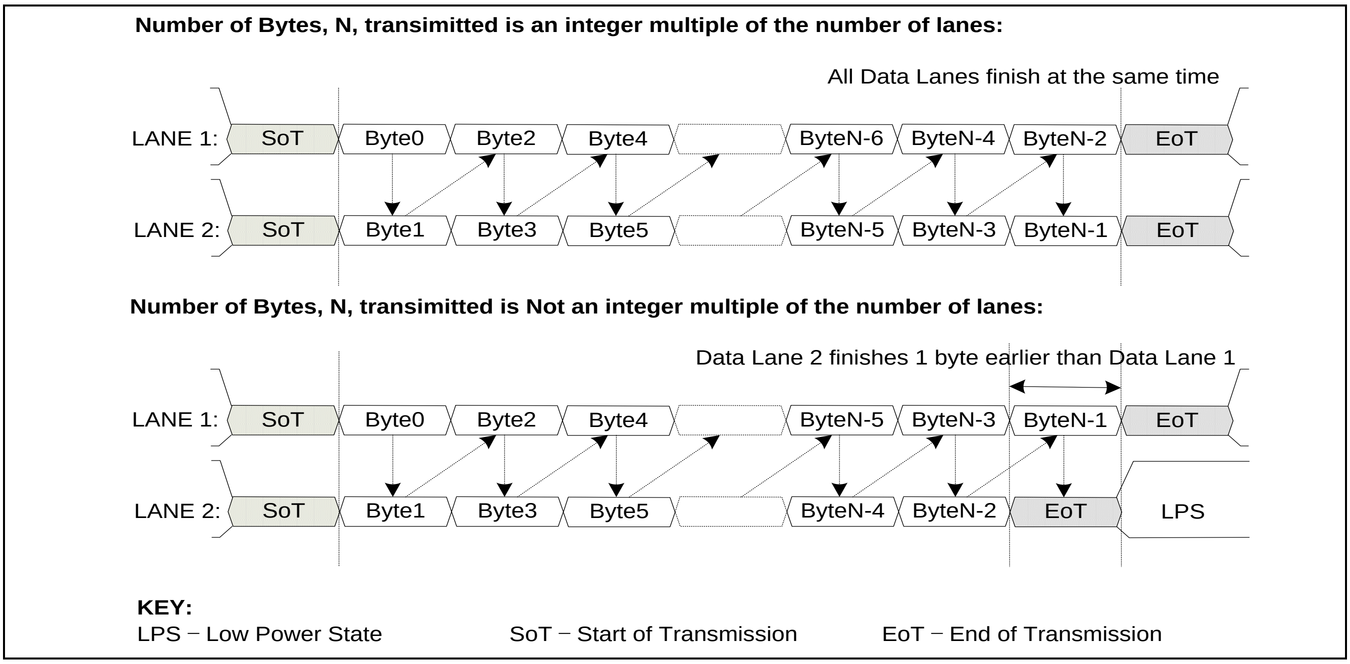


Figure 24 Two Lane Multi-Lane Example

2.7.3.2 Low Level Protocol

The Low Level Protocol (LLP) is a byte orientated, packet based protocol that supports the transport of arbitrary data using Short and Long packet formats. For simplicity, all examples in this section are single Lane configurations.

Low Level Protocol Features:

- Transport of arbitrary data (Payload independent)
- 8-bit word size
- Support for up to four interleaved virtual channels on the same link
- Special packets for frame start, frame end, line start and line end information
- Descriptor for the type, pixel depth and format of the Application Specific Payload data
- 16-bit Checksum Code for error detection

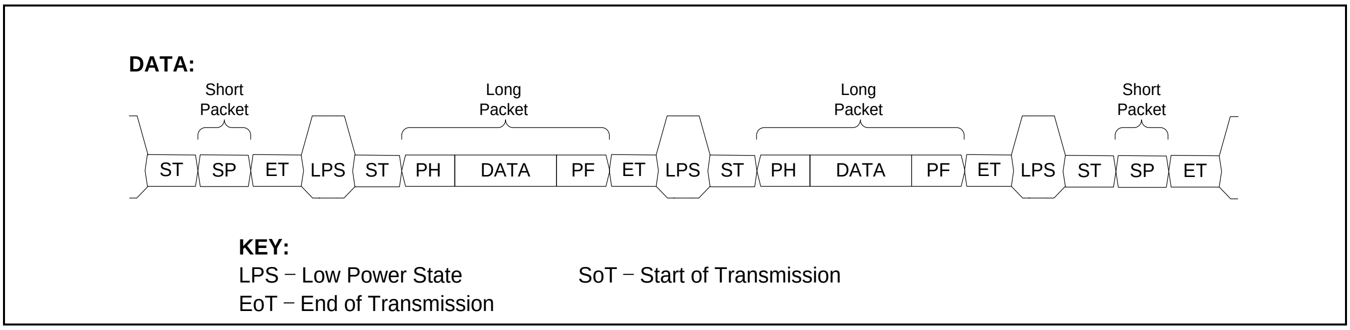


Figure 25 Low Level Protocol Packet Overview

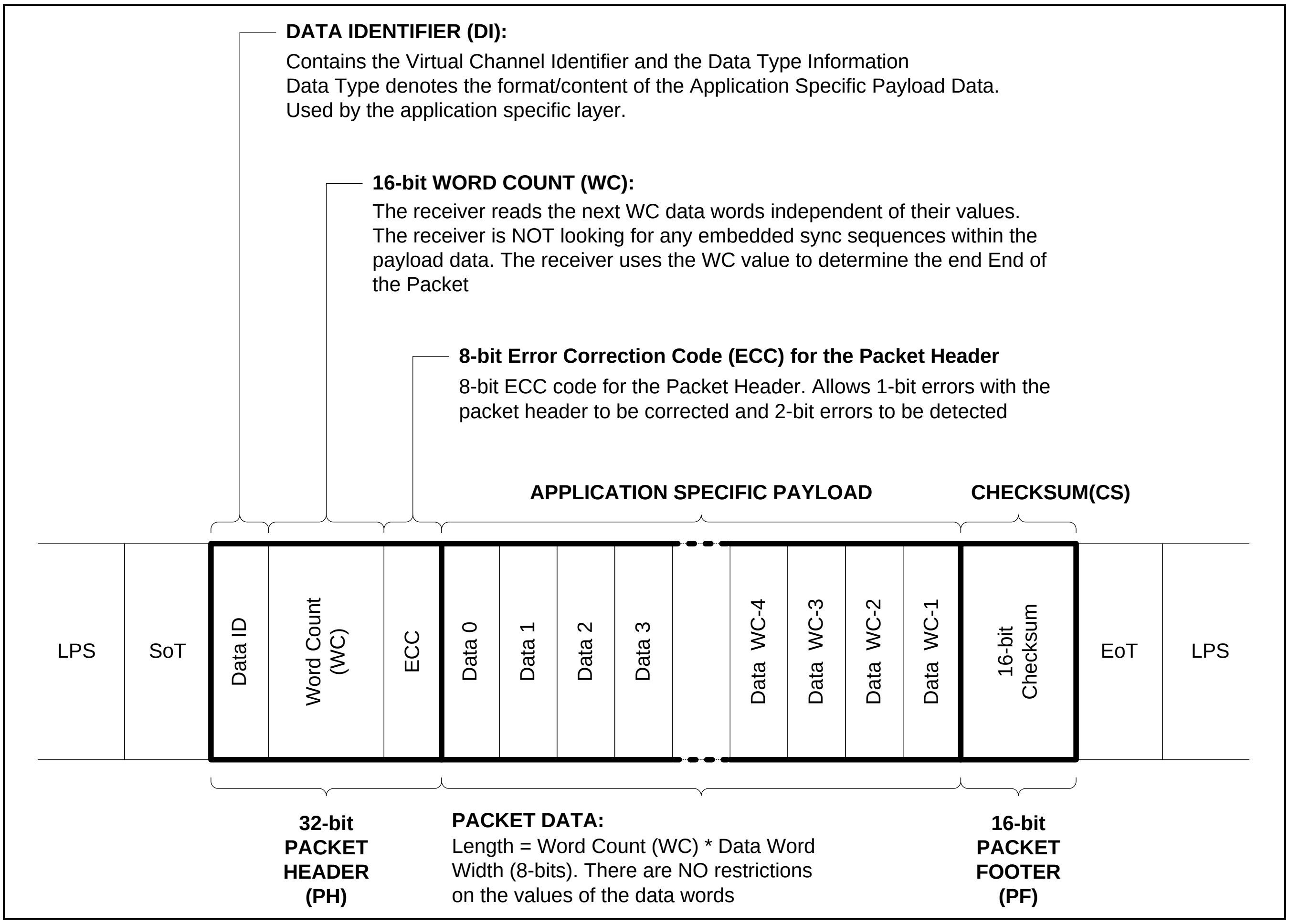


Figure 26 Long Packet Structure

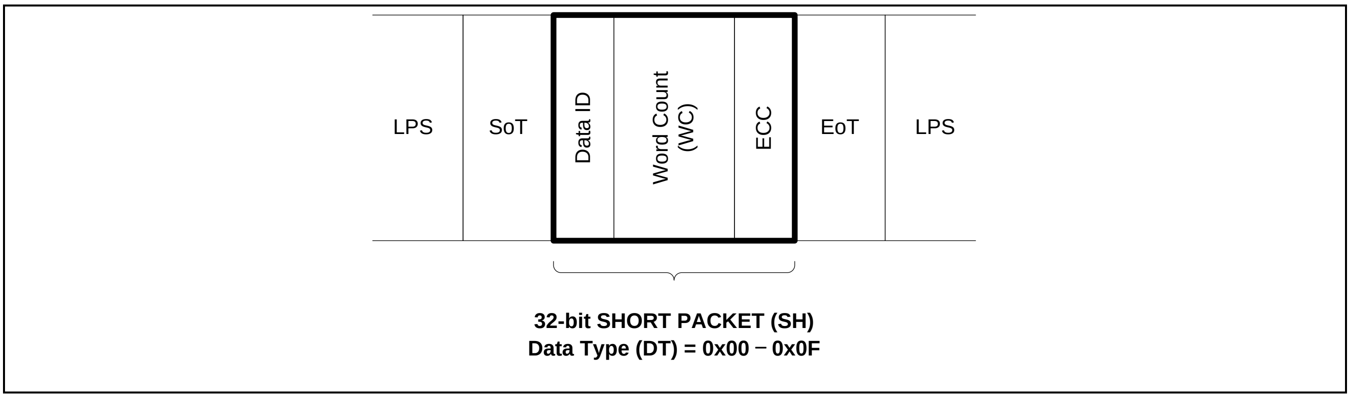


Figure 27 Short Packet Structure

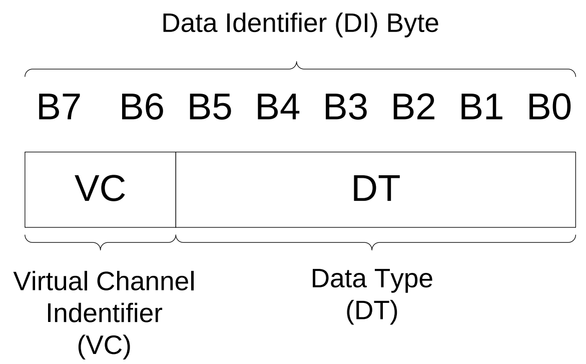


Figure 28 Data Identifier Byte

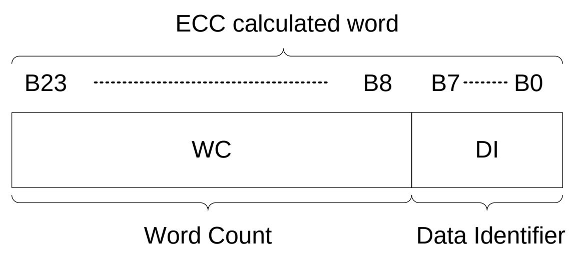


Figure 29 ECC calculated word

2.7.3.3 Data Type (DT)

The data type value specifies the format and content of the payload data. A maximum of sixty-four data types are supported.

Table 2-3 Data Type Classes

Data Type	Description
0x00 – 0x07	Synchronization Short Packet Data Types
0x08 – 0x0F	Generic Short Packet Data Types
0x10 – 0x17	Generic Long Packet Data Types
0x18 – 0x1F	YUV Data
0x20 – 0x27	RGB Data
0x28 – 0x2F	RAW Data
0x30 – 0x37	User Defined Byte-based Data
0x38 – 0x3F	Reserved

2.7.3.4 Synchronization Short Packet Data Type Codes

Short Packet Data Types shall be transmitted using only the Short Packet format.

Table 2-4 Synchronization Short Packet Data Type Codes

Data Type	Description
0x00	Frame Start Code
0x01	Frame End Code
0x02	Line Start Code (Optional)
0x03	Line End Code (Optional)
0x04 – 0x07	Reserved

2.7.3.4.1 Frame Synchronization Packets

Each image frame shall begin with a Frame Start (FS) Packet containing the Frame Start Code. Each image frame shall end with a Frame End (FE) Packet containing the Frame End Code.
For FS and FE synchronization packets the Short Packet Data Field shall contain a 16-bit frame number. This frame number shall be the same for the FS and FE synchronization packets corresponding to a given frame.
The 16-bit frame number, when used, shall always be non-zero to distinguish it from the use-case where frame number is inoperative and remains set to zero.

The behavior of the 16-bit frame number shall be as one of the following

- Frame number is always zero – frame number is inoperative.
- Frame number increments by 1 for every FS packet with the same Virtual Channel and is periodically reset to one e.g. 1, 2, 1, 2, 1, 2, 1, 2 or 1, 2, 3, 4, 1, 2, 3, 4

The frame number must be a non-zero value.

2.7.3.4.2 Line Synchronization Packets

Line synchronization packets are optional. For Line Start (LS) and Line End (LE) synchronization packets the Short Packet Data Field shall contain a 16-bit line number. This line number shall be the same for the LS and LE packets corresponding to a given line. Line numbers are logical line numbers and are not necessarily equal to the physical line numbers. The 16-bit line number, when used, shall always be non-zero to distinguish it from the case where line number is inoperative and remains set to zero.

2.7.3.5 Data Type Interleaving

The Data Type value uniquely defines the data format for that packet of data.

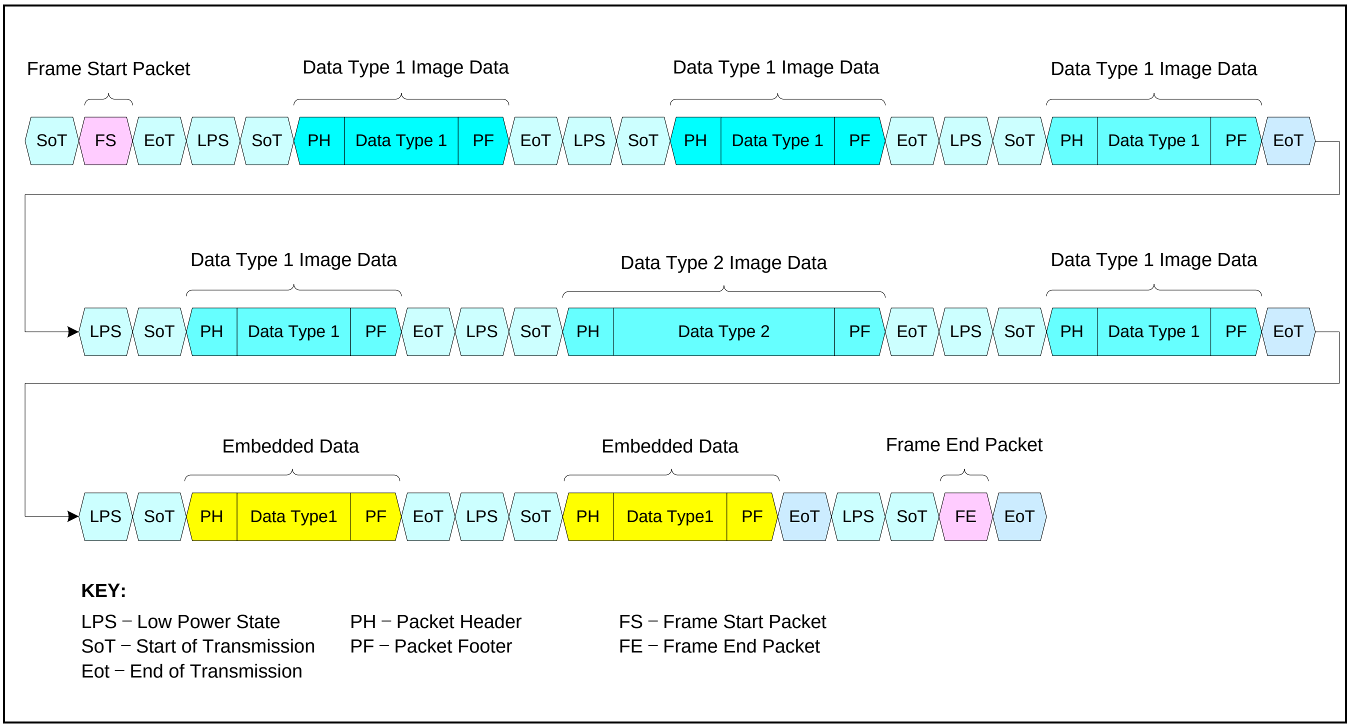


Figure 30 Interleaved Data Transmission Using Data Type Value

All of the packets within the same virtual channel, independent of the Data Type value, share the same frame start/end and line start/end synchronization information. By definition, all of the packets, independent of data type, between a Frame Start and a Frame End packet within the same virtual channel belong to the same frame.

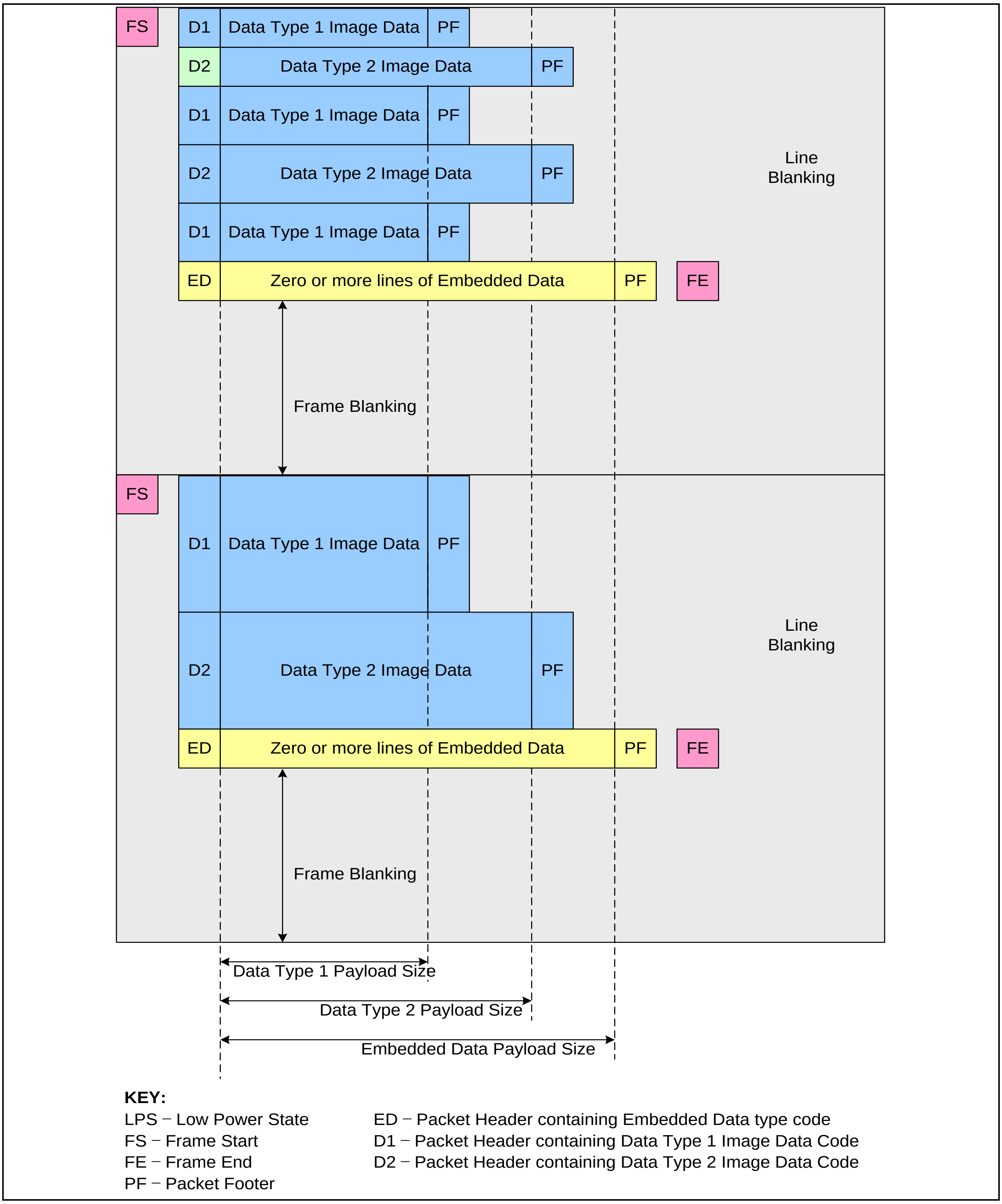
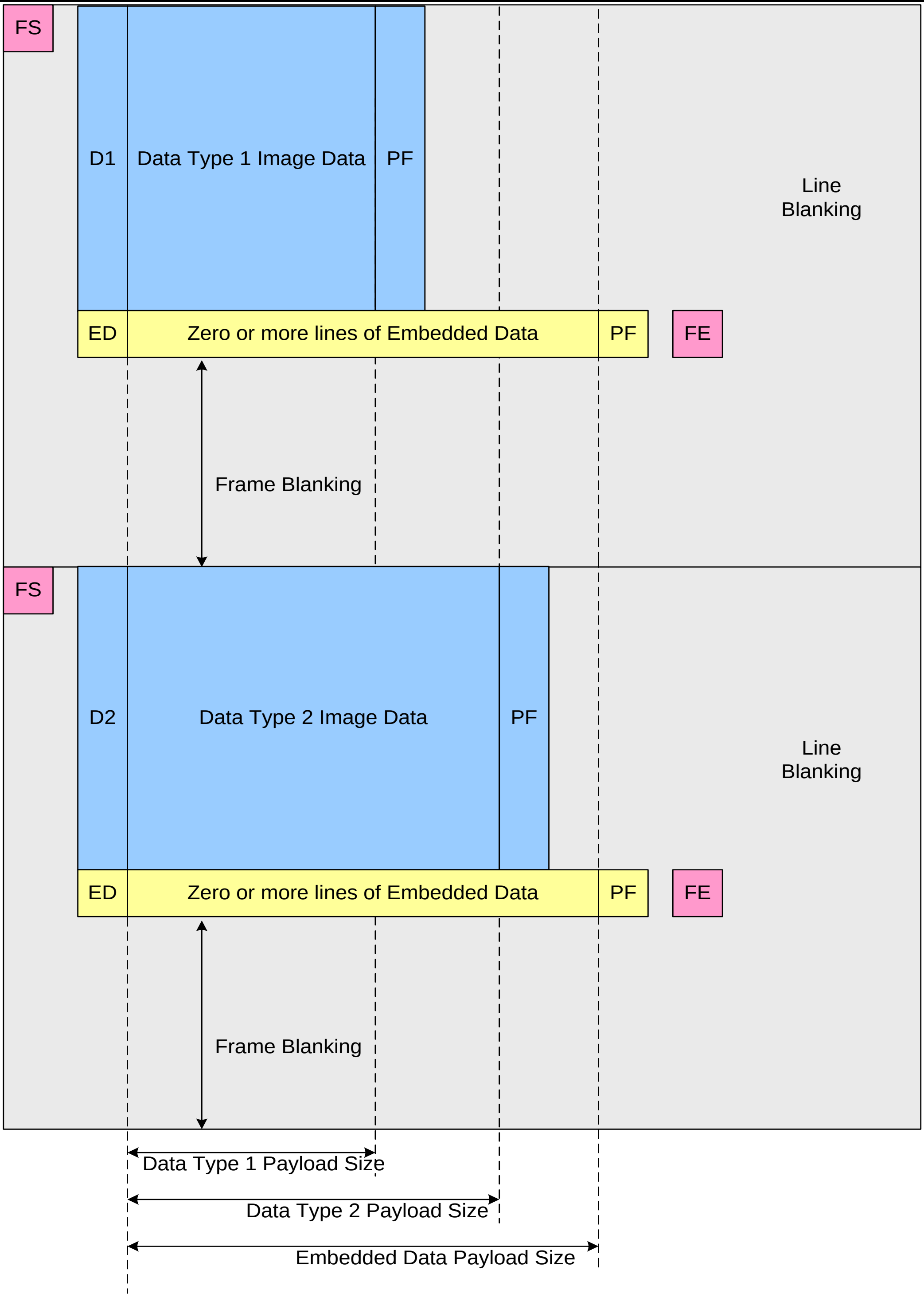


Figure 31 Packet Level Interleaved Data Transmission



KEY:

LPS – Low Power State
FS – Frame Start
FE – Frame End
PF – Packet Footer

ED – Packet Header containing Embedded Data type code
D1 – Packet Header containing Data Type 1 Image Data Code
D2 – Packet Header containing Data Type 2 Image Data Code

Figure 32 Frame Level Interleaved Data Transmission

2.7.3.6 Generic 8-bit Long Packet Data Types

Table 2-5 defines the generic 8-bit Long packet data types.

Table 2-5 Generic 8-bit Long Packet Data Types

Data Type	Description
0x10	Null
0x11	Blanking Data
0x12	Embedded 8-bit non Image Data

2.7.3.6.1 Null and Blanking Data

For both the null and blanking data types the receiver must ignore the content of the packet payload data. A blanking packet differs from a null packet in terms of its significance within a video data stream. A null packet has no meaning whereas the blanking packet may be used, for example, as the blanking lines between frames in an ITU-R BT.656 style video stream.

2.7.3.6.2 Embedded Information

It is possible to embed extra lines containing additional information to the end of each picture frame the If embedded information exists, and then the lines containing the embedded data must use the embedded data code in the data identifier. There may be zero or more line of embedded data at the end of the frame. These lines are termed the frame footer.

2.7.3.7 YUV Image Data

Table 2-6 YUV Image Data Types

Data Type	Description
0x18	YUV420 8-bit(Reserved)
0x1A	Legacy YUV420 8-bit(Reserved)
0x1C	YUV420 8-bit (Chroma Shifted Pixel Sampling)(Reserved)
0x1E	YUV422 8-bit

2.7.3.7.1 YUV422 8-bit (0x1E)

YUV422 8-bit data transmission is performed by transmitting a UYVY sequence. This sequence is illustrated in Figure 33.

Table 2-7 specifies the packet size constraints for YUV422 8-bit packet. The length of each packet must be a multiple of the values in the table.

Table 2-7 YUV422 8-bit Packet Data Size Constraints

Pixels	Bytes	Bits
2	4	32

Bit order in transmission follows the general CSI-2 rule, LSB first. The pixel to byte mapping is illustrated in Figure 34.

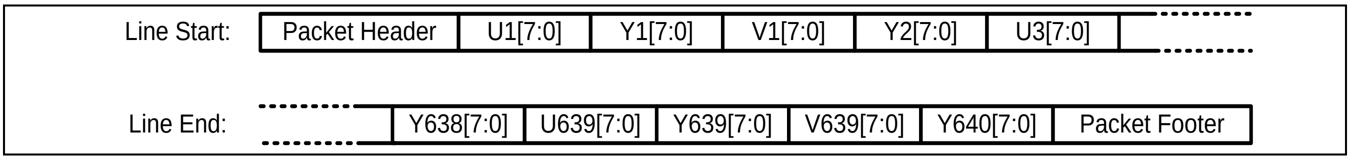


Figure 33 YUV422 8-bit Transmission

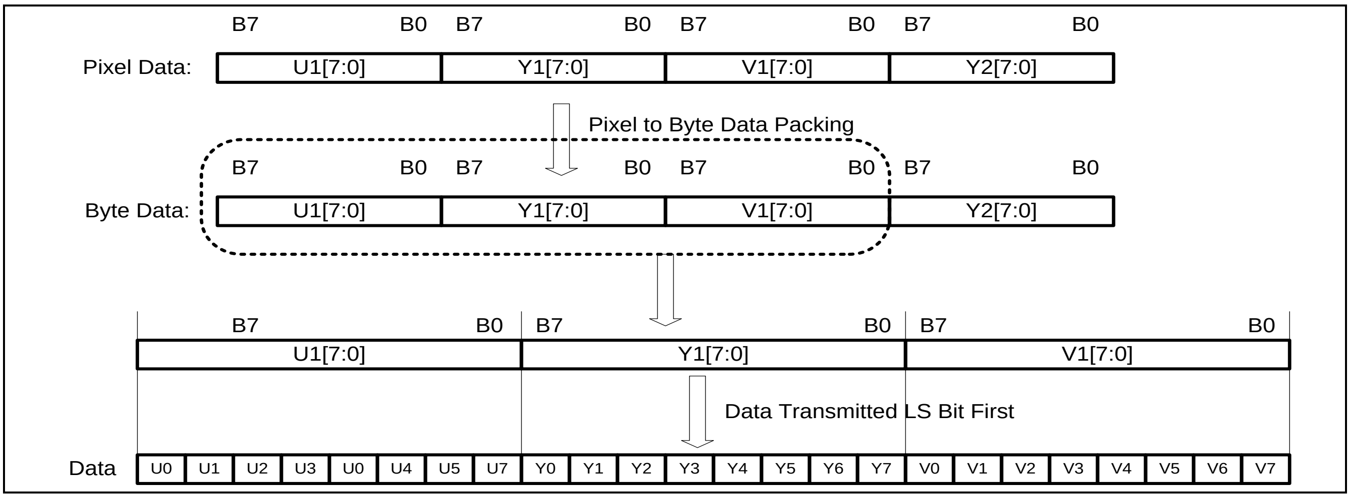


Figure 34 YUV422 8-bit Pixel to Byte Packing Bitwise Illustration

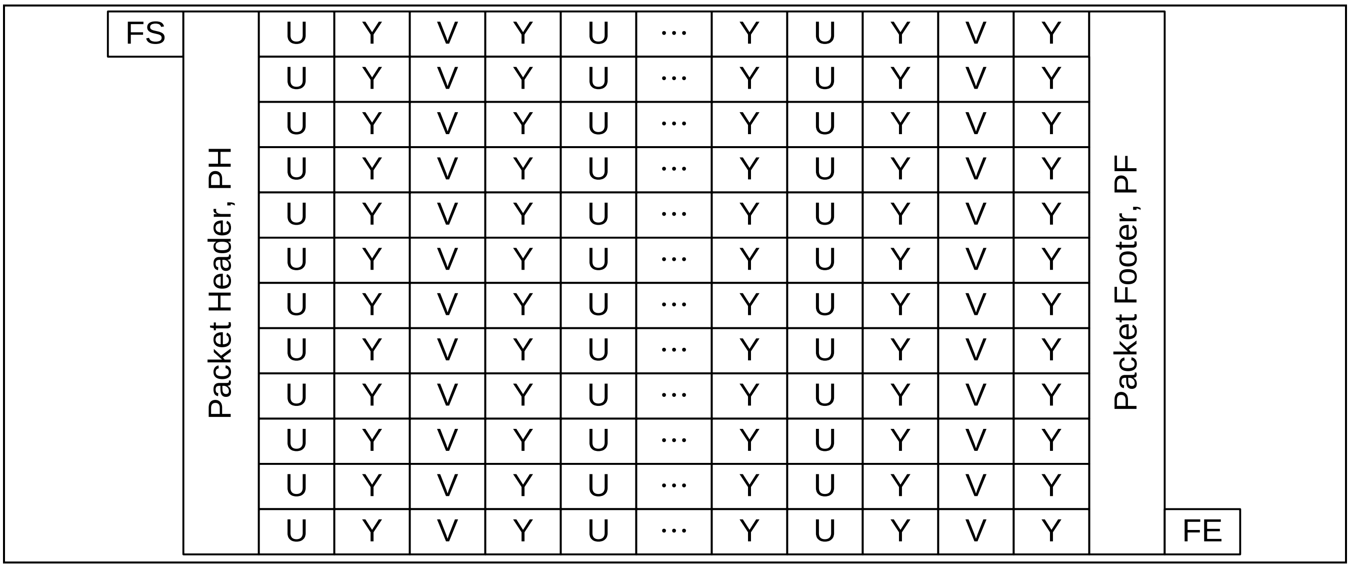


Figure 35 YUV422 8-bit Frame Format

2.7.3.8 RGB Image Data

Table 2-8 RGB Image Data Types

Data Type	Description
0x22	RGB565
0x24	RGB888

2.7.3.8.1 RGB888 (0x24)

RGB888 data transmission is performed by transmitting a BGR byte sequence. This sequence is illustrated in Figure 36. The RGB888 frame format is illustrated in Figure 38. Table 2-9 specifies the packet size constraints for RGB888 packets. The length of each packet must be a multiple of the values in the table.

Table 2-9 RGB888 Packet Data Size Constraints

Pixels	Bytes	Bits
1	3	24

Bit order in transmission follows the general CSI-2 rule, LSB first. The pixel to byte mapping is illustrated in Figure 37.

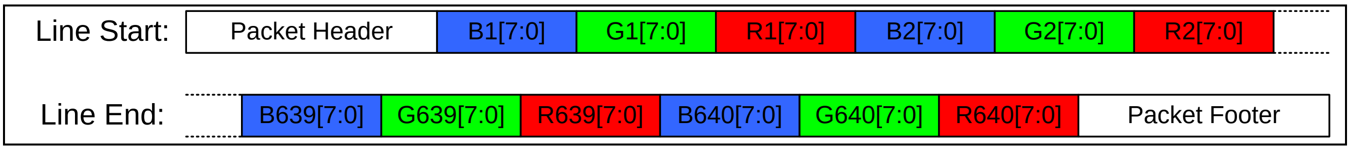


Figure 36 RGB888 Transmission

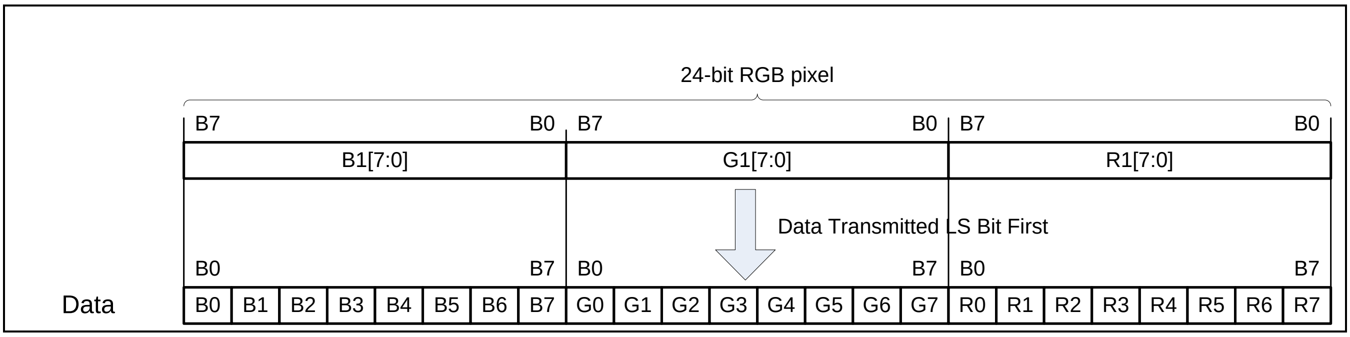


Figure 37 RGB888 Transmission in CSI-2 Bus Bitwise Illustration

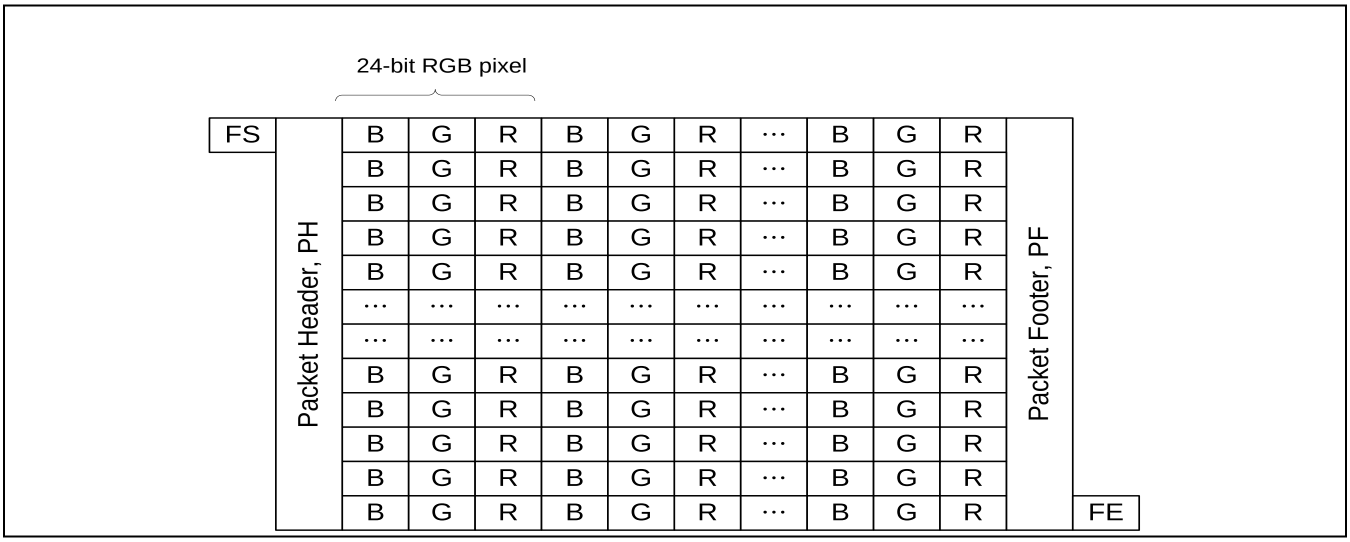


Figure 38 RGB888 Frame Format

2.7.3.8.2 RGB565 (0x22)

RGB565 data transmission is performed by transmitting B0…B4, G0…G5, R0…R4 in a 16-bit sequence. This sequence is illustrated in Figure 39. The frame format for RGB565 is presented in the Figure 41. Table 2-10 specifies the packet size constraints for RGB565 packets. The length of each packet must be a multiple of the values in the table.

Table 2-10 RGB565 Packet Data Size Constraints

Pixels	Bytes	Bits
1	2	16

Bit order in transmission follows the general CSI-2 rule, LSB first. In RGB565 case the length of one data word is 16-bits, not eight bits. The word wise flip is done for 16-bit BGR words i.e. instead of flipping each byte (8-bits), each two bytes (16-bits) are flipped. This is illustrated in Figure 40.

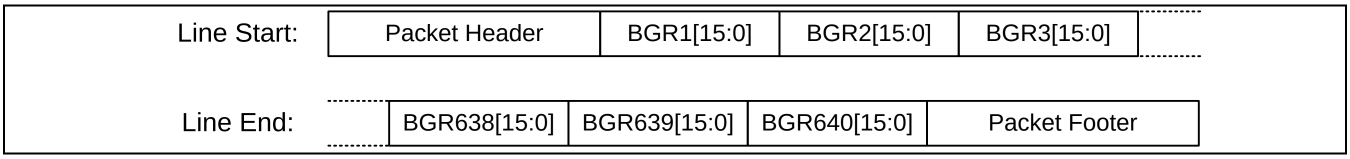


Figure 39 RGB565 Transmission with 16-bit BGR words

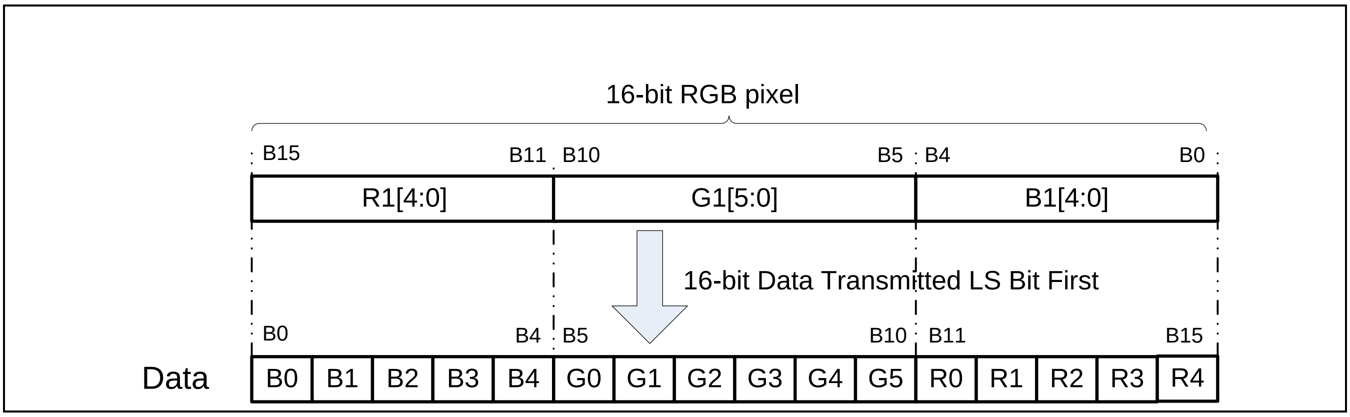


Figure 40 RGB565 Transmission on CSI-2 Bus Bitwise Illustration

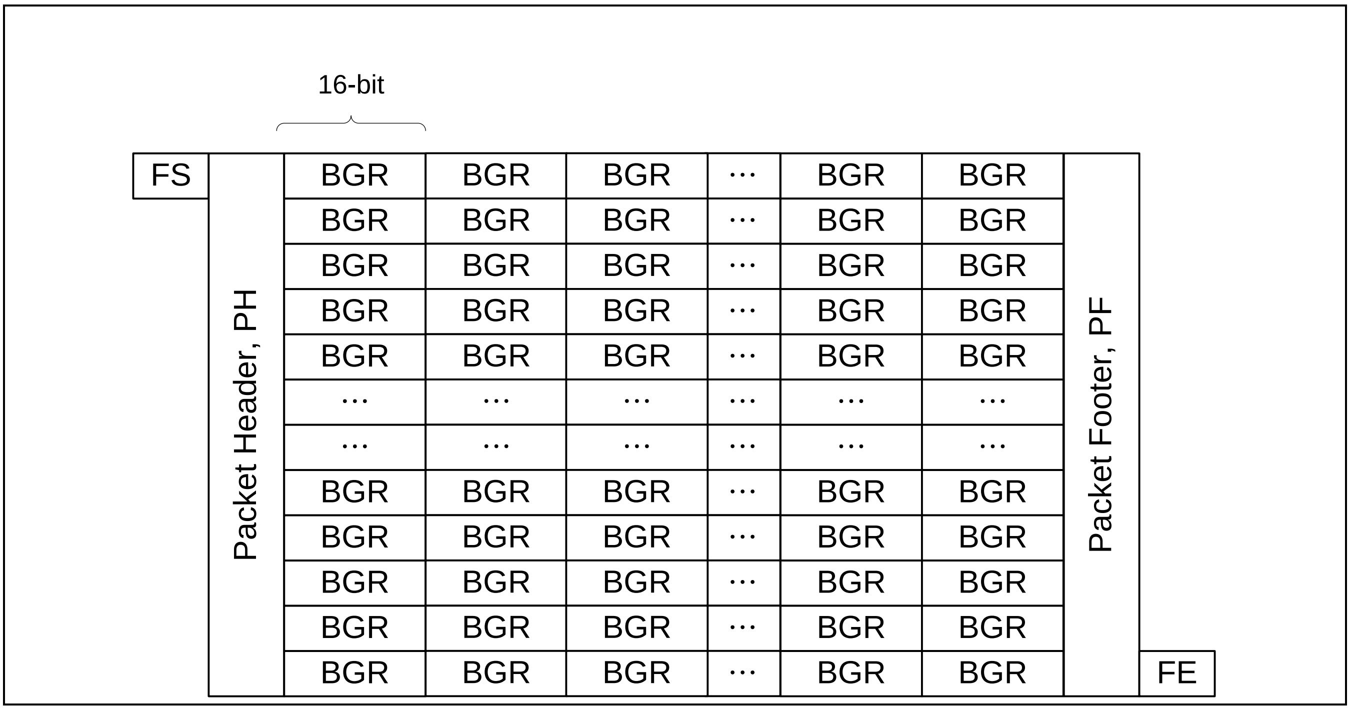


Figure 41 RGB565 Frame format

2.7.3.9 RAW Image Data

Table 2-11 RAW Image Data Types

Data Type	Description
0x2A	RAW8
0x2B	RAW10

2.7.3.9.1 RAW8

The 8-bit Raw data transmission is performed by transmitting the pixel data over a CSI-2 bus. Table 2-12 specifies the packet size constraints for RAW8 packets. The length of each packet must be a multiple of the values in the table.

Table 2-12 RAW8 Packet Data Size Constraints

Pixels	Bytes	Bits
1	1	8

This sequence is illustrated in Figure 42 (VGA case). Bit order in transmission follows the general CSI-2 rule, LSB first.

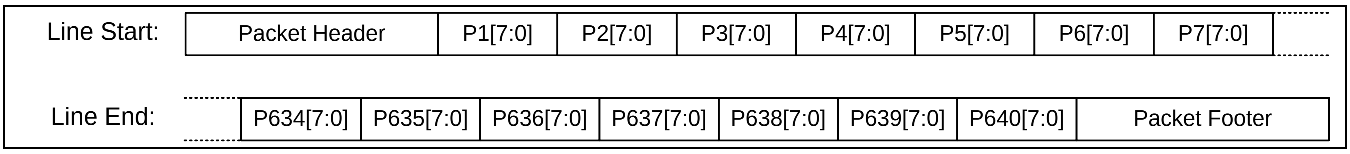


Figure 42 RAW8 Transmission

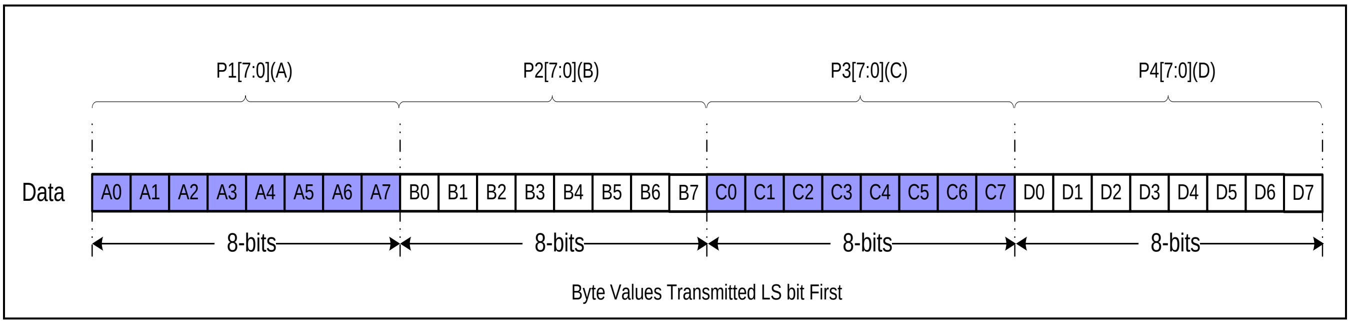


Figure 43 RAW8 Data Transmission on CSI-2 Bus Bitwise Illustration

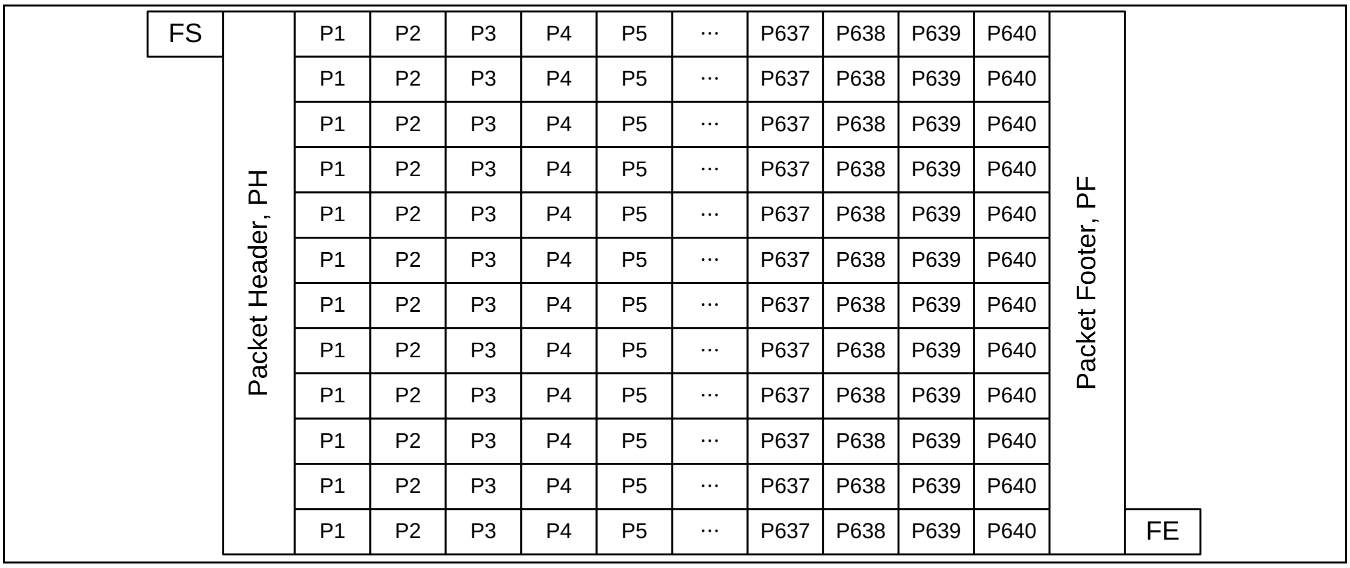


Figure 44 RAW8 Frame Format

2.7.3.9.2 RAW10

The transmission of 10-bit Raw data is accomplished by packing the 10-bit pixel data to look like 8-bit data format. Table 2-13 specifies the packet size constraints for RAW10 packets. The length of each packet must be a multiple of the values in the table.

Table 2-13 Packet Data Size Constraints

Pixels	Bytes	Bits
4	5	40

This sequence is illustrated in Figure 45 (VGA case). Bit order in transmission follows the general CSI-2 rule, LSB first.

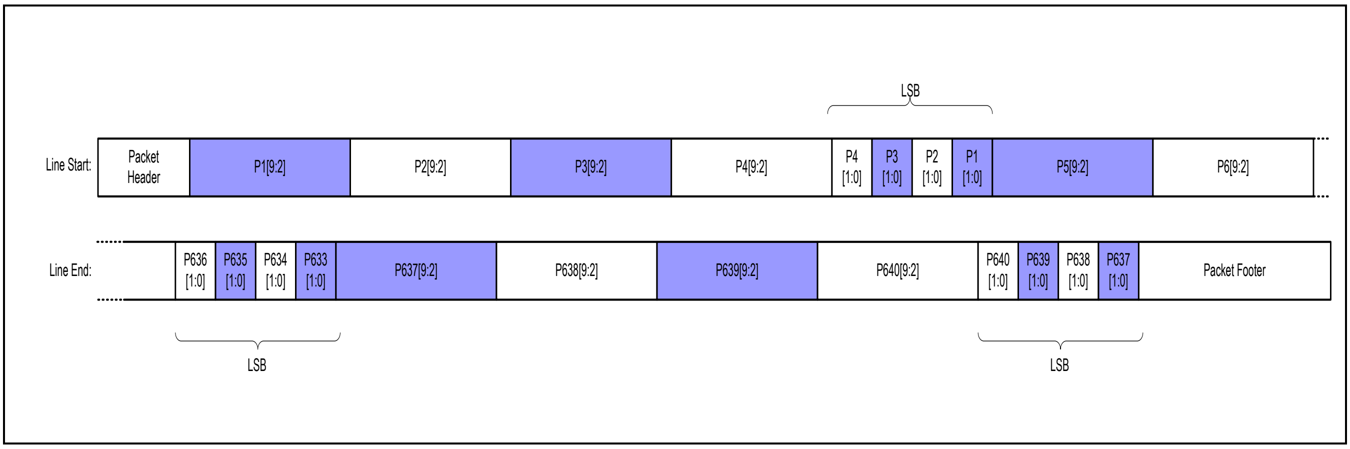


Figure 45 RAW10 Transmission

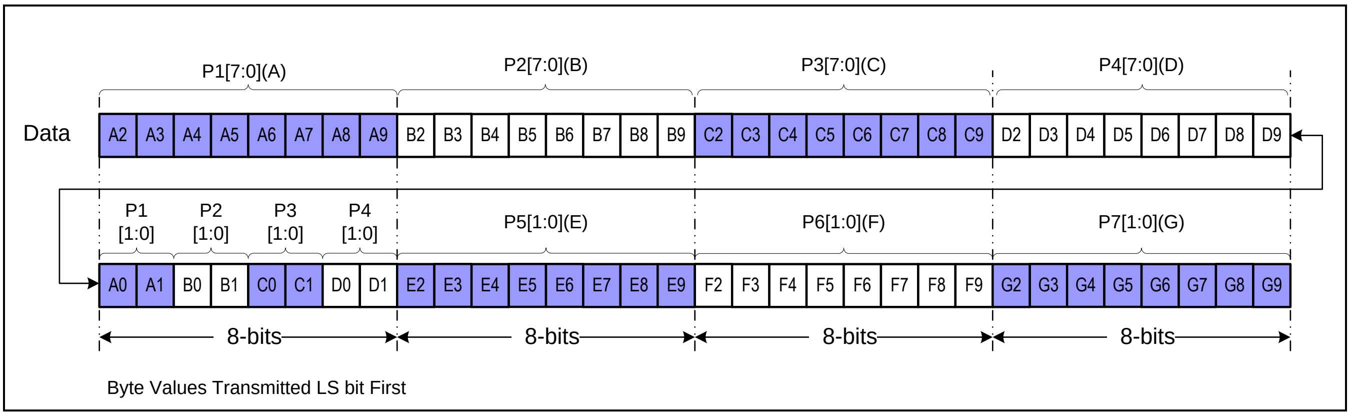


Figure 46 RAW10 Data Transmission on CSI-2 Bus Bitwise Illustration

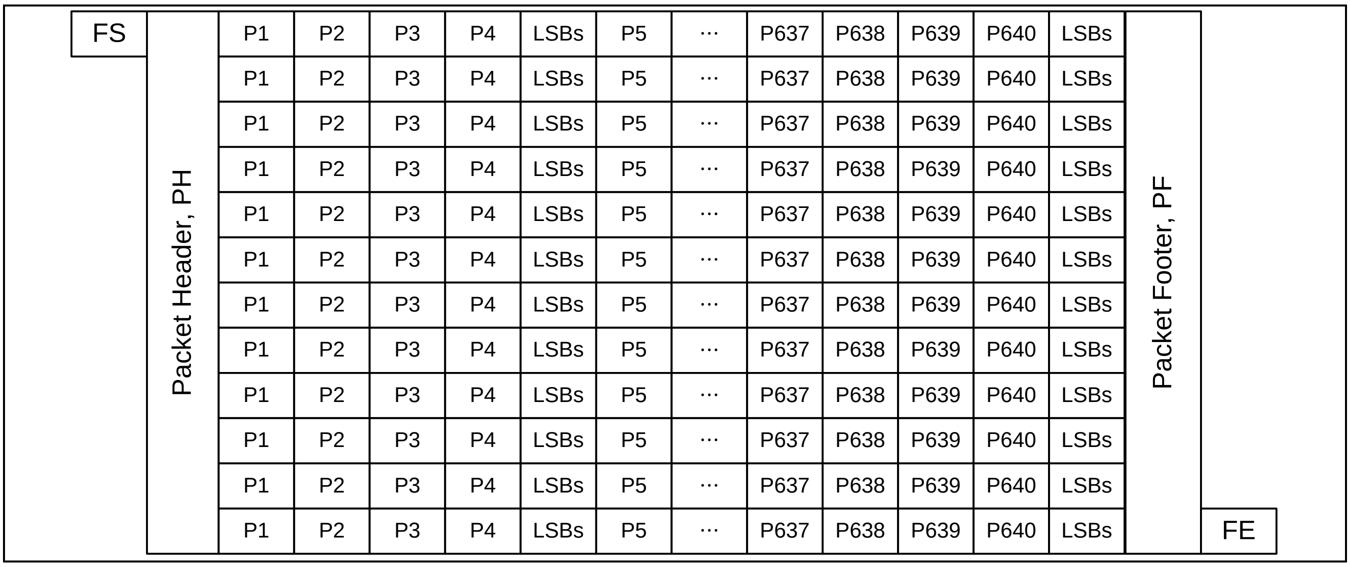


Figure 47 RAW10 Frame Format

2.7.3.10 User Defined Data Formats

The User Defined Data Type values shall be used to transmit arbitrary byte-based data, such as JPEG, over the CSI-2 bus. Bit order in transmission follows the general CSI-2 rule, LSB first.

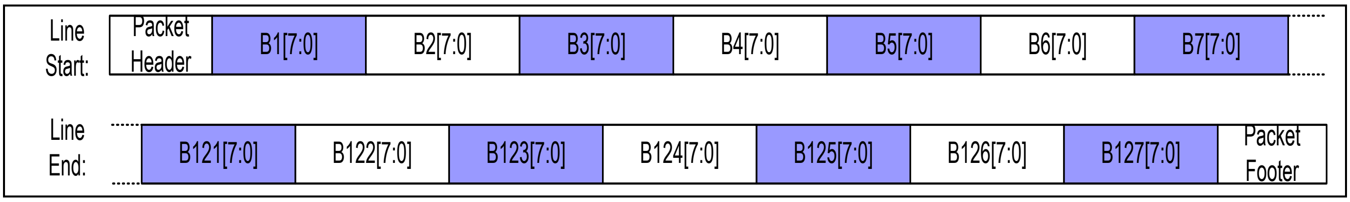


Figure 48 User Defined 8-bit Data (128 Byte Packet)

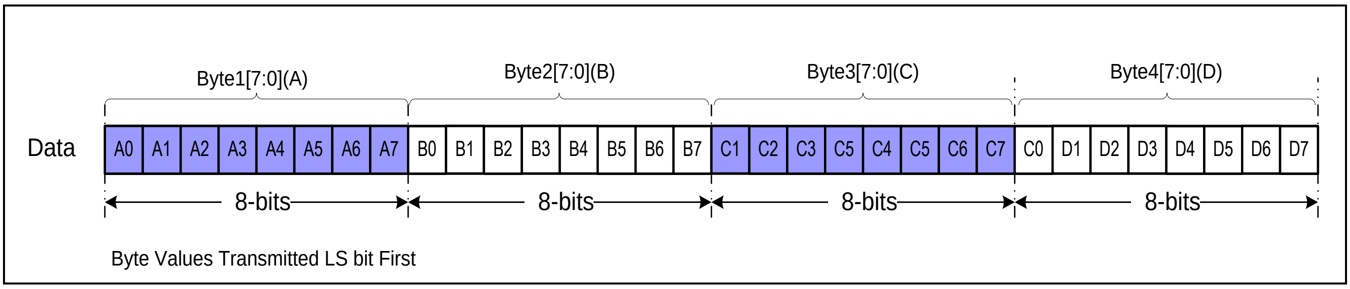


Figure 49 User Defined 8-bit Data Transmission on CSI-2 Bus Bitwise Illustration

The packet data size in bits shall be divisible by 8, i.e. whole number of bytes shall be transmitted.

Table 2-14 defines the User Defined data type codes.

Table 2-14 User Defined 8-bit Data Types

Data Type	Description
0x30	User Defined 8-bit Data Type 1
0x31	User Defined 8-bit Data Type 2
0x32	User Defined 8-bit Data Type 3
0x33	User Defined 8-bit Data Type 4
0x34 – 0x37	Reserved

2.8 CONTROL INTERFACE DESCRIPTION

The I2C interface is a two-wire bi-directional serial bus. Both wires (Serial Clock Line -SCL and Serial Data Line - SDA) are connected to a positive supply via a pull-up resistor, and when the bus is free both lines are high. The output stage of the device must have an open-drain or open collector type IO cell so that a wired-AND function between all devices that are connected on the bus can be performed.

The two-wire serial interface defines several different transmission stages as follows:

- A start bit
- The slave device 7-bit address
- An (No) acknowledge bit coming from slave.
- An 8-bit or 16-bit message (address and/or data).
- A stop bit (or another 8bit or 16bit message in multiple Read/Write access)

The data on the SDA pin must be stable during the high period of the clock (SCL) as shown in the figure below. Only the master may change the data while SCL is high. A high-to-low transition marks a START condition, and a low-to-high a STOP condition.

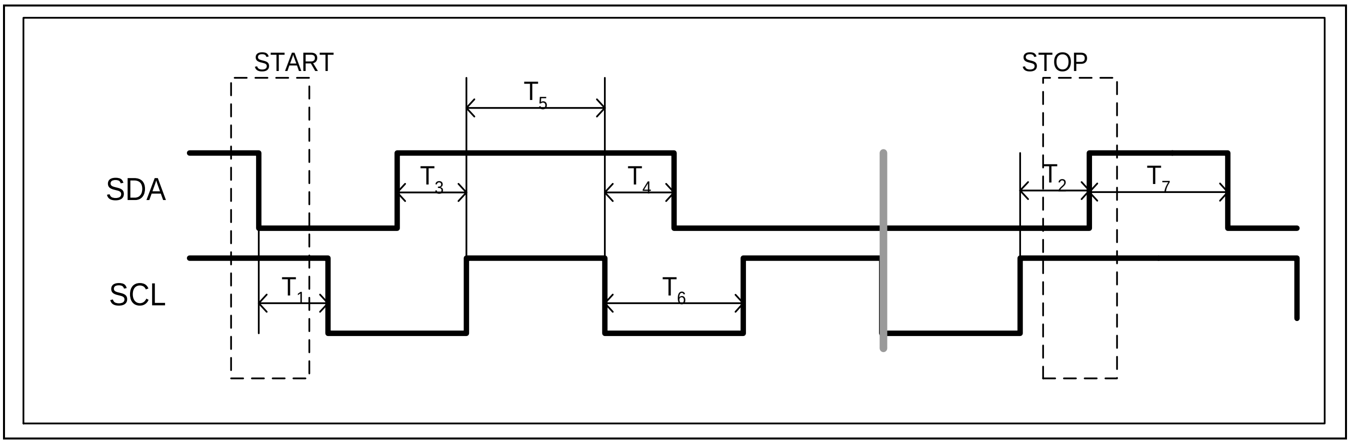


Figure 50 I2C Communication timing chart

Table 2-15 I2C Communication Characteristics

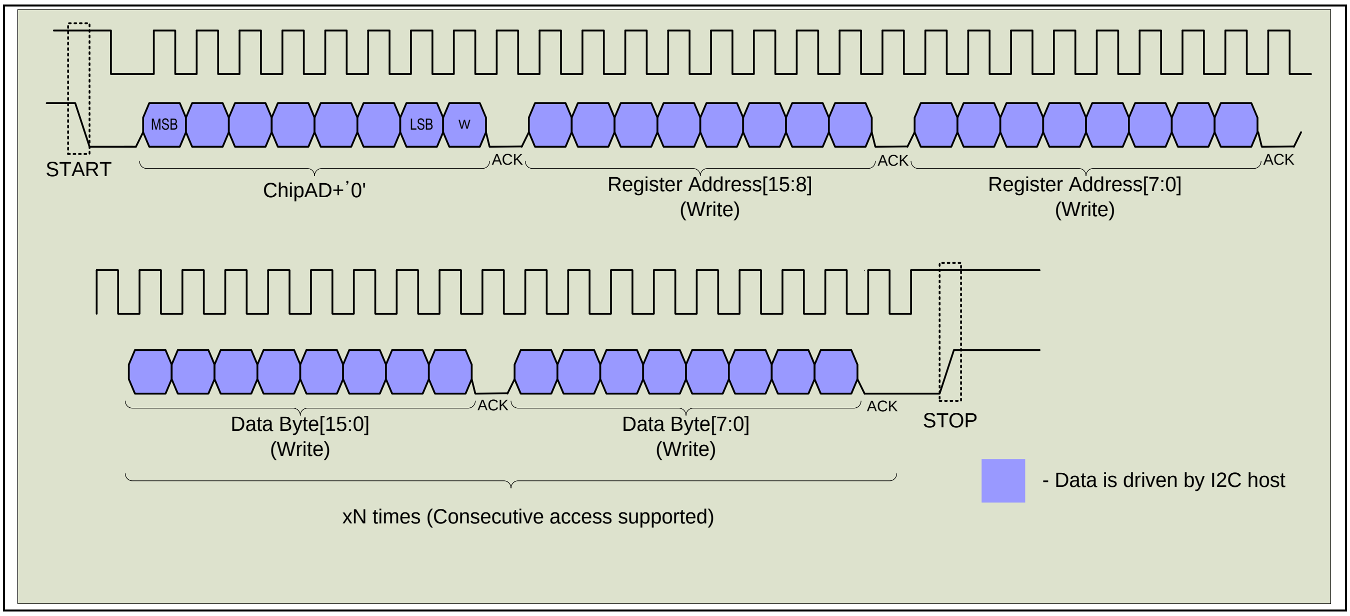
Symbol	Description	Typical Mode		Fast Mode		Units
		Min.	Max	Min.	Max	
	SCL clock frequency	0	100	0	400	kHz
T1	Hold time for START condition	0.4	-	0.6	-	us
T2	Setup time for STOP condition	4.0	-	0.6	-	us
T3	Data setup time	250	-	160	-	ns
T4	Data hold time	0	3.45	0	0.9	us
T5	High period of the SCL clock	4.0	-	0.6	-	us
T6	Low period of the SCL clock	4.7	-	1.3	-	us
T7	Bus free time between STOP and START condition	4.7	-	1.3	-	us

	Rise time for both SDA and SCL signals		1000		300	ns
	Fall time for both SDA and SCL signals		300		300	ns
Cb	Capacitive load for each bus line		400		400	pF

The master device activates a START condition, and sends the first byte of data that contains the 7-bit address, and a direction bit (R/W#, 1 for read, 0 for write). The addressed device answers by pulling down the SDA line as an acknowledge procedure.

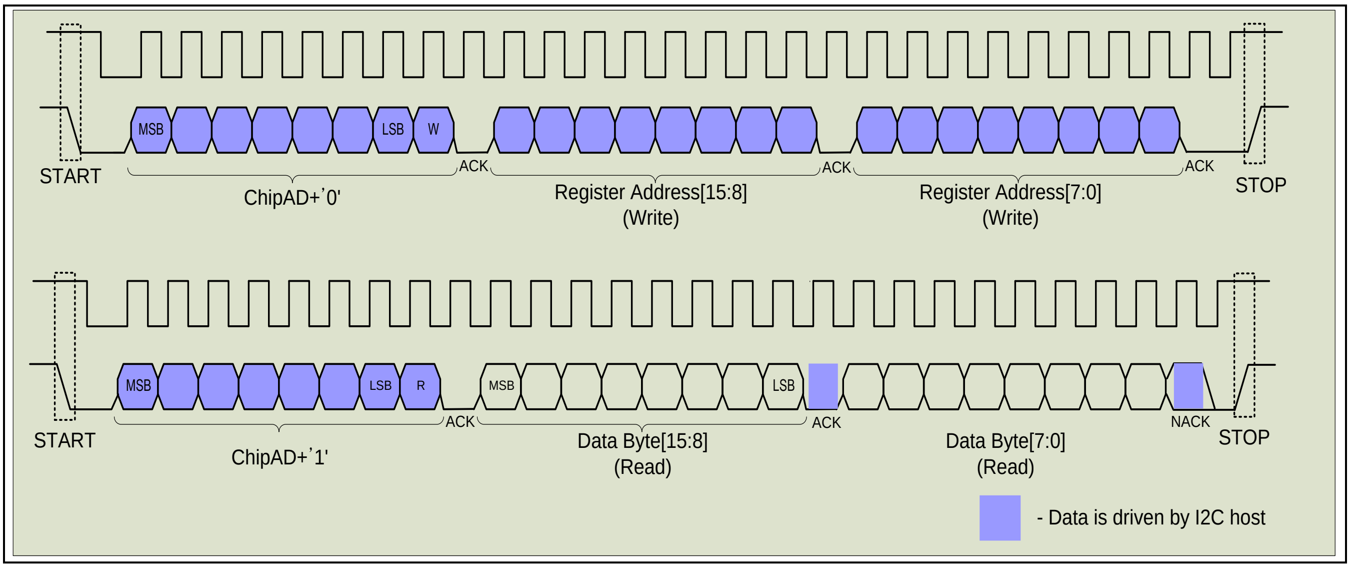
Detailed sequences of read and write data transfers are shown in the figures below.

- The colored boxes represent master-to-slave data transfer.
- The clear boxes represent slave-to-master data transfer.



NOTE: The device address can be changed by pin configuration of IIC_ID, which is described in Pad Description.

Figure 51 Example of I2C Write Timing (16 Address, 2 data bytes)



NOTE: The device address can be changed by pin configuration of IIC_ID, which is described in Pad Description

Figure 52 Example of I2C Single Read Timing (16 Address, 2 data bytes)

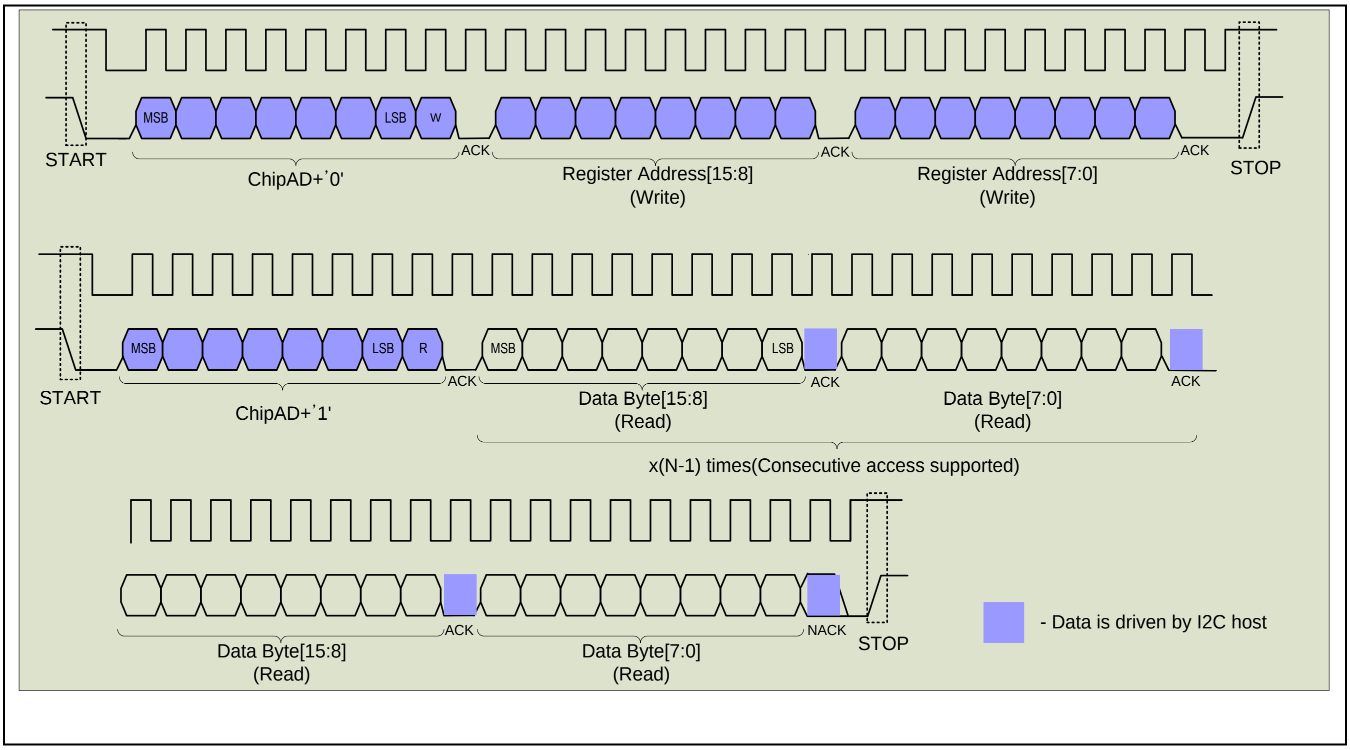


Figure 53 Example of I2C multiple (N) Read Timing (16 Address, 2 data bytes)

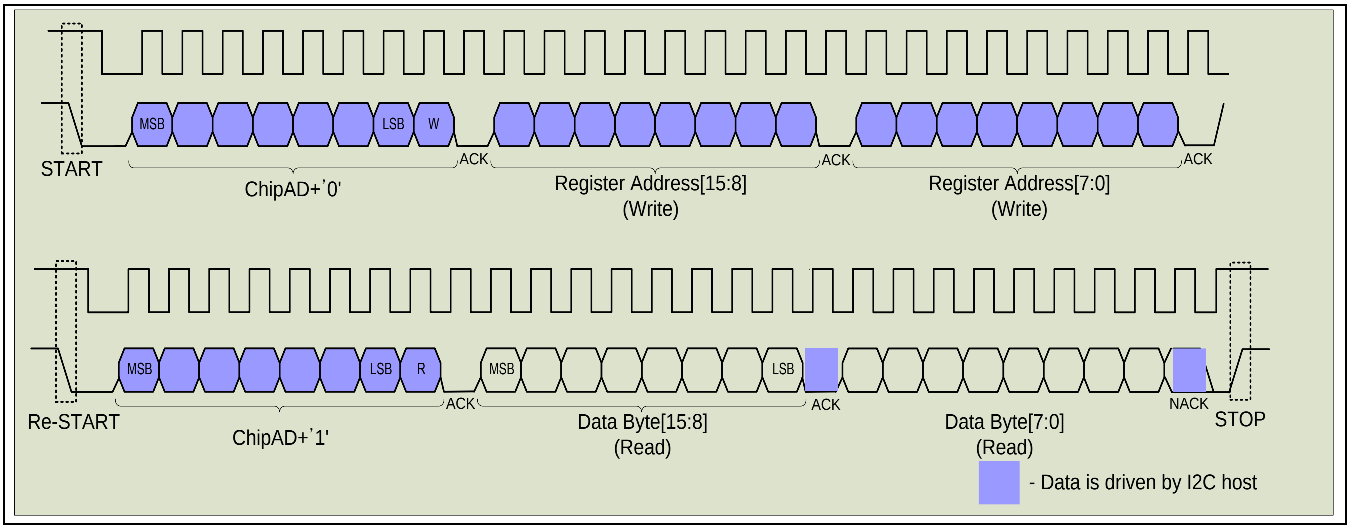


Figure 54 I2C Example of Single Read access with Repeated Start (16 Address, 2 data bytes)

Table 2-16 Device address mapping table

{IIC_ID_1, IIC_ID_0}	Device Address
00	0111_1000b/78h
01	0111_1010b/7Ah
10	0101_1010b/5Ah
11	1010_1100b/ACh

3 FUNCTIONAL DESCRIPTION

3.1 BLOCK DIAGRAM

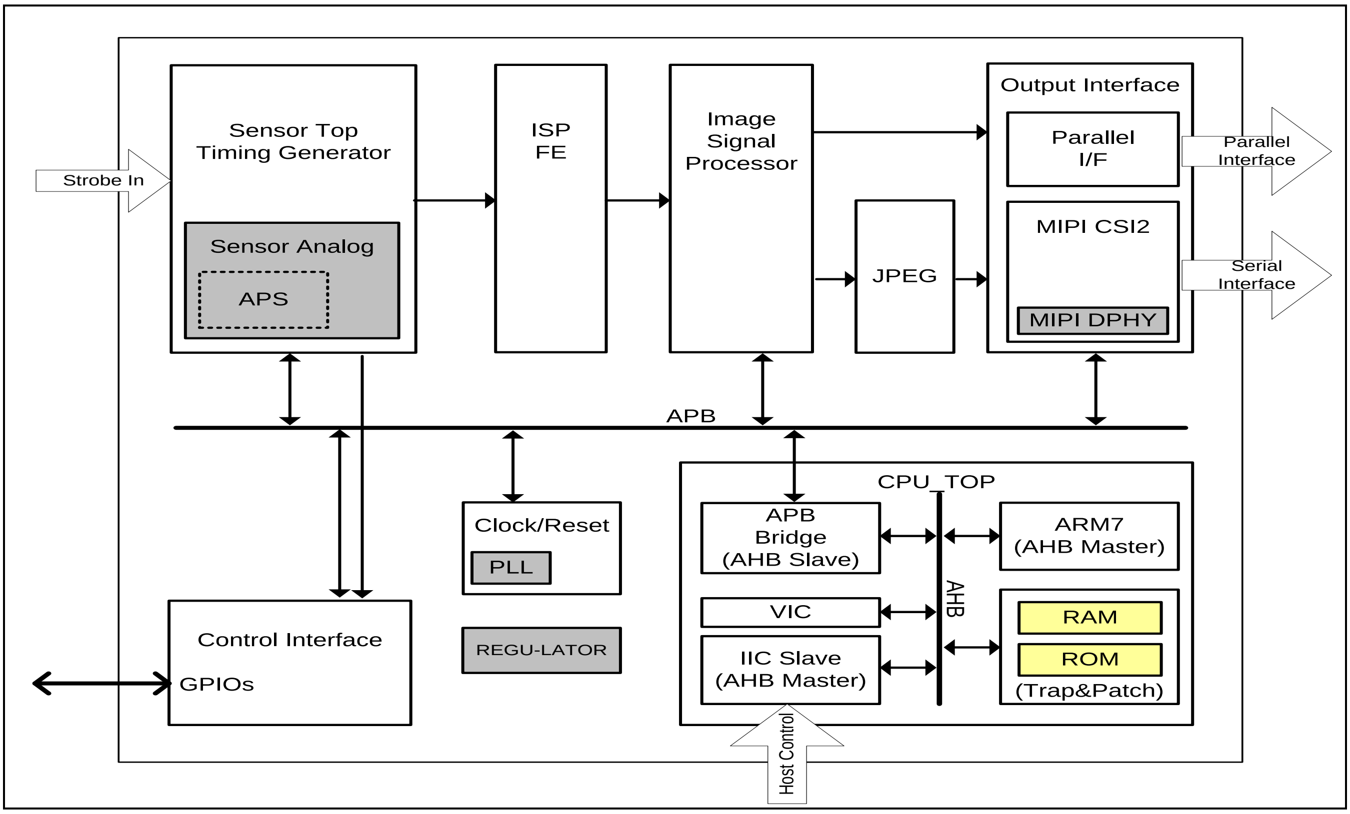


Figure 55 Functional block diagram

3.1.1 ANALOG TO DIGITAL CONVERTER (ADC)

The image sensor has an on-chip ADC. Column parallel ADC scheme is used for low power analog processing.

3.1.1.1 Correlated Double Sampling (CDS)

The analog output signal of each pixel includes some temporal random noise caused by pixel reset and some fixed pattern noise by the in-pixel amplifier offset deviation. To eliminate these noise components, a correlated double sampling (CDS) circuit is used before analogue to digital conversion. The effective signal level of each pixel is measured by the difference between the pre-reset pixel value and its current charged one. Therefore its value is sampled twice during a pixel period-- one for the reference (reset) level detection and the other for actual signal level measurement.

3.1.1.2 Programmable Analogue Gain

The analogue gain of pixel signal could be configured via Gain Control Register. As increasing the signal gain control register, the ADC conversion range slope becomes decreased and its output code value is increased. The gain increased as following equation:

(Channel Gain) = Analog_Gain(reg) / 32

3.1.2 TIMING GENERATOR FUNCTIONS

3.1.2.1 CIS Raw Data Output

GTG supports configurable-bit CIS raw data.

3.1.2.1.1 Pixel Array Addresses

An addressable pixel array is defined as the pixel address range to be read. The addressable pixel array can be assigned anywhere on the pixel array. The addressed region of the pixel array is controlled by x_addr_start, y_addr_start, x_addr_end and y_addr_end register.

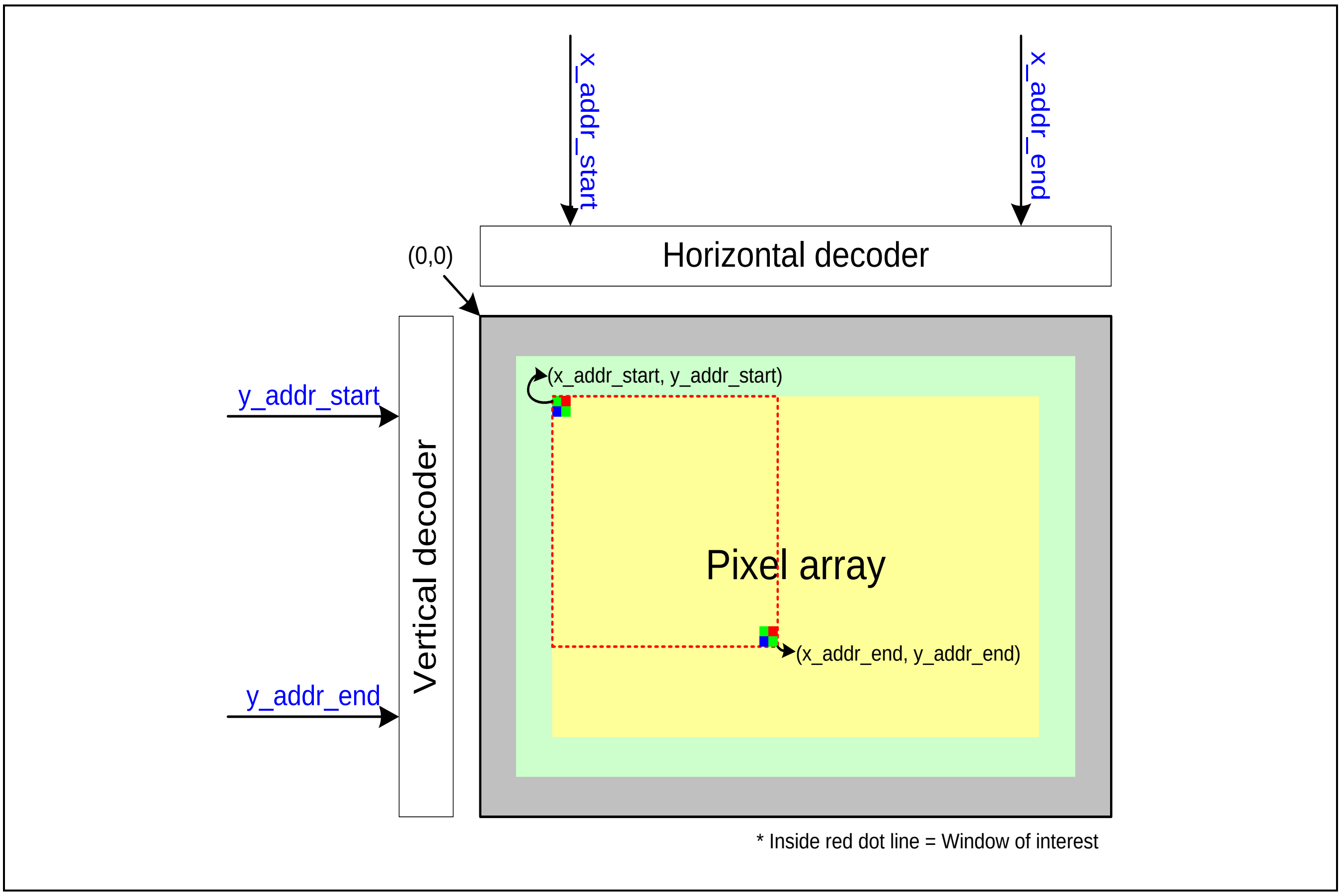


Figure 56 Window of interest of Pixel Array

3.1.2.1.2 Horizontal Mirror/Vertical Flip

The pixel data is normally read out from left to right in the horizontal direction and from top to bottom in the vertical direction. By configuring the mirror/flip mode register, the read-out sequence can optionally be reversed, and pixel data is read out from right to left in horizontal mirror mode and from bottom to top in vertical flip mode. Four possible pixel readout schemes are supported, as illustrated below.

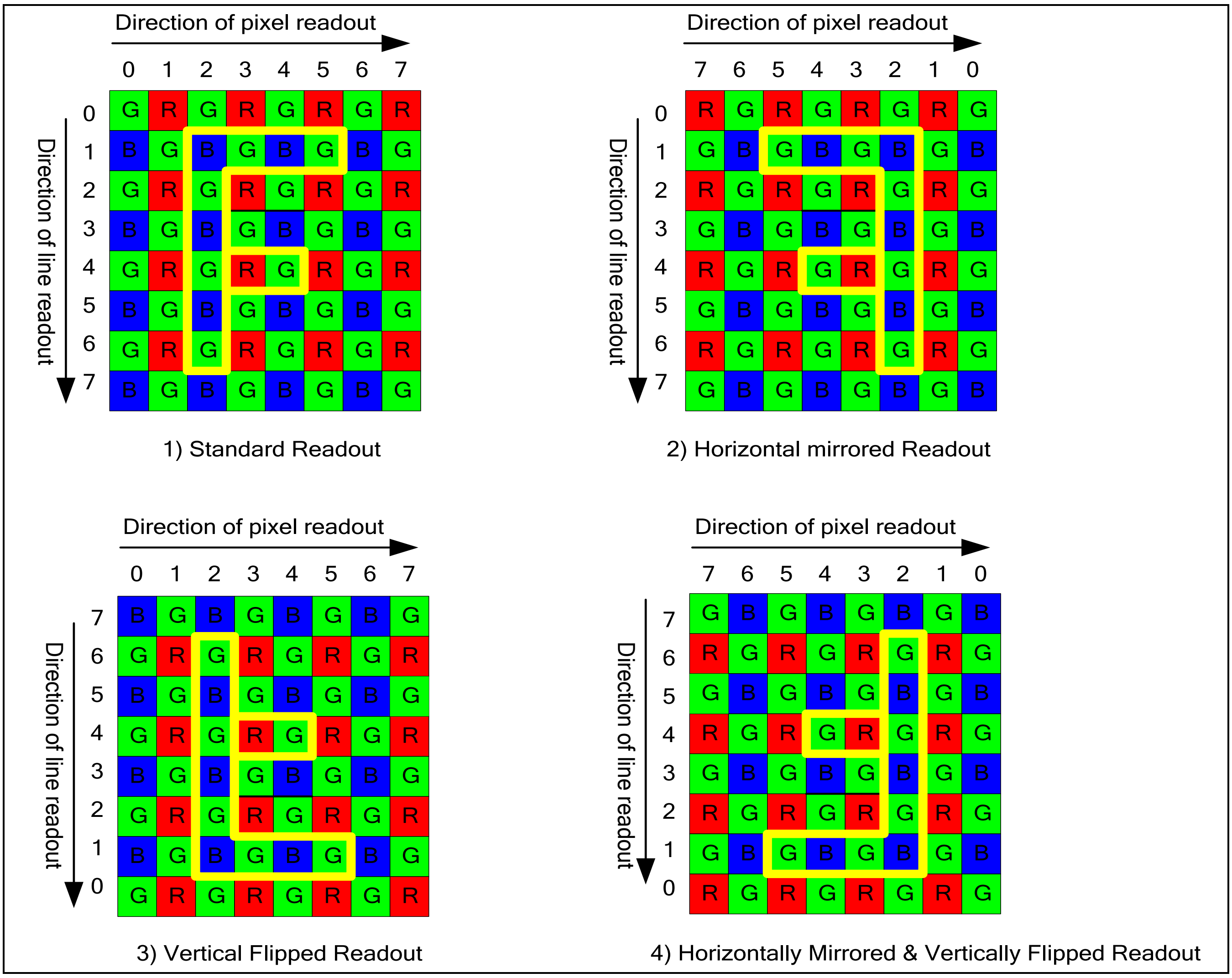


Figure 57 Horizontal Mirror and Vertical Flip

3.1.2.1.3 Sub-Sampled Readout

By programming x and y odd and even increment registers (x_even_inc, x_odd_inc, y_even_inc, y_odd_inc), the sensor can be configured to read out sub-sampled pixel data.

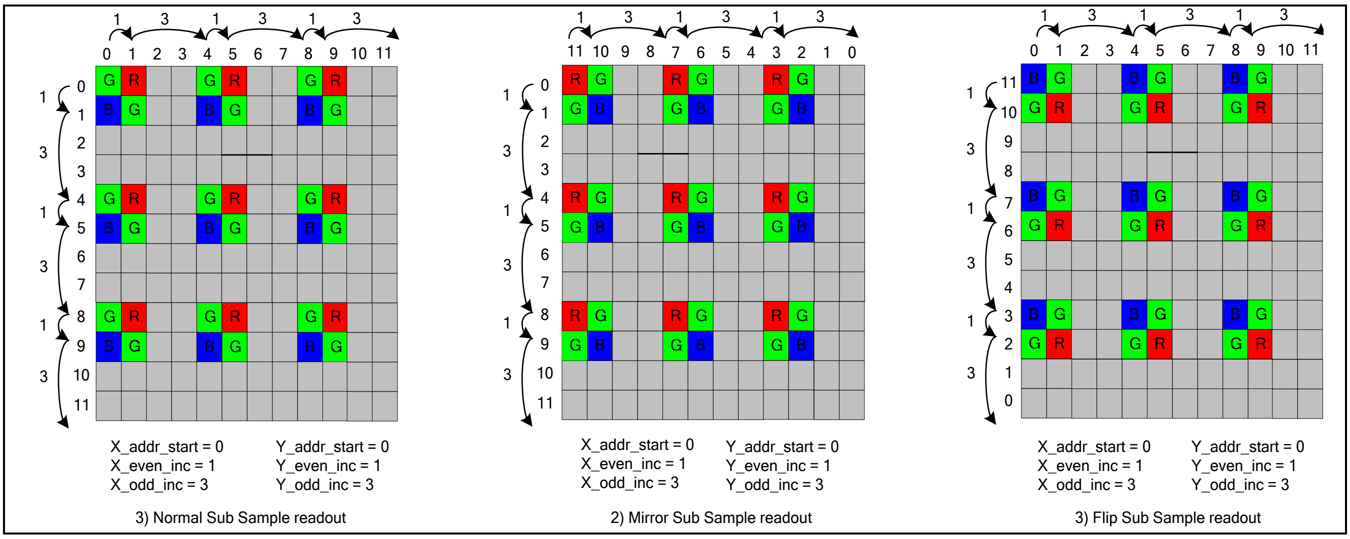


Figure 58 Sub-sampled readout

NOTE: All figure examples are related to the green first array structure. Generic TG also supports red first array structures.

3.1.2.1.4 Frame Rate Control (Virtual Frame)

The line rate and the frame rate can be configured through tailoring the size of the virtual frame. The virtual frame's width and depth are controlled by the line_length_pck and frame_length_lines register. The horizontal and vertical blanking timing (horizontal blanking time: *line_length_pck* – *x_output_size*, vertical blanking time: *frame_length_lines* – *y_output_size*) should meet system requirements.

Frame rate = TGCLK / (frame_length_lines * line_length_pck)

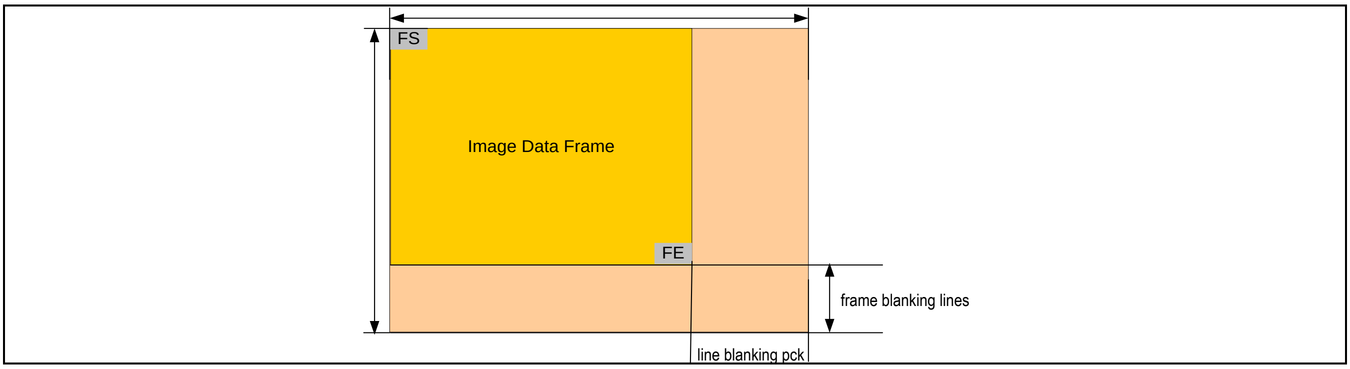


Figure 59 Virtual Frame Timing

3.1.2.1.5 Integration Time Control (Electronic Shutter Control)

The pixel integration time is controlled by the electronic shutter.. During the shutter operation, the amount of time – integration time – is determined by the column Step Integration Time Control Register (fine_integration_time) and the line Step Integration Time Control Register (coarse_integration_time). The total integration time of the sensor module can be calculated using the following equation:

Total_integration_time = {(coarse_integration_time * line_length_pck) + fine_integration_time + const} * pclk period[sec]

3.1.2.2 Adaptive APS Control (AAC)

The AAC function is the pixel power control method for preview mode and low power control.

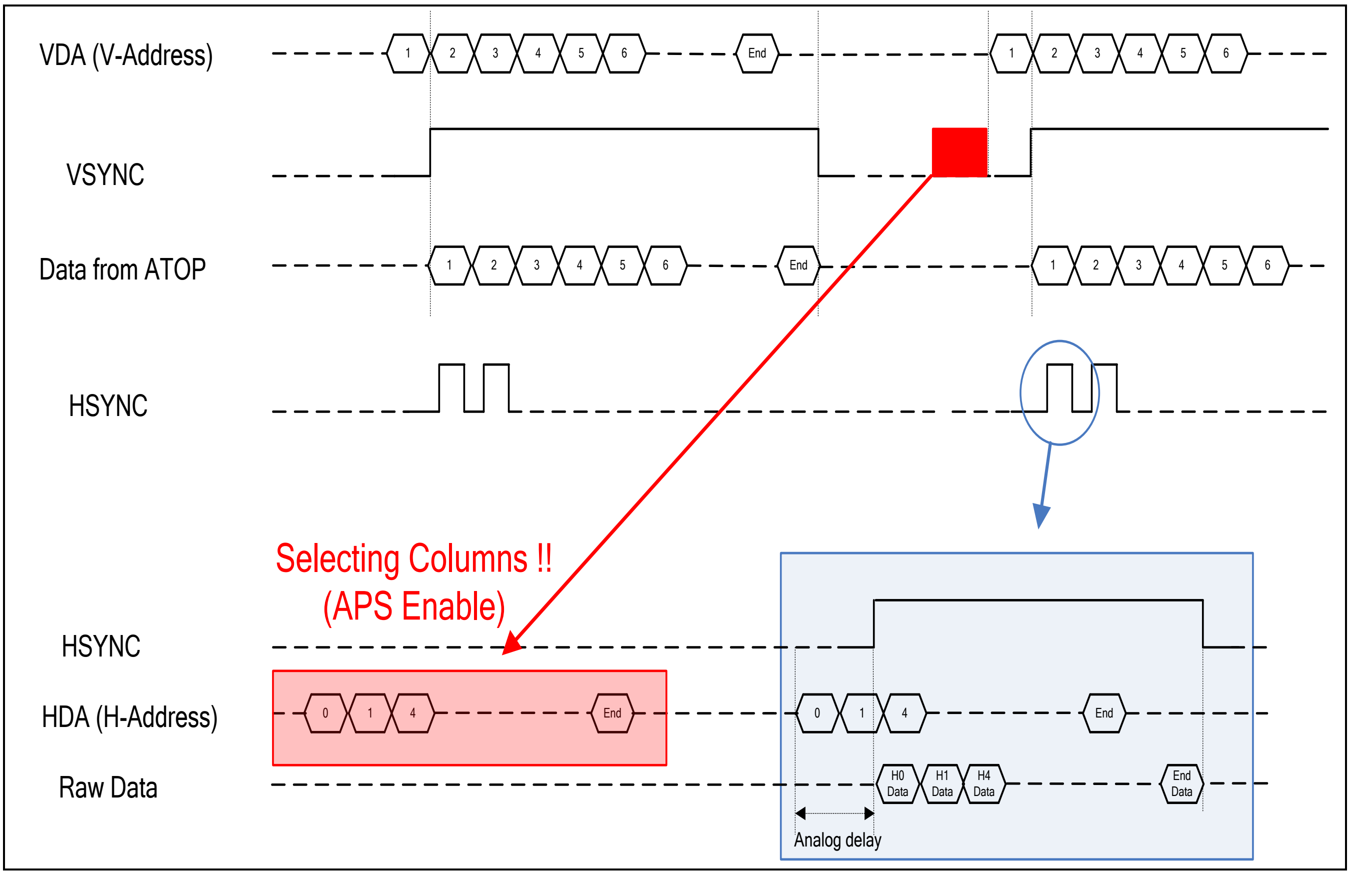


Figure 60 Adaptive APS Control

3.1.3 IMAGE SIGNAL PROCESSOR

3.1.3.1 Auto Exposure (AE)

The embedded AE control algorithm measures the luminance level of selected windows (ROI), and compares it with the AE target value, which is adaptive to the scene type and rendering options. The image brightness is adjusted by controlling analog and digital gains and image sensor integration time. The algorithm has various options to control convergence speed so as to handle illumination changes.

3.1.3.2 Auto White Balance (AWB)

The AWB algorithm adjusts image colors to best match human perceptions by controlling R, G, and B digital gain. The algorithm uses various statistics channels – warm, outdoor, low brightness, general, special color and so on. Each statistics channel applies a distinctive filter on normalized r and b plane and the filtered data are used for illuminant estimation. The algorithm has also a scene type detector which improves the accuracy of the illuminant estimation.

3.1.3.3 Auto Focus (AF)

The auto-focus algorithm analyzes sharpness data gathered from the image, and determines the direction and distance for the lens to move in order to achieve a focused image. Movement commands are sent to a lens actuator driver. Special treatments are applied to saturated image areas. Both automatic and manual operation modes are supported. During a still image capture, the focus is adjusted further to an optimal location following a shutter button half-press. Once achieved, the optimal focus is locked and additional information regarding the confidence rate of the AF algorithm convergence is also passed to the host processor. In the manual mode, the lens position may be controlled by the user. The auto-focus algorithm could issue direct commands to an actuator driver IC via I2C, PWM or stepping-motor interfaces. Options for searching (Full/Peak-Detection, Global/Local, Coarse/Fine and so on) and device-dependant actuator characteristics compensation are also implemented.

3.1.3.4 Auto Flicker Correction

Flickers may occur when the sensor integration time is not an integral multiple of the half cycle of the electrical supply of the predominant illumination. For example, under a 50Hz or 60Hz fluorescent lamp, flicker could appear if the integration time is smaller than 1/100 or 1/120, respectively. The algorithm can detect the frequency of the illumination and adjust the integration time automatically and hence avoid the flicker from appearing.

3.1.3.5 Lens Shading Correction

Two complimentary methods of shading correction are used– one uses parabolic shading compensation, and the other one applies a grid model to remove residual effects. Shading correction is also adaptive to illuminations.

3.1.3.6 Color Interpolation

RGB values at each pixel location of the Bayer plane are derived from a group of neighboring pixels. The algorithm uses multiple approaches such as text and natural modes. Distinctive decisions are made for each pixel in the image.

3.1.3.7 Color Correction

A variety of color profiles are used for color representation improvement. The decision about the profile is taken based on scene brightness and illumination type. Color correction is done using non-linear transformation.

3.1.3.8 Defect Pixel Correction

This algorithm detects and corrects from isolated single bad pixels to clusters with 3 hot bad pixels on the raw image data on the fly. Maximum hot pixels could be configured from 1 to 3 and cold pixels from 1 to 2.

3.1.3.9 Denoising

The denoising algorithm implements an "edge-preserving smoothing" algorithm. It averages pixels that are close in value to the central pixel. Neighboring pixels are equalized before averaging. The denoising algorithm features a slope estimation feature, enabling efficient noise reduction on edges and smooth shades. Denoising power can change radially to provide adequate effect as a function of lens shading compensation.

3.1.3.10 Gamma Correction

Gamma correction tables are used for the following color components:

- R, G and B – Three channels independently

Gamma settings can change dynamically as a function of illumination intensity, contrast ratio and noise index.

3.1.3.11 Image Downscaling

The image from the sensor can be downscaled to an arbitrary even size smaller than or equal to 3M by same ratios in X and Y dimensions, with an accuracy within a margin of 3 to 5 pixels. More precise output sizes can be achieved by cropping. Among other resolutions, QXGA, UXGA, SXGA, SVGA, VGA, QVGA, QQVGA, CIF, and QCIF resolutions are supported. To increase frame rate, averaged sub-sampled scaling is also supported for output sizes of SVGA and below.

3.1.3.12 Special Effects

The special effects may be used to create a Sepia (warm tone), Aqua (cool tone), Monochrome, Negative mono, Negative color, Sketch effect on the image.

3.1.3.13 Output Formatting

The ISP outputs 8-bit processed video data in the form of standard YUV ITU-R.656/601 or RGB data. Raw sensor data in Bayer format may also be outputted with 8-10 bit accuracy.

3.1.3.14 Image Rendition Control Options

There are a number of image rendition related controls available to the host, such as Brightness, Contrast, Saturation, configurable sharpness, and Glamour and so on.

3.1.4 JPEG

3.1.4.1 Overview

The JPEG core compressed the image on-the-fly according to the programmed Quantization and Huffman tables, and it produces an ISO/IEC 1098-1 compatible data stream. The JPEG encoder configuration and control is performed by the on-the-fly FW according to host settings using simple register interface.

The FW provides full output size/rate control.

JPEG rotation support is implemented to accelerate full resolution JPEG rotation.

3.1.4.2 Features

- Baseline ISO/IEC 10918-1 JPEG compliance
- Programmable Huffman Tables (2DC, 2AC0 and Quantization tables (4))
- Auto output size/rate control

- One-pass compression ratio regulation
- JPEG rotation support
- Any image size
- Motion JPEG encoding

3.1.4.3 Functional Description

The JPEG unit is responsible for performing the stream compression logic. It receives YUV422 stream, it performs the raster-to-block conversion and sends Y, U, V blocks toward the JPEG encoder. The JPEG encoder outputs the JPEG code with a JPEG header toward the chip data output.

The incoming YUV422 stream is send to Raster-to-Block conversion. A Raster-to-Block unit packs the YUV 4:2:2 image in the memory and reads it back in MCU (macro block unit) format for compression. It forwards MCUs to the MCU controller and the MCU controller delivers block (8x8) after block (8x8) toward the JPEG encoder core for compression. Code interface logic receives the compressed code from the JPEG core during compression, and sends the code to the Output block.

3.1.4.4 JPEG output size and rate control

In general, there are two different sets of methods for controlling the rate of a JPEG stream. One set of methods is controlling the output data bandwidth, and the other one is about controlling the total size of the JPEG output stream.

The bit rate control feature constantly inspects the size of the previous JPEG frame in order to modify the JPEG quality factor of the next frame so it would match a target bit-per-pixel value (which is correlative to target file size).

This method is used for iterative adaptation of the quality factor based on image contents, required size, frame size and other factors.

The host may control the target bit-per-pixel in 8:8 fractional integer, i.e. sensitivity of up to 1/256 bit-per-pixel. Different targets may be defined for preview and capture configurations. Since bit rate control is an iterative process, sudden changes in image contents may cause exceeding or falling short of the target JPEG file size.

The bit-rate control algorithm should overcome such situation within 1-2 frames time. In order to avoid exceeding the target JPEG file size in any case it is recommended to set the target BPP (bit per pixel) to about 15% less of the actual target, so minor overflows will not result in exceeding the actual limit. In addition, when invoking a capture request while in preview, there is an option to delay the capture in one frame in order to let the JPEG core adapt to the new resolution.

3.1.4.5 JPEG Rotation Support

When JPEG rotation support feature is used, the JPEG encoder outputs a JPEG stream in which all macro blocks (16x8 pixels) are rotated according to the host request (90/180/270 degrees with or without mirror). However, the macro blocks order remains unchanged as the original JPEG stream.

To complete the rotation the host receives the rotated macro blocks JPEG stream and rearranges the macro blocks in according to the rotation request. The macro blocks are identified by special JPEG restart markers at the beginning of each macro block. Using JPEG rotation support (macro-block rotation) may speed up the JPEG rotation process up to a factor of 100 and more, since instead of performing complex arithmetic computations for JPEG decoding, bit-by-bit rotation processing and JPEG encoding, the JPEG data file is simply rearranged - essentially byte aligned blocks copy actions.

Another benefit is the required memory for the image rotation which is similar to the memory required to store a compressed image rather than full uncompressed frame.

Reference host application which implements the macro-blocks re-arrangement is available from Samsung.

The following block diagram illustrates JPEG rotation support feature:

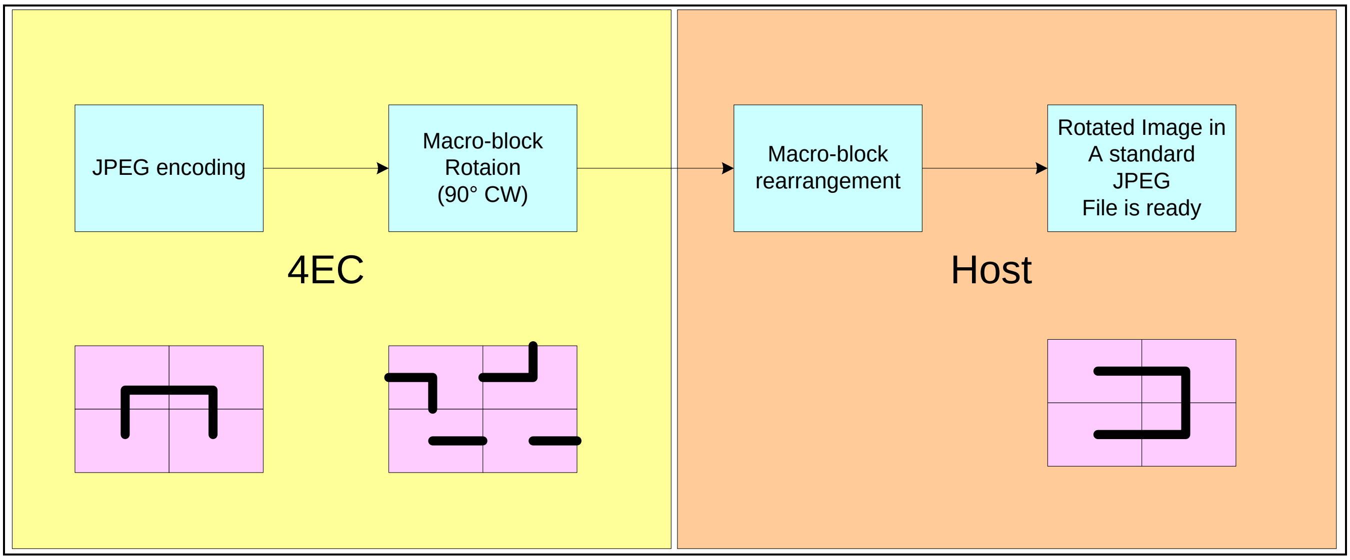
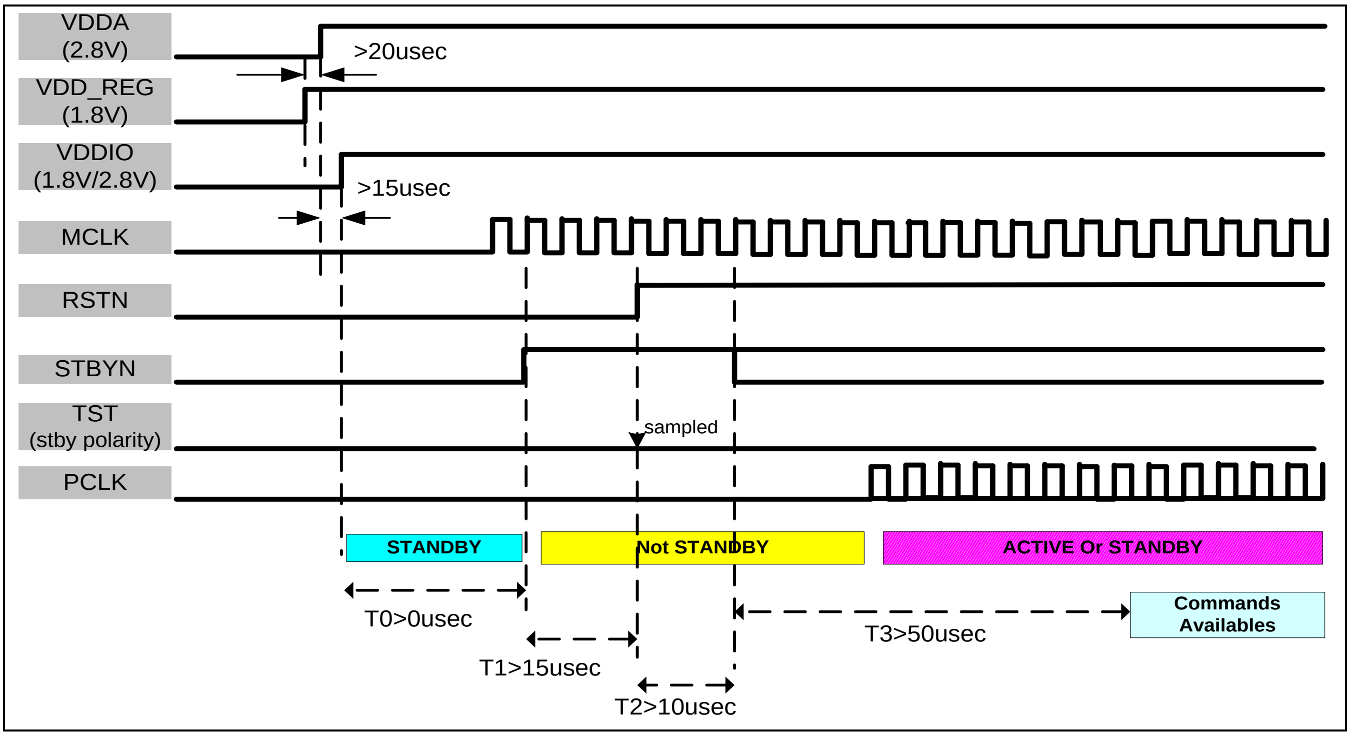


Figure 61 JPEG Rotation Support Example

4 TIMING SPECIFICATIONS

4.1 POWER-UP/DOWN SEQUENCE

4.1.1 POWER-UP SEQUENCE

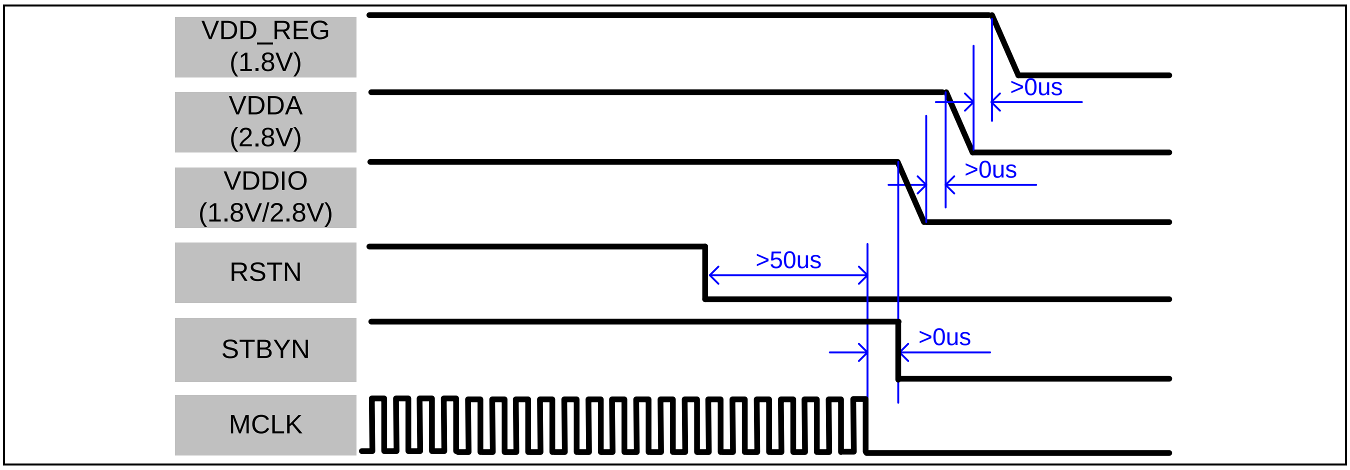


NOTE: If internal regulator is not used, VDD_REG apply to 1.2V.

Figure 62 Power-Up Sequence

- When STBYN=RSTN='0' then the chip in STANDBY state.
- STBYN pin de-asserted (at least 15usec before RSTN).
  - This time is required for Wake-Up process by HW (like main REG turn-on, exit from Fail-Safe and RESET signal propagation).
  - Then chip enter RESET state.
- RSTN goes to '1' (chip start init process).
- STBYN may stay '1' or change to '0' (at least 10usec after RSTN, for RESET signal propagation).
  - If stay at '1' - state is active, and STREAM ON is performed.
  - If change to '0' – chip enter to STANDBY mode by FW.
  - TST is STANDBY polarity control. When TST=0, STBYN is active low. When TST=1, STBYN is active high. TST pin state is sampled for STANDBY polarity when RSTN goes high.

4.1.2 POWER-DOWN SEQUENCE



NOTE: If internal regulator is not used, VDD_REG apply to 1.2V.

Figure 63 Power-Down Sequence

4.1.3 STANDBY MODE(HARDWARE STANDBY MODE)

4.1.3.1 Entering and Exiting standby

Hardware standby mode supported at VDD 1.8V regulated mode, but not supported at VDD 1.2V direct mode (VDD_MAIN and VDD_ALIVE direct connect to 1.2V power).

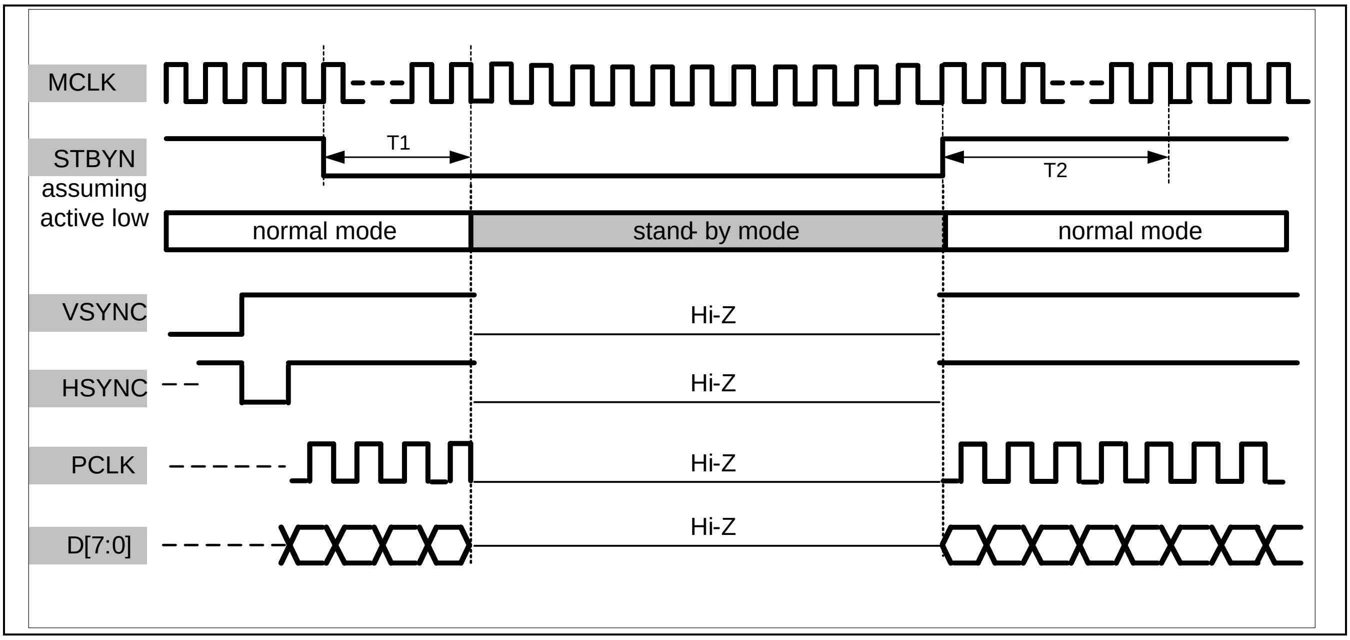


Figure 64 Standby – Entry & Exit waveform

Table 4-1 Standby timing cycle

Symbol	Description	Min.	Max	Unit
T1	To output tri-state delay	TBD(20)	-	Cycle
T2	To output valid delay	TBD(100,000)	-	Cycle

5 ELECTRICAL CHARACTERISTICS

5.1 ABSOLUTE MAXIMUM RATING

Table 5-1 Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
I/O Digital Power (2.8V or 1.8V)	V_{DDIO}	-0.3 to 3.8	V
Analog Power (2.8V)	V_{DDA}	-0.3 to 3.8	
Core Digital Power (1.2V)	V_{DDD}	-0.3 to 2.0	
Input Voltage	V_I	-0.3 to 3.8	
Ambient Temperature	T_A	-20 to +60	°C
Storage Temperature	T_S	-40 to +85	

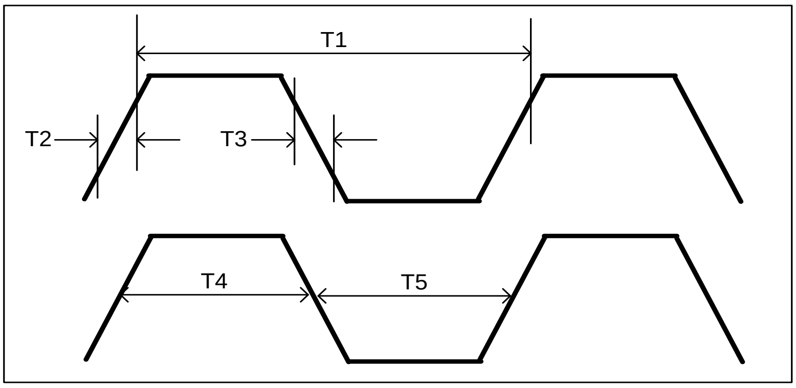
5.2 DC CHARACTERISTICS

Table 5-2 DC Characteristics

NOTE: (V_{DDIO1} = 2.8V ± 0.2V, V_{DDIO2} = 1.8V ± 0.1V , V_{DDD} = 1.2V ± 0.1V, Ta = -20 to + 60 °C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DDA}		2.6	2.8	3.0	V
	V_{DDD}		1.1	1.2	1.3	
	V_{DDIO1}		2.6	2.8	3.0	
	V_{DDIO2}		1.7	1.8	1.9	
High-Level Input Voltage	V_{IH}		0.7* V_{DDIO}	-	-	
Low-Level Input Voltage	V_{IL}		-	-	0.2* V_{DDIO}	
High Level Output Voltage	V_{OH}	Output High Voltage(@Ioh=-100uA)	V_{DDIO}- 0.2	-	-	
Low-Level Output Voltage	V_{OL}	Output Low voltage(@Iol=100uA)	-	-	0.2	
High-Level Input Current	I_{IH}	$V_I = V_{DDIO}$	-10		10	uA
		$V_I = V_{DDIO}$ (with Pull-Down)	-	-	72	
Low-Level Input Current	I_{IL}	$V_I = V_{SS}$	-10	-	10	
		$V_I = V_{SS}$ (with Pull-Up)	-72	-	-	
Standby Current	I_{STBY}	STBYN = Low, MCLK = Low (0 lux Illumination)	-	200	300	
Supply Current	I_{DD}	Serial Output Mode @15fps	-	280	310	mA
		Parallel Output Mode @15fps	-	280	310	
Power Consumption	P_{DD}	Serial Output Mode @15fps	-	-	468	mW
		Parallel Output Mode @15fps	-	-	468	
Input Capacitance	C_{IN}		-	-	10	pF

5.3 MCLK DESCRIPTION



Parameter		Min	Max	Unit
MCLK Frequency		24	54	MHz
MCLK Period	T1	18.5	41.67	ns
MCLK Rise Time	T2	-	6	ns
MCLK Fall Time	T3	-	6	ns
MCLK Duty Tolerance	max(T4,T5)/min(T4,T5)	1	1.2	-

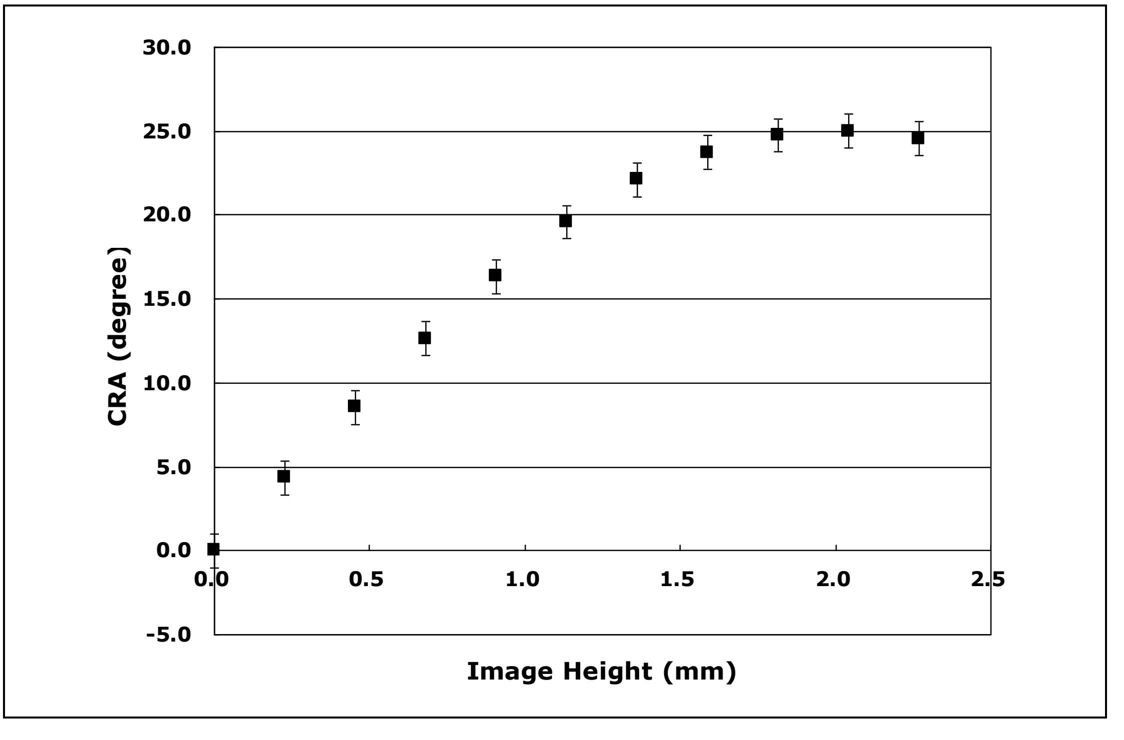
[NOTE]

The conditions for Vil and Vih in the Electrical Characteristics are also applied to MCLK.

5.4 CRA SPEC

Table 5-3 CRA Spec.

CRA (degree)				
Field	I.H. (mm)	Center	Upper	Under
0.0	0	0.0	0.0	0.0
0.1	0.227	4.3	5.3	3.3
0.2	0.454	8.5	9.5	7.5
0.3	0.680	12.6	13.6	11.6
0.4	0.907	16.3	17.3	15.3
0.5	1.134	19.6	20.6	18.6
0.6	1.361	22.1	23.1	21.1
0.7	1.588	23.7	24.7	22.7
0.8	1.814	24.7	25.7	23.7
0.9	2.041	25.0	26.0	24.0
1.0	2.268	24.5	25.5	23.5



6 REGISTER DESCRIPTION

Address	Initialization Parameters	Default	Size	RW	Description
0x700001A4	REG_FWverControlStr_usFWsenID	0x4EC0	2	R	Version information
0x700001A6	REG_FWverControlStr_usHWversion	0x0011	2	R	Revision information
0x700001F8	REG_TC_IPRM_InClockLSBs	0x5DC0	2	RW	Input clock in KHz (lower 16 bit)
0x700001FA	REG_TC_IPRM_InClockMSBs	0x0000	2	RW	Input clock in KHz (upper 16 bit)
0x700001FC	REG_TC_IPRM_LedGpio	0x0001	2	RW	Number of GPIO for LED
0x700001FE	REG_TC_IPRM_CM_Init_AfModeType	0x0000	2	RW	Auto-focus driver type: 0 - AFD_NONE 1 - AFD_APPLICATION 2 - AFD_VCM_PWM 3 - AFD_VCM_I2C 4 - AFD_SIDM 5 - AFD_STM
0x70000200	REG_TC_IPRM_CM_Init_PwmConfig1	0x0000	2	RW	PWM configuration bit mask: [0:3] : Number of PWM ports in use (up to 6) [4:7], [8:11], [12:15] : PWM 0-2 mapping according to the following list: 1 - PWM_gpio1 2 - PWM_gpio2 3 - PWM_gpio3 4 - PWM_gpio4 5 - PWM_gpio5 6 - PWM_gpio6 7 - PWM_gpio7 8 - PWM_gpio8
0x70000202	REG_TC_IPRM_CM_Init_PwmConfig2	0x0000	2	RW	PWM configuration bit mask: [0:3], [4:7], [8:11] : PWM 3-5 mapping according to PwmConfig1 list
0x70000204	REG_TC_IPRM_CM_Init_GpioConfig1	0x0000	2	RW	GPIO configuration bit mask: [0:3] : Number of GPIO ports in use (up to 7)

					[4:7], [8:11], [12:15] : GPIO 0-2 mapping according to the following list: 1 - GPIO_gpio1 2 - GPIO_gpio2 3 - GPIO_gpio3 4 - GPIO_gpio4 5 - GPIO_gpio5 6 - GPIO_gpio6 7 - GPIO_gpio7 8 - GPIO_gpio8
0x70000206	REG_TC_IPRM_CM_Init_GpioConfig2	0x0000	2	RW	GPIO configuration bit mask: [0:3], [4:7], [8:11] : GPIO 3-6 mapping according to GpioConfig1 list
0x70000208	REG_TC_IPRM_CM_Init_AdcConfig	0x0042	2	RW	ADC configuration bit mask: [0:2] : Number of ADC ports in use (up to 2) [3:5], [6:8] : ADC 0-1 mapping
0x7000020A	REG_TC_IPRM_CM_Init_AdcRateKhz	0x03E8	2	RW	ADC sampling rate in KHz (equal to all channels)
0x7000020C	REG_TC_IPRM_CM_Init_Mi2cBits	0x0000	2	RW	Master I2C configuration bit mask: [0:7] : Device ID (0 - No slave I2C connected) [8:9] : Clock 0 - MI2C_C_gpio1 1 - MI2C_C_gpio3 2 - MI2C_C_gpio5 3 - MI2C_C_gpio7 [10:11] : Data 0 - MI2C_D_gpio2 1 - MI2C_D_gpio4 2 - MI2C_D_gpio6 3 - MI2C_D_gpio8 [12:13] : Read type 0 - MI2C_RD_8BIT 1 - MI2C_RD_16BIT_LSB_FST 2 - MI2C_RD_16BIT_MSB_FST 14: Drive SCL pad manually
0x7000020E	REG_TC_IPRM_CM_Init_Mi2cRateKhz	0x0000	2	RW	Initial IIC Speed for AF (Khz)
0x70000210	REG_TC_IPRM_InitHwErr	0x0000	2	R	0x00 : NoError 0x01 : NO_LED_GPIO 0x02 : TOO_MANY_PWMS 0x03 : PWM_USED_TWICE 0x04 : GPIO_USED_TWICE 0x05 : TOO_MANY_ADCS 0x06 : ADC_USED_TWICE 0x07 : DRV_NOT_EXIST 0x08 : DRV_HW_INIT_ERROR 0x09 : GPIO_0_NOT_EXIST

0x70000212	REG_TC_IPRM_UseNPviClocks	0x0001	2	RW	Number of PLL configurations to be computed for PVI (0-2)
0x70000214	REG_TC_IPRM_UseNMipiClocks	0x0000	2	RW	Number of PLL configurations to be computed for MIPI (0-2) Total sum of UseNPviClocks and UseNMipiClocks can not be greater than 3 UseNPviClocks and UseNMipiClocks are also indexes which determine what is used among following clock sets.
0x70000216	REG_TC_IPRM_NumberOfMipiLanes	0x0001	2	RW	Number of MIPI lanes (0: PVI, 1: 1 lane MIPI, 2: 2 lane MIPI)
0x70000218	REG_TC_IPRM_bBlockInternalPllCalc	0x0000	2	RW	Use external PLL settings rather than internal FW calculation. That is, If this is set, then PLL calculation of FW is prohibited.
0x7000021A	REG_TC_IPRM_OpClk4KHz_0	0x1770	2	RW	First system clock frequency in KHz divided by 4
0x7000021C	REG_TC_IPRM_MinOutRate4KHz_0	0x05DC	2	RW	Minimal output rate of first clock in KHz divided by 4
0x7000021E	REG_TC_IPRM_MaxOutRate4KHz_0	0x1770	2	RW	Maximal output rate of first clock in KHz divided by 4
0x70000220	REG_TC_IPRM_OpClk4KHz_1	0x1770	2	RW	Second system clock frequency in KHz divided by 4
0x70000222	REG_TC_IPRM_MinOutRate4KHz_1	0x1770	2	RW	Minimal output rate of second clock in KHz divided by 4
0x70000224	REG_TC_IPRM_MaxOutRate4KHz_1	0x2328	2	RW	Maximal output rate of second clock in KHz divided by 4
0x70000226	REG_TC_IPRM_OpClk4KHz_2	0x0BB8	2	RW	Third system clock frequency in KHz divided by 4
0x70000228	REG_TC_IPRM_MinOutRate4KHz_2	0x05DC	2	RW	Minimal output rate of third clock in KHz divided by 4
0x7000022A	REG_TC_IPRM_MaxOutRate4KHz_2	0x1770	2	RW	Maximal output rate of third clock in KHz divided by 4
0x7000022C	REG_TC_IPRM_InitParamsUpdated	0x0000	2	RW	Update values in FW and invoke FW initialization
0x7000022E	REG_TC_IPRM_ErrorInfo	0x0000	2	R	Error code received from FW This Error is occurred when f/w failed to find PLL setting for input value. 0x00 : NoError 0x01 : MaxClocksError 0x02 : CreatePllError

					0x03 : InitHwError
0x70000230	REG_TC_UserBrightness	0x0000	2	RW	Control brightness value
0x70000232	REG_TC_UserContrast	0x0000	2	RW	Control contrast value
0x70000234	REG_TC_UserSaturation	0x0000	2	RW	Control saturation value
0x70000236	REG_TC_UserSharpBlur	0x0000	2	RW	Control sharpness value
0x70000238	REG_TC_UserGlamour	0x0000	2	RW	Control glamour value
0x7000023A	REG_TC_UserExposureVal88	0x0100	2	RW	Control exposure value
0x7000023C	REG_TC_GP_SpecialEffects	0x0000	2	RW	Special effect 0 : Normal 1 : MONOCHROME (BW) 2 : Negative Mono 3 : Negative Color 4 : Sepia 5 : AQUA 6 : Reddish 7 : Bluish 8 : Greenish 9 : Sketch 10 : Emboss color 11 : Emboss Mono
0x7000023E	REG_TC_GP_EnablePreview	0x0000	2	RW	Enable/disable preview output
0x70000240	REG_TC_GP_EnablePreviewChanged	0x0000	2	RW	Synchronize FW with Enable preview request
0x70000242	REG_TC_GP_EnableCapture	0x0000	2	RW	Invoke capture request
0x70000244	REG_TC_GP_EnableCaptureChanged	0x0000	2	RW	Synchronize FW with capture request
0x70000246	REG_TC_GP_InvokeHighSpeedSingleAF	0x0000	2	RW	Boolean control flag. When set the system invokes High-Speed Single AF mode, which uses cropped input from the sensor to increase frame rate during the search. There is no preview output during High-Speed AF mode. This flag is cleared automatically by the FW.
0x70000248	REG_TC_GP_bCaptureAfterHighSpeedAF	0x0000	2	RW	Boolean option flag for High-Speed AF mode. When set to TRUE the system after High-Speed AF mode (when the search is finished) immediately switches into Capture

					mode. When set to FALSE the system will switch back to the normal Preview mode.
0x7000024A	REG_TC_GP_bMacroModeHighSpeedAF	0x0000	2	RW	Boolean option flag for High-Speed AF mode. When set to TRUE then High-Speed AF mode performs search in Macro range.
0x7000024C	REG_TC_GP_HighSpeedAfWinMask	0x0002	2	RW	High-Speed AF mode AF window selection register. The system will crop sensor input to the AF window selected by this register. = 1 : only outer AF window is used = 2 : only inner AF window is used = 3 : Both AF windows are used
0x7000024E	REG_TC_GP_NewConfigSync	0x0000	2	RW	Set this flag when sending a new configuration. The FW clears the flag once a configuration has been applied.
0x70000250	REG_TC_GP_PrevReqInputWidth	0x0A20	2	RW	Preview sensor input window width: Equal or greater than output width
0x70000252	REG_TC_GP_PrevReqInputHeight	0x0798	2	RW	Preview sensor input window height: Equal or greater than output height
0x70000254	REG_TC_GP_PrevInputWidthOfs	0x0000	2	RW	Preview sensor input window X offset
0x70000256	REG_TC_GP_PrevInputHeightOfs	0x0000	2	RW	Preview sensor input window Y offset
0x70000258	REG_TC_GP_CapReqInputWidth	0x0A20	2	RW	Capture sensor input window width: Equal or greater than output width
0x7000025A	REG_TC_GP_CapReqInputHeight	0x0798	2	RW	Capture sensor input window height: Equal or greater than output height
0x7000025C	REG_TC_GP_CapInputWidthOfs	0x0000	2	RW	Capture sensor input window X offset
0x7000025E	REG_TC_GP_CapInputHeightOfs	0x0000	2	RW	Capture sensor input window Y offset
0x70000260	REG_TC_GP_InputsChangeRequest	0x0000	2	RW	Synchronize FW with input values
0x70000262	REG_TC_GP_bUseReqInputInPre	0x0000	2	RW	0 : Disable this option 1 : Cropping sensor when preview configuration is changing
0x70000264	REG_TC_GP_bUseReqInputInCap	0x0000	2	RW	0 : Disable this option 1 : Cropping sensor when capture configuration is changing
0x70000266	REG_TC_GP_ActivePrevConfig	0x0000	2	RW	Index number of active preview configuration

0x70000268	REG_TC_GP_PrevConfigChanged	0x0000	2	RW	Synchronize FW with new preview configuration
0x7000026A	REG_TC_GP_PrevOpenAfterChange	0x0001	2	RW	A flag that signals if, after the configuration change, the output should be enabled or not
0x7000026C	REG_TC_GP_ErrorPrevConfig	0x0000	2	R	Error code received from FW for preview calculation 0x00 : NoError 0x01 : PrevConfigIdxTooHigh 0x02 : CapConfigIdxTooHigh 0x04 : ClockIdxTooHigh 0x05 : BadDsFixedHsync 0x06 : BEST_FRRATE_NOT_ALLOWED 0x07 : BAD_DS_RATIO 0x08 : BAD_INPUT_WIDTH 0x09 : PviDivError 0x0A : PviConfigNotFit 0x0B : TOO_BIG_MAX_FR_TIME 0x0C : INTERNAL_ERROR_1 0x0D : INTERNAL_ERROR_2 0x0E : BadInputSizes 0x0F : BadDsOutputSize 0x10 : DS_FOR_BAYER 0x11 : UserHblankTooSmall 0x12 : UserVblankTooSmall 0x13 : CISNoBayer 0x14 : BppTooBig 0x15 : TooSmallSpoofSize 0x16 : TooSmallJpegBuffer
0x7000026E	REG_TC_GP_ActiveCapConfig	0x0000	2	RW	Index number of active capture configuration
0x70000270	REG_TC_GP_CapConfigChanged	0x0000	2	RW	Synchronize FW with new capture configuration
0x70000272	REG_TC_GP_ErrorCapConfig	0x0000	2	R	Error code received from FW for capture calculation 0x00 : NoError 0x01 : PrevConfigIdxTooHigh 0x02 : CapConfigIdxTooHigh 0x04 : ClockIdxTooHigh 0x05 : BadDsFixedHsync 0x06 : BEST_FRRATE_NOT_ALLOWED 0x07 : BAD_DS_RATIO 0x08 : BAD_INPUT_WIDTH 0x09 : PviDivError 0x0A : PviConfigNotFit 0x0B : TOO_BIG_MAX_FR_TIME 0x0C : INTERNAL_ERROR_1 0x0D : INTERNAL_ERROR_2 0x0E : BadInputSizes 0x0F : BadDsOutputSize 0x10 : DS_FOR_BAYER

					0x11 : UserHblankTooSmall 0x12 : UserVblankTooSmall 0x13 : CISNoBayer 0x14 : BppTooBig 0x15 : TooSmallSpoofSize 0x16 : TooSmallJpegBuffer
0x70000274	REG_TC_GP_GasTable Changed	0x0000	2	RW	Synchronize FW with updated Gas table settings - Start to decode RNP data and apply
0x7000027E	REG_TC_GP_bCheckP VIRange	0x0001	2	RW	0 : Do not check PVI output clock range when changing configuration 1 : Check PVI output clock range when changing configuration
0x70000280	REG_TC_GP_usSubsa mpledZoomStep	0x0001	2	RW	If the user wants to change zoom step, the user changes this value and commands preview configuration change
0x70000282	REG_TC_GP_bSubsam pledPreviewMode	0x0000	2	RW	0 : Using scaler to display preview 1 : Using only sub-sampling & cropping to display preview
0x70000284	REG_TC_GP_bBypass ScalerJpg	0x0000	2	RW	0 : Using normal mode 1 : Using power save mode (Bypassing scaler if output size is full size Disable clock sourcing if JPEG block is not used)
0x7000028A	REG_TC_GP_bUse1Fr ameCaptureMode	0x0000	2	RW	0 : Using continuous frame capture mode 1 : Using single frame capture mode via OIF control 2 : Using single frame capture mode via PAD control - Please refer to "skl_PadControlOption" register
0x7000028C	REG_TC_AF_AfCmd	0x0000	2	RW	0x00 : IDLE - Stands for [NO COMMAND] 0x01 : ABORT - Aborts currently executing command (except INIT command) 0x02 : SLEEP - AF Sleep command: affects AFD subsystem ? actuator IC power down 0x03 : INIT - Initialize AF subsystem (AF driver, AF algorithm) 0x04 : MANUAL - Manual AF command 0x05 : SINGLE - Single AF command 0X06 : CONTINUOUS - Continuous AF command

					0x07 : RESERVED - Reserved AF command (can be inserted using Trap-and-Patch)
0x7000028E	REG_TC_AF_AfCmdParam	0x0000	2	RW	Sleep ON / Sleep OFF 0 : Sleep OFF (Return from Power Down state); 1 : Sleep ON (Go to Power Down state) Specify lens position or Special option [0-255] : Lens position; [0x0100 | offset] : Move lens using positive offset (0-255); [0x0200 | offset] : Move lens using negative offset (0-255) Macro Mode 0x0001 : Macro mode High-speed mode (special option) 0x8000 : Force high-speed mode (this bit is set by the system) Macro Mode 0x0001 : Macro mode High-speed mode (special option) 0x8000 : Force high-speed mode (this bit is set by the system)
0x70000290	REG_TC_AF_AfCmdError	0x0000	2	RW	AF_NO_ERROR = 0, AF_DRV_ERROR = 1, AF_DRV_NOT_INITIALIZED = 2, AF_DRV_SLEEP = 3
0x70000294	REG_TC_AF_FstWinStartX	0x0000	2	RW	Set auto-focus statistics 1st window Start X coordinate (top left corner, not center)
0x70000296	REG_TC_AF_FstWinStartY	0x0000	2	RW	Set auto-focus statistics 1st window Start Y coordinate (top left corner, not center)
0x70000298	REG_TC_AF_FstWinSizeX	0x0000	2	RW	Set auto-focus statistics 1st window width in pixels
0x7000029A	REG_TC_AF_FstWinSizeY	0x0000	2	RW	Set auto-focus statistics 1st window height in pixels
0x7000029C	REG_TC_AF_ScndWinStartX	0x0000	2	RW	Set auto-focus statistics 2nd window Start X coordinate (top left corner, not center)
0x7000029E	REG_TC_AF_ScndWinStartY	0x0000	2	RW	Set auto-focus statistics 2nd window Start Y coordinate (top left corner, not center)
0x700002A0	REG_TC_AF_ScndWinSizeX	0x0000	2	RW	Set auto-focus statistics 2nd window width in pixels
0x700002A2	REG_TC_AF_ScndWinSizeY	0x0000	2	RW	Set auto-focus statistics 2nd window height in pixels
0x700002A4	REG_TC_AF_WinSizes	0x0000	2	RW	Synchronize FW with updated statistics

	Updated				window settings
0x700002A6	REG_0TC_PCFG_usWidth	0x0A20	2	RW	Width of Output image
0x700002A8	REG_0TC_PCFG_usHeight	0x0798	2	RW	Height of Output image
0x700002AA	REG_0TC_PCFG_Format	0x0005	2	RW	Output format : 0 : FORMAT_RGB565 1 : FORMAT_RGB888 5 : FORMAT_FULL_YUV (YUV422 0-255) 6 : FORMAT_CROPPED_YUV (YUV422 16-240) 7 : FORMAT_BAYER (Bayer format) 9 : FORMAT_JPEG
0x700002AC	REG_0TC_PCFG_usMaxOut4KHzRate	0xB3B0	2	RW	Upper limit of output clock(PCLK) in KHz unit
0x700002AE	REG_0TC_PCFG_usMinOut4KHzRate	0x05DC	2	RW	Lower limit of output clock(PCLK) in KHz unit There is a minimum required output clock which is calculated by FW automatically based on image size, output format and so on. If this required clock can be placed in the range which is limited by above upper limit and lower limit, then trial for Configuration change will be succeeded. If not, then Configuration change will not happen
0x700002B0	REG_0TC_PCFG_OutClkPerPix88	0x0100	2	RW	This register can limit FPS in JPEG mode to prevent OIF buffer overflow, but this value can not guarantee prevention of overflow. This register's format is 8.8 fixed point - Maximum output byte per pixel
0x700002B2	REG_0TC_PCFG_uBpp88	0x0300	2	RW	The target JPEG file size of preview mode The format of this register is 8.8 fixed point The user can calculate JPEG file size as below : (BPP88 * Image Size) / 2048 If the inspection of BRC is on, BRC will use Bpp88 of capture mode
0x700002B4	REG_0TC_PCFG_PVIMask	0x0042	2	RW	[0] : PVI_B_MSB_FIRST_BIT - When this bit is set the order of the output data will be switched G1B1 R1G1 G2B2 R2G2 instead R1G1 G1B1 R2G2 G2B2 etc [1] : PVI_B_CLK_NEG_EDGE_BIT - Define the clock edge which data is changed - if bit set - on Negative edge [2] : PVI_B_VALIDV_ACTIVE_LOW_BIT

					- When bit is set VALIDV set to 0 on new frame and later reset to 1 [3] : PVI_B_VALIDH_ACTIVE_LOW_BIT - When bit is set VALIDH set to 0 on new line and later reset to 1 [4] : PVI_B_UV_BEFORE_Y_BIT - 0b : Y0 U0/V0 Y1 V0/U0 Y2 U2/V2, 1b : U0/V0 Y0 V0/U0 Y1 U2/V2 Y2 [5] : PVI_B_V_BEFORE_U_BIT - 0b : Y0 U0 Y1 V0 or U0 Y0 V0 Y1, 1b : Y0 V0 Y1 U0 or V0 Y0 U0 Y1 [6] : PVI_B_VCLK_OUT_ACTIVE_NO_DATA - Additional modes (no clock on v-sync, clock overlap h-sync etc.) are set separately [7] : PVI_BAYER_2_BYTES_BIT - When bit is set Bayer output is 10 or 12 bits streamed out as two bytes (2 clocks per pixel) as 8+2 or 8+4 bits (FORMAT_BAYER + FORMAT_PROCESSED_BAYER) [8] : PVI_BAYER_8_BITS_BIT - When bit is set Bayer output is 8 bits (FORMAT_BAYER) [9] : PVI_BAYER_12_BITS_BIT - When bit is set Bayer output is 12 bits (FORMAT_BAYER) [10] : PVI_B_JPEG_DT_MARKER_BITS_BIT - When bit is set JPEG DT marker is enabled [11] : PVI_PBAYER_ENABLE_BIT - Whe bit is set and Format is set to Bayer, Processed Bayer will be output [13:12] : PVI_PBAYER_ORDER - 00h : Gr First, 01h : R First, 02h : B First, 03h : Gb First
0x700002B6	REG_0TC_PCFG_OIF Mask	0x0000	2	RW	[0:2] : OIF_QF_QUAL_MASK 000 : OIF_QC_CONT_MODE - PVI Clock always on - Legacy mode of continuous clock 001 : OIF_QC_QUAL_MODE1 - Qualified clock - on vsync rise and fall and on hsync valid - Legacy qualified clock 101 : OIF_QC_QUAL_MODE2 - Qualified clock - on hsync valid but no clock on vsync. Only on data. 010 : OIF_QC_QUAL_MODE3 - Qualified clock - on vsync rise and fall and on overlap hsync valid - Legacy qualified clock + new overlap H-sync 110 : OIF_QC_QUAL_MODE4 - Qualified clock - on overlap hsync valid but no clock on vsync. Only on data + overlap H-sync.

					[3] : OIF_B_USE_ITU656_MARKERS - Please refer the ""REG_TC_OIF_ITU656bits"" register [4] : OIF_B_SPOOF_ENABLE - The user must set a JPEG total packet size to bigger than 0 to use this option. This option just informs the tool that CIS is working in Spoof mode, so although the user writes a '1' to this bit, the CIS will be no affected. [5] : OIF_B_SPOOF_USE_VIDEO_PTR [6] : OIF_B_ENABLE_JPEG8 [7] : OIF_B_ENABLE_SEMC_MODE [9] : OIF_B_MIPI_VIA_PVI_TST [10] : OIF_B_USE_FIXED_HSYNC_DELTA [11] : OIF_B_VSYNC_SRC_SELECT [12] : OIF_B_JPEG8_SI_PADDING - Padding 0x0A at JPEG8 status info[7:4], using with the OIF_B_ENABLE_JPEG8 [13] : OIF_B_Scalado_JPEG
0x700002B8	REG_0TC_PCFG_usJpegPacketSize	0x01E0	2	RW	The size of JPEG packet of preview mode - If the user wants to use a none Spoof mode, this value must be set to multiple of 12
0x700002BA	REG_0TC_PCFG_usJpegTotalPackets	0x0000	2	RW	The number of JPEG packets of preview mode 0 : Spoof mode is disabled This value > 0 : Spoof mode is enabled
0x700002BC	REG_0TC_PCFG_uClockInd	0x0000	2	RW	System clock index (0~2)
0x700002BE	REG_0TC_PCFG_usFrTimeType	0x0000	2	RW	Frame rate type : 0 : FR_TIME_DYNAMIC 1 : FR_TIME_FIXED_NOT_ACCURATE 2 : FR_TIME_FIXED_ACCURATE
0x700002C0	REG_0TC_PCFG_FrRateQualityType	0x0000	2	RW	Frame rate quality : 0 : FRVSQ_DYNAMIC 1 : FRVSQ_BEST_FRRATE 2 : FRVSQ_BEST_QUALITY
0x700002C2	REG_0TC_PCFG_usMaxFrTimeMsecMult10	0x1964	2	RW	Required frame time for fixed FR / maximal frame time for dynamic FR (Units are in 0.1 ms) (for example, 333 for 33.3 ms)
0x700002C4	REG_0TC_PCFG_usMinFrTimeMsecMult10	0x0000	2	RW	Minimal frame time for dynamic FR. Not valid for fixed FR (Units are in 0.1 ms)
0x700002C6	REG_0TC_PCFG_sSaturation	0x0000	2	RW	Device correction saturation control

0x700002C8	REG_0TC_PCFG_sSharpBlur	0x0000	2	RW	Device correction sharpness control
0x700002CA	REG_0TC_PCFG_sGlamour	0x0000	2	RW	Device correction glamour control
0x700002CC	REG_0TC_PCFG_sColorTemp	0x0000	2	RW	Device correction color temperature control
0x700002CE	REG_0TC_PCFG_uDeviceGammaIndex	0x0000	2	RW	Device correction Gamma table index
0x700002D0	REG_0TC_PCFG_uPrevMirror	0x0000	2	RW	Preview mirror mode (X/Y) - Bit mask
0x700002D2	REG_0TC_PCFG_uCaptureMirror	0x0000	2	RW	Capture mirror mode (X/Y) - Bit mask
0x700002D6	REG_1TC_PCFG_usWidth	0x0400	2	RW	Please refer to REG_0TC_PCFG
0x700002D8	REG_1TC_PCFG_usHeight	0x0300	2	RW	Please refer to REG_0TC_PCFG
0x700002DA	REG_1TC_PCFG_Format	0x0005	2	RW	Please refer to REG_0TC_PCFG
0x700002DC	REG_1TC_PCFG_usMaxOut4KHzRate	0xB3B0	2	RW	Please refer to REG_0TC_PCFG
0x700002DE	REG_1TC_PCFG_usMinOut4KHzRate	0x05DC	2	RW	Please refer to REG_0TC_PCFG
0x700002E0	REG_1TC_PCFG_OutClkPerPix88	0x0100	2	RW	Please refer to REG_0TC_PCFG
0x700002E2	REG_1TC_PCFG_uBpp88	0x0300	2	RW	Please refer to REG_0TC_PCFG
0x700002E4	REG_1TC_PCFG_PVIMask	0x0042	2	RW	Please refer to REG_0TC_PCFG
0x700002E6	REG_1TC_PCFG_OIFMask	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x700002E8	REG_1TC_PCFG_usJpegPacketSize	0x01E0	2	RW	Please refer to REG_0TC_PCFG
0x700002EA	REG_1TC_PCFG_usJpegTotalPackets	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x700002EC	REG_1TC_PCFG_uClockInd	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x700002EE	REG_1TC_PCFG_usFrTimeType	0x0000	2	RW	Please refer to REG_0TC_PCFG

0x700002F0	REG_1TC_PCFG_FrRateQualityType	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x700002F2	REG_1TC_PCFG_usMaxFrTimeMsecMult10	0x1964	2	RW	Please refer to REG_0TC_PCFG
0x700002F4	REG_1TC_PCFG_usMinFrTimeMsecMult10	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x700002F6	REG_1TC_PCFG_sSaturation	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x700002F8	REG_1TC_PCFG_sSharpBlur	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x700002FA	REG_1TC_PCFG_sGlamour	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x700002FC	REG_1TC_PCFG_sColorTemp	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x700002FE	REG_1TC_PCFG_uDeviceGammaIndex	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x70000300	REG_1TC_PCFG_uPrevMirror	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x70000302	REG_1TC_PCFG_uCaptureMirror	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x70000306	REG_2TC_PCFG_usWidth	0x0320	2	RW	Please refer to REG_0TC_PCFG
0x70000308	REG_2TC_PCFG_usHeight	0x0258	2	RW	Please refer to REG_0TC_PCFG
0x7000030A	REG_2TC_PCFG_Format	0x0005	2	RW	Please refer to REG_0TC_PCFG
0x7000030C	REG_2TC_PCFG_usMaxOut4KHzRate	0xB3B0	2	RW	Please refer to REG_0TC_PCFG
0x7000030E	REG_2TC_PCFG_usMinOut4KHzRate	0x05DC	2	RW	Please refer to REG_0TC_PCFG
0x70000310	REG_2TC_PCFG_OutClkPerPix88	0x0100	2	RW	Please refer to REG_0TC_PCFG
0x70000312	REG_2TC_PCFG_uBpp88	0x0300	2	RW	Please refer to REG_0TC_PCFG
0x70000314	REG_2TC_PCFG_PVIMask	0x0042	2	RW	Please refer to REG_0TC_PCFG
0x70000316	REG_2TC_PCFG_OIFMask	0x0000	2	RW	Please refer to REG_0TC_PCFG

0x70000318	REG_2TC_PCFG_usJpegPacketSize	0x01E0	2	RW	Please refer to REG_0TC_PCFG
0x7000031A	REG_2TC_PCFG_usJpegTotalPackets	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x7000031C	REG_2TC_PCFG_uClockInd	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x7000031E	REG_2TC_PCFG_usFrTimeType	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x70000320	REG_2TC_PCFG_FrRateQualityType	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x70000322	REG_2TC_PCFG_usMaxFrTimeMsecMult10	0x1964	2	RW	Please refer to REG_0TC_PCFG
0x70000324	REG_2TC_PCFG_usMinFrTimeMsecMult10	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x70000326	REG_2TC_PCFG_sSaturation	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x70000328	REG_2TC_PCFG_sSharpBlur	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x7000032A	REG_2TC_PCFG_sGlamour	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x7000032C	REG_2TC_PCFG_sColorTemp	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x7000032E	REG_2TC_PCFG_uDeviceGammaIndex	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x70000330	REG_2TC_PCFG_uPrevMirror	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x70000332	REG_2TC_PCFG_uCaptureMirror	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x70000336	REG_3TC_PCFG_usWidth	0x0280	2	RW	Please refer to REG_0TC_PCFG
0x70000338	REG_3TC_PCFG_usHeight	0x01E0	2	RW	Please refer to REG_0TC_PCFG
0x7000033A	REG_3TC_PCFG_Format	0x0005	2	RW	Please refer to REG_0TC_PCFG
0x7000033C	REG_3TC_PCFG_usMaxOut4KHzRate	0xB3B0	2	RW	Please refer to REG_0TC_PCFG
0x7000033E	REG_3TC_PCFG_usMinOut4KHzRate	0x05DC	2	RW	Please refer to REG_0TC_PCFG

0x70000340	REG_3TC_PCFG_OutClkPerPix88	0x0100	2	RW	Please refer to REG_0TC_PCFG
0x70000342	REG_3TC_PCFG_uBpp88	0x0300	2	RW	Please refer to REG_0TC_PCFG
0x70000344	REG_3TC_PCFG_PVIMask	0x0042	2	RW	Please refer to REG_0TC_PCFG
0x70000346	REG_3TC_PCFG_OIFMask	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x70000348	REG_3TC_PCFG_usJpegPacketSize	0x01E0	2	RW	Please refer to REG_0TC_PCFG
0x7000034A	REG_3TC_PCFG_usJpegTotalPackets	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x7000034C	REG_3TC_PCFG_uClockInd	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x7000034E	REG_3TC_PCFG_usFrTimeType	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x70000350	REG_3TC_PCFG_FrRateQualityType	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x70000352	REG_3TC_PCFG_usMaxFrTimeMsecMult10	0x1964	2	RW	Please refer to REG_0TC_PCFG
0x70000354	REG_3TC_PCFG_usMinFrTimeMsecMult10	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x70000356	REG_3TC_PCFG_sSaturation	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x70000358	REG_3TC_PCFG_sSharpBlur	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x7000035A	REG_3TC_PCFG_sGlamour	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x7000035C	REG_3TC_PCFG_sColorTemp	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x7000035E	REG_3TC_PCFG_uDeviceGammaIndex	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x70000360	REG_3TC_PCFG_uPrevMirror	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x70000362	REG_3TC_PCFG_uCaptureMirror	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x70000366	REG_4TC_PCFG_usWidth	0x0140	2	RW	Please refer to REG_0TC_PCFG

0x70000368	REG_4TC_PCFG_usHeight	0x00F0	2	RW	Please refer to REG_0TC_PCFG
0x7000036A	REG_4TC_PCFG_Format	0x0005	2	RW	Please refer to REG_0TC_PCFG
0x7000036C	REG_4TC_PCFG_usMaxOut4KHzRate	0xB3B0	2	RW	Please refer to REG_0TC_PCFG
0x7000036E	REG_4TC_PCFG_usMinOut4KHzRate	0x05DC	2	RW	Please refer to REG_0TC_PCFG
0x70000370	REG_4TC_PCFG_OutClkPerPix88	0x0100	2	RW	Please refer to REG_0TC_PCFG
0x70000372	REG_4TC_PCFG_uBpp88	0x0300	2	RW	Please refer to REG_0TC_PCFG
0x70000374	REG_4TC_PCFG_PVIMask	0x0042	2	RW	Please refer to REG_0TC_PCFG
0x70000376	REG_4TC_PCFG_OIFMask	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x70000378	REG_4TC_PCFG_usJpegPacketSize	0x01E0	2	RW	Please refer to REG_0TC_PCFG
0x7000037A	REG_4TC_PCFG_usJpegTotalPackets	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x7000037C	REG_4TC_PCFG_uClockInd	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x7000037E	REG_4TC_PCFG_usFrTimeType	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x70000380	REG_4TC_PCFG_FrRateQualityType	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x70000382	REG_4TC_PCFG_usMaxFrTimeMsecMult10	0x1964	2	RW	Please refer to REG_0TC_PCFG
0x70000384	REG_4TC_PCFG_usMinFrTimeMsecMult10	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x70000386	REG_4TC_PCFG_sSaturation	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x70000388	REG_4TC_PCFG_sSharpBlur	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x7000038A	REG_4TC_PCFG_sGlamour	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x7000038C	REG_4TC_PCFG_sColorTemp	0x0000	2	RW	Please refer to REG_0TC_PCFG

0x7000038E	REG_4TC_PCFG_uDeviceGammaIndex	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x70000390	REG_4TC_PCFG_uPrevMirror	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x70000392	REG_4TC_PCFG_uCaptureMirror	0x0000	2	RW	Please refer to REG_0TC_PCFG
0x70000396	REG_0TC_CCFG_uCaptureMode	0x0000	2	RW	0 : Do not use AE/AWB 1 : Use AE/AWB for movie mode
0x70000398	REG_0TC_CCFG_usWidth	0x0A20	2	RW	Width of Output image
0x7000039A	REG_0TC_CCFG_usHeight	0x0798	2	RW	Height of Output image
0x7000039C	REG_0TC_CCFG_Format	0x0009	2	RW	Output format : 0 : FORMAT_RGB565 1 : FORMAT_RGB888 5 : FORMAT_FULL_YUV (YUV422 0-255) 6 : FORMAT_CROPPED_YUV (YUV422 16-240) 7 : FORMAT_BAYER (Bayer format) 9 : FORMAT_JPEG
0x7000039E	REG_0TC_CCFG_usMaxOut4KHzRate	0xB3B0	2	RW	Upper limit of output clock(PCLK) in KHz unit
0x700003A0	REG_0TC_CCFG_usMinOut4KHzRate	0x05DC	2	RW	Lower limit of output clock(PCLK) in KHz unit There is a minimum required output clock which is calculated by FW automatically based on image size, output format and so on. If this required clock can be placed in the range which is limited by above upper limit and lower limit, then trial for Configuration change will be successed. If not, then Configuration change will not happen
0x700003A2	REG_0TC_CCFG_OutClkPerPix88	0x0100	2	RW	This register can limit FPS in JPEG mode to prevent OIF buffer overflow, but this value can not guarantee prevention of overflow. This register's format is 8.8 fixed point - Maximum output byte per pixel
0x700003A4	REG_0TC_CCFG_uBpp88	0x0300	2	RW	The target JPEG file size of capture mode The format of this register is 8.8 fixed point The user can calculate target JPEG file size as below : ("This register value" * Image Size) / 2048

0x700003A6	REG_0TC_CCFG_PVI Mask	0x0042	2	RW	[0] : PVI_B_MSB_FIRST_BIT - When this bit is set the order of the output data will be switched G1B1 R1G1 G2B2 R2G2 instead R1G1 G1B1 R2G2 G2B2 etc [1] : PVI_B_CLK_NEG_EDGE_BIT - Define the clock edge which data is changed - if bit set - on Negative edge [2] : PVI_B_VALIDV_ACTIVE_LOW_BIT - When bit is set VALIDV set to 0 on new frame and later reset to 1 [3] : PVI_B_VALIDH_ACTIVE_LOW_BIT - When bit is set VALIDH set to 0 on new line and later reset to 1 [4] : PVI_B_UV_BEFORE_Y_BIT - 0b : Y0 U0/V0 Y1 V0/U0 Y2 U2/V2, 1b : U0/V0 Y0 V0/U0 Y1 U2/V2 Y2 [5] : PVI_B_V_BEFORE_U_BIT - 0b : Y0 U0 Y1 V0 or U0 Y0 V0 Y1, 1b : Y0 V0 Y1 U0 or V0 Y0 U0 Y1 [6] : PVI_B_VCLK_OUT_ACTIVE_NO_DATA - Additional modes (no clock on v-sync, clock overlap h-sync etc.) are set separately [7] : PVI_BAYER_2_BYTES_BIT - When bit is set Bayer output is 10 or 12 bits streamed out as two bytes (2 clocks per pixel) as 8+2 or 8+4 bits (FORMAT_BAYER + FORMAT_PROCESSED_BAYER) [8] : PVI_BAYER_8_BITS_BIT - When bit is set Bayer output is 8 bits (FORMAT_BAYER) [9] : PVI_BAYER_12_BITS_BIT - When bit is set Bayer output is 12 bits (FORMAT_BAYER) [10] : PVI_B_JPEG_DT_MARKER_BITS_BIT - When bit is set JPEG DT marker is enabled [11] : PVI_PBAYER_ENABLE_BIT - Whe bit is set and Format is set to Bayer, Processed Bayer will be output [13:12] : PVI_PBAYER_ORDER - 00h : Gr First, 01h : R First, 02h : B First, 03h : Gb First
0x700003A8	REG_0TC_CCFG_OIF Mask	0x0000	2	RW	[0:2] : OIF_QF_QUAL_MASK 000 : OIF_QC_CONT_MODE - PVI Clock always on - Legacy mode of continuous clock 001 : OIF_QC_QUAL_MODE1 - Qualified clock - on vsync rise and fall and on hsync valid - Legacy qualified clock 101 : OIF_QC_QUAL_MODE2 - Qualified clock - on hsync valid but no

					clock on vsync. Only on data. 010 : OIF_QC_QUAL_MODE3 - Qualified clock - on vsync rise and fall and on overlap hsync valid - Legacy qualified clock + new overlap H-sync 110 : OIF_QC_QUAL_MODE4 - Qualified clock - on overlap hsync valid but no clock on vsync. Only on data + overlap H-sync. [3] : OIF_B_USE_ITU656_MARKERS - Please refer the ""REG_TC_OIF_ITU656bits"" register [4] : OIF_B_SPOOF_ENABLE - The user must set a JPEG total packet size to bigger than 0 to use this option. This option just informs the tool that CIS is working in Spoof mode, so although the user writes a '1' to this bit, the CIS will be no affected. [5] : OIF_B_SPOOF_USE_VIDEO_PTR [6] : OIF_B_ENABLE_JPEG8 [7] : OIF_B_ENABLE_SEMC_MODE [9] : OIF_B_MIPI_VIA_PVI_TST [10] : OIF_B_USE_FIXED_HSYNC_DELTA [11] : OIF_B_VSYNC_SRC_SELECT [12] : OIF_B_JPEG8_SI_PADDING - Padding 0x0A at JPEG8 status info[7:4], using with the OIF_B_ENABLE_JPEG8 [13] : OIF_B_Scalado_JPEG
0x700003AA	REG_0TC_CCFG_usJpegPacketSize	0x01E0	2	RW	The size of JPEG packet of capture mode - If the user wants to use a none Spoof mode, this value must be set to multiple of 12 - If the user uses none Spoof interleave mode, packet size will be fixed by header size(636)
0x700003AC	REG_0TC_CCFG_usJpegTotalPackets	0x0000	2	RW	The number of JPEG packets of capture mode 0 : Spoof mode is disabled This value > 0 : Spoof mode is enabled
0x700003AE	REG_0TC_CCFG_uClockInd	0x0000	2	RW	System clock index (0~2)
0x700003B0	REG_0TC_CCFG_usFrTimeType	0x0000	2	RW	Frame rate type : 0 : FR_TIME_DYNAMIC 1 : FR_TIME_FIXED_NOT_ACCURATE 2 : FR_TIME_FIXED_ACCURATE
0x700003B2	REG_0TC_CCFG_FrRateQualityType	0x0002	2	RW	Frame rate quality : 0 : FRVSQ_DYNAMIC 1 : FRVSQ_BEST_FRRATE 2 : FRVSQ_BEST_QUALITY

0x700003B4	REG_0TC_CCFG_usMaxFrTimeMsecMult10	0x1964	2	RW	Required frame time for fixed FR / maximal frame time for dynamic FR (Units are in 0.1 ms) (for example, 333 for 33.3 ms)
0x700003B6	REG_0TC_CCFG_usMinFrTimeMsecMult10	0x0000	2	RW	Minimal frame time for dynamic FR. Not valid for fixed FR (Units are in 0.1 ms)
0x700003B8	REG_0TC_CCFG_sSaturation	0x0000	2	RW	Device correction saturation control
0x700003BA	REG_0TC_CCFG_sSharpBlur	0x0000	2	RW	Device correction sharpness control
0x700003BC	REG_0TC_CCFG_sGlamour	0x0000	2	RW	Device correction glamour control
0x700003BE	REG_0TC_CCFG_sColorTemp	0x0000	2	RW	Device correction color temperature control
0x700003C0	REG_0TC_CCFG_uDeviceGammaIndex	0x0000	2	RW	Device correction Gamma table index
0x700003C2	REG_1TC_CCFG_uCaptureMode	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x700003C4	REG_1TC_CCFG_usWidth	0x0500	2	RW	Please refer to REG_0TC_CCFG
0x700003C6	REG_1TC_CCFG_usHeight	0x03C0	2	RW	Please refer to REG_0TC_CCFG
0x700003C8	REG_1TC_CCFG_Format	0x0009	2	RW	Please refer to REG_0TC_CCFG
0x700003CA	REG_1TC_CCFG_usMaxOut4KHzRate	0xB3B0	2	RW	Please refer to REG_0TC_CCFG
0x700003CC	REG_1TC_CCFG_usMinOut4KHzRate	0x05DC	2	RW	Please refer to REG_0TC_CCFG
0x700003CE	REG_1TC_CCFG_OutClkPerPix88	0x0100	2	RW	Please refer to REG_0TC_CCFG
0x700003D0	REG_1TC_CCFG_uBpp88	0x0300	2	RW	Please refer to REG_0TC_CCFG
0x700003D2	REG_1TC_CCFG_PVIMask	0x0042	2	RW	Please refer to REG_0TC_CCFG
0x700003D4	REG_1TC_CCFG_OIFMask	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x700003D6	REG_1TC_CCFG_usJpegPacketSize	0x01E0	2	RW	Please refer to REG_0TC_CCFG

0x700003D8	REG_1TC_CCFG_usJpegTotalPackets	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x700003DA	REG_1TC_CCFG_uClockInd	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x700003DC	REG_1TC_CCFG_usFrTimeType	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x700003DE	REG_1TC_CCFG_FrRateQualityType	0x0002	2	RW	Please refer to REG_0TC_CCFG
0x700003E0	REG_1TC_CCFG_usMaxFrTimeMsecMult10	0x1964	2	RW	Please refer to REG_0TC_CCFG
0x700003E2	REG_1TC_CCFG_usMinFrTimeMsecMult10	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x700003E4	REG_1TC_CCFG_sSaturation	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x700003E6	REG_1TC_CCFG_sSharpBlur	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x700003E8	REG_1TC_CCFG_sGlamour	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x700003EA	REG_1TC_CCFG_sColorTemp	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x700003EC	REG_1TC_CCFG_uDeviceGammaIndex	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x700003EE	REG_2TC_CCFG_uCaptureMode	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x700003F0	REG_2TC_CCFG_usWidth	0x0320	2	RW	Please refer to REG_0TC_CCFG
0x700003F2	REG_2TC_CCFG_usHeight	0x0258	2	RW	Please refer to REG_0TC_CCFG
0x700003F4	REG_2TC_CCFG_Format	0x0009	2	RW	Please refer to REG_0TC_CCFG
0x700003F6	REG_2TC_CCFG_usMaxOut4KHzRate	0xB3B0	2	RW	Please refer to REG_0TC_CCFG
0x700003F8	REG_2TC_CCFG_usMinOut4KHzRate	0x05DC	2	RW	Please refer to REG_0TC_CCFG
0x700003FA	REG_2TC_CCFG_OutClkPerPix88	0x0100	2	RW	Please refer to REG_0TC_CCFG
0x700003FC	REG_2TC_CCFG_uBpp88	0x0300	2	RW	Please refer to REG_0TC_CCFG

0x700003FE	REG_2TC_CCFG_PVIMask	0x0042	2	RW	Please refer to REG_0TC_CCFG
0x70000400	REG_2TC_CCFG_OIFMask	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x70000402	REG_2TC_CCFG_usJpegPacketSize	0x01E0	2	RW	Please refer to REG_0TC_CCFG
0x70000404	REG_2TC_CCFG_usJpegTotalPackets	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x70000406	REG_2TC_CCFG_uClockInd	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x70000408	REG_2TC_CCFG_usFrTimeType	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x7000040A	REG_2TC_CCFG_FrRateQualityType	0x0002	2	RW	Please refer to REG_0TC_CCFG
0x7000040C	REG_2TC_CCFG_usMaxFrTimeMsecMult10	0x1964	2	RW	Please refer to REG_0TC_CCFG
0x7000040E	REG_2TC_CCFG_usMinFrTimeMsecMult10	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x70000410	REG_2TC_CCFG_sSaturation	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x70000412	REG_2TC_CCFG_sSharpBlur	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x70000414	REG_2TC_CCFG_sGlamour	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x70000416	REG_2TC_CCFG_sColorTemp	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x70000418	REG_2TC_CCFG_uDeviceGammaIndex	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x7000041A	REG_3TC_CCFG_uCaptureMode	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x7000041C	REG_3TC_CCFG_usWidth	0x0280	2	RW	Please refer to REG_0TC_CCFG
0x7000041E	REG_3TC_CCFG_usHeight	0x01E0	2	RW	Please refer to REG_0TC_CCFG
0x70000420	REG_3TC_CCFG_Format	0x0009	2	RW	Please refer to REG_0TC_CCFG
0x70000422	REG_3TC_CCFG_usMaxOut4KHzRate	0xB3B0	2	RW	Please refer to REG_0TC_CCFG

0x70000424	REG_3TC_CCFG_usMinOut4KHzRate	0x05DC	2	RW	Please refer to REG_0TC_CCFG
0x70000426	REG_3TC_CCFG_OutClkPerPix88	0x0100	2	RW	Please refer to REG_0TC_CCFG
0x70000428	REG_3TC_CCFG_uBpp88	0x0300	2	RW	Please refer to REG_0TC_CCFG
0x7000042A	REG_3TC_CCFG_PVIMask	0x0042	2	RW	Please refer to REG_0TC_CCFG
0x7000042C	REG_3TC_CCFG_OIFMask	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x7000042E	REG_3TC_CCFG_usJpegPacketSize	0x01E0	2	RW	Please refer to REG_0TC_CCFG
0x70000430	REG_3TC_CCFG_usJpegTotalPackets	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x70000432	REG_3TC_CCFG_uClockInd	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x70000434	REG_3TC_CCFG_usFrTimeType	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x70000436	REG_3TC_CCFG_FrRateQualityType	0x0002	2	RW	Please refer to REG_0TC_CCFG
0x70000438	REG_3TC_CCFG_usMaxFrTimeMsecMult10	0x1964	2	RW	Please refer to REG_0TC_CCFG
0x7000043A	REG_3TC_CCFG_usMinFrTimeMsecMult10	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x7000043C	REG_3TC_CCFG_sSaturation	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x7000043E	REG_3TC_CCFG_sSharpBlur	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x70000440	REG_3TC_CCFG_sGlamour	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x70000442	REG_3TC_CCFG_sColorTemp	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x70000444	REG_3TC_CCFG_uDeviceGammaIndex	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x70000446	REG_4TC_CCFG_uCaptureMode	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x70000448	REG_4TC_CCFG_usWidth	0x0140	2	RW	Please refer to REG_0TC_CCFG

0x7000044A	REG_4TC_CCFG_usHeight	0x00F0	2	RW	Please refer to REG_0TC_CCFG
0x7000044C	REG_4TC_CCFG_Format	0x0009	2	RW	Please refer to REG_0TC_CCFG
0x7000044E	REG_4TC_CCFG_usMaxOut4KHzRate	0xB3B0	2	RW	Please refer to REG_0TC_CCFG
0x70000450	REG_4TC_CCFG_usMinOut4KHzRate	0x05DC	2	RW	Please refer to REG_0TC_CCFG
0x70000452	REG_4TC_CCFG_OutClkPerPix88	0x0100	2	RW	Please refer to REG_0TC_CCFG
0x70000454	REG_4TC_CCFG_uBpp88	0x0300	2	RW	Please refer to REG_0TC_CCFG
0x70000456	REG_4TC_CCFG_PVIMask	0x0042	2	RW	Please refer to REG_0TC_CCFG
0x70000458	REG_4TC_CCFG_OIFMask	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x7000045A	REG_4TC_CCFG_usJpegPacketSize	0x01E0	2	RW	Please refer to REG_0TC_CCFG
0x7000045C	REG_4TC_CCFG_usJpegTotalPackets	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x7000045E	REG_4TC_CCFG_uClockInd	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x70000460	REG_4TC_CCFG_usFrTimeType	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x70000462	REG_4TC_CCFG_FrRateQualityType	0x0002	2	RW	Please refer to REG_0TC_CCFG
0x70000464	REG_4TC_CCFG_usMaxFrTimeMsecMult10	0x1964	2	RW	Please refer to REG_0TC_CCFG
0x70000466	REG_4TC_CCFG_usMinFrTimeMsecMult10	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x70000468	REG_4TC_CCFG_sSaturation	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x7000046A	REG_4TC_CCFG_sSharpBlur	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x7000046C	REG_4TC_CCFG_sGlamour	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x7000046E	REG_4TC_CCFG_sColorTemp	0x0000	2	RW	Please refer to REG_0TC_CCFG

0x70000470	REG_4TC_CCFG_uDeviceGammaIndex	0x0000	2	RW	Please refer to REG_0TC_CCFG
0x70000472	REG_TC_CFGUSERSET_NColsHBLank	0x0000	2	RW	When > 0, defines the exact delta between timing columns and readout columns (H-Blank length)
0x70000474	REG_TC_CFGUSERSET_NLinesVBLank	0x0000	2	RW	When > 0 and frame type is "FR_TIME_FIXED_ACCURATE", defines the exact delta between timing lines and readout lines (B-Blank length)
0x70000476	REG_TC_BRC_BRC_type	0x0000	2	RW	[0] : BRC_ON [1] : INSPECTION_ON - This option must be used with [0] = 1b. - If the user uses a preview with YUV and a capture with JPEG, CIS will predict JPEG size in YUV preview mode. But, JPEG HW will be working in YUV mode too. And the result of prediction can be wrong case by case. - The inspection will be active only when preview dimensions are 16*8 multiply [2] : AUTO_SPOOF_BRC - This option must be used with [0] = 1b. - If the user uses this option, CIS will set a target JPEG size with Spoof size.(Please refer "jpeg_BppAutoBrcSpoofPercentage") [3] : LIMIT_MAX_Q_BY_USER - When the user uses the BRC, maximum quality value is limited by the user sets quality value("REG_TC_BRC_usPrevQuality", "REG_TC_BRC_usCaptureQuality")
0x70000478	REG_TC_BRC_usPrevQuality	0x0055	2	RW	The JPEG quality of the preview mode when the user turns off BRC Recommended values : - Best Quality : 85d - Good Quality : 50d - Poor Quality : 20d Note : Maximum/Minimum quality value can be limited
0x7000047A	REG_TC_BRC_usCaptureQuality	0x0055	2	RW	The JPEG quality of the capture mode when the user turns off BRC Recommended values : - Best Quality : 85d - Good Quality : 50d - Poor Quality : 20d Note : Maximum/Minimum quality value can be limited
0x7000047C	REG_TC_THUMB_Thumb_bActive	0x0000	2	RW	0 : JPEG interleave mode is off 1 : JPEG interleave mode is on - This option can be used in JPEG capture

					mode
0x7000047E	REG_TC_THUMB_Thumb_uWidth	0x0000	2	RW	The width of the video image during JPEG interleave mode
0x70000480	REG_TC_THUMB_Thumb_uHeight	0x0000	2	RW	The height of the video image during JPEG interleave mode
0x70000482	REG_TC_THUMB_Thumb_Format	0x0001	2	RW	The format of video during JPEG interleave mode 0 : FORMAT_RGB565 1 : FORMAT_RGB888 5 : FORMAT_FULL_YUV (YUV422 0-255)
0x7000048E	REG_TC_PZOOM_us88TargetZoom	0x0100	2	RW	Target zoom ratio
0x70000490	REG_TC_PZOOM_us88ZoomStep	0x0019	2	RW	One step ratio
0x70000492	REG_TC_PZOOM_usZoomSpeed	0x000A	2	RW	Continuous zoom speed
0x70000494	REG_TC_PZOOM_PrevZoomReqInputWidth	0x0A20	2	RW	Preview zoom width
0x70000496	REG_TC_PZOOM_PrevZoomReqInputHeight	0x0798	2	RW	Preview zoom height
0x70000498	REG_TC_PZOOM_PrevZoomReqInputWidthOfs	0x0000	2	RW	Preview zoom horizontal offset
0x7000049A	REG_TC_PZOOM_PrevZoomReqInputHeightOfs	0x0000	2	RW	Preview zoom vertical offset
0x7000049C	REG_TC_PZOOM_CapZoomReqInputWidth	0x0A20	2	RW	Capture zoom width
0x7000049E	REG_TC_PZOOM_CapZoomReqInputHeight	0x0798	2	RW	Capture zoom height
0x700004A0	REG_TC_PZOOM_CapZoomReqInputWidthOfs	0x0000	2	RW	Capture zoom horizontal offset
0x700004A2	REG_TC_PZOOM_CapZoomReqInputHeightOfs	0x0000	2	RW	Capture zoom vertical offset
0x700004A4	REG_TC_PZOOM_ePzoomState	0x0000	2	RW	Pseudo zoom state. 0 : IDLE 1 : STEPPING_UP 2 : STEPPING_DOWN 3 : ONE_STEP_UP 4 : ONE_STEP_DOWN 5 : GO_TARGET

					6 : FORCE_OUT_CROP
0x700004A6	REG_SF_USER_LeiLow	0x0000	2	RW	Set LEI low value.
0x700004A8	REG_SF_USER_LeiHigh	0x0000	2	RW	Set LEI high value.
0x700004AA	REG_SF_USER_LeiChanged	0x0000	2	RW	Synchronize FW with LEI value change
0x700004AC	REG_SF_USER_Exposure	0x0000	2	RW	Set exposure low value.
0x700004AE	REG_SF_USER_ExposureHigh	0x0000	2	RW	Set exposure high value.
0x700004B0	REG_SF_USER_ExposureChanged	0x0000	2	RW	Synchronize FW with exposure value change
0x700004B2	REG_SF_USER_TotalGain	0x0000	2	RW	Set total gain value
0x700004B4	REG_SF_USER_TotalGainChanged	0x0000	2	RW	Synchronize FW with total gain change
0x700004B6	REG_SF_USER_ExtraGain	0x0000	2	RW	Set extra gain value.
0x700004B8	REG_SF_USER_ExtraGainChanged	0x0000	2	RW	Synchronize FW with total gain change
0x700004BA	REG_SF_USER_Rgain	0x0000	2	RW	Set red gain value
0x700004BC	REG_SF_USER_RgainChanged	0x0000	2	RW	Synchronize FW with red gain change
0x700004BE	REG_SF_USER_Ggain	0x0000	2	RW	Set green gain value
0x700004C0	REG_SF_USER_GgainChanged	0x0000	2	RW	Synchronize FW with green gain change
0x700004C2	REG_SF_USER_Bgain	0x0000	2	RW	Set blue gain value
0x700004C4	REG_SF_USER_BgainChanged	0x0000	2	RW	Synchronize FW with blue gain change
0x700004C6	REG_SF_USER_RGBGainChanged	0x0000	2	RW	Synchronize FW with RGB gain change simultaneously
0x700004C8	REG_SF_USER_aGain	0x0000	2	RW	Set analog gain value
0x700004CA	REG_SF_USER_aGainChanged	0x0000	2	RW	Synchronize FW with analog gain change
0x700004CC	REG_SF_USER_dGain	0x0000	2	RW	Set digital gain value

0x700004CE	REG_SF_USER_dGainChanged	0x0000	2	RW	Synchronize FW with digital gain change
0x700004D0	REG_SF_USER_IsoType	0x0000	2	RW	ISO type state. 1 : ISO mode Auto. 2 : ISO mode classic. 3 : ISO mode sport.
0x700004D2	REG_SF_USER_IsoVal	0x0000	2	RW	Set ISO value.
0x700004D4	REG_SF_USER_IsoChanged	0x0000	2	RW	Synchronize FW with total ISO change
0x700004D6	REG_SF_USER_FlickerQuant	0x0000	2	RW	Setting a flicker quantization: 0: no AFC, 1: 50 Hz, 2: 60 Hz
0x700004D8	REG_SF_USER_FlickerQuantChanged	0x0000	2	RW	Synchronize FW with flicker quantization change
0x700004DA	REG_TC_OIF_VsyncPulseWidth	0x0000	2	RW	Writing this value to 0xD000B068[7:0] If this value is not zero, 0xD000B068[8] = 1. Or 0xD000B068[8] = 0 It should be used in only the 601 mode.
0x700004DC	REG_TC_OIF_ITU656bits	0x0000	2	RW	If the user uses a "OIF_B_USE_ITU656_MARKERS" option, this value will be written at 0xD000B052 (It is a HW register, so please see a HW register map) - ITU-656 bit mask : 0x01 : OIF_656_MARKER_BIT 0x02 : OIF_656_SYNC_BIT 0x04 : OIF_656_QUAL_BIT 0x08 : OIF_656_FIELD_BIT 0x10 : OIF_656_BLANK_LINE_BIT
0x700004DE	REG_TC_OIF_ITU656Blank	0x0020	2	RW	If the user uses the ITU656 mdoe, this value will be written at 0xD000B056 (It is a HW register, so please see a HW register map)
0x700004E4	REG_TC_OIF_CfgChanged	0x0000	2	RW	Trigger for applying an OIF configuration to HW
0x700004E6	REG_TC_DBG_AutoAlgEnBits	0x077F	2	RW	Auto-algorithms enable/disable : [0] : AA_ALL [1] : AA_AE_ACTIVE [2] : AA_DIV_LEI [3] : AA_WB_ACTIVE [4] : AA_USE_WB_FOR_ISP [5] : AA_FLICKER [6] : AA_FIT [9] : AA_WR_ISP_HW [10] : AA_WR_SEN_HW

0x700004E8	REG_TC_DBG_IspBypass	0x0000	2	RW	Bypass FW operation
0x700004EA	REG_TC_DBG_ReInitCmd	0x0000	2	RW	Invoke FW "soft reset"
0x700004EC	REG_HIGH_FPS_RTA_SyncMode	0x0000	2	RW	0 : The high FPS mode is disabled 1 : The high FPS mode is enabled - In this mode, AE/AWB will need more frames than normal mode for processing
0x700004EE	REG_HIGH_FPS_uConfigSetClocksDiv40	0x11CC	2	RW	This value is used when configuration is changing on high frame mode. (If the user wants to use the BRC function, the user must increase this value about twice.)
0x700004F0	REG_HIGH_FPS_uSetStreamClocksDiv40	0xFFFF	2	RW	This value is used when configuration is changing on high frame mode. (If the user wants to use the BRC function, the user must increase this value about twice.)
0x70000520	REG_INFO_usNormBrightLsb	0x0000	2	R	The value of normalized brightness
0x70000522	REG_INFO_usNormBrightMsb	0x0000	2	R	The value of normalized brightness
0x70000524	REG_INFO_PrevActual_usMinFrTimeMsecMult10	0x0000	2	R	Calculated minimum frame time for preview setting
0x70000526	REG_INFO_PrevActual_usOut4KHzRate	0x0000	2	R	Calculated output PCLK for preview setting
0x70000528	REG_INFO_CaptActual_usMinFrTimeMsecMult10	0x0000	2	R	Calculated minimum frame time for capture setting
0x7000052A	REG_INFO_CaptActual_usOut4KHzRate	0x0000	2	R	Calculated output PCLK for capture setting
0x7000052E	REG_INFO_AfActual_usOut4KHzRate	0x0000	2	R	Calculated output PCLK for AF setting
0x70000530	REG_INFO_CaptureDone	0x0000	2	R	If first capture frame was outputted this value will be set to 1
0x70000548	lt_uLimitOption	0x0000	2	RW	AE boundary option. 0 : use default option. Use register lt_uLimitHigh and lt_uLimitLow 1 : Change boundary accoding to normbr, use register lt_NormBr and lt_uLimit 2 : Change boundary accoding to contrast,

					use register lt_Contrast and lt_uLimit
0x7000054C	lt_NormBr[0]	0x00000001	4	RW	Bondary tuning input register. Input data is norm br.
0x70000550	lt_NormBr[1]	0x00000100	4	RW	Bondary tuning input register. Input data is norm br.
0x70000554	lt_NormBr[2]	0x00001000	4	RW	Bondary tuning input register. Input data is norm br.
0x70000558	lt_NormBr[3]	0x00005000	4	RW	Bondary tuning input register. Input data is norm br.
0x7000055C	lt_NormBr[4]	0x0000A000	4	RW	Bondary tuning input register. Input data is norm br.
0x70000560	lt_Contrast[0]	0x0032	2	RW	Bondary tuning input register. Input data is contrast value.
0x70000562	lt_Contrast[1]	0x0042	2	RW	Bondary tuning input register. Input data is contrast value.
0x70000564	lt_Contrast[2]	0x0052	2	RW	Bondary tuning input register. Input data is contrast value.
0x70000566	lt_Contrast[3]	0x0062	2	RW	Bondary tuning input register. Input data is contrast value.
0x70000568	lt_Contrast[4]	0x0072	2	RW	Bondary tuning input register. Input data is contrast value.
0x7000056A	lt_uLimit[0]	0x0008	2	RW	Boundary setting ouput value, value is according to lt_NormBr or lt_iLimit.
0x7000056C	lt_uLimit[1]	0x0009	2	RW	Boundary setting ouput value, value is according to lt_NormBr or lt_iLimit.
0x7000056E	lt_uLimit[2]	0x0010	2	RW	Boundary setting ouput value, value is according to lt_NormBr or lt_iLimit.
0x70000570	lt_uLimit[3]	0x0011	2	RW	Boundary setting ouput value, value is according to lt_NormBr or lt_iLimit.
0x70000572	lt_uLimit[4]	0x0013	2	RW	Boundary setting ouput value, value is according to lt_NormBr or lt_iLimit.
0x70000582	lt_uSlowFilterCoef	0x0000	2	RW	Slow filter coefficient. As value approaches to 0x100, AE convergence progresses slowly.
0x70000588	lt_uInitPostToleranceCnt	0x0002	2	RW	Number of times of AE action in boundary.
0x700005D4	lt_MBR_uMaxAnGain	0x0400	2	RW	Max analog gain in MBR mode.
0x700005D6	lt_MBR_uMaxDigGain	0x0400	2	RW	Max digital gain in MBR mode.

0x700005D8	lt_MBR_ulExpIn[0]	0x00000190	4	RW	MBR exposure table.
0x700005DC	lt_MBR_ulExpIn[1]	0x00000A3C	4	RW	MBR exposure table.
0x700005E0	lt_MBR_ulExpIn[2]	0x00001A08	4	RW	MBR exposure table.
0x700005E4	lt_MBR_ulExpIn[3]	0x00003414	4	RW	MBR exposure table.
0x700005E8	lt_MBR_ulExpIn[4]	0x0000DEC8	4	RW	MBR exposure table.
0x700005EC	lt_MBR_ulExpOut[0]	0x00000190	4	RW	MBR exposure table.
0x700005F0	lt_MBR_ulExpOut[1]	0x0000051C	4	RW	MBR exposure table.
0x700005F4	lt_MBR_ulExpOut[2]	0x00000D04	4	RW	MBR exposure table.
0x700005F8	lt_MBR_ulExpOut[3]	0x00001A08	4	RW	MBR exposure table.
0x700005FC	lt_MBR_ulExpOut[4]	0x00006F64	4	RW	MBR exposure table.
0x70000600	lt_uLeiInit[0]	0x04B0	2	RW	Initial value of LEI.
0x70000608	lt_ExpGain_uSubsamplingmode	0x0000	2	RW	Exposure table number in subsampling mode.
0x7000060A	lt_ExpGain_uNonSubsampling	0x0000	2	RW	Exposure table number in non-subsampling mode.
0x7000060C	lt_ExpGain_ExpCurveGainMaxStr[0]_uMaxAnGain	0x0400	2	RW	Analog gain max for exptable 1
0x7000060E	lt_ExpGain_ExpCurveGainMaxStr[0]_uMaxDigGain	0x0200	2	RW	Analog gain max for exptable 1
0x70000610	lt_ExpGain_ExpCurveGainMaxStr[0]_ulExpIn[0]	0x00000001	4	RW	Exposure table1
0x70000614	lt_ExpGain_ExpCurveGainMaxStr[0]_ulExpIn[1]	0x00000A3C	4	RW	Exposure table1
0x70000618	lt_ExpGain_ExpCurveGainMaxStr[0]_ulExpIn[2]	0x00000D04	4	RW	Exposure table1
0x7000061C	lt_ExpGain_ExpCurveG	0x00000	4	RW	Exposure table1

	ainMaxStr[0]_ulExpIn[3]	FA0			
0x70000620	lt_ExpGain_ExpCurveGainMaxStr[0]_ulExpIn[4]	0x00001A08	4	RW	Exposure table1
0x70000624	lt_ExpGain_ExpCurveGainMaxStr[0]_ulExpIn[5]	0x00003414	4	RW	Exposure table1
0x70000628	lt_ExpGain_ExpCurveGainMaxStr[0]_ulExpIn[6]	0x00006828	4	RW	Exposure table1
0x7000062C	lt_ExpGain_ExpCurveGainMaxStr[0]_ulExpIn[7]	0x0000DEC8	4	RW	Exposure table1
0x70000630	lt_ExpGain_ExpCurveGainMaxStr[0]_ulExpIn[8]	0x0000DEC8	4	RW	Exposure table1
0x70000634	lt_ExpGain_ExpCurveGainMaxStr[0]_ulExpIn[9]	0x0000DEC8	4	RW	Exposure table1
0x70000638	lt_ExpGain_ExpCurveGainMaxStr[0]_ulExpOut[0]	0x00000001	4	RW	Exposure table1
0x7000063C	lt_ExpGain_ExpCurveGainMaxStr[0]_ulExpOut[1]	0x00000A3C	4	RW	Exposure table1
0x70000640	lt_ExpGain_ExpCurveGainMaxStr[0]_ulExpOut[2]	0x00000D04	4	RW	Exposure table1
0x70000644	lt_ExpGain_ExpCurveGainMaxStr[0]_ulExpOut[3]	0x00000FA0	4	RW	Exposure table1
0x70000648	lt_ExpGain_ExpCurveGainMaxStr[0]_ulExpOut[4]	0x00001A08	4	RW	Exposure table1
0x7000064C	lt_ExpGain_ExpCurveGainMaxStr[0]_ulExpOut[5]	0x00003414	4	RW	Exposure table1
0x70000650	lt_ExpGain_ExpCurveGainMaxStr[0]_ulExpOut[6]	0x00006828	4	RW	Exposure table1
0x70000654	lt_ExpGain_ExpCurveGainMaxStr[0]_ulExpOut[7]	0x0000DEC8	4	RW	Exposure table1
0x70000658	lt_ExpGain_ExpCurveGainMaxStr[0]_ulExpOut[8]	0x0000DEC8	4	RW	Exposure table1

0x7000065C	lt_ExpGain_ExpCurveGainMaxStr[0]_ulExpOut[9]	0x0000DEC8	4	RW	Exposure table1
0x70000660	lt_ExpGain_ExpCurveGainMaxStr[1]_uMaxAnGain	0x0400	2	RW	Analog gain max for exptable 2
0x70000662	lt_ExpGain_ExpCurveGainMaxStr[1]_uMaxDigGain	0x0200	2	RW	Analog gain max for exptable 2
0x70000664	lt_ExpGain_ExpCurveGainMaxStr[1]_ulExpIn[0]	0x00000001	4	RW	Exposure table2
0x70000668	lt_ExpGain_ExpCurveGainMaxStr[1]_ulExpIn[1]	0x00000A3C	4	RW	Exposure table2
0x7000066C	lt_ExpGain_ExpCurveGainMaxStr[1]_ulExpIn[2]	0x00000D04	4	RW	Exposure table2
0x70000670	lt_ExpGain_ExpCurveGainMaxStr[1]_ulExpIn[3]	0x00000FA0	4	RW	Exposure table2
0x70000674	lt_ExpGain_ExpCurveGainMaxStr[1]_ulExpIn[4]	0x00001A08	4	RW	Exposure table2
0x70000678	lt_ExpGain_ExpCurveGainMaxStr[1]_ulExpIn[5]	0x00003414	4	RW	Exposure table2
0x7000067C	lt_ExpGain_ExpCurveGainMaxStr[1]_ulExpIn[6]	0x00006828	4	RW	Exposure table2
0x70000680	lt_ExpGain_ExpCurveGainMaxStr[1]_ulExpIn[7]	0x0000DEC8	4	RW	Exposure table2
0x70000684	lt_ExpGain_ExpCurveGainMaxStr[1]_ulExpIn[8]	0x0000DEC8	4	RW	Exposure table2
0x70000688	lt_ExpGain_ExpCurveGainMaxStr[1]_ulExpIn[9]	0x0000DEC8	4	RW	Exposure table2
0x7000068C	lt_ExpGain_ExpCurveGainMaxStr[1]_ulExpOut[0]	0x00000001	4	RW	Exposure table2
0x70000690	lt_ExpGain_ExpCurveGainMaxStr[1]_ulExpOut[1]	0x00000A3C	4	RW	Exposure table2
0x70000694	lt_ExpGain_ExpCurveGainMaxStr[1]_ulExpOut[2]	0x00000D04	4	RW	Exposure table2
0x70000698	lt_ExpGain_ExpCurveGainMaxStr[1]_ulExpOut[	0x00000FA0	4	RW	Exposure table2

	3]				
0x7000069C	lt_ExpGain_ExpCurveGainMaxStr[1]_ulExpOut[4]	0x00001A08	4	RW	Exposure table2
0x700006A0	lt_ExpGain_ExpCurveGainMaxStr[1]_ulExpOut[5]	0x00003414	4	RW	Exposure table2
0x700006A4	lt_ExpGain_ExpCurveGainMaxStr[1]_ulExpOut[6]	0x00006828	4	RW	Exposure table2
0x700006A8	lt_ExpGain_ExpCurveGainMaxStr[1]_ulExpOut[7]	0x0000DEC8	4	RW	Exposure table2
0x700006AC	lt_ExpGain_ExpCurveGainMaxStr[1]_ulExpOut[8]	0x0000DEC8	4	RW	Exposure table2
0x700006B0	lt_ExpGain_ExpCurveGainMaxStr[1]_ulExpOut[9]	0x0000DEC8	4	RW	Exposure table2
0x700006C6	skl_bUseAviHdr	0x0000	2	RW	1 : Using motion JPEG header instead of JFIF in movie mode
0x700006C8	skl_bBlockCaptureOnBadBRC	0x0000	2	RW	0 : Turning off this option 1 : Skipping the first frame of capture to avoid size overflow when the user uses a BRC in JPEG mode
0x70000700	skl_bNoVoutInterrupt	0x0000	2	RW	0 : Checking the OIF error 1 : Not checking the OIF error
0x70000702	skl_CheckPviError	0x0001	2	RW	0 : Not checking the PVI error 1 : Checking the PVI error
0x70000732	skl_PadControlOption	0x1FFF	2	RW	If the user select "REG_TC_GP_bUse1FrameCaptureMode" to option '2', PAD control HW register will be written this value to disable output
0x70000734	SARR_usGammaLutRGBIndoor[0][0]	0x0000	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1023
0x70000736	SARR_usGammaLutRGBIndoor[0][1]	0x0001	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1024

0x70000738	SARR_usGammaLutRGBIndoor[0][2]	0x0007	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1025
0x7000073A	SARR_usGammaLutRGBIndoor[0][3]	0x002D	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1026
0x7000073C	SARR_usGammaLutRGBIndoor[0][4]	0x0075	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1027
0x7000073E	SARR_usGammaLutRGBIndoor[0][5]	0x00E9	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1028
0x70000740	SARR_usGammaLutRGBIndoor[0][6]	0x0143	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1029
0x70000742	SARR_usGammaLutRGBIndoor[0][7]	0x016C	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1030
0x70000744	SARR_usGammaLutRGBIndoor[0][8]	0x0190	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1031
0x70000746	SARR_usGammaLutRGBIndoor[0][9]	0x01CC	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1032
0x70000748	SARR_usGammaLutRGBIndoor[0][10]	0x01FF	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1033
0x7000074A	SARR_usGammaLutRGBIndoor[0][11]	0x022A	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1034
0x7000074C	SARR_usGammaLutRGBIndoor[0][12]	0x0252	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1035

0x7000074E	SARR_usGammaLutRGBIndoor[0][13]	0x0296	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1036
0x70000750	SARR_usGammaLutRGBIndoor[0][14]	0x02D6	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1037
0x70000752	SARR_usGammaLutRGBIndoor[0][15]	0x033C	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1038
0x70000754	SARR_usGammaLutRGBIndoor[0][16]	0x038D	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1039
0x70000756	SARR_usGammaLutRGBIndoor[0][17]	0x03D0	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1040
0x70000758	SARR_usGammaLutRGBIndoor[0][18]	0x03F7	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1041
0x7000075A	SARR_usGammaLutRGBIndoor[0][19]	0x03FF	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1042
0x7000075C	SARR_usGammaLutRGBIndoor[1][0]	0x0000	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1043
0x7000075E	SARR_usGammaLutRGBIndoor[1][1]	0x0001	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1044
0x70000760	SARR_usGammaLutRGBIndoor[1][2]	0x0007	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1045
0x70000762	SARR_usGammaLutRGBIndoor[1][3]	0x002D	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1046

0x70000764	SARR_usGammaLutRGBIndoor[1][4]	0x0075	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1047
0x70000766	SARR_usGammaLutRGBIndoor[1][5]	0x00E9	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1048
0x70000768	SARR_usGammaLutRGBIndoor[1][6]	0x0143	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1049
0x7000076A	SARR_usGammaLutRGBIndoor[1][7]	0x016C	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1050
0x7000076C	SARR_usGammaLutRGBIndoor[1][8]	0x0190	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1051
0x7000076E	SARR_usGammaLutRGBIndoor[1][9]	0x01CC	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1052
0x70000770	SARR_usGammaLutRGBIndoor[1][10]	0x01FF	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1053
0x70000772	SARR_usGammaLutRGBIndoor[1][11]	0x022A	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1054
0x70000774	SARR_usGammaLutRGBIndoor[1][12]	0x0252	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1055
0x70000776	SARR_usGammaLutRGBIndoor[1][13]	0x0296	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1056
0x70000778	SARR_usGammaLutRGBIndoor[1][14]	0x02D6	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1057

0x7000077A	SARR_usGammaLutRGBIndoor[1][15]	0x033C	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1058
0x7000077C	SARR_usGammaLutRGBIndoor[1][16]	0x038D	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1059
0x7000077E	SARR_usGammaLutRGBIndoor[1][17]	0x03D0	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1060
0x70000780	SARR_usGammaLutRGBIndoor[1][18]	0x03F7	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1061
0x70000782	SARR_usGammaLutRGBIndoor[1][19]	0x03FF	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1062
0x70000784	SARR_usGammaLutRGBIndoor[2][0]	0x0000	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1063
0x70000786	SARR_usGammaLutRGBIndoor[2][1]	0x0001	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1064
0x70000788	SARR_usGammaLutRGBIndoor[2][2]	0x0007	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1065
0x7000078A	SARR_usGammaLutRGBIndoor[2][3]	0x002D	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1066
0x7000078C	SARR_usGammaLutRGBIndoor[2][4]	0x0075	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1067
0x7000078E	SARR_usGammaLutRGBIndoor[2][5]	0x00E9	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1068

0x70000790	SARR_usGammaLutRGBIndoor[2][6]	0x0143	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1069
0x70000792	SARR_usGammaLutRGBIndoor[2][7]	0x016C	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1070
0x70000794	SARR_usGammaLutRGBIndoor[2][8]	0x0190	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1071
0x70000796	SARR_usGammaLutRGBIndoor[2][9]	0x01CC	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1072
0x70000798	SARR_usGammaLutRGBIndoor[2][10]	0x01FF	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1073
0x7000079A	SARR_usGammaLutRGBIndoor[2][11]	0x022A	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1074
0x7000079C	SARR_usGammaLutRGBIndoor[2][12]	0x0252	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1075
0x7000079E	SARR_usGammaLutRGBIndoor[2][13]	0x0296	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1076
0x700007A0	SARR_usGammaLutRGBIndoor[2][14]	0x02D6	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1077
0x700007A2	SARR_usGammaLutRGBIndoor[2][15]	0x033C	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1078
0x700007A4	SARR_usGammaLutRGBIndoor[2][16]	0x038D	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1079

0x700007A6	SARR_usGammaLutRGBIndoor[2][17]	0x03D0	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1080
0x700007A8	SARR_usGammaLutRGBIndoor[2][18]	0x03F7	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1081
0x700007AA	SARR_usGammaLutRGBIndoor[2][19]	0x03FF	2	RW	RGB Indoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1082
0x700007AC	SARR_usGammaLutRGBOutdoor[0][0]	0x0000	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1023
0x700007AE	SARR_usGammaLutRGBOutdoor[0][1]	0x0001	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1024
0x700007B0	SARR_usGammaLutRGBOutdoor[0][2]	0x0007	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1025
0x700007B2	SARR_usGammaLutRGBOutdoor[0][3]	0x002D	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1026
0x700007B4	SARR_usGammaLutRGBOutdoor[0][4]	0x0075	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1027
0x700007B6	SARR_usGammaLutRGBOutdoor[0][5]	0x00E9	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1028
0x700007B8	SARR_usGammaLutRGBOutdoor[0][6]	0x0143	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1029
0x700007BA	SARR_usGammaLutRGBOutdoor[0][7]	0x016C	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1030

0x700007BC	SARR_usGammaLutRGBOutdoor[0][8]	0x0190	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1031
0x700007BE	SARR_usGammaLutRGBOutdoor[0][9]	0x01CC	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1032
0x700007C0	SARR_usGammaLutRGBOutdoor[0][10]	0x01FF	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1033
0x700007C2	SARR_usGammaLutRGBOutdoor[0][11]	0x022A	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1034
0x700007C4	SARR_usGammaLutRGBOutdoor[0][12]	0x0252	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1035
0x700007C6	SARR_usGammaLutRGBOutdoor[0][13]	0x0296	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1036
0x700007C8	SARR_usGammaLutRGBOutdoor[0][14]	0x02D6	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1037
0x700007CA	SARR_usGammaLutRGBOutdoor[0][15]	0x033C	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1038
0x700007CC	SARR_usGammaLutRGBOutdoor[0][16]	0x038D	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1039
0x700007CE	SARR_usGammaLutRGBOutdoor[0][17]	0x03D0	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1040
0x700007D0	SARR_usGammaLutRGBOutdoor[0][18]	0x03F7	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1041

0x700007D2	SARR_usGammaLutRGBOutdoor[0][19]	0x03FF	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1042
0x700007D4	SARR_usGammaLutRGBOutdoor[1][0]	0x0000	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1043
0x700007D6	SARR_usGammaLutRGBOutdoor[1][1]	0x0001	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1044
0x700007D8	SARR_usGammaLutRGBOutdoor[1][2]	0x0007	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1045
0x700007DA	SARR_usGammaLutRGBOutdoor[1][3]	0x002D	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1046
0x700007DC	SARR_usGammaLutRGBOutdoor[1][4]	0x0075	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1047
0x700007DE	SARR_usGammaLutRGBOutdoor[1][5]	0x00E9	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1048
0x700007E0	SARR_usGammaLutRGBOutdoor[1][6]	0x0143	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1049
0x700007E2	SARR_usGammaLutRGBOutdoor[1][7]	0x016C	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1050
0x700007E4	SARR_usGammaLutRGBOutdoor[1][8]	0x0190	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1051
0x700007E6	SARR_usGammaLutRGBOutdoor[1][9]	0x01CC	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1052

0x700007E8	SARR_usGammaLutRGBOutdoor[1][10]	0x01FF	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1053
0x700007EA	SARR_usGammaLutRGBOutdoor[1][11]	0x022A	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1054
0x700007EC	SARR_usGammaLutRGBOutdoor[1][12]	0x0252	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1055
0x700007EE	SARR_usGammaLutRGBOutdoor[1][13]	0x0296	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1056
0x700007F0	SARR_usGammaLutRGBOutdoor[1][14]	0x02D6	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1057
0x700007F2	SARR_usGammaLutRGBOutdoor[1][15]	0x033C	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1058
0x700007F4	SARR_usGammaLutRGBOutdoor[1][16]	0x038D	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1059
0x700007F6	SARR_usGammaLutRGBOutdoor[1][17]	0x03D0	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1060
0x700007F8	SARR_usGammaLutRGBOutdoor[1][18]	0x03F7	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1061
0x700007FA	SARR_usGammaLutRGBOutdoor[1][19]	0x03FF	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1062
0x700007FC	SARR_usGammaLutRGBOutdoor[2][0]	0x0000	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1063

0x700007FE	SARR_usGammaLutRGBOutdoor[2][1]	0x0001	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1064
0x70000800	SARR_usGammaLutRGBOutdoor[2][2]	0x0007	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1065
0x70000802	SARR_usGammaLutRGBOutdoor[2][3]	0x002D	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1066
0x70000804	SARR_usGammaLutRGBOutdoor[2][4]	0x0075	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1067
0x70000806	SARR_usGammaLutRGBOutdoor[2][5]	0x00E9	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1068
0x70000808	SARR_usGammaLutRGBOutdoor[2][6]	0x0143	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1069
0x7000080A	SARR_usGammaLutRGBOutdoor[2][7]	0x016C	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1070
0x7000080C	SARR_usGammaLutRGBOutdoor[2][8]	0x0190	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1071
0x7000080E	SARR_usGammaLutRGBOutdoor[2][9]	0x01CC	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1072
0x70000810	SARR_usGammaLutRGBOutdoor[2][10]	0x01FF	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1073
0x70000812	SARR_usGammaLutRGBOutdoor[2][11]	0x022A	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1074

0x70000814	SARR_usGammaLutRGBOutdoor[2][12]	0x0252	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1075
0x70000816	SARR_usGammaLutRGBOutdoor[2][13]	0x0296	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1076
0x70000818	SARR_usGammaLutRGBOutdoor[2][14]	0x02D6	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1077
0x7000081A	SARR_usGammaLutRGBOutdoor[2][15]	0x033C	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1078
0x7000081C	SARR_usGammaLutRGBOutdoor[2][16]	0x038D	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1079
0x7000081E	SARR_usGammaLutRGBOutdoor[2][17]	0x03D0	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1080
0x70000820	SARR_usGammaLutRGBOutdoor[2][18]	0x03F7	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1081
0x70000822	SARR_usGammaLutRGBOutdoor[2][19]	0x03FF	2	RW	RGB Outdoor gamma LUT. First index relates to channel (R,G,B). Second index relates to input RGB brightness. Values are 10 bit 0-1082
0x70000824	seti_bUseOutdoorGamma	0x0001	2	RW	Outdoor gamma LUT On/Off register
0x70000EEC	setot_usSubSXBayerOffset	0x000A	2	RW	Make sensor X start offset to make in subsapling mode.
0x70000EEE	setot_usFullXBayerOffset	0x0014	2	RW	Make sensor X start offset to make in full size mode.
0x70000EF0	setot_usOffsetAddLine	0x0014	2	RW	Sensor minimum blank addline offset.
0x70000F2A	AFC_Default60Hz	0x0001	2	RW	Default frequency: 1 – 60Hz, 0 – 50Hz.
0x70000F2C	AFC_bUseDoubleQuant	0x0000	2	RW	0 : Using a integer shutter of flicker 1 : Using a doubled integer shutter of flicker

0x70000F32	AFC_usFrQuantNum	0x0001	2	RW	Use Standing wave Flicker. 1 : Use 1 Quant F/R 2: Use 2 Quant F/R
0x7000101C	awbb_IndoorGrZones_ m_BGrid[0]_m_left	0x02EE	2	RW	Indoor Zone Parameter
0x7000101E	awbb_IndoorGrZones_ m_BGrid[0]_m_right	0x0348	2	RW	Indoor Zone Parameter
0x70001020	awbb_IndoorGrZones_ m_BGrid[1]_m_left	0x02C6	2	RW	Indoor Zone Parameter
0x70001022	awbb_IndoorGrZones_ m_BGrid[1]_m_right	0x032A	2	RW	Indoor Zone Parameter
0x70001024	awbb_IndoorGrZones_ m_BGrid[2]_m_left	0x029E	2	RW	Indoor Zone Parameter
0x70001026	awbb_IndoorGrZones_ m_BGrid[2]_m_right	0x030C	2	RW	Indoor Zone Parameter
0x70001028	awbb_IndoorGrZones_ m_BGrid[3]_m_left	0x0280	2	RW	Indoor Zone Parameter
0x7000102A	awbb_IndoorGrZones_ m_BGrid[3]_m_right	0x02EE	2	RW	Indoor Zone Parameter
0x7000102C	awbb_IndoorGrZones_ m_BGrid[4]_m_left	0x0262	2	RW	Indoor Zone Parameter
0x7000102E	awbb_IndoorGrZones_ m_BGrid[4]_m_right	0x02D0	2	RW	Indoor Zone Parameter
0x70001030	awbb_IndoorGrZones_ m_BGrid[5]_m_left	0x0244	2	RW	Indoor Zone Parameter
0x70001032	awbb_IndoorGrZones_ m_BGrid[5]_m_right	0x02B2	2	RW	Indoor Zone Parameter
0x70001034	awbb_IndoorGrZones_ m_BGrid[6]_m_left	0x0226	2	RW	Indoor Zone Parameter
0x70001036	awbb_IndoorGrZones_ m_BGrid[6]_m_right	0x0294	2	RW	Indoor Zone Parameter
0x70001038	awbb_IndoorGrZones_ m_BGrid[7]_m_left	0x0203	2	RW	Indoor Zone Parameter
0x7000103A	awbb_IndoorGrZones_ m_BGrid[7]_m_right	0x0276	2	RW	Indoor Zone Parameter
0x7000103C	awbb_IndoorGrZones_ m_BGrid[8]_m_left	0x01E0	2	RW	Indoor Zone Parameter
0x7000103E	awbb_IndoorGrZones_	0x0258	2	RW	Indoor Zone Parameter

	m_BGrid[8]_m_right				
0x70001040	awbb_IndoorGrZones_ m_BGrid[9]_m_left	0x01BD	2	RW	Indoor Zone Parameter
0x70001042	awbb_IndoorGrZones_ m_BGrid[9]_m_right	0x0235	2	RW	Indoor Zone Parameter
0x70001044	awbb_IndoorGrZones_ m_BGrid[10]_m_left	0x01AE	2	RW	Indoor Zone Parameter
0x70001046	awbb_IndoorGrZones_ m_BGrid[10]_m_right	0x0212	2	RW	Indoor Zone Parameter
0x70001048	awbb_IndoorGrZones_ m_BGrid[11]_m_left	0x0190	2	RW	Indoor Zone Parameter
0x7000104A	awbb_IndoorGrZones_ m_BGrid[11]_m_right	0x01EF	2	RW	Indoor Zone Parameter
0x7000104C	awbb_IndoorGrZones_ m_BGrid[12]_m_left	0x0000	2	RW	Indoor Zone Parameter
0x7000104E	awbb_IndoorGrZones_ m_BGrid[12]_m_right	0x0000	2	RW	Indoor Zone Parameter
0x70001050	awbb_IndoorGrZones_ m_BGrid[13]_m_left	0x0000	2	RW	Indoor Zone Parameter
0x70001052	awbb_IndoorGrZones_ m_BGrid[13]_m_right	0x0000	2	RW	Indoor Zone Parameter
0x70001054	awbb_IndoorGrZones_ m_BGrid[14]_m_left	0x0000	2	RW	Indoor Zone Parameter
0x70001056	awbb_IndoorGrZones_ m_BGrid[14]_m_right	0x0000	2	RW	Indoor Zone Parameter
0x70001058	awbb_IndoorGrZones_ m_BGrid[15]_m_left	0x0000	2	RW	Indoor Zone Parameter
0x7000105A	awbb_IndoorGrZones_ m_BGrid[15]_m_right	0x0000	2	RW	Indoor Zone Parameter
0x7000105C	awbb_IndoorGrZones_ m_BGrid[16]_m_left	0x0000	2	RW	Indoor Zone Parameter
0x7000105E	awbb_IndoorGrZones_ m_BGrid[16]_m_right	0x0000	2	RW	Indoor Zone Parameter
0x70001060	awbb_IndoorGrZones_ m_BGrid[17]_m_left	0x0000	2	RW	Indoor Zone Parameter
0x70001062	awbb_IndoorGrZones_ m_BGrid[17]_m_right	0x0000	2	RW	Indoor Zone Parameter

0x70001064	awbb_IndoorGrZones_m_BGrid[18]_m_left	0x0000	2	RW	Indoor Zone Parameter
0x70001066	awbb_IndoorGrZones_m_BGrid[18]_m_right	0x0000	2	RW	Indoor Zone Parameter
0x70001068	awbb_IndoorGrZones_m_BGrid[19]_m_left	0x0000	2	RW	Indoor Zone Parameter
0x7000106A	awbb_IndoorGrZones_m_BGrid[19]_m_right	0x0000	2	RW	Indoor Zone Parameter
0x7000106C	awbb_IndoorGrZones_m_GridStep	0x00000005	4	RW	Indoor Zone Parameter
0x70001070	awbb_IndoorGrZones_ZInfo_m_GridSz	0x0000000C	4	RW	Indoor Zone Parameter
0x70001074	awbb_IndoorGrZones_m_Boffs	0x0000017C	4	RW	Indoor Zone Parameter
0x70001078	awbb_OutdoorGrZones_m_BGrid[0]_m_left	0x0230	2	RW	Outdoor Zone Parameter
0x7000107A	awbb_OutdoorGrZones_m_BGrid[0]_m_right	0x029E	2	RW	Outdoor Zone Parameter
0x7000107C	awbb_OutdoorGrZones_m_BGrid[1]_m_left	0x021C	2	RW	Outdoor Zone Parameter
0x7000107E	awbb_OutdoorGrZones_m_BGrid[1]_m_right	0x028A	2	RW	Outdoor Zone Parameter
0x70001080	awbb_OutdoorGrZones_m_BGrid[2]_m_left	0x0208	2	RW	Outdoor Zone Parameter
0x70001082	awbb_OutdoorGrZones_m_BGrid[2]_m_right	0x0276	2	RW	Outdoor Zone Parameter
0x70001084	awbb_OutdoorGrZones_m_BGrid[3]_m_left	0x01F4	2	RW	Outdoor Zone Parameter
0x70001086	awbb_OutdoorGrZones_m_BGrid[3]_m_right	0x0262	2	RW	Outdoor Zone Parameter
0x70001088	awbb_OutdoorGrZones_m_BGrid[4]_m_left	0x01E0	2	RW	Outdoor Zone Parameter
0x7000108A	awbb_OutdoorGrZones_m_BGrid[4]_m_right	0x024E	2	RW	Outdoor Zone Parameter
0x7000108C	awbb_OutdoorGrZones_m_BGrid[5]_m_left	0x01CC	2	RW	Outdoor Zone Parameter
0x7000108E	awbb_OutdoorGrZones_m_BGrid[5]_m_right	0x023A	2	RW	Outdoor Zone Parameter

0x70001090	awbb_OutdoorGrZones _m_BGrid[6]_m_left	0x01B8	2	RW	Outdoor Zone Parameter
0x70001092	awbb_OutdoorGrZones _m_BGrid[6]_m_right	0x0226	2	RW	Outdoor Zone Parameter
0x70001094	awbb_OutdoorGrZones _m_BGrid[7]_m_left	0x01B8	2	RW	Outdoor Zone Parameter
0x70001096	awbb_OutdoorGrZones _m_BGrid[7]_m_right	0x0212	2	RW	Outdoor Zone Parameter
0x70001098	awbb_OutdoorGrZones _m_BGrid[8]_m_left	0x01B8	2	RW	Outdoor Zone Parameter
0x7000109A	awbb_OutdoorGrZones _m_BGrid[8]_m_right	0x01FE	2	RW	Outdoor Zone Parameter
0x7000109C	awbb_OutdoorGrZones _m_BGrid[9]_m_left	0x01AE	2	RW	Outdoor Zone Parameter
0x7000109E	awbb_OutdoorGrZones _m_BGrid[9]_m_right	0x01EA	2	RW	Outdoor Zone Parameter
0x700010A0	awbb_OutdoorGrZones _m_BGrid[10]_m_left	0x0000	2	RW	Outdoor Zone Parameter
0x700010A2	awbb_OutdoorGrZones _m_BGrid[10]_m_right	0x0000	2	RW	Outdoor Zone Parameter
0x700010A4	awbb_OutdoorGrZones _m_BGrid[11]_m_left	0x0000	2	RW	Outdoor Zone Parameter
0x700010A6	awbb_OutdoorGrZones _m_BGrid[11]_m_right	0x0000	2	RW	Outdoor Zone Parameter
0x700010A8	awbb_OutdoorGrZones _m_GridStep	0x00000 004	4	RW	Outdoor Zone Parameter
0x700010AC	awbb_OutdoorGrZones _ZInfo_m_GridSz	0x00000 00A	4	RW	Outdoor Zone Parameter
0x700010B0	awbb_OutdoorGrZones _m_Boffs	0x00000 244	4	RW	Outdoor Zone Parameter
0x700010B4	awbb_LowBrGrZones_ m_BGrid[0]_m_left	0x034D	2	RW	Low Brightness Zone Parameter
0x700010B6	awbb_LowBrGrZones_ m_BGrid[0]_m_right	0x045B	2	RW	Low Brightness Zone Parameter
0x700010B8	awbb_LowBrGrZones_ m_BGrid[1]_m_left	0x02EA	2	RW	Low Brightness Zone Parameter
0x700010BA	awbb_LowBrGrZones_ m_BGrid[1]_m_right	0x0445	2	RW	Low Brightness Zone Parameter

0x700010BC	awbb_LowBrGrZones_ m_BGrid[2]_m_left	0x02A4	2	RW	Low Brightness Zone Parameter
0x700010BE	awbb_LowBrGrZones_ m_BGrid[2]_m_right	0x0428	2	RW	Low Brightness Zone Parameter
0x700010C0	awbb_LowBrGrZones_ m_BGrid[3]_m_left	0x0254	2	RW	Low Brightness Zone Parameter
0x700010C2	awbb_LowBrGrZones_ m_BGrid[3]_m_right	0x03FB	2	RW	Low Brightness Zone Parameter
0x700010C4	awbb_LowBrGrZones_ m_BGrid[4]_m_left	0x0207	2	RW	Low Brightness Zone Parameter
0x700010C6	awbb_LowBrGrZones_ m_BGrid[4]_m_right	0x03C7	2	RW	Low Brightness Zone Parameter
0x700010C8	awbb_LowBrGrZones_ m_BGrid[5]_m_left	0x01CF	2	RW	Low Brightness Zone Parameter
0x700010CA	awbb_LowBrGrZones_ m_BGrid[5]_m_right	0x0365	2	RW	Low Brightness Zone Parameter
0x700010CC	awbb_LowBrGrZones_ m_BGrid[6]_m_left	0x019E	2	RW	Low Brightness Zone Parameter
0x700010CE	awbb_LowBrGrZones_ m_BGrid[6]_m_right	0x031A	2	RW	Low Brightness Zone Parameter
0x700010D0	awbb_LowBrGrZones_ m_BGrid[7]_m_left	0x0170	2	RW	Low Brightness Zone Parameter
0x700010D2	awbb_LowBrGrZones_ m_BGrid[7]_m_right	0x02DB	2	RW	Low Brightness Zone Parameter
0x700010D4	awbb_LowBrGrZones_ m_BGrid[8]_m_left	0x0149	2	RW	Low Brightness Zone Parameter
0x700010D6	awbb_LowBrGrZones_ m_BGrid[8]_m_right	0x029E	2	RW	Low Brightness Zone Parameter
0x700010D8	awbb_LowBrGrZones_ m_BGrid[9]_m_left	0x0122	2	RW	Low Brightness Zone Parameter
0x700010DA	awbb_LowBrGrZones_ m_BGrid[9]_m_right	0x025D	2	RW	Low Brightness Zone Parameter
0x700010DC	awbb_LowBrGrZones_ m_BGrid[10]_m_left	0x00FE	2	RW	Low Brightness Zone Parameter
0x700010DE	awbb_LowBrGrZones_ m_BGrid[10]_m_right	0x022E	2	RW	Low Brightness Zone Parameter
0x700010E0	awbb_LowBrGrZones_ m_BGrid[11]_m_left	0x00E4	2	RW	Low Brightness Zone Parameter

0x700010E2	awbb_LowBrGrZones_m_BGrid[11]_m_right	0x01F1	2	RW	Low Brightness Zone Parameter
0x700010E4	awbb_LowBrGrZones_m_GridStep	0x00000006	4	RW	Low Brightness Zone Parameter
0x700010E8	awbb_LowBrGrZones_ZInfo_m_GridSz	0x0000000C	4	RW	Low Brightness Zone Parameter
0x700010EC	awbb_LowBrGrZones_m_Boffs	0x000000D6	4	RW	Low Brightness Zone Parameter
0x700010F0	awbb_CrclLowT_R_c	0x0000034B	4	RW	Low Temperature circle zone parameter
0x700010F4	awbb_CrclLowT_B_c	0x0000019E	4	RW	Low Temperature circle zone parameter
0x700010F8	awbb_CrclLowT_Rad_c	0x0000EF10	4	RW	Low Temperature circle zone parameter
0x700011B0	awbb_FaceZone_m_BGrid[0]_m_left	0x0334	2	RW	Face color zone parameter
0x700011B2	awbb_FaceZone_m_BGrid[0]_m_right	0x0352	2	RW	Face color zone parameter
0x700011B4	awbb_FaceZone_m_BGrid[1]_m_left	0x0316	2	RW	Face color zone parameter
0x700011B6	awbb_FaceZone_m_BGrid[1]_m_right	0x0334	2	RW	Face color zone parameter
0x700011B8	awbb_FaceZone_m_BGrid[2]_m_left	0x02F8	2	RW	Face color zone parameter
0x700011BA	awbb_FaceZone_m_BGrid[2]_m_right	0x0316	2	RW	Face color zone parameter
0x700011BC	awbb_FaceZone_m_BGrid[3]_m_left	0x02DA	2	RW	Face color zone parameter
0x700011BE	awbb_FaceZone_m_BGrid[3]_m_right	0x02F8	2	RW	Face color zone parameter
0x700011C0	awbb_FaceZone_m_BGrid[4]_m_left	0x02B7	2	RW	Face color zone parameter
0x700011C2	awbb_FaceZone_m_BGrid[4]_m_right	0x02DA	2	RW	Face color zone parameter
0x700011C4	awbb_FaceZone_m_BGrid[5]_m_left	0x0294	2	RW	Face color zone parameter
0x700011C6	awbb_FaceZone_m_BGrid[5]_m_right	0x02BC	2	RW	Face color zone parameter

0x700011C8	awbb_FaceZone_m_BGrid[6]_m_left	0x026C	2	RW	Face color zone parameter
0x700011CA	awbb_FaceZone_m_BGrid[6]_m_right	0x0294	2	RW	Face color zone parameter
0x700011CC	awbb_FaceZone_m_BGrid[7]_m_left	0x0249	2	RW	Face color zone parameter
0x700011CE	awbb_FaceZone_m_BGrid[7]_m_right	0x0271	2	RW	Face color zone parameter
0x700011D0	awbb_FaceZone_m_BGrid[8]_m_left	0x0226	2	RW	Face color zone parameter
0x700011D2	awbb_FaceZone_m_BGrid[8]_m_right	0x024E	2	RW	Face color zone parameter
0x700011D4	awbb_FaceZone_m_BGrid[9]_m_left	0x0000	2	RW	Face color zone parameter
0x700011D6	awbb_FaceZone_m_BGrid[9]_m_right	0x0000	2	RW	Face color zone parameter
0x700011D8	awbb_FaceZone_ZInfo_m_GridStep	0x00000005	4	RW	Face color zone parameter
0x700011DC	awbb_FaceZone_ZInfo_m_GridSz	0x00000009	4	RW	Face color zone parameter
0x700011E0	awbb_FaceZone_ZInfo_m_Boffs	0x0000015E	4	RW	Face color zone parameter
0x700011E4	awbb_FaceZone_y_threshold[0]	0x0010	2	RW	Face color zone parameter
0x700011E6	awbb_FaceZone_y_threshold[1]	0x0050	2	RW	Face color zone parameter
0x700011E8	awbb_FaceZone_y_threshold[2]	0x0080	2	RW	Face color zone parameter
0x700011EA	awbb_FaceZone_y_threshold[3]	0x00B0	2	RW	Face color zone parameter
0x700011F0	awbb_IntcR	0x0130	2	RW	White locus tuning parameter r
0x700011F2	awbb_IntcB	0x0135	2	RW	White locus tuning parameter b
0x700011F8	awbb_MinNumOfInitialPatchesB	0x0014	2	RW	Minimum number of patches tuning parameter for general scene detection
0x700011FA	awbb_MinNumOfLowBrInitialPatchesB	0x0014	2	RW	Minimum number of patches tuning parameter for low brightness scene detection

0x700011FC	awbb_MinNumOfFinalPatches	0x000C	2	RW	Minimum number of patches tuning parameter for general scene detection
0x700011FE	awbb_MinNumOfLowBrFinalPatches	0x001E	2	RW	Minimum number of patches tuning parameter for LowBr scene detection
0x70001200	awbb_MinNumOfLowBr0_FinalPatches	0x0046	2	RW	Minimum number of patches tuning parameter for LowBr scene detection
0x70001202	awbb_LowBr0_PatchNumZone	0x0019	2	RW	Minimum number of patches tuning parameter for LowBr scene detection
0x70001204	awbb_MinNumOfOutdoorPatches	0x000C	2	RW	Minimum number of patches tuning parameter for Outdoor scene detection
0x70001228	awbb_YThreshHigh	0x00A0	2	RW	Awb Luminance level threshold
0x7000122A	awbb_YThreshLow_Norm	0x0020	2	RW	Awb Luminance level threshold
0x7000122C	awbb_YThreshLow_Low	0x0010	2	RW	Awb Luminance level threshold
0x7000122E	awbb_SCDQueueNormBr_dwMinThr	0x001E	2	RW	Scnen Detection smothing queue parameter
0x70001230	awbb_SCDQueueNormBr_dwMaxThr	0x05DC	2	RW	Scnen Detection smothing queue parameter
0x70001232	awbb_SCDQueueNormBr_dConvSpeed	0x00A0	2	RW	Scnen Detection smothing queue parameter
0x70001234	awbb_SCDQueueRminusB_dwMinThr	0x000F	2	RW	Scnen Detection smothing queue parameter
0x70001236	awbb_SCDQueueRminusB_dwMaxThr	0x0028	2	RW	Scnen Detection smothing queue parameter
0x70001238	awbb_SCDQueueRminusB_dConvSpeed	0x00A0	2	RW	Scnen Detection smothing queue parameter
0x7000123A	awbb_SDFilterSize	0x0004	2	RW	Scnen Detection smothing queue parameter
0x7000123C	awbb_SCDetectionMap_SEC_SceneDetectionMap[0][0]	0x00	1	RW	outdoor scene weight LUT for AWB scene detection map
0x7000123D	awbb_SCDetectionMap_SEC_SceneDetectionMap[0][1]	0x00	1	RW	outdoor scene weight LUT for AWB scene detection map
0x7000123E	awbb_SCDetectionMap_SEC_SceneDetectionMap[0][2]	0x00	1	RW	outdoor scene weight LUT for AWB scene detection map
0x7000123F	awbb_SCDetectionMap_SEC_SceneDetection	0x00	1	RW	outdoor scene weight LUT for AWB scene

	Map[0][3]				detection map
0x70001240	awbb_SCDetectionMap _SEC_SceneDetection Map[0][4]	0x00	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001241	awbb_SCDetectionMap _SEC_SceneDetection Map[1][0]	0x00	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001242	awbb_SCDetectionMap _SEC_SceneDetection Map[1][1]	0x00	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001243	awbb_SCDetectionMap _SEC_SceneDetection Map[1][2]	0x00	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001244	awbb_SCDetectionMap _SEC_SceneDetection Map[1][3]	0x00	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001245	awbb_SCDetectionMap _SEC_SceneDetection Map[1][4]	0x00	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001246	awbb_SCDetectionMap _SEC_SceneDetection Map[2][0]	0x00	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001247	awbb_SCDetectionMap _SEC_SceneDetection Map[2][1]	0x00	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001248	awbb_SCDetectionMap _SEC_SceneDetection Map[2][2]	0x00	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001249	awbb_SCDetectionMap _SEC_SceneDetection Map[2][3]	0x00	1	RW	outdoor scene weight LUT for AWB scene detection map
0x7000124A	awbb_SCDetectionMap _SEC_SceneDetection Map[2][4]	0x00	1	RW	outdoor scene weight LUT for AWB scene detection map
0x7000124B	awbb_SCDetectionMap _SEC_SceneDetection Map[3][0]	0x00	1	RW	outdoor scene weight LUT for AWB scene detection map
0x7000124C	awbb_SCDetectionMap _SEC_SceneDetection Map[3][1]	0x00	1	RW	outdoor scene weight LUT for AWB scene detection map
0x7000124D	awbb_SCDetectionMap _SEC_SceneDetection	0x00	1	RW	outdoor scene weight LUT for AWB scene

	Map[3][2]				detection map
0x7000124E	awbb_SCDetectionMap _SEC_SceneDetection Map[3][3]	0x00	1	RW	outdoor scene weight LUT for AWB scene detection map
0x7000124F	awbb_SCDetectionMap _SEC_SceneDetection Map[3][4]	0x00	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001250	awbb_SCDetectionMap _SEC_SceneDetection Map[4][0]	0x00	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001251	awbb_SCDetectionMap _SEC_SceneDetection Map[4][1]	0x00	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001252	awbb_SCDetectionMap _SEC_SceneDetection Map[4][2]	0x00	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001253	awbb_SCDetectionMap _SEC_SceneDetection Map[4][3]	0x00	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001254	awbb_SCDetectionMap _SEC_SceneDetection Map[4][4]	0x00	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001255	awbb_SCDetectionMap _SEC_SceneDetection Map[5][0]	0x05	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001256	awbb_SCDetectionMap _SEC_SceneDetection Map[5][1]	0x55	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001257	awbb_SCDetectionMap _SEC_SceneDetection Map[5][2]	0x55	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001258	awbb_SCDetectionMap _SEC_SceneDetection Map[5][3]	0x55	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001259	awbb_SCDetectionMap _SEC_SceneDetection Map[5][4]	0x54	1	RW	outdoor scene weight LUT for AWB scene detection map
0x7000125A	awbb_SCDetectionMap _SEC_SceneDetection Map[6][0]	0x55	1	RW	outdoor scene weight LUT for AWB scene detection map
0x7000125B	awbb_SCDetectionMap _SEC_SceneDetection	0xAA	1	RW	outdoor scene weight LUT for AWB scene

	Map[6][1]				detection map
0x7000125C	awbb_SCDetectionMap _SEC_SceneDetection Map[6][2]	0xAA	1	RW	outdoor scene weight LUT for AWB scene detection map
0x7000125D	awbb_SCDetectionMap _SEC_SceneDetection Map[6][3]	0xAA	1	RW	outdoor scene weight LUT for AWB scene detection map
0x7000125E	awbb_SCDetectionMap _SEC_SceneDetection Map[6][4]	0x54	1	RW	outdoor scene weight LUT for AWB scene detection map
0x7000125F	awbb_SCDetectionMap _SEC_SceneDetection Map[7][0]	0xBF	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001260	awbb_SCDetectionMap _SEC_SceneDetection Map[7][1]	0xFF	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001261	awbb_SCDetectionMap _SEC_SceneDetection Map[7][2]	0xFF	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001262	awbb_SCDetectionMap _SEC_SceneDetection Map[7][3]	0xFE	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001263	awbb_SCDetectionMap _SEC_SceneDetection Map[7][4]	0x54	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001264	awbb_SCDetectionMap _SEC_SceneDetection Map[8][0]	0x6F	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001265	awbb_SCDetectionMap _SEC_SceneDetection Map[8][1]	0xFF	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001266	awbb_SCDetectionMap _SEC_SceneDetection Map[8][2]	0xFF	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001267	awbb_SCDetectionMap _SEC_SceneDetection Map[8][3]	0xFE	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001268	awbb_SCDetectionMap _SEC_SceneDetection Map[8][4]	0x54	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001269	awbb_SCDetectionMap _SEC_SceneDetection	0x1B	1	RW	outdoor scene weight LUT for AWB scene

	Map[9][0]				detection map
0x7000126A	awbb_SCDetectionMap_SEC_SceneDetectionMap[9][1]	0xFF	1	RW	outdoor scene weight LUT for AWB scene detection map
0x7000126B	awbb_SCDetectionMap_SEC_SceneDetectionMap[9][2]	0xFF	1	RW	outdoor scene weight LUT for AWB scene detection map
0x7000126C	awbb_SCDetectionMap_SEC_SceneDetectionMap[9][3]	0xFE	1	RW	outdoor scene weight LUT for AWB scene detection map
0x7000126D	awbb_SCDetectionMap_SEC_SceneDetectionMap[9][4]	0x54	1	RW	outdoor scene weight LUT for AWB scene detection map
0x7000126E	awbb_SCDetectionMap_SEC_SceneDetectionMap[10][0]	0x06	1	RW	outdoor scene weight LUT for AWB scene detection map
0x7000126F	awbb_SCDetectionMap_SEC_SceneDetectionMap[10][1]	0xFF	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001270	awbb_SCDetectionMap_SEC_SceneDetectionMap[10][2]	0xFF	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001271	awbb_SCDetectionMap_SEC_SceneDetectionMap[10][3]	0xFE	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001272	awbb_SCDetectionMap_SEC_SceneDetectionMap[10][4]	0x54	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001273	awbb_SCDetectionMap_SEC_SceneDetectionMap[11][0]	0x01	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001274	awbb_SCDetectionMap_SEC_SceneDetectionMap[11][1]	0xBF	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001275	awbb_SCDetectionMap_SEC_SceneDetectionMap[11][2]	0xBF	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001276	awbb_SCDetectionMap_SEC_SceneDetectionMap[11][3]	0xBE	1	RW	outdoor scene weight LUT for AWB scene detection map
0x70001277	awbb_SCDetectionMap_SEC_SceneDetection	0x54	1	RW	outdoor scene weight LUT for AWB scene

	Map[11][4]				detection map
0x70001278	awbb_SCDetectionMap_SEC_StartR_B	0xFE82	2	RW	outdoor scene weight LUT parameter
0x7000127A	awbb_SCDetectionMap_SEC_StepR_B	0x001E	2	RW	outdoor scene weight LUT parameter
0x7000127C	awbb_SCDetectionMap_SEC_SunnyNB	0x0E74	2	RW	outdoor scene weight LUT parameter
0x7000127E	awbb_SCDetectionMap_SEC_StepNB	0x0122	2	RW	outdoor scene weight LUT parameter
0x70001280	awbb_SCDetectionMap_SEC_LowTempR_B	0x00E4	2	RW	Low temp threshold
0x70001282	awbb_SCDetectionMap_SEC_SunnyNBZone	0x0096	2	RW	Sunny threshold
0x70001284	awbb_SCDetectionMap_SEC_LowTempR_BZone	0x000E	2	RW	Low temp threshold
0x700013A4	awbb_GridCorr_R[0][0]	0xFFFE	2	RW	WB grid correction tuning parameter
0x700013A6	awbb_GridCorr_R[0][1]	0xFFFE	2	RW	WB grid correction tuning parameter
0x700013A8	awbb_GridCorr_R[0][2]	0x0000	2	RW	WB grid correction tuning parameter
0x700013AA	awbb_GridCorr_R[0][3]	0x0000	2	RW	WB grid correction tuning parameter
0x700013AC	awbb_GridCorr_R[0][4]	0x0000	2	RW	WB grid correction tuning parameter
0x700013AE	awbb_GridCorr_R[0][5]	0x0000	2	RW	WB grid correction tuning parameter
0x700013B0	awbb_GridCorr_R[1][0]	0xFFFD	2	RW	WB grid correction tuning parameter
0x700013B2	awbb_GridCorr_R[1][1]	0xFFFD	2	RW	WB grid correction tuning parameter
0x700013B4	awbb_GridCorr_R[1][2]	0x0000	2	RW	WB grid correction tuning parameter
0x700013B6	awbb_GridCorr_R[1][3]	0x0000	2	RW	WB grid correction tuning parameter
0x700013B8	awbb_GridCorr_R[1][4]	0x0000	2	RW	WB grid correction tuning parameter
0x700013BA	awbb_GridCorr_R[1][5]	0x0000	2	RW	WB grid correction tuning parameter
0x700013BC	awbb_GridCorr_R[2][0]	0xFFFC	2	RW	WB grid correction tuning parameter
0x700013BE	awbb_GridCorr_R[2][1]	0xFFFC	2	RW	WB grid correction tuning parameter
0x700013C0	awbb_GridCorr_R[2][2]	0x0000	2	RW	WB grid correction tuning parameter
0x700013C2	awbb_GridCorr_R[2][3]	0x0000	2	RW	WB grid correction tuning parameter

0x700013C4	awbb_GridCorr_R[2][4]	0x0000	2	RW	WB grid correction tuning parameter
0x700013C6	awbb_GridCorr_R[2][5]	0x0000	2	RW	WB grid correction tuning parameter
0x700013C8	awbb_GridCorr_B[0][0]	0x000C	2	RW	WB grid correction tuning parameter
0x700013CA	awbb_GridCorr_B[0][1]	0x0006	2	RW	WB grid correction tuning parameter
0x700013CC	awbb_GridCorr_B[0][2]	0x0000	2	RW	WB grid correction tuning parameter
0x700013CE	awbb_GridCorr_B[0][3]	0x0000	2	RW	WB grid correction tuning parameter
0x700013D0	awbb_GridCorr_B[0][4]	0x0000	2	RW	WB grid correction tuning parameter
0x700013D2	awbb_GridCorr_B[0][5]	0x0000	2	RW	WB grid correction tuning parameter
0x700013D4	awbb_GridCorr_B[1][0]	0x000C	2	RW	WB grid correction tuning parameter
0x700013D6	awbb_GridCorr_B[1][1]	0x0006	2	RW	WB grid correction tuning parameter
0x700013D8	awbb_GridCorr_B[1][2]	0x0000	2	RW	WB grid correction tuning parameter
0x700013DA	awbb_GridCorr_B[1][3]	0x0000	2	RW	WB grid correction tuning parameter
0x700013DC	awbb_GridCorr_B[1][4]	0x0000	2	RW	WB grid correction tuning parameter
0x700013DE	awbb_GridCorr_B[1][5]	0x0000	2	RW	WB grid correction tuning parameter
0x700013E0	awbb_GridCorr_B[2][0]	0x000C	2	RW	WB grid correction tuning parameter
0x700013E2	awbb_GridCorr_B[2][1]	0x0006	2	RW	WB grid correction tuning parameter
0x700013E4	awbb_GridCorr_B[2][2]	0x0000	2	RW	WB grid correction tuning parameter
0x700013E6	awbb_GridCorr_B[2][3]	0x0000	2	RW	WB grid correction tuning parameter
0x700013E8	awbb_GridCorr_B[2][4]	0x0000	2	RW	WB grid correction tuning parameter
0x700013EA	awbb_GridCorr_B[2][5]	0x0000	2	RW	WB grid correction tuning parameter
0x700013EC	awbb_GridCorr_R_Out[0][0]	0xFFFE	2	RW	WB grid correction tuning parameter
0x700013EE	awbb_GridCorr_R_Out[0][1]	0xFFFE	2	RW	WB grid correction tuning parameter
0x700013F0	awbb_GridCorr_R_Out[0][2]	0x0000	2	RW	WB grid correction tuning parameter
0x700013F2	awbb_GridCorr_R_Out[0][3]	0x0000	2	RW	WB grid correction tuning parameter
0x700013F4	awbb_GridCorr_R_Out[0][4]	0x0000	2	RW	WB grid correction tuning parameter
0x700013F6	awbb_GridCorr_R_Out[	0x0000	2	RW	WB grid correction tuning parameter

	0][5]				
0x700013F8	awbb_GridCorr_R_Out[1][0]	0xFFFD	2	RW	WB grid correction tuning parameter
0x700013FA	awbb_GridCorr_R_Out[1][1]	0xFFFD	2	RW	WB grid correction tuning parameter
0x700013FC	awbb_GridCorr_R_Out[1][2]	0x0000	2	RW	WB grid correction tuning parameter
0x700013FE	awbb_GridCorr_R_Out[1][3]	0x0000	2	RW	WB grid correction tuning parameter
0x70001400	awbb_GridCorr_R_Out[1][4]	0x0000	2	RW	WB grid correction tuning parameter
0x70001402	awbb_GridCorr_R_Out[1][5]	0x0000	2	RW	WB grid correction tuning parameter
0x70001404	awbb_GridCorr_R_Out[2][0]	0xFFFC	2	RW	WB grid correction tuning parameter
0x70001406	awbb_GridCorr_R_Out[2][1]	0xFFFC	2	RW	WB grid correction tuning parameter
0x70001408	awbb_GridCorr_R_Out[2][2]	0x0000	2	RW	WB grid correction tuning parameter
0x7000140A	awbb_GridCorr_R_Out[2][3]	0x0000	2	RW	WB grid correction tuning parameter
0x7000140C	awbb_GridCorr_R_Out[2][4]	0x0000	2	RW	WB grid correction tuning parameter
0x7000140E	awbb_GridCorr_R_Out[2][5]	0x0000	2	RW	WB grid correction tuning parameter
0x70001410	awbb_GridCorr_B_Out[0][0]	0x000C	2	RW	WB grid correction tuning parameter
0x70001412	awbb_GridCorr_B_Out[0][1]	0x0006	2	RW	WB grid correction tuning parameter
0x70001414	awbb_GridCorr_B_Out[0][2]	0x0000	2	RW	WB grid correction tuning parameter
0x70001416	awbb_GridCorr_B_Out[0][3]	0x0000	2	RW	WB grid correction tuning parameter
0x70001418	awbb_GridCorr_B_Out[0][4]	0x0000	2	RW	WB grid correction tuning parameter
0x7000141A	awbb_GridCorr_B_Out[0][5]	0x0000	2	RW	WB grid correction tuning parameter

0x7000141C	awbb_GridCorr_B_Out[1][0]	0x000C	2	RW	WB grid correction tuning parameter
0x7000141E	awbb_GridCorr_B_Out[1][1]	0x0006	2	RW	WB grid correction tuning parameter
0x70001420	awbb_GridCorr_B_Out[1][2]	0x0000	2	RW	WB grid correction tuning parameter
0x70001422	awbb_GridCorr_B_Out[1][3]	0x0000	2	RW	WB grid correction tuning parameter
0x70001424	awbb_GridCorr_B_Out[1][4]	0x0000	2	RW	WB grid correction tuning parameter
0x70001426	awbb_GridCorr_B_Out[1][5]	0x0000	2	RW	WB grid correction tuning parameter
0x70001428	awbb_GridCorr_B_Out[2][0]	0x000C	2	RW	WB grid correction tuning parameter
0x7000142A	awbb_GridCorr_B_Out[2][1]	0x0006	2	RW	WB grid correction tuning parameter
0x7000142C	awbb_GridCorr_B_Out[2][2]	0x0000	2	RW	WB grid correction tuning parameter
0x7000142E	awbb_GridCorr_B_Out[2][3]	0x0000	2	RW	WB grid correction tuning parameter
0x70001430	awbb_GridCorr_B_Out[2][4]	0x0000	2	RW	WB grid correction tuning parameter
0x70001432	awbb_GridCorr_B_Out[2][5]	0x0000	2	RW	WB grid correction tuning parameter
0x70001434	awbb_GridConst_1[0]	0x0338	2	RW	WB grid correction tuning parameter
0x70001436	awbb_GridConst_1[1]	0x0358	2	RW	WB grid correction tuning parameter
0x70001438	awbb_GridConst_1[2]	0x0378	2	RW	WB grid correction tuning parameter
0x7000143A	awbb_GridConst_2[0]	0x0F50	2	RW	WB grid correction tuning parameter
0x7000143C	awbb_GridConst_2[1]	0x0F94	2	RW	WB grid correction tuning parameter
0x7000143E	awbb_GridConst_2[2]	0x0FD8	2	RW	WB grid correction tuning parameter
0x70001440	awbb_GridConst_2[3]	0x103C	2	RW	WB grid correction tuning parameter
0x70001442	awbb_GridConst_2[4]	0x10C8	2	RW	WB grid correction tuning parameter
0x70001444	awbb_GridConst_2[5]	0x11B8	2	RW	WB grid correction tuning parameter
0x70001446	awbb_GridCoeff_R_1	0x02C4	2	RW	WB grid correction tuning parameter

0x70001448	awbb_GridCoeff_B_1	0x02E4	2	RW	WB grid correction tuning parameter
0x7000144A	awbb_GridCoeff_R_2	0x0308	2	RW	WB grid correction tuning parameter
0x7000144C	awbb_GridCoeff_B_2	0x029C	2	RW	WB grid correction tuning parameter
0x7000144E	awbb_RGainOff	0x0000	2	RW	R WB gain offset
0x70001450	awbb_BGainOff	0x0000	2	RW	B WB gain offset
0x70001452	awbb_GGainOff	0x0000	2	RW	G WB gain offset
0x7000145E	awbb_GainsInit[0]	0x053C	2	RW	Initial WB gain value
0x70001460	awbb_GainsInit[1]	0x0400	2	RW	Initial WB gain value
0x70001462	awbb_GainsInit[2]	0x055C	2	RW	Initial WB gain value
0x70001464	awbb_WpFilterMinThr	0x001E	2	RW	White point filter control parameter
0x70001466	awbb_WpFilterMaxThr	0x0190	2	RW	White point filter control parameter
0x70001468	awbb_WpFilterCoef	0x00A0	2	RW	White point filter control parameter
0x7000146A	awbb_WpFilterSize	0x0004	2	RW	White point filter control parameter
0x7000146C	awbb_GridEnable	0x0000	2	RW	AWB grid correction mode control parameter
0x7000146E	awbb_otp_disable	0x0001	2	RW	AWB Module compensation using external memory disable
0x70001484	TVAR_ae_BrAve	0x003D	2	RW	The target average brightness
0x70001492	ae_WeightTbl_16[0]	0x0101	2	RW	AE WeightTbl
0x70001494	ae_WeightTbl_16[1]	0x0101	2	RW	AE WeightTbl
0x70001496	ae_WeightTbl_16[2]	0x0101	2	RW	AE WeightTbl
0x70001498	ae_WeightTbl_16[3]	0x0101	2	RW	AE WeightTbl
0x7000149A	ae_WeightTbl_16[4]	0x0101	2	RW	AE WeightTbl
0x7000149C	ae_WeightTbl_16[5]	0x0201	2	RW	AE WeightTbl
0x7000149E	ae_WeightTbl_16[6]	0x0102	2	RW	AE WeightTbl
0x700014A0	ae_WeightTbl_16[7]	0x0101	2	RW	AE WeightTbl
0x700014A2	ae_WeightTbl_16[8]	0x0101	2	RW	AE WeightTbl
0x700014A4	ae_WeightTbl_16[9]	0x0202	2	RW	AE WeightTbl
0x700014A6	ae_WeightTbl_16[10]	0x0202	2	RW	AE WeightTbl

0x700014A8	ae_WeightTbl_16[11]	0x0101	2	RW	AE WeightTbl
0x700014AA	ae_WeightTbl_16[12]	0x0101	2	RW	AE WeightTbl
0x700014AC	ae_WeightTbl_16[13]	0x0802	2	RW	AE WeightTbl
0x700014AE	ae_WeightTbl_16[14]	0x0208	2	RW	AE WeightTbl
0x700014B0	ae_WeightTbl_16[15]	0x0101	2	RW	AE WeightTbl
0x700014B2	ae_WeightTbl_16[16]	0x0201	2	RW	AE WeightTbl
0x700014B4	ae_WeightTbl_16[17]	0x0A04	2	RW	AE WeightTbl
0x700014B6	ae_WeightTbl_16[18]	0x040A	2	RW	AE WeightTbl
0x700014B8	ae_WeightTbl_16[19]	0x0102	2	RW	AE WeightTbl
0x700014BA	ae_WeightTbl_16[20]	0x0402	2	RW	AE WeightTbl
0x700014BC	ae_WeightTbl_16[21]	0x0805	2	RW	AE WeightTbl
0x700014BE	ae_WeightTbl_16[22]	0x0508	2	RW	AE WeightTbl
0x700014C0	ae_WeightTbl_16[23]	0x0204	2	RW	AE WeightTbl
0x700014C2	ae_WeightTbl_16[24]	0x0403	2	RW	AE WeightTbl
0x700014C4	ae_WeightTbl_16[25]	0x0505	2	RW	AE WeightTbl
0x700014C6	ae_WeightTbl_16[26]	0x0505	2	RW	AE WeightTbl
0x700014C8	ae_WeightTbl_16[27]	0x0304	2	RW	AE WeightTbl
0x700014CA	ae_WeightTbl_16[28]	0x0302	2	RW	AE WeightTbl
0x700014CC	ae_WeightTbl_16[29]	0x0303	2	RW	AE WeightTbl
0x700014CE	ae_WeightTbl_16[30]	0x0303	2	RW	AE WeightTbl
0x700014D0	ae_WeightTbl_16[31]	0x0203	2	RW	AE WeightTbl
0x70001798	jpeg_BrcMinQuality	0x0010	2	RW	Minimum quality factor if the user will be using BRC
0x7000179E	jpeg_BppAutoBrcSpoofPercentage	0x00DA	2	RW	The percentage of JPEG size in the Spoof mode (Format of this register is 8.8 fixed point) If the user uses the "AUTO_SPOOF_BRC" mode, Target size of JPEG will be decided as below : Target JPEG size = Spoof total size * (this register value / 256) – Int
0x700017A0	jpeg_BrcFactorForHalfSizes[0]	0x0114	2	RW	Tuning value for BRC

0x700017A2	jpeg_BrcFactorForHalfSizes[1]	0x0166	2	RW	Tuning value for BRC
0x700017A4	jpeg_BrcFactorForHalfSizes[2]	0x011A	2	RW	Tuning value for BRC
0x700017A6	jpeg_BrcInspectionCropToFull	0x0115	2	RW	Tuning value for BRC
0x700017A8	jpeg_QFvsFSbase[0]	0x0000	2	RW	Tuning value for BRC
0x700017AA	jpeg_QFvsFSbase[1]	0x007A	2	RW	Tuning value for BRC
0x700017AC	jpeg_QFvsFSbase[2]	0x00A1	2	RW	Tuning value for BRC
0x700017AE	jpeg_QFvsFSbase[3]	0x00C5	2	RW	Tuning value for BRC
0x700017B0	jpeg_QFvsFSbase[4]	0x00E3	2	RW	Tuning value for BRC
0x700017B2	jpeg_QFvsFSbase[5]	0x0100	2	RW	Tuning value for BRC
0x700017B4	jpeg_QFvsFSbase[6]	0x0126	2	RW	Tuning value for BRC
0x700017B6	jpeg_QFvsFSbase[7]	0x015E	2	RW	Tuning value for BRC
0x700017B8	jpeg_QFvsFSbase[8]	0x01BE	2	RW	Tuning value for BRC
0x700017BA	jpeg_QFvsFSbase[9]	0x02DE	2	RW	Tuning value for BRC
0x700017BC	jpeg_HighQFvsFSbase[0]	0x02DE	2	RW	Tuning value for BRC
0x700017BE	jpeg_HighQFvsFSbase[1]	0x0313	2	RW	Tuning value for BRC
0x700017C0	jpeg_HighQFvsFSbase[2]	0x034F	2	RW	Tuning value for BRC
0x700017C2	jpeg_HighQFvsFSbase[3]	0x0397	2	RW	Tuning value for BRC
0x700017C4	jpeg_HighQFvsFSbase[4]	0x03F4	2	RW	Tuning value for BRC
0x700017C6	jpeg_HighQFvsFSbase[5]	0x047F	2	RW	Tuning value for BRC
0x700017C8	jpeg_HighQFvsFSbase[6]	0x055A	2	RW	Tuning value for BRC
0x700017CA	jpeg_HighQFvsFSbase[7]	0x05E6	2	RW	Tuning value for BRC
0x700017CC	jpeg_HighQFvsFSbase[8]	0x0842	2	RW	Tuning value for BRC

0x700017CE	jpeg_HighQFvsFSbase[9]	0x0C00	2	RW	Tuning value for BRC
0x700017D0	jpeg_HighQFvsFSbase[10]	0x0C1C	2	RW	Tuning value for BRC
0x700017D4	jpeg_pLumQT	0x00002EBF	4	RW	The address of JPEG Q table for luma
0x700017D8	jpeg_pChromQT	0x00002EFF	4	RW	The address of JPEG Q table for chroma
0x700017DC	jpeg_ManualMBCV	0x0000	2	RW	0 : Using auto MBCV value Others : Using custome value for MBCV
0x70001826	fls_afl_FlashWP_Weight2[0]	0x0100	2	RW	Flash AWB tuning weight value.
0x70001828	fls_afl_FlashWP_Weight2[1]	0x00A0	2	RW	Flash AWB tuning weight value.
0x7000182A	fls_afl_FlashWP_Weight2[2]	0x0080	2	RW	Flash AWB tuning weight value.
0x7000182C	fls_afl_FlashWP_Weight2[3]	0x0040	2	RW	Flash AWB tuning weight value.
0x7000182E	fls_afl_FlashWP_Weight2[4]	0x0020	2	RW	Flash AWB tuning weight value.
0x70001830	fls_afl_FlashWP_Lei_Thres2[0]	0x0100	2	RW	Flash AWB tuning threshold value.
0x70001832	fls_afl_FlashWP_Lei_Thres2[1]	0x00A0	2	RW	Flash AWB tuning threshold value.
0x70001834	fls_afl_FlashWP_Lei_Thres2[2]	0x0080	2	RW	Flash AWB tuning threshold value.
0x70001836	fls_afl_FlashWP_Lei_Thres2[3]	0x0040	2	RW	Flash AWB tuning threshold value.
0x70001838	fls_afl_FlashWP_Lei_Thres2[4]	0x0020	2	RW	Flash AWB tuning threshold value.
0x70001894	senHal_SenBinFactor	0x0002	2	RW	Number of subsampling factor. (ex 2 : 1/2 subsampling, 4: 1/4 subsampling)
0x70001896	senHal_SamplingType	0x0001	2	RW	Subsampling type setting. 0 : FULL SIZE MODE. 1 : Digital subsampling mode. 2 : PLA subsampling mode. 3 : CA subsampling mode.
0x7000189A	senHal_PLAOption	0x0002	2	RW	1 : Using horizontal PLA option 2 : Using vertical PLA option

0x70001A70	senHal_usForbiddenNoGain	0x0000	2	RW	LEI is less than this register value. F/W does not use gain.
0x70001AEA	senHal_SubF404Tune	0x0000	2	RW	Sensor tuning value.
0x70001AEC	senHal_FullF404Tune	0x0000	2	RW	Sensor tuning value.
0x70001AEE	senHal_bAlwaysAAC	0x0000	2	RW	AAC mode enable.
0x70001AF4	senHal_TuneStr_AngTuneData1[0]	0xF400	2	RW	Additional analog tuning.
0x70001AF6	senHal_TuneStr_AngTuneData1[1]	0x7C53	2	RW	Additional analog tuning.
0x70001AF8	senHal_TuneStr_AngTuneData1[2]	0x4E34	2	RW	Additional analog tuning.
0x70001AFA	senHal_TuneStr_AngTuneData2[0]	0xF416	2	RW	Additional analog tuning.
0x70001AFC	senHal_TuneStr_AngTuneData2[1]	0x5000	2	RW	Additional analog tuning.
0x70001AFE	senHal_TuneStr_AngTuneData2[2]	0x1000	2	RW	Additional analog tuning.
0x70001B00	senHal_TuneStr_AngTuneData3[0]	0x0000	2	RW	Additional analog tuning.
0x70001B02	senHal_TuneStr_AngTuneData3[1]	0x0000	2	RW	Additional analog tuning.
0x70001B04	senHal_TuneStr_AngTuneData3[2]	0x0000	2	RW	Additional analog tuning.
0x70001B06	senHal_TuneStr_AngTuneData4[0]	0x0000	2	RW	Additional analog tuning.
0x70001B08	senHal_TuneStr_AngTuneData4[1]	0x0000	2	RW	Additional analog tuning.
0x70001B0A	senHal_TuneStr_AngTuneData4[2]	0x0000	2	RW	Additional analog tuning.
0x70001B0C	senHal_TuneStr_AngTuneData5[0]	0x0000	2	RW	Additional analog tuning.
0x70001B0E	senHal_TuneStr_AngTuneData5[1]	0x0000	2	RW	Additional analog tuning.
0x70001B10	senHal_TuneStr_AngTuneData5[2]	0x0000	2	RW	Additional analog tuning.
0x70001B12	senHal_TuneStr_AngTuneData6[0]	0x0000	2	RW	Additional analog tuning.

0x70001B14	senHal_TuneStr_AngTuneData6[1]	0x0000	2	RW	Additional analog tuning.
0x70001B16	senHal_TuneStr_AngTuneData6[2]	0x0000	2	RW	Additional analog tuning.
0x70001B18	senHal_TuneStr_AngTuneData7[0]	0x0000	2	RW	Additional analog tuning.
0x70001B1A	senHal_TuneStr_AngTuneData7[1]	0x0000	2	RW	Additional analog tuning.
0x70001B1C	senHal_TuneStr_AngTuneData7[2]	0x0000	2	RW	Additional analog tuning.
0x70001B1E	senHal_TuneStr_AngTuneData8[0]	0x0000	2	RW	Additional analog tuning.
0x70001B20	senHal_TuneStr_AngTuneData8[1]	0x0000	2	RW	Additional analog tuning.
0x70001B22	senHal_TuneStr_AngTuneData8[2]	0x0000	2	RW	Additional analog tuning.
0x70001B24	senHal_TuneStr_AngTuneData9[0]	0x0000	2	RW	Additional analog tuning.
0x70001B26	senHal_TuneStr_AngTuneData9[1]	0x0000	2	RW	Additional analog tuning.
0x70001B28	senHal_TuneStr_AngTuneData9[2]	0x0000	2	RW	Additional analog tuning.
0x70001B2A	senHal_TuneStr2_usAngTuneGainTh	0x0000	2	RW	Analog gain threshold for tuning register.
0x70001B2C	senHal_TuneStr2_AngTuneF4CA[0]	0x0074	2	RW	Analog setting tune.
0x70001B2E	senHal_TuneStr2_AngTuneF4CA[1]	0x008D	2	RW	Analog setting tune.
0x70001B30	senHal_TuneStr2_AngTuneF4C2[0]	0x006E	2	RW	Analog setting tune.
0x70001B32	senHal_TuneStr2_AngTuneF4C2[1]	0x0084	2	RW	Analog setting tune.
0x7000210C	Mon_LT_uStableCntr	0x0000	2	R	AE stable frame number.
0x70002114	Mon_LT_ulCrntTargetLei	0x00000000	4	R	Actual LEI achieved by FW.
0x70002138	Mon_LT_uSenMinExp	0x0000	2	R	Minimum exposure
0x70002536	Mon_AFC_usFlExpQua	0x0000	2	R	0FA0h : 50Hz flicker canceller 0D04h : 60Hz flicker canceller

	nt				0001h : Flicker canceller off
0x70002BC0	Mon_AAIO_PrevAcqCtxt_ME_LEI_Exp	0x00000000	4	R	Current exposure value. 1/400 msec
0x70002BC4	Mon_AAIO_PrevAcqCtxt_ME_AGain	0x0000	2	R	Current Again value 8.8 format.
0x70002BC6	Mon_AAIO_PrevAcqCtxt_ME_DGain	0x0000	2	R	Current Dgain value 8.8 format.
0x70002EEE	Mon_AF_search_usStatus	0x0000	2	R	AF search status: 0x0000 : Idle AF search 0x0001 : AF search in progress 0x0002 : AF search success 0x0003 : Low confidence position 0x0004 : AF search is cancelled
0x70003036	Mon_DIS_DetectMotion	0x0000	2	R	Detect motion 0 : No motion 1 : Detect motion.