

Institut für Technische Informatik

Abteilung Eingebettete Systeme

Universität Stuttgart

Pfaffenwaldring 5b

D-70569 Stuttgart

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**Heuristics for Design Time Optimization of
System-on-Chip Memory Power
Consumption**

Jinpeng Li

Studiengang: INFOTECH (Information Technology)

Prüfer: Prof. Dr.-Ing. Martin Radetzki

Betreuer: M.Sc. Manuel Strobel

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Abstract

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1 Introduction

1.1 Memory power optimization

In the field of embedded systems design nowadays, power consumption becomes one of the most important design factors especially in the domain of Systems-on-Chip. One of the important issues to design power-efficient embedded system is the power consumed by memories and memory related components. Some researchers have claimed that large fraction of power is dissipated by memories [SER16; BMP00; Mai+07]. Thus, memory power optimization plays a significant role in the design of power-efficient embedded systems. One of the most effective and common approaches to reduce memory power consumption is the memory partitioning method which is proposed in several articles and books [SER16; BMP00; Mai+07; His05; MBP02, p.43].

The rationale of memory partitioning is , on the one hand, to split one single large memory into several small memory instances which can be accessed individually. On the other hand, according to the profiled memory access patterns, frequently accessed address ranges are grouped to smaller memory instances while seldom accessed address ranges are grouped to the larger ones. Therefore, the memory power optimization can be achieved by the facts that smaller memory instances consume less power and the larger memory instances are seldom accessed. There are two central concepts for memory power optimization using the memory partitioning method. One concept is the allocation α which is a set of memory instances of certain memory types. Memory types are defined by the physical characteristic parameters such instance size, area, read current and so on. The other concept is the binding β of application code and data fragments to the selected memory instances. The code and data fragments of an application are referred as profiles of this application. And each application is represented by a set of profiles. Every profile is characterized by some user-defined parameters. Because all the code and data should be stored in the memories, each profile should be bound to exactly one memory instance [SER16]. A configuration for the memory system is defined as the combination of an allocation of memory instances and the corresponding binding for the application profiles. The goal of memory power optimization is to find a configuration among all possible configurations such that the overall power consumed by all selected memory instances is the lowest under certain predefined constraints.

Obviously, the memory power optimization is one of the combinatorial optimizations since the process is to find the optimal solution from a finite solution space of a problem set. There are many algorithms that can be applied to solve this kind of problems in the domain of combinatorial optimization. One approach is the integer linear programming (ILP) which solves the optimization problem through a mathematical model described by certain

integer linear relationship. This approach is proposed in [SER16] to solve the memory power optimization problem. Another commonly applied approach is the heuristic algorithm which is based on searching mechanisms. Many classical combinatorial optimization problems such as traveling sales man (TSP) problem have been solved by using heuristic algorithms.

1.2 Heuristic Algorithms

Heuristic algorithm is a technique that searches for a near optimal solution of a optimization problem within a reasonable time. It is often used when the exact optimal solution can not be found by the conventional algorithms. When solving a optimization problem with a very large solution space, the algorithms trying to find the exact optimal solution may be ideal. However, the computation time of such algorithms may be not acceptable in practice. In such cases, the user of heuristic algorithm can find a good solution in a reasonable time. Though the solution provided by heuristic algorithm may not be the exact optimal one, it still can be considered as a valuable solution of the optimization problem. One key feature of heuristic algorithm is the trade-off between efficiency and precision. The solution quality and the computation time can be balanced by users according to their requirements.

There are exiting a lot of heuristics. Some algorithms are problem-dependent that cannot be applied to other problems. The most widely used algorithms are problem-independent which are usually called metaheuristic. Such algorithm usually consists of a base framework with several parameters. The framework is independent from the optimization problem sets while the parameters should be set up according to the problem. In the recent years, there is a new trend of heuristic which is called hyper-heuristic. The hyper-heuristic provides a high-level strategy to seek one or several low-level heuristics for generating a proper algorithm for a optimization problem. The hyper-heuristic is a cutting-edge technique and is beyond the knowledge of this paper. The metaheuristics are the main focus for the optimization problem. To be clarified, the heuristics discussed in the rest of this paper are metaheuristics.

A Appendix

Appendix goes here...

B List of Figures

C List of Abbreviations

MPSoC Multiprocessor System-on-Chip

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