A Direct RF-to-Information Converter for Reception and Wideband Interferer Detection Employing Pseudo-Random LO Modulation

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***Abstract* — The Direct RF-to-Information Converter (DRF2IC) unifies high sensitivity signal reception, narrowband spectrum sensing and energy-efficient wideband interferer detection into a fast-reconfigurable and easily scalable architecture. In reception mode, the DRF2IC RF front-end (RFFE) consumes 46.5mW and delivers 40MHz RF bandwidth, 41.5dB conversion gain, 3.6dB NF and -2dBm B1dB. 72dB out-of-channel blocker rejection is achieved in narrowband sensing mode. In compressed sensing wideband interferer detection mode, 66dB operational dynamic range, 40dB instantaneous dynamic range, 1.43GHz instantaneous bandwidth (IBW) is demonstrated and 6 interferers scattered over 1.26GHz are detected in 1.2uS consuming 58.5mW.**

I. Introduction

Advances in dynamic shared spectrum access (DSSA) systems especially in future dense, small-cell network deployments will force us to rethink the radio transceiver. Long and static radio links will often be replaced by short dynamic links. Multiple peer devices with similar levels of access privilege will opportunistically access a shared pool of spectrum spanning e.g., 700MHz to 6GHz. The next generation of radio receivers will need to be spectrum aware, frequency agile, wideband and interference robust.

Energy-efficient wideband interferer detection is a key enabler of future spectrum-aware receivers. Compressed sensing (CS) detectors [5-7] deliver a combination of sensitivity, bandwidth, scan time and energy consumption particularly suitable for DSSA. While the MWC [7] does significantly reduce energy consumption compared to a sweeping spectrum analyzer, it employs a direct RF *lowpass* architecture (Fig. 1) that does not scale well to higher frequencies, as the pseudo-random sequence (PRBS) length and clock frequency scale up with the maximum signal frequency. The QAIC [6] does scale well with frequency but requires a dual heterodyne RF chain.

So far, signal reception [1], narrowband sensing [2,3] and wideband interferer detection [5-7] functions have been implemented on distinct hardware blocks. Going forward unified and flexible system architectures are needed to achieve the cost, size and power targets in mass-market applications. Building upon the direct-conversion RF chain preferred for signal reception and combining it with a modulated LO generator and CS signal processing, the DRF2IC presented here unifies signal reception, narrowband sensing and CS wideband interferer detection into a single reconfigurable and scalable architecture.

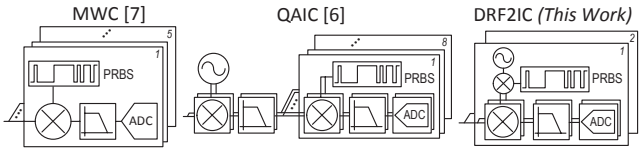

Fig. 1. Evolution of the compressed-sensing wideband detector RF front-end architecture.

II. Using a Modulated LO to Create Wide RF Bandpass Responses with a Narrowband Direct-Conversion Receiver

The DRF2IC RF front-end (Fig. 2) is configured for *high sensitivity signal reception* in mode 1 by disabling the LO modulator and using a standard quadrature LO at f_{LO} to generate a single narrow-band RF conversion-gain response around f_{LO}.

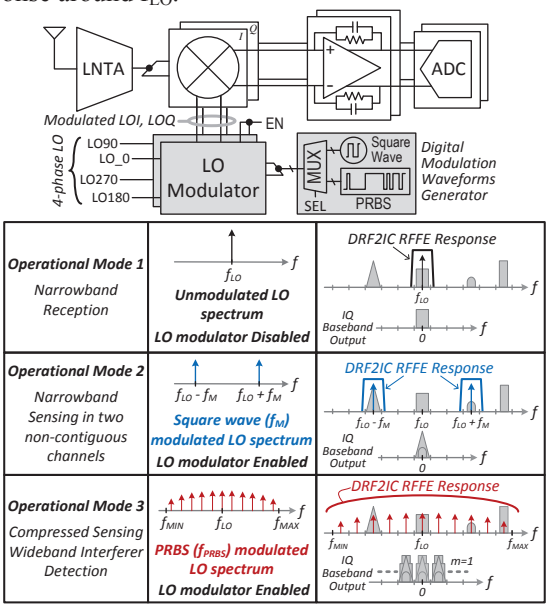

Fig. 2. The DRF2IC RFFE concept and its modes of operation.

In mode 2, an LO at f_{LO} is BPSK modulated with a square wave at f_M. The resulting LO now consists of two tones at (f_{LO}-f_M) and (f_{LO}+f_M) resulting in two narrow-band RF conversion-gain responses around the two LO

tones. For *wideband detection* in mode 3, an LO at f_{LO} is BPSK modulated with a PRBS (i.e. m-sequence) of length N and clock frequency f_{PRBS}. The resulting LO spectrum consists of a series of tones centered at f_{LO} and spaced by the desired resolution bandwidth RBW=f_{PRBS}/N. The TIA response is now up-converted to multiple RF frequencies separated by RBW to create a very wide conversion gain profile with a 3dB bandwidth extending from f_{MIN}=(f_{LO}–f_{PRBS}/2) to f_{MAX}=(f_{LO}+f_{PRBS}/2). *All N bins of width RBW from across the entire RF input spectrum (f_{MIN} to f_{MAX}) are folded into multiple 2m+1 (m=0,1,2…) complex IF frequencies. CS DSP can now be used to recover the location of interferers in the input spectrum*.

III. DRF2IC System Implementation

A. System Architecture and Configuration Options

In mode 1, the DRF2IC system in Fig. 3 employs the RFFE common-source (C-S) and common-gate (C-G) LNTA paths with the digital baseband (DBB) and noise cancellation DSP to form an FTNC receiver [1]. The C-S, C-G path mixers are driven with the same 25% duty-cycle, 4-phase LO by setting LOSEL to 0. Both LO modulators are disabled by setting EN1 and EN2 to 0. When receiving a single channel, only the middle branches (csY_0 and cgY_0) of the C-S and C-G path DBB blocks are used.

In mode 2, only one LO modulator is enabled (EN1=1, EN2=0). Both the C-S and C-G path mixers are driven with the same (LOSEL=0) square-wave modulated LO to implement simultaneous narrowband sensing of two non-contiguous channels with noise cancellation.

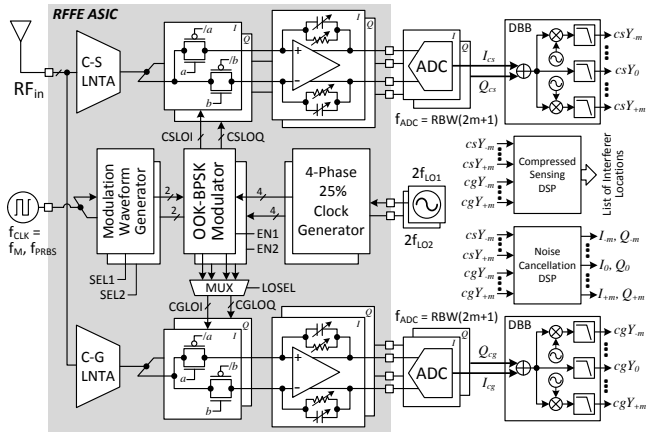

Fig. 3. The DRF2IC system architecture.

In modes 3a and 3b, [LOSEL,EN1,EN2]=[1,1,1] and the C-S, C-G path mixers are driven with two independent sets of LOs modulated with two distinct PRBSs. Using CS DSP the DRF2IC performs wideband interferer detection in a *single band* (mode 3a) with f_{LO1}=f_{LO2} in Fig. 3 or in *two disjoint bands* (mode 3b) with $f_{LO1} \neq f_{LO2}$. Earlier implementations [6] of CS interferer detector chips require several baseband branches (16 in [6]) multiplying the signal at IF with PRBSs to obtain enough measurements to detect multiple (3 in [6]) interferers. In contrast, the DRF2IC produces enough independent measurements to detect 6 interferers with the standard 4 branches in an FTNC [1] receiver *by using the higher order IF responses resulting from mixing the input signal with PRBS modulated LOs.* The DRF2IC RFFE produces R=2M (M=2m+1 and m=0,1,2…) complex measurements (csY_{-m} to csY_{+m} and cgY_{-m} to cgY_{+m}) from the two IQ outputs (I_{cs}, Q_{cs} and I_{cg}, Q_{cg}) by setting the TIA bandwidth f_{TIA}=RBW(m+1/2) and A/D frequency f_{ADC}=RBW(2m+1). Each IQ output pair is multiplied by orthogonal sinusoids of frequencies that are integer multiples of the RBW in the DBB to extract the higher order IF responses. The DRF2IC needs only 2 PRBSs to generate e.g. R=18 (m=4) complex measurements. In contrast, [6] requires 8 PRBSs to produce 8 complex measurements. Requiring only a small number of PRBSs, the DRF2IC can select maximal-length pseudo-random sequences with the desired optimal flat spectral profiles. Furthermore, compared to [7] the DRF2IC significantly reduces the PRBS length, clock frequency and the number of multipliers in the CS DSP [4] for frequency ranges (f_{MIN} to f_{MAX}) when f_{MIN} >> 0.

B. Circuit Implementation

The DRF2IC RFFE ASIC (Fig. 8) including bias and control circuitry was implemented on 0.56mm^2 in 65nm CMOS. The cascoded C-S and C-G LNTAs (Fig. 4) in the RFFE provide 113mS and 30mS of transconductance gain and together consume 15.5mW from 1.15V. The input return loss of the C-S, C-G LNTA combination is better than -12dB from 600MHz to 3GHz. The passive mixers use transmission gates. The TIAs are implemented with two-stage Miller-compensated OTAs (Fig. 4) and use 4-bit programmable feedback resistors and 3-bit programmable feedback capacitors for gain and baseband bandwidth control. The 4 TIAs together consume 24mW. The 25% duty-cycle, 4-phase LO generator and LO drivers consume 7mW. The 2 maximal-length pseudo-random sequence generators in the modulation waveform generator employ a linear feedback shift register (LFSR) architecture and consume 3.4mW at a clock frequency of 1.26GHz.

The on-off keyed (OOK) BPSK LO modulator core (MOD core in Fig. 4) uses custom high-speed NOR and NAND gates. The MOD core has three valid output states. When EN=0, the MOD core passes the input LO signal to its output unaltered. When EN=1, the MOD core either maintains or flips the polarity of its differential output relative to its input when the logic values of the control signals C[0], C[1] are complements of each other. When C[1]=C[0]=1, both outputs of the MOD core are set to logic 0. Each LO modulator core consumes 720uW at an input LO signal switching frequency of 2.5GHz.

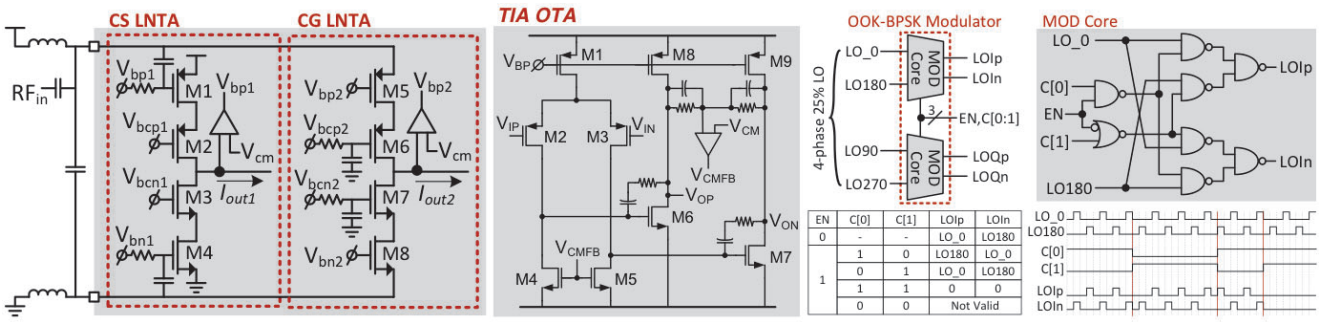

Fig. 4. Key circuit blocks of the DRF2IC RFFE. Cascoded inverter based common-source and common-gate LNTAcombination. Two-stage Miller-compensated OTA used in TIAs. OOK-BPSK LO modulator architecture, core schematic, truth table and waveforms.

IV. Measurement Results

In reception mode 1, the DRF2IC RFFE chip consumes 46.5mW from 1.15V and at 2.1GHz delivers 40MHz of RF bandwidth, 41.5dB conversion gain (Fig. 5), -2dBm B1dB for a blocker at 1.47GHz or 2.73GHz. It further achieves 3.6dB NF (after cancellation), -26dBm P1dB, -11dBm in-channel IIP3 and +4dBm out-of-channel IIP3 (with tones at 200MHz and 395MHz offsets).

In narrowband sensing mode 2, with f_{LO}=2.1GHz and f_M=315MHz the RFFE response consists of two 36dB conversion gain peaks with 40MHz of RF bandwidth at 1.785GHz and 2.415GHz (Fig. 5). The DRF2IC consumes 50mW and simultaneously senses two disjoint channels with a cancelled NF of 7.3dB rejecting an out-of-channel blocker at midband by 72dB. A NF degradation in mode 2 compared to mode 1 is expected and is due to noise downconversion from two RF channels and gain reduction.

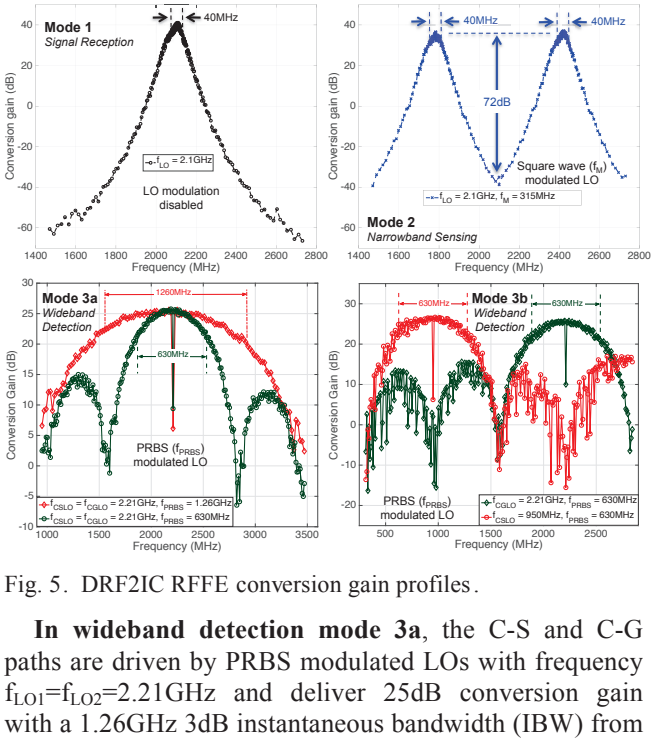

Fig. 5. DRF2IC RFFE conversion gain profiles.

In wideband detection mode 3a, the C-S and C-G paths are driven by PRBS modulated LOs with frequency f_{LO1}=f_{LO2}=2.21GHz and deliver 25dB conversion gain with a 1.26GHz 3dB instantaneous bandwidth (IBW) from f_{MIN}=1.58GHz to f_{MAX}=2.84GHz when f_{PRBS}=1.26GHz (Fig. 5). An IBW of 630MHz from f_{MIN}=1.895GHz to f_{MAX}=2.525GHz is achieved when f_{PRBS}=630MHz. The DRF2IC system is scaled (Fig. 6) from detecting 3 to 6 10MHz interferers in mode 3a with a detection probability P_D>90% and a false alarm P_{FA}<10% by increasing f_{ADC} from 63MHz to 105MHz and increasing the total number of DBB (I and Q) branches R from 10 (m=2) to 18 (m=4). The CS DSP uses 125 samples from each of the 10 (or 18) measurements to detect e.g. up to 3 20MHz or 6 10MHz interferers scattered over a 1.26GHz span in 1.2uS. When detecting up to 3 20MHz or 6 10MHz wide interferes with P_D>90% and P_{FA}<10%, the minimum and maximum detectable interferer levels are -71dBm and -4.8dBm thus achieving a 66dB operational dynamic range.

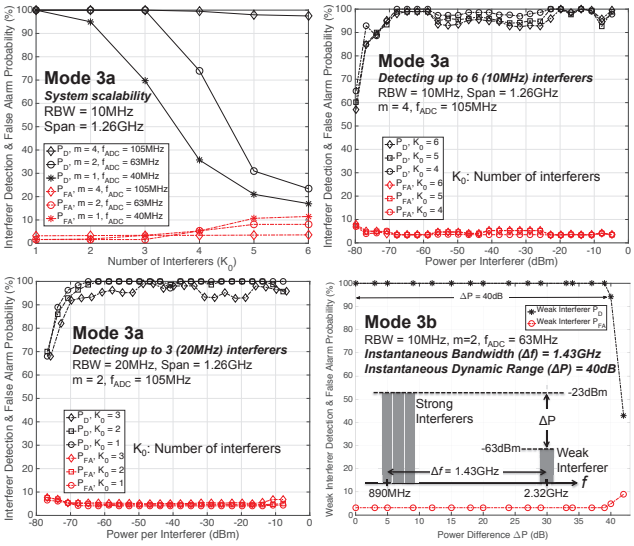

Fig. 6. DRF2IC system scalability, multi-interferer detection capability, dynamic range and bandwidth demonstration.

In wideband detection mode 3b, *two disjoint bands* (e.g. 635MHz to 1.265GHz and 1.895GHz to 2.525GHz in Fig. 5) can be simultaneously monitored by uncoupling the C-S and C-G paths and driving their mixers with distinct LOs (f_{LO1}=950MHz, f_{LO2}=2.21GHz) modulated with PRBSs. The instantaneous dynamic range (IDR) in

Fig. 6 is measured by sweeping the power of a weak interferer at 2.32GHz while fixing the power of 3 strong interferers at 890MHz. The IDR (ΔP in Fig. 6) is the maximum power difference between the strong and weak interferers such that P_D>90% and P_{FA}<10% is maintained for the weak interferer. IDR of 40dB and IBW of 1.43GHz is achieved in mode 3b. The calibration approach in [7] may be used to further improve IDR. The DRF2IC RFFE consumes 58.5mW from 1.15V in modes 3a and 3b.

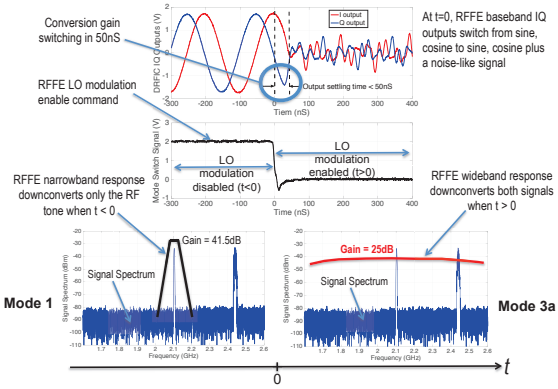

Fig. 7. Time required by the DRF2IC RFFE to switch from narrowband mode 1 to wideband mode 3a.

Fast Mode Switching: A tone at 2.105GHz and a 20MHz noise-like signal at 2.44GHz are used to measure the DRF2IC RFFE mode switching time. Initially in mode 1 with f_{LO}=2.1GHz, the RFFE down-converts the RF tone to baseband and rejects the noise-like signal. At time t=0 the RFFE is switched from mode 1 to mode 3a by enabling LO modulation and the baseband signal switches from a 5MHz sinusoid to a superposition of the sinusoid and the noise-like signal in 50nS.

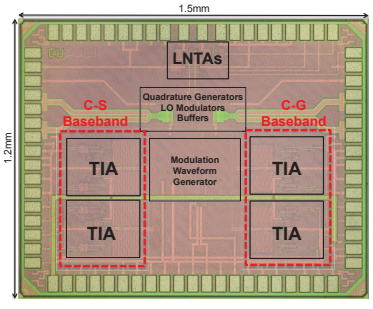

Fig. 8. DRF2IC RFFE ASIC die photo.

V. Comparison to the State of Art

The DRF2IC performance in reception mode adjusted for bandwidth parallels the state-of-art (SoA) FTNC [1]. In CS wideband detection mode, the DRF2IC achieves up to a 12.2x reduction in RFFE energy consumption and a 26x improvement in detector figure of merit (FOM = IDR*IBW/Energy with units dB*GHz/nJ). The DRF2IC RFFE architecture further enables an estimated 7.4x reduction in complexity (i.e. number of multiplications) of the compressed sensing DSP [4].

TABLE I
DRF2IC Performance Comparison with Recent Compressed Sensing Wideband Interferer Detectors

		QAIC [6]	MWC [7]	This Work
CMOS Technology	[nm]	65	65	65
Supply Voltage	[V]	1.15	1.2	1.15
Number of Branches in the RFFE		16	5	4
Number of Detected Interferers		3	4	6
Measured Input Frequency Range	[GHz]	2.7-3.7	0-0.9	0.635-2.84
Measured RFFE Chip Power	[mW]	80	704	58.5
*Estimated RFFE Power with LNA, PLL, ADCs	[mW]	120	897 #	110
Scan Time	[uS]	4.4	1.2	1.2
RFFE Energy per Scan	[nJ]	528	1076	132
RFFE Energy per Detected Interferer	[nJ]	176	269	22
Relative RFFE Energy per Detected Interferer		8	12.2	1
&Estimated Number of Multiplications in CS DSP		800	4440	600
Measured Instantaneous Dynamic Range	[dB]	18	37	40
Measured Instantaneous Bandwidth	[GHz]	1	0.9	1.43
Detector RFFE Figure of Merit (FOM)	[dB*GHz/nJ]	0.1	0.12	2.6

* Measured power is scaled to a common input frequency range: f_{MIN}=2.7GHz to f_{MAX}=3.7GHz
# A single shared shift register bank (length 740, clock 7.4GHz) for all branches in [7] is assumed
& Number of multiplications per interferer per sample when scanning 2.7-3.7GHz with RBW=10MHz

VI. Conclusions

The DRF2IC is a reconfigurable architecture employing a flexible LO modulator and two direct-conversion IQ branch pairs. Coupling its two IQ pairs, the DRF2IC can perform noise cancellation in a single channel or perform CS wideband interferer detection over a single wideband frequency span. Furthermore, the DRF2IC RFFE has a unique feature that allows the user to uncouple its two IQ pairs and perform CS interferer detection in two disjoint wideband frequency spans thereby achieving an SoA combination of energy consumption, instantaneous bandwidth and instantaneous dynamic range.

Acknowledgment

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References

[1] D. Murphy et al., "A Blocker-Tolerant Wideband Noise-Cancelling Receiver with a 2dB Noise Figure," *ISSCC*, 2012.

[2] M. Alink et al., "A 50MHz-to-1.5GHz Cross-Correlation CMOS Spectrum Analyzer for Cognitive Radio with 89dB SFDR in 1MHz RBW," pp. 1-6, *DySPAN*, 2010.

[3] A. Goel et al., "A 130-nm CMOS 100-Hz–6-GHz Reconfigurable Vector Signal Analyzer and Software-Defined Receiver," *IEEE Trans. Microwave Theory and Techniques*, pp. 1375-1389, 2012.

[4] J. A. Tropp and A. C. Gilbert, "Signal recovery from random measurements via orthogonal matching pursuit", *IEEE Trans. Inf. Theory*, pp. 4655-4666, 2007.

[5] J. Yoo et al., "A 100MHz-2GHz 12.5x sub-Nyquist Rate Receiver in 90nm CMOS," *RFIC*., pp. 31-34, 2012.

[6] R. T. Yazicigil et al., "A 2.7-to-3.7GHz Rapid Interferer Detector Exploiting Compressed Sampling with a Quadrature Analog-to-Information Converter," *ISSCC*, 2015.

[7] D. Adams et al., "A Mixer Frontend for a Four-Channel Modulated Converter with 62dB Blocker Rejection", *RFIC, pp 286-289,* 2016.