# Lab4\_GRP15\_SESS205 REPORT

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| LogicalStep\_Lab4\_top.vhd |
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| Meek\_meally.vhd |
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| Bin\_counter4bit.vhd |
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| Error\_handler.vhd |
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| Marco\_extender.vhd |
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| Bidir\_shift\_reg.vhd |
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| Grabbalar.vhd |
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| Simulation of the 8bit Shift Register |
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| Simulation of the 8bit Binary Counter |
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| State diagram of Mealy SM |
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| State diagram of Moore SM1 |
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| State diagram of Moore SM2 |
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| Mealy Form for Mealy SM |
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| Moore Form for Moore SM1 |
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| Moore Form for Moore SM2 |
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| Fitter Report on Resources Utilization by Entity |
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