

# *Kartik Lakshminarasimhan*

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<b>Skills</b>	Languages	C++, Python, Bash
	Hardware	Verilog, Bluespec System Verilog
	Libraries	STL, pthreads
	Tools	Intel Pin, Intel Vtune Amplifier, Xilinx
	Platforms	Xilinx Spartan-V
	Simulators	Sniper
<b>Relevant Experience</b>	<b>Graduate Research Assistant</b>	Fall'17 - Present
	Performance Lab, Ghent University	
	<b>Graduate Technical Intern</b>	May'16 - December'16
	Microarchitecture Research Labs, Intel, Bangalore, India	
	Developed a visualization tool(in python and C++) aiding the analysis to find performance bottlenecks and improving IPC gains. Workload characterization using VTune Amplifier	
	<b>Graduate Research Assistant</b>	Fall'14 - Spring'16
<b>Education</b>	Computer Architecture Group, University of Connecticut	
	<b>Part-time Research Trainee</b>	August '11 - May '14
	High Performance Computing Group, Waran Research Foundation(WARFT), Chennai, India	
	<b>Ghent University</b>	Fall'17 - Summer'22(expected)
	Doctor of Philosophy, Computer Science and Engineering	
<b>Publications</b>	<b>University of Connecticut</b>	August '14 - December'16
	Master of Science, Electrical and Computer Engineering	GPA : 3.4/4
	Graduate Courses (Applied Probability and Stochastic Process, Advanced Storage Systems, Neural Computing, Computer Architecture, Advanced Computer Architecture, Machine Learning[Coursera])	
	Thesis: WCET Analysis for Concurrent Execution of Multiple Applications on Safety Critical Embedded Multicores	
	<b>Anna University, Chennai</b>	August '10 - May'14
<b>Publications</b>	Bachelor of Engineering, Electronics and Communication	First Class
	Relevant coursework : VLSI Design (Theory and Laboratory), Digital Design (Theory and Laboratory), Data Structures and Object Oriented Design, Microprocessors and Microcontrollers	
	<b>Co-authored</b>	
	The Forward Slice Core Microarchitecture, <b>K. Lakshminarasimhan</b> , A. Naithani, J. Feliu Perez, and L. Eeckhout, International Conference on Parallel Architectures and Compilation Techniques (PACT), Oct 2020	
	A Lightweight Spatio-temporally Partitioned Multicore Architecture for Concurrent Execution of Safety Critical Workloads, Q.Shi, <b>K.Lakshminarasimhan</b> , C. Noll, E. Scholte, O.Khan SAE 2016 Aerospace Systems and Technology Conference(ASTC), September, 2016	
<b>Publications</b>	Efficient Parallelization of Path Planning Workload on Single-chip Shared-memory Multicores M. Ahmad, <b>K. Lakshminarasimhan</b> , O. Khan, to appear in IEEE High Performance Extreme Computing Conference, (HPEC'15), September 2015	

Performance and Energy Efficient Cache System Design : Simultaneous Execution of Multiple Applications across Heterogeneous Cores, Venkateswaran Nagarajan, **K.Lakshminarasimhan**, et al. presented at IEEE Symposium on VLSI(ISVLSI'13), Natal, Brazil

## Projects

### **Complexity-effective microarchitectures**

Fall17 - Present

Exploring the performance gap between in-order and OOO cores by adding simple structures on top of an in-order cores (Simulator used : Sniper)

### **Multiprogram support for Graphite Many-core Simulator**

Fall14 ,Summer'15

Part of a team to implement multiprogram support in the lite (no memory/system call emulation) mode of Graphite simulator. Studied the multiprogramming methodology in Dynamic Binary Translation(DBT) based simulators of ZSim(uses PIN and system calls) and Sniper(uses PinPoint and PinPlay and Unix Pipes).

### **Cache sensitivity of Loop-Tiled Matrix Algorithms**

Spring'15

Conducted various cache sensitivity studies in Graphite and ZSim(state of the art cache partitioning schemes) on Loop-tiled Matrix Algorithms.

### **Partitioning Shared Resources in a Multicore**

Summer'15, Fall'15

Implemented Way-Partitioning in shared last level cache, spatial and temporal partitioning of shared memory controllers.

### **Code Optimization for Path Planning Algorithms**

Fall'14

Optimized the data Structures in path-planning algorithms(Dijkstra,A\*,D\*) for reduced code completion time in a simulator(Java).

### **Computation and Learning in Biological Neuron Models**

Spring,Summer'15

Studied computation and learning mechanisms in biological neural models of Hodgkin Huxley and Izhikevich.

### **Parallel Support Vector Machines Training using Pthreads**

Spring'16

Implemented scalable serial and parallel versions of : Kernel trick in SVM and simplified version of Sequential Minimization Optimization Algorithm.

### **ARM Bus Architecture Design**

December'13 - April'14

Designed and implemented AXI-APB bridge architecture in AMBA 3.0 using Bluespec System Verilog.

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Dr.Niranjan Soundararajan

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Prof.Marten Van Dijk

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