AESOP Embedded Forum
Sejong Lee (http://www.aesop-embedded.org)

개 요

이 문서는 S3C6400 데이터시트에서
제 31장 UART를 번역한 자료입니다.

제 31장. UART

이번 장은 S3C6400 RISC 마이크로프로세서의
UART (범용 비동기 송신/수신) 시리얼 포트를 설명하고 있습니다.

31.1 개관

S3C6400의 UART는 4개의 독립적인 비동기 시리얼 I/O (SIO) 포트를 제공한다. 각각의 비동기 시리얼 I/O (SIO) 포트는 인터럽트 기반 또는 DMA 기반의 모드로 동작할 수 있다. 다시 말하면, UART는 인터럽트나 DMA 요청을 발생시킬 수 있다, 데이터를 전송하기 위해, MEM과 UART 사이에서. UART는 PCLK를 사용해서 최대 115.2K bps의 비트율을 지원한다. 만약 외부 장치가 EXT_UCLK0이나 EXT-UCLK1을 가진 UART를 제공한다면 UART는 빠른 속도로 동작할 수 있다. 각각의 UART 채널은 수신 및 전송을 위한 두 개의 64바이트 FIFO를 가지고 있다.

S3C6400의 UART는 조절가능한 baud rate, 적외선 전송/수신, 한 개나 두 개의 stop bit 삽입, 5 비트, 6비트, 7비트 또는 8비트 데이터 폭과 패리티 검사를 포함하고 있다.

각각의 UART는 baud-rate(통신속도) 생성기, transmitter, reciever와 control unit을 포함하고 있다. Figure 31-1에 보이는 것처럼. 통신속도 생성기는 PCLK, EXT-UCLK0 또는 EXT_UCLK1에 의해 설정할 수 있다. Transmitter와 receiver는 64바이트 FIFO와 data shifter를 포함하고 있다. FIFO에 데이터가 써지면 transmit shifter에 복사한다, 전송하기 전에. 그리고 데이터는 시프트되어 나간다, Transmit data pin(TxDn)에 의해. 한 편 수신된 데이터는 시프트된다. receive data pin (RxDn)으로부터, 그 다음 shifter에서 FIFO로 복사한다.

31.2 특징

UART는 다음의 특징을 가지고 있다.

- RxD0, TxD0, RxD1, TxD1, RxD2, TxD2, RxD3, TxD3 (DMA기반이나 인터럽트 기반으로 동작하는)
- UART Ch0, 1, 2, 3 (IrDA 1.0과 64바이트 FIFO를 가진)
- UART Ch0, 1 (nRTS0, nCTS0, nRTS1, nCTS1을 가진)
- High speed 동작 지원 (UART Ch1, 3에 한해서)
- 전송/수신에 대한 handshake(데이터 전송에 앞서 서로 제어신호 교환) 지원

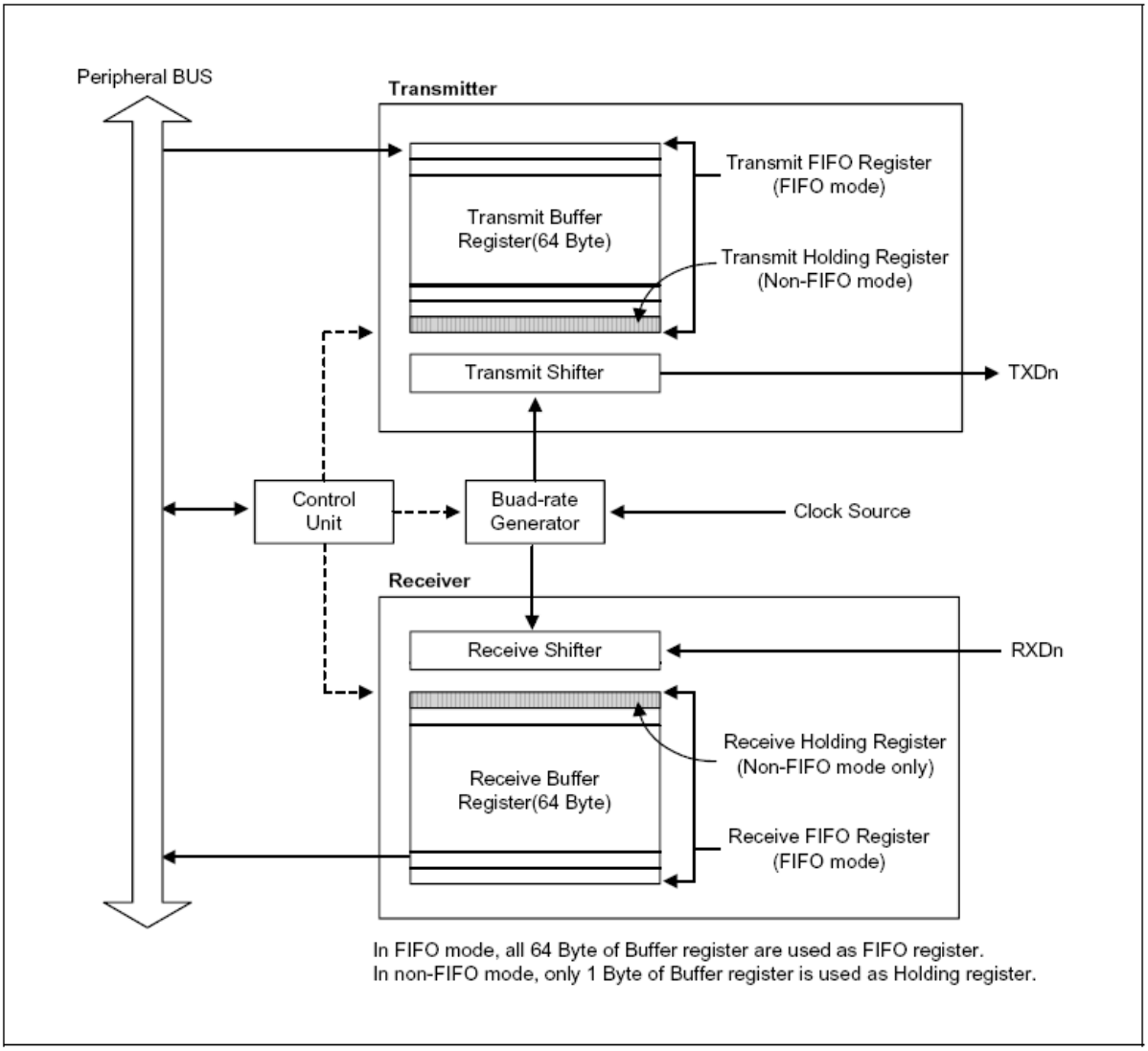

Figure 31-1. UART Block Diagram

31.3 요약

다음 부분은 UART 동작을 설명하고 있다. UART 동작은 데이터전송, 데이터수신, 인터럽트생성, baud-rate생성, Looback(되돌림) 모드, Infra-red(적외선) 모드, auto flow control(자동흐름제어)를 포함하고 있다.

31.3.1 데이터 전송

전송을 위한 데이터 frame(짜임)은 프로그램 가능하다. 데이터 프레임은 start 비트와 5~8 데이터비트, 추가적으로 패리티비트와 1~2 stop 비트로 구성되어 있다. 이것은 line control register (ULCONn)에 의해 설정할 수 있다. Transmitter는 또한 break condition을 생성할 수 있는데, 한 프레임 전송시간동안 시리얼 출력을 논리 0 상태로 강제한다. 현재의 transmission word 이후에 이 블록 전송 break transmit는 전송완료된다. Break signal 전송후에 Tx FIFO (Non-FIFO 모드에서는 Tx holding register)로 계속 데이터를 전송한다

31.3.2 데이터 수신

전송하는 것처럼 수신을 위한 데이터 프레임도 역시 프로그램 가능하다. 데이터 프레임은 line control register (ULCONn)에 있고 start 비트와 5~8 데이터비트, 추가적으로 패리티비트와 1~2 stop 비트로 구성되어 있다. Receiver는 이상동작에러, 패리티에러, 프레임에러, break condition을 감지할 수 있다. 각각은 error flag를 설정할 수 있다.

- 이상동작 에러는 새로운 데이터가 오래된 데이터를 덥어쓰는 것을 나타낸다, 오래된 데이터를 읽기전에.
- 패리티 에러는 receiver가 예상치못한 패리티 상태를 감지했을 때를 가리킨다.
- 프레임 에러는 수신된 데이터가 유효한 stop bit를 가지고 있지 않을 때를 나타낸다.
- Break condition은 RxDn 입력이 1프레임 전송시간보다 더 긴 시간동안 논리0상태를 잡고 있을 때를 나타낸다.

수신 time-out 상태는 3word 시간(this interval follows the setting of Word Length bit)동안 어떤 데이터도 받지 못했을 때 발생하고 Rx FIFO는 FIFO 모드에서 비어있지 않다.

31.3.3 Auto Flow Control(AFC) 자동 흐름 제어

UART0과 UART1은 nRTS와 nCTS로 자동흐름제어를 지원한다. 만약을 대비하여 외부 UART에 연결할 수 있다. 만약 UART를 모뎀에 연결하고 싶다면 UMCONn 레지스터의 자동흐름제어 비트를 불가능하게 해야하고 소프트웨어적으로 nRTS 신호를 제어해야 한다.

AFC(자동흐름제어)에서 nRTS는 receiver의 상태에 의존하고 nCTS 신호는 transmitter의 동작을 제어한다. UART의 transmitter는 오직 nCTS 신호가 동작할 때에만 FIFO에서 데이터를 전송한다. (AFC에서, nCTS는 다른 UART의 FIFO가 데이터를 받을 준비가 되었다는 것을 의미한다.)
UART가 데이터를 받기전에,
Receive FIFO가 2바이트 이상의 여유를 가지고 있을 때 nRTS는 활성화 상태이어야 하고
receive FIFO가 1바이트 이하의 여유를 가지고 있을 때 비활성화 상태이어야 한다.
(AFC에서 nRTS는 receive FIFO가 데이터를 수신할 준비가 되었다는 뜻이다.)

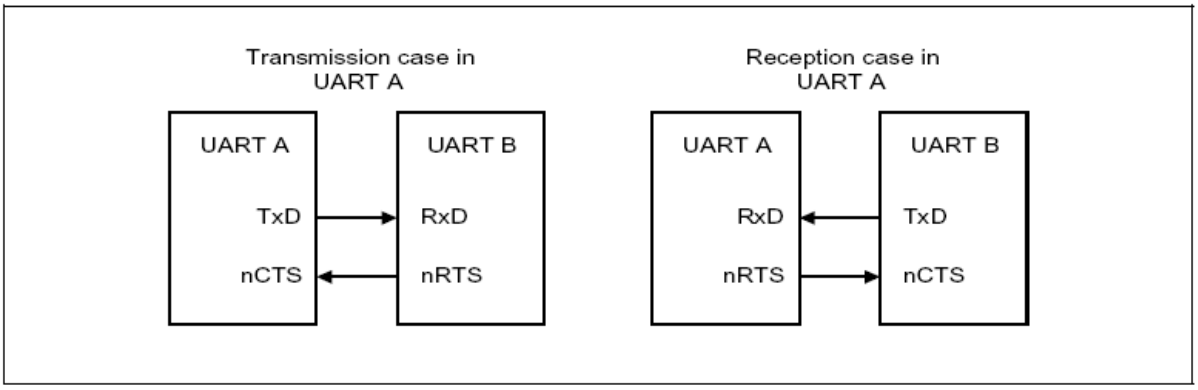

Figure 31-2. UART AFC interface

31.3.3.1 비(Non) 자동흐름제어 예제 (소프트웨어적으로 nRTS와 nCTS를 제어)

Rx 동작 (with FIFO)

1. receive 모드 선택 (인터럽트 또는 DMA 모드)
2. Rx FIFO trigger 레벨을 16으로 선택
   UFSTATn 레지스터의 Rx FIFO 계수값을 체크. 만약 값이 16보다 작으면 UMCONn[0] 값을 1(nRTS 활성화)로 설정해야 한다. 그리고 만약 값이 같거나 16보다 크다면 값을 0(nRTS 비활성화)으로 설정해야 한다.
3. 2번 항목을 반복한다.

Tx 동작 (with FIFO)

1. transmit 모드 선택 (인터럽트 또는 DMA 모드)
2. UMSTATn[0]값 체크. 만약 값이 1(nCTS 활성화)이면 Tx FIFO 레지섵에 데이터를 써야 한다.
3. 2번 항목을 반복한다.

31.3.4 RS-232C 인터페이스

UART를 모뎀 인터페이스(널 모뎀 대신)에 연결하기 위해서는 nRTS, nCTS, nDSR, nDTR, DCD, nRI 신호가 필요하다. 그러나 S3C6400의 UART는 nRTS와 nCTS를 지원한다. 이 경우, 사용자는 소프트웨어적으로 일반 I/O를 사용해서 이 신호를 제어할 수 있다. 왜냐하면 AFC는 RS-232C 인터페이스를 지원하지 않기 때문이다.

31.3.5 Interrupt / DMA request Generation (인터럽트 / DMA 요청 발생)

S3C6400의 각각의 UART는 7가지 상태(Tx/Rx/Error) 신호를 가지고 있는데, Overrun error(이상동작에러), 패리티에러, 프레임에러, Break, Receive buffer data ready, Transmit buffer empty, Transmit shifter empty, . 이렇게 해서 7가지 이다. 7개 상태 신호는 모두 UART 상태 레지스터(UTRSTATn/UERSTATn)에 대응하여 나타낸다.

Overrun error, 패리티에러, 프레임에러, break condition은 receive error status를 참조한다. 각각은 receive error status interrupt 요청을 일으킬 수 있다, 만약 receive-error-status-interrupt-enable 비트가 control register인 UCONn에서 1로 설정되었다면. Receive-error-status-interrupt-request가 감지되었을 때, 이 신호는 UERSTSTn의 값을 읽어서 인식할 수 있도록 요청을 야기한다.

Receiver가 FIFO 모드에서 receiver shifter의 데이터를 receive FIFO 레지스터로 전송하고 수신한 데이터의 개수가 Rx FIFO trigger level에 도달했을 때, Rx 인터럽트가 발생한다. Rx 인터럽트는 control register (UCONn)에서 receive 모드가 1(interrupt request 또는 polling mode)로 선택되었을 때 발생한다.

Non-FIFO 모드에서 receive shifter의 데이터를 receive holding register로 전송하는 것은 interrupt request나 polling mode에 한해서 Rx 인터럽트를 일으킨다.

Transmitter가 transmit FIFO 레지스터에서 transmit shifter로 데이터를 전송하고 transmit FIFO에 남은 데이터의 수가 Tx FIFO level에 도달하면 Tx 인터럽트가 발생한다. Tx 인터럽트는 control register의 transmit mode가 Interrupt request나 polling mode처럼 선택되었을 때 발생한다. Non-FIFO 모드에서 transmit holding register에서 transmit shifter로 데이터를 전송하는 것은 interrupt request나 polling mode에 한해서 Tx 인터럽트를 발생시킨다.

Tx 인터럽트는 언제나 transmit FIFO에 있는 데이터의 수가 trigger level 보다 작을때면 요구된다는 것에 주의하자. 이 말은 인트럽트는 사용자가 Tx 버퍼를 채우지 않는 한 Tx 인터럽트를 활성화 하자마자 요구된다는 것이다. (prior to that.) Tx 버퍼를 먼저 채운 후 그 다음에 Tx 인터럽트를 활성화하는 것을 추천한다.

S3C6400의 인터럽트 콘트롤러는 level-trigger 타입이다. 사용자는 'Level' 처럼 인터럽트 타입을 설정해야 한다. UART control register를 프로그램 할 때면 언제나.

만약 control register의 receive 모드와 transmit 모드가 DAMn request 모드로 선택되었다면, DMAn 요청은 위에서 말한 상황에서 Rx나 Tx 인터럽트 대신에 발생한다.

Table 31-1. Interrupts in Connection with FIFO

Type	FIFO Mode	Non-FIFO Mode
Rx interrupt	Generated whenever receive data reaches the trigger level of receive FIFO. Generated when the number of data in FIFO does not reaches Rx FIFO trigger Level and does not receive any data during 3 words time (receive time out). This interval follows the setting of Word Length bit.	Generated by the receive holding register whenever receive buffer becomes full.
Tx interrupt	Generated whenever transmit data reaches the trigger level of transmit FIFO (Tx FIFO trigger Level).	Generated by the transmit holding register whenever transmit buffer is empty.
Error interrupt	Generated when frame error, parity error, or break signal are detected. Generated when it gets to the top of the receive FIFO without reading out data in it (overrun error).	Generated by all errors. However if another error occurs at the same time, only one interrupt is generated.

31.3.6 UART ERROR STATUS FIFO (UART 에러 상태 FIFO)

UART는 Rx FIFO 레지스터외에 error status FIFO를 가지고 있다. Error status FIFO는 FIFO 레지스터에서 어떤 데이터가 에러를 가지고 수신되었는지를 나타낸다. Error 인터럽트는 데이터가 에러를 가지고 있을 때에만 발생한다. (is ready to read out.) Error status FIFO를 clear하기 위해 에러를 가진 URXHn와 UERSTATn을 읽어내야 한다.

예를들면:

UART Rx FIFO가 A,B,C,D,E 캐릭터를 순차적으로 수신하고 'B'를 받는동안 프레임 에러가 발생하고 'D'를 받는동안 패리티 에러가 발생했다고 가정해보자.

실제 UART가 수신한 에러는 어떤 error interrupt도 생성하지 않는다. 왜냐하면 에러를 가지고 수신한 character는 아직 읽지 않았기 때문이다. Error interrupt는 character를 읽을 때 발생한다.

Figure 31-3 shows the UART receiving the five characters including the two errors.

Time	Sequence Flow	Error Interrupt	Note
#0	When no character is read out	-	
#1	A, B, C, D, and E is received	-	
#2	After A is read out	The frame error (in B) interrupt occurs.	The 'B' has to be read out.
#3	After B is read out	-	
#4	After C is read out	The parity error (in D) interrupt occurs.	The 'D' has to be read out.
#5	After D is read out	-	
#6	After E is read out	-	

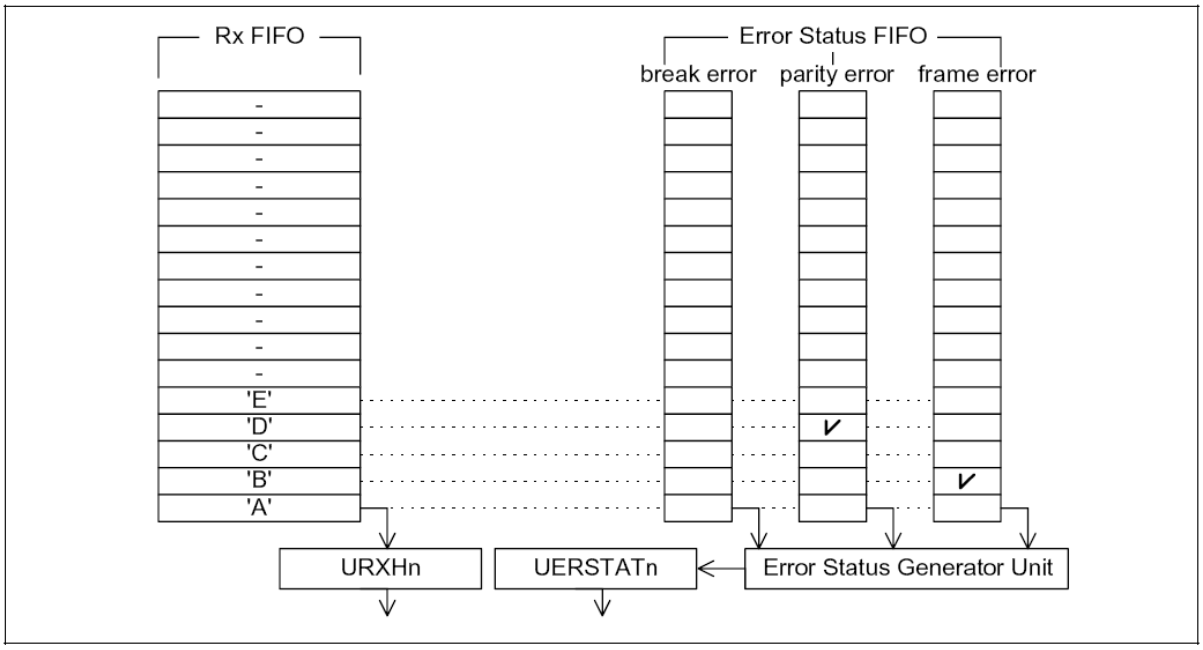

Figure 31-3. Example showing UART Receiving 5 Characters with 2 Errors

31.3.7 Infra-Red (IR) Mode (적외선 모드)

S3C6400의 UART block은 적외선 송신과 수신을 지원한다. 이것은 UART의 line control register (ULCONn)에 있는 infra-red-mode 비트를 설정함으로서 선택할 수 있다. Figure31.4는 어떻게 IR 모드를 실행하는지 설명하고 있다.

적외선 전송모드에서, 전송펄스는 3/16 비율로 된다. 보통의 시리얼 전송율 (transmit data 비트가 0) 적외선 수신모드에서 receiver는 3/16 펄스 기간을 감지해야 한다. Zero 값(frame timing diagram을 보자, Figure 31-6과 Figure 31-7)을 인식하기 위해.

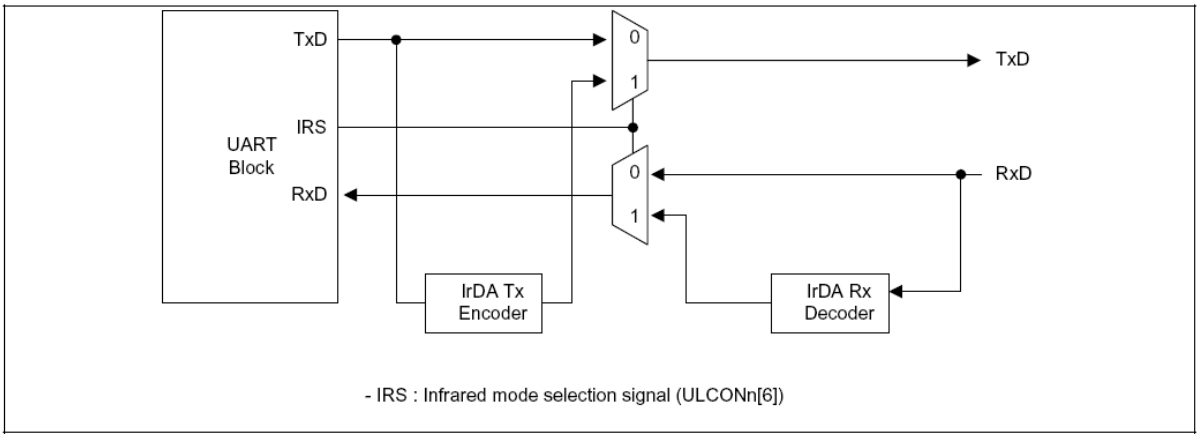

Figure 31-4. IrDA Function Block Diagram

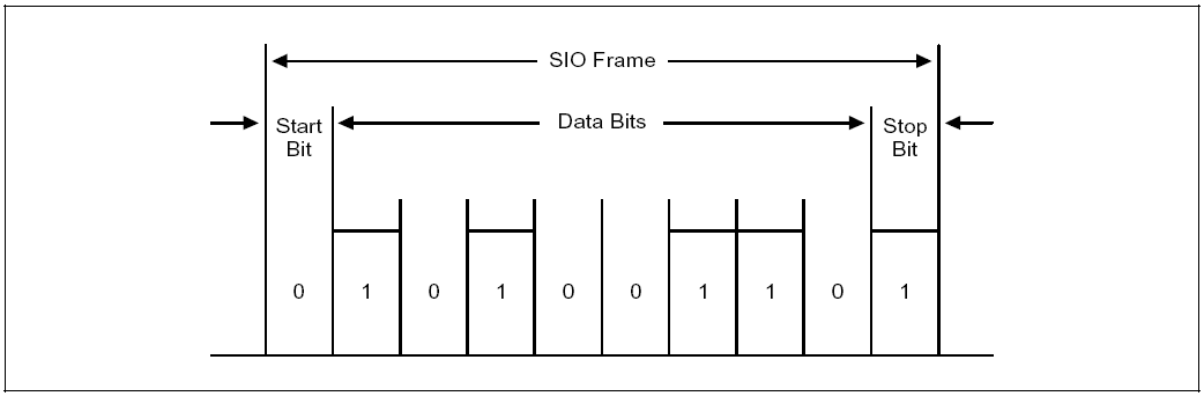

Figure 31-5. Serial I/O Frame Timing Diagram (Normal UART)

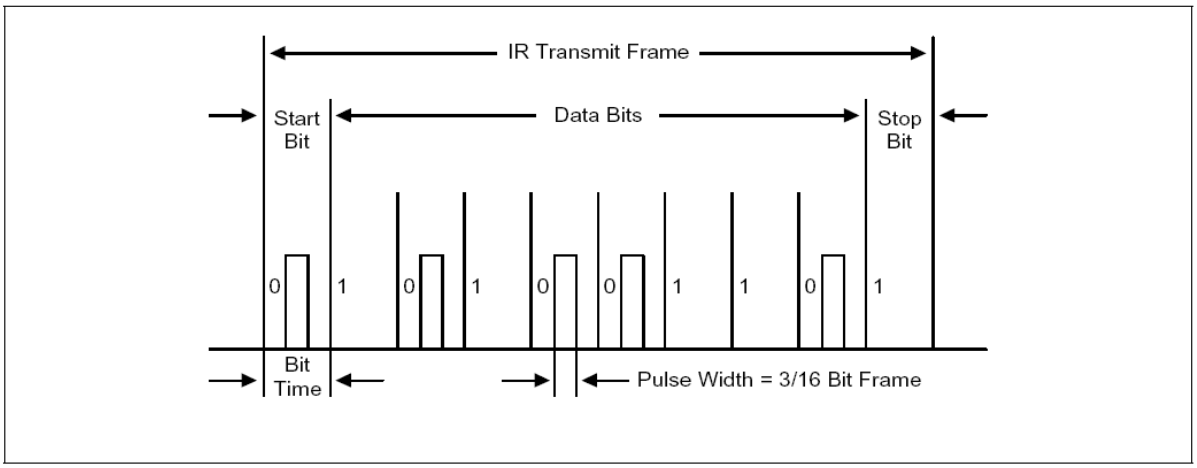

Figure 31-6. Infra-Red Transmit Mode Frame Timing Diagram

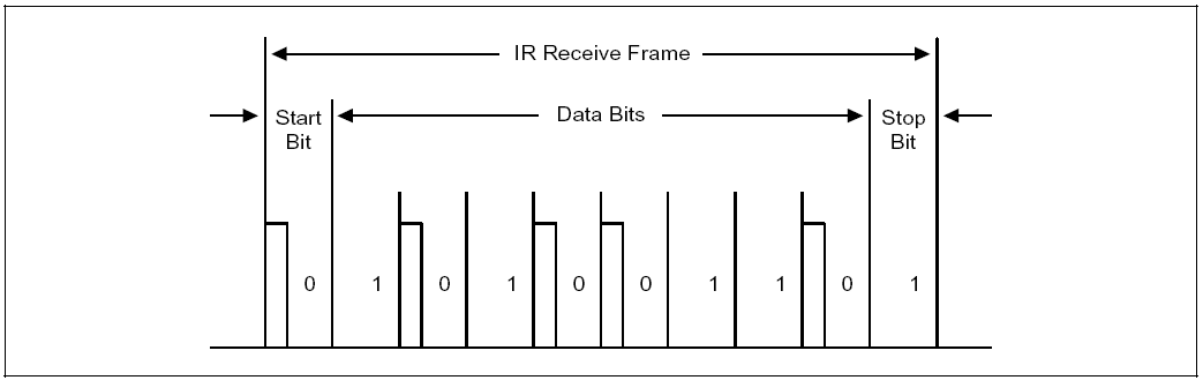

Figure 31-7. Infra-Red Receive Mode Frame Timing Diagram

31.4 외부 인터페이스

Name	Type	Description
XuRXD[0]	Input	Receive data for UART0
XuTXD[0]	Output	Transmit data for UART0
XuCTSn[0]	Input	Clear to Send(active low) for UART0
XuRTSn[0]	Output	Request to Send(active low) for UART0
XuRXD[1]	Input	Receive data for UART1
XuTXD[1]	Output	Transmit data for UART1
XuCTSn[1]	Input	Clear to Send(active low) for UART1
XuRTSn[1]	Output	Request to Send(active low) for UART1
XuRXD[2]	Input	Receive data for UART2
XuTXD[2]	Output	Transmit data for UART2
XuRXD[3]	Input	Receive data for UART3
XuTXD[3]	Output	Transmit data for UART3

NOTE: UART 외부 핀은 다른 콘트롤러와 공유된다. CFCON, IrDA 등등 처럼. UART에서 이 pad를 사용하기 위해, GPIO는 UART가 시작하기 전에 반드시 설정해야 한다. 더 많은 정보는 올바른 GPIO 설정을 위해 이 설명서의 GPIO chapter를 참고하자.

31.5 레지스터 요약

31.5.1 MEMORY MAP

Register	Address	R/W	Description	Reset Value
ULCON0	0x7F005000	R/W	UART channel 0 line control register	0x00
UCON0	0x7F005004	R/W	UART channel 0 control register	0x00
UFCON0	0x7F005008	R/W	UART channel 0 FIFO control register	0x0
UMCON0	0x7F00500C	R/W	UART channel 0 Modem control register	0x0
UTRSTAT0	0x7F005010	R	UART channel 0 Tx/Rx status register	0x6
UERSTAT0	0x7F005014	R	UART channel 0 Rx error status register	0x0
UFSTAT0	0x7F005018	R	UART channel 0 FIFO status register	0x00
UMSTAT0	0x7F00501C	R	UART channel 0 Modem status register	0x0
UTXH0	0x7F005020	W	UART channel 0 transmit buffer register	-
URXH0	0x7F005024	R	UART channel 0 receive buffer register	0x00
UBRDIV0	0x7F005028	R/W	UART channel 0 Baud rate divisior register	0x0000
UDIVSLOT0	0x7F00502C	R/W	UART channel 0 Dividing slot register	0x0000
UINTP0	0x7F005030	R/W	UART channel 0 Interrupt Pending Register	0x0
UINTSP0	0x7F005034	R/W	UART channel 0 Interrupt Source Pending Register	0x0
UINTM0	0x7F005038	R/W	UART channel 0 Interrupt Mask Register	0x0
ULCON1	0x7F005400	R/W	UART channel 1 line control register	0x00
UCON1	0x7F005404	R/W	UART channel 1 control register	0x00
UFCON1	0x7F005408	R/W	UART channel 1 FIFO control register	0x0
UMCON1	0x7F00540C	R/W	UART channel 1 Modem control register	0x0
UTRSTAT1	0x7F005410	R	UART channel 1 Tx/Rx status register	0x6
UERSTAT1	0x7F005414	R	UART channel 1 Rx error status register	0x0
UFSTAT1	0x7F005418	R	UART channel 1 FIFO status register	0x00
UMSTAT1	0x7F00541C	R	UART channel 1 Modem status register	0x0
UTXH1	0x7F005420	W	UART channel 1 transmit buffer register	-
URXH1	0x7F005424	R	UART channel 1 receive buffer register	0x00
UBRDIV1	0x7F005428	R/W	UART channel 1 Baud rate divisior register	0x0000
UDIVSLOT1	0x7F00542C	R/W	UART channel 1 Dividing slot register	0x0000
UINTP1	0x7F005430	R/W	UART channel 1 Interrupt Pending Register	0x0
UINTSP1	0x7F005434	R/W	UART channel 1 Interrupt Source Pending Register	0x0
UINTM1	0x7F005438	R/W	UART channel 1 Interrupt Mask Register	0x0

Register	Address	R/W	Description	Reset Value
ULCON2	0x7F005800	R/W	UART channel 2 line control register	0x00
UCON2	0x7F005804	R/W	UART channel 2 control register	0x00
UFCON2	0x7F005808	R/W	UART channel 2 FIFO control register	0x0
UTRSTAT2	0x7F005810	R	UART channel 2 Tx/Rx status register	0x6
UERSTAT2	0x7F005814	R	UART channel 2 Rx error status register	0x0
UFSTAT2	0x7F005818	R	UART channel 2 FIFO status register	0x00
UTXH2	0x7F005820	W	UART channel 2 transmit buffer register	-
URXH2	0x7F005824	R	UART channel 2 receive buffer register	0x00
UBRDIV2	0x7F005828	R/W	UART channel 2 Baud rate divisior register	0x0000
UDIVSLOT2	0x7F00582C	R/W	UART channel 2 Dividing slot register	0x0000
INTP2	0x7F005830	R/W	UART channel 2 Interrupt Pending Register	0x0
UINTSP2	0x7F005834	R/W	UART channel 2 Interrupt Source Pending Register	0x0
UINTM2	0x7F005838	R/W	UART channel 2 Interrupt Mask Register	0x0
ULCON3	0x7F005C00	R/W	UART channel 3 line control register	0x00
UCON3	0x7F005C04	R/W	UART channel 3 control register	0x00
UFCON3	0x7F005C08	R/W	UART channel 3 FIFO control register	0x0
UTRSTAT3	0x7F005C10	R	UART channel 3 Tx/Rx status register	0x6
UERSTAT3	0x7F005C14	R	UART channel 3 Rx error status register	0x0
UFSTAT3	0x7F005C18	R	UART channel 3 FIFO status register	0x00
UTXH3	0x7F005C20	W	UART channel 3 transmit buffer register	-
URXH3	0x7F005C24	R	UART channel 3 receive buffer register	0x00
UBRDIV3	0x7F005C28	R/W	UART channel 3 Baud rate divisior register	0x0000
UDIVSLOT3	0x7F005C2C	R/W	UART channel 3 Dividing slot register	0x0000
INTP3	0x7F005C30	R/W	UART channel 3 Interrupt Pending Register	0x0
UINTSP3	0x7F005C34	R/W	UART channel 3 Interrupt Source Pending Register	0x0
UINTM3	0x7F005C38	R/W	UART channel 3 Interrupt Mask Register	0x0

31.6 Individual register description (따로 떨어진(단일의) 레지스터 요약)

31.6.1 UART LINE CONTROL REGISTER

Register	Address	R/W	Description	Reset Value
ULCON0	0x7F005000	R/W	UART channel 0 line control register	0x00
ULCON1	0x7F005400	R/W	UART channel 1 line control register	0x00
ULCON2	0x7F005800	R/W	UART channel 2 line control register	0x00
ULCON3	0x7F005C00	R/W	UART channel 3 line control register	0x00

There are three UART line control registers including ULCON0, ULCON1, ULCON2 and ULCON3 in the UART block.

ULCONn	Bit	Description	Initial State
Reserved	[7]		0
Infra-Red Mode	[6]	Determine whether or not to use the Infra-Red mode. 0 = Normal mode operation 1 = Infra-Red Tx/Rx mode	0
Parity Mode	[5:3]	Specify the type of parity generation and checking during UART transmit and receive operation. 0xx = No parity 100 = Odd parity 101 = Even parity 110 = Parity forced/checked as 1 111 = Parity forced/checked as 0	000
Number of Stop Bit	[2]	Specify how many stop bits are to be used for end-of-frame signal. 0 = One stop bit per frame 1 = Two stop bit per frame	0
Word Length	[1:0]	Indicate the number of data bits to be transmitted or received per frame. 00 = 5-bit 01 = 6-bit 10 = 7-bit 11 = 8-bit	00

31.6.2 UART CONTROL REGISTER

Register	Address	R/W	Description	Reset Value
UCON0	0x7F005004	R/W	UART channel 0 control register	0x00
UCON1	0x7F005404	R/W	UART channel 1 control register	0x00
UCON2	0x7F005804	R/W	UART channel 2 control register	0x00
UCON3	0x7F005C04	R/W	UART channel 3 control register	0x00

There are three UART control registers including UCON0, UCON1, UCON2 and UCON3 in the UART block.

UCONn	Bit	Description	Initial State
Clock Selection	[11:10]	Select PCLK or EXT_UCLK0[4] or EXT_UCLK1[4] clock for the UART baud rate. x0 = PCLK : DIV_VAL[1] = (PCLK / (bps x 16)) -1 01 = EXT_UCLK0: DIV_VAL[1] = (EXT_UCLK0 / (bps x 16)) –1 11 = EXT_UCLK1: DIV_VAL[1] = (EXT_UCLK1 / (bps x 16)) –1	0
Tx Interrupt Type	[9]	Interrupt request type.[2] 0 = Pulse (Interrupt is requested as soon as the Tx buffer becomes empty in Non-FIFO mode or reaches Tx FIFO Trigger Level in FIFO mode.) 1 = Level (Interrupt is requested while Tx buffer is empty in Non-FIFO mode or reaches Tx FIFO Trigger Level in FIFO mode.)	0
Rx Interrupt Type	[8]	Interrupt request type. [2] 0 = Pulse (Interrupt is requested the instant Rx buffer receives the data in Non-FIFO mode or reaches Rx FIFO Trigger Level in FIFO mode.) 1 = Level (Interrupt is requested while Rx buffer is receiving data in Non-FIFO mode or reaches Rx FIFO Trigger Level in FIFO mode.)	0
Rx Time Out Enable	[7]	Enable/Disable Rx time-out interrupts when UART FIFO is enabled. The interrupt is a receive interrupt.[3] 0 = Disable 1 = Enable	0
Rx Error Status Interrupt Enable	[6]	Enable the UART to generate an interrupt upon an exception, such as a break, frame error, parity error, or overrun error during a receive operation. 0 = Do not generate receive error status interrupt. 1 = Generate receive error status interrupt.	0
Loop-back Mode	[5]	Setting loop-back bit to 1 cause the UART to enter the loop-back mode. This mode is provided for test purposes only. 0 = Normal operation 1 = Loop-back mode	0
Send Break Signal	[4]	Setting this bit causes the UART to send a break during 1 frame time. This bit is automatically cleared after sending the break signal. 0 = Normal transmit 1 = Send break signal	0

UCONn	Bit	Description	Initial State
Transmit Mode	[3:2]	Determine which function is currently able to write Tx data to the UART transmit buffer register. 00 = Disable 01 = Interrupt request or polling mode 10 = DMA request (DMA_UART0) 11 = DMA request (DMA_UART1)	00
Receive Mode	[1:0]	Determine which function is currently able to read data from UART receive buffer register. 00 = Disable 01 = Interrupt request or polling mode 10 = DMA request (DMA_UART0) 11 = DMA request (DMA_UART1)	00

NOTES:

1) DIV_VAL = UBRDIVn + (num of 1's in UDIVSLOTn)/16. Refer to UART Buad Rate Configure Registers.
2) S3C6400 is using a level-triggered interrupt controller. Therefore, these bits must be set to 1 for every transfer.
3) When the UART does not reach the FIFO trigger level and does not receive data during 3 word time in DMA receive mode with FIFO, the Rx interrupt will be generated (receive time out), and the you must check the FIFO status and read out the rest.
4) EXT_UCLK0 clock is external clock.(XpwmECLK PAD input)
   EXT_UCLK1 clock is generated clock by SYSCON. SYSCON generates EXT_UCLK1 for dividing EPLL or MPLL output.

31.6.3 UART FIFO CONTROL REGISTER

Register	Address	R/W	Description	Reset Value
UFCON0	0x7F005008	R/W	UART channel 0 FIFO control register	0x0
UFCON1	0x7F005408	R/W	UART channel 1 FIFO control register	0x0
UFCON2	0x7F005808	R/W	UART channel 2 FIFO control register	0x0
UFCON3	0x7F005C08	R/W	UART channel 3 FIFO control register	0x0

There are three UART FIFO control registers including UFCON0, UFCON1, UFCON2 and UFCON3 in the UART block.

UFCONn	Bit	Description	Initial State
Tx FIFO Trigger Level	[7:6]	Determine the trigger level of transmit FIFO. 00 = Empty 01 = 16-byte 10 = 32-byte 11 = 48-byte	00
Rx FIFO Trigger Level	[5:4]	Determine the trigger level of receive FIFO. 00 = 1-byte 01 = 8-byte 10 = 16-byte 11 = 32-byte	00
Reserved	[3]		0
Tx FIFO Reset	[2]	Auto-cleared after resetting FIFO 0 = Normal 1= Tx FIFO reset	0
Rx FIFO Reset	[1]	Auto-cleared after resetting FIFO 0 = Normal 1= Rx FIFO reset	0
FIFO Enable	[0]	0 = Disable 1 = Enable	0

31.6.4 UART MODEM CONTROL REGISTER

Register	Address	R/W	Description	Reset Value
UMCON0	0x7F00500C	R/W	UART channel 0 Modem control register	0x0
UMCON1	0x7F00540C	R/W	UART channel 1 Modem control register	0x0
Reserved	0x7F00580C	-	Reserved	Undef
Reserved	0x7F005C0C	-	Reserved	Undef

There are two UART MODEM control registers including UMCON0 and UMCON1 in the UART block.

UMCONn	Bit	Description	Initial State
RTS trigger Level	[7:5]	When AFC bit is enabled, these bits determine when to inactivate nRTS signal. 000 = When RX FIFO contains 63 bytes. 001 = When RX FIFO contains 56 bytes. 010 = When RX FIFO contains 48 bytes. 011 = When RX FIFO contains 40 bytes. 100 = When RX FIFO contains 32 bytes. 101 = When RX FIFO contains 24 bytes. 110 = When RX FIFO contains 16 bytes. 111 = When RX FIFO contains 8 bytes.	000
Auto Flow Control (AFC)	[4]	0 = Disable 1 = Enable	0
Modem Interrupt enable	[3]	Modem interrupt enable 0 = Disable 1 = Enable	000
Reserved	[2:1]	These bits must be 0's	000
Request to Send	[0]	If AFC bit is enabled, this value will be ignored. In this case the S3C6400 will control nRTS automatically. If AFC bit is disabled, nRTS must be controlled by software. 0 = 'H' level (Inactivate nRTS) 1 = 'L' level (Activate nRTS)	0

NOTE: UART 2 does not support AFC function, because the S3C6400X has no nRTS2 and nCTS2.
UART 3 does not support AFC function, because the S3C6400X has no nRTS3 and nCTS3.

31.6.5 UART TX/RX STATUS REGISTER

Register	Address	R/W	Description	Reset Value
UTRSTAT0	0x7F005010	R	UART channel 0 Tx/Rx status register	0x6
UTRSTAT1	0x7F005410	R	UART channel 1 Tx/Rx status register	0x6
UTRSTAT2	0x7F005810	R	UART channel 2 Tx/Rx status register	0x6
UTRSTAT3	0x7F005C10	R	UART channel 3 Tx/Rx status register	0x6

There are three UART Tx/Rx status registers including UTRSTAT0, UTRSTAT1, UTRSTAT2 and UTRSTAT3 in the UART block.

UTRSTATn	Bit	Description	Initial State
Transmitter empty	[2]	Set to 1 automatically when the transmit buffer register has no valid data to transmit and the transmit shift register is empty. 0 = Not empty 1 = Transmitter (transmit buffer & shifter register) empty	1
Transmit buffer empty	[1]	Set to 1 automatically when transmit buffer register is empty. 0 =The buffer register is not empty 1 = Empty (In Non-FIFO mode, Interrupt or DMA is requested. In FIFO mode, Interrupt or DMA is requested, when Tx FIFO Trigger Level is set to 00 (Empty)) If the UART uses the FIFO, you must check Tx FIFO Count bits and Tx FIFO Full bit in the UFSTAT register instead of this bit.	1
Receive buffer data ready	[0]	Set to 1 automatically whenever receive buffer register contains valid data, received over the RXDn port. 0 = Empty 1 = The buffer register has a received data (In Non-FIFO mode, Interrupt or DMA is requested) If the UART uses the FIFO, you must check Rx FIFO Count bits and Rx FIFO Full bit in the UFSTAT register instead of this bit.	0

31.6.6 UART ERROR STATUS REGISTER

Register	Address	R/W	Description	Reset Value
UERSTAT0	0x7F005014	R	UART channel 0 Rx error status register	0x0
UERSTAT1	0x7F005414	R	UART channel 1 Rx error status register	0x0
UERSTAT2	0x7F005814	R	UART channel 2 Rx error status register	0x0
UERSTAT3	0x7F005C14	R	UART channel 3 Rx error status register	0x0

There are three UART Rx error status registers including UERSTAT0, UERSTAT1, UERSTAT2 and UERSTAT3 in the UART block.

UERSTATn	Bit	Description	Initial State
Break Detect	[3]	Set to 1 automatically to indicate that a break signal has been received. 0 = Send Break signal is not received 1 = Send Break (signal is received Interrupt is requested.)	0
Frame Error	[2]	Set to 1 automatically whenever a frame error occurs during reception operation. 0 = No frame error during reception 1 = Frame error (Interrupt is requested.)	0
Parity Error	[1]	Set to 1 automatically whenever a parity error occurs during receive operation. 0 = No parity error during reception 1 = Parity error (Interrupt is requested.)	0
Overrun Error	[0]	Set to 1 automatically whenever an overrun error occurs during receive operation. 0 = No overrun error during reception 1 = Overrun error (Interrupt is requested.)	0

NOTE: These bits (UERSATn[3:0]) are automatically cleared to 0 when the UART error status register is read.

31.6.7 UART FIFO STATUS REGISTER

Register	Address	R/W	Description	Reset Value
UFSTAT0	0x7F005018	R	UART channel 0 FIFO status register	0x00
UFSTAT1	0x7F005418	R	UART channel 1 FIFO status register	0x00
UFSTAT2	0x7F005818	R	UART channel 2 FIFO status register	0x00
UFSTAT3	0x7F005C18	R	UART channel 3 FIFO status register	0x00

There are three UART FIFO status registers including UFSTAT0, UFSTAT1, UFSTAT2 and UFSTAT3 in the UART block.

UFSTATn	Bit	Description	Initial State
Reserved	[15]		0
Tx FIFO Full	[14]	Set to 1 automatically whenever transmit FIFO is full during transmit operation 0 = 0-byte ≤ Tx FIFO data ≤ 63-byte 1 = Full	0
Tx FIFO Count	[13:8]	Number of data in Tx FIFO	0
Reserved	[7]		0
Rx FIFO Full	[6]	Set to 1 automatically whenever receive FIFO is full during receive operation 0 = 0-byte ≤ Rx FIFO data ≤ 63-byte 1 = Full	0
Rx FIFO Count	[5:0]	Number of data in Rx FIFO	0

31.6.8 UART MODEM STATUS REGISTER

Register	Address	R/W	Description	Reset Value
UMSTAT0	0x7F00501C	R	UART channel 0 Modem status register	0x0
UMSTAT1	0x7F00541C	R	UART channel 1 Modem status register	0x0
Reserved	0x7F00581C	-	Reserved	Undef
Reserved	0x7F005C1C	-	Reserved	Undef

There are two UART modem status registers including UMSTAT0 and UMSTAT1 in the UART block.

UMSTAT0	Bit	Description	Initial State
Reserved	[7:5]	reserved	000
Delta CTS	[4]	Indicate that the nCTS input to the S3C6400 has changed state since the last time it was read by CPU. (Figure 31-8) 0 = Has not changed 1 = Has changed	0
Reserved	[3:1]	reserved	00
Clear to Send	[0]	0 = CTS signal is not activated (nCTS pin is high) 1 = CTS signal is activated (nCTS pin is low)	0

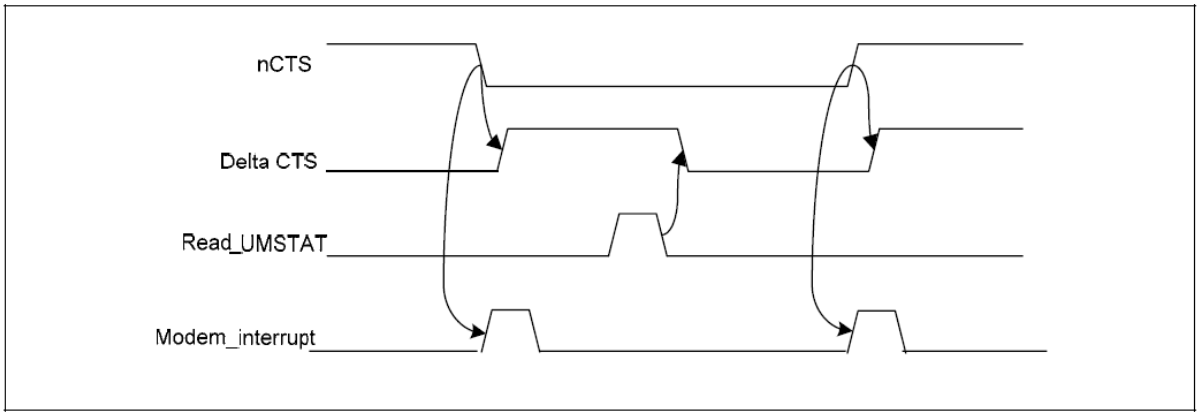

Figure 31-8. nCTS and Delta CTS Timing Diagram

31.6.9 UART TRANSMIT BUFFER REGISTER (HOLDING REGISTER & FIFO REGISTER)

Register	Address	R/W	Description	Reset Value
UTXH0	0x7F005020	W	UART channel 0 transmit buffer register	-
UTXH1	0x7F005420	W	UART channel 1 transmit buffer register	-
UTXH2	0x7F005820	W	UART channel 2 transmit buffer register	-
UTXH3	0x7F005C20	W	UART channel 3 transmit buffer register	-

There are four UART transmitting buffer registers including UTXH0, UTXH1, UTXH2 and UTXH3 in the UART block. UTXHn has an 8-bit data for transmitting data.

UTXHn	Bit	Description	Initial State
TXDATAn	[7:0]	Transmit data for UARTn	-

31.6.10 UART RECIVE BUFFER REGISTER (HOLDING REGISTER & FIFO REGISTER)

There are four UART receiving buffer registers including URXH0, URXH1, URXH2 and URXH3 in the UART block. URXHn has an 8-bit data for received data.

Register	Address	R/W	Description	Reset Value
URXH0	0x7F005024	R	UART channel 0 receive buffer register	0x00
URXH1	0x7F005424	R	UART channel 1 receive buffer register	0x00
URXH2	0x7F005824	R	UART channel 2 receive buffer register	0x00
URXH3	0x7F005C24	R	UART channel 3 receive buffer register	0x00

URXHn	Bit	Description	Initial State
RXDATAn	[7:0]	Receive data for UARTn	0x00

NOTE: When an overrun error occurs, the URXHn must be read. If not, the next received data will also make an overrun error, even though the overrun bit of UERSTATn had been cleared.

31.6.11 UART Baud Rate 설정 레지스터

4개의 UART baud rate 제수(나눗수) 레지스터가 있고 UART 블록의 UBRDIV0, UBRDIV1, UBRDIV2, UBRDIV3를 포함하고 있다.

값은 baud rate 제수 레지스터 (UBRDIVn)와 dividing slot 레지스터 (UDIVSLOTn)에 저장되고, 이것은 다음의 시리얼 Tx/Rx 클럭 비율(baud rate)을 결정하는데 사용된다.

DIV_VAL = UBRDIVn + (num of 1's in UDIVSLOTn)/16
DIV_VAL = (PCLK / (bps x 16)) –1
DIV_VAL = (EXT_UCLK0 / (bps x 16)) –1
or
DIV_VAL = (EXT_UCLK1 / (bps x 16)) –1

Divisor는 1에서 (2^16-1) 까지여야만 한다.
UDIVSLOT를 사용하면 사용자가 좀더 정확한 baud rate를 만들 수 있다.
예를들어 만약 baud-rate가 115200 bps이고 EXT_UCLK0이 UART baud-rate 클럭과 40MHz 이면, UBRDIVn과 UDIVSLOTn은

DIV_VAL = (40000000 / (115200 x 16)) -1
= 21.7 -1
= 20.7

UBRDIVn = 20 (integer part of DIV_VAL)
(num of 1's in UDIVSLOTn)/16 = 0.7
then, (num of 1's in UDIVSLOTn) = 11
so, UDIVSLOTn can be 16'b1110_1110_1110_1010 or 16'b0111_0111_0111_0101, etc.

우리는 다음의 표에 나타낸 것처럼 UDIVSLOTn을 선택하길 추천한다.

Num of 1's	UDIVSLOTn	Num of 1's	UDIVSLOTn
0	0x0000(0000_0000_0000_0000b)	8	0x5555(0101_0101_0101_0101b)
1	0x0080(0000_0000_0000_1000b)	9	0xD555(1101_0101_0101_0101b)
2	0x0808(0000_1000_0000_1000b)	10	0xD5D5(1101_0101_1101_0101b)
3	0x0888(0000_1000_1000_1000b)	11	0xDDD5(1101_1101_1101_0101b)
4	0x2222(0010_0010_0010_0010b)	12	0xDDDD(1101_1101_1101_1101b)
5	0x4924(0100_1001_0010_0100b)	13	0xDFDD(1101_1111_1101_1101b)
6	0x4A52(0100_1010_0101_0010b)	14	0xDFDF(1101_1111_1101_1111b)
7	0x54AA(0101_0100_1010_1010b)	15	0xFFDF(1111_1111_1101_1111b)

31.6.12 Baud-Rate Error Tolerance (통신속도 에러 허용치)

UART Frame error should be less than 1.87%(3/160)
tUPCLK = (UBRDIVn + 1) x 16 x 1Frame / (PCLK ,EXT_UCLK0 or EXT_UCLK1) tUPCLK: Real UART Clock
tEXTUARTCLK = 1Frame / baud-rate tEXTUARTCLK: Ideal UART Clock
UART error = (tUPCLK – tEXTUARTCLK) / tEXTUARTCLK x 100%

NOTE: 1Frame = start bit + data bit + parity bit + stop bit.

31.6.13 UART 클럭과 PCLK와의 관계

PCLK와 UARTCLK에서 클럭 주파수의 비율에 제약이 있다.

UARTCLK 주파수는 5.5보다 크면 안되고 PCLK 주파수보다 3배이상 빠르면 안된다.

$F_{UARTCLK} <= 5.5/3 \times F_{PCLK}$ **$F_{UARTCLK} = baudrate \times 16$**

이것은 receive data를 receive FIFO로 write하는 충분한 시간을 허락한다.

Register	Address	R/W	Description	Reset Value
UBRDIV0	0x7F005028	R/W	Baud rate divisior register 0	0x0000
UBRDIV1	0x7F005428	R/W	Baud rate divisior register 1	0x0000
UBRDIV2	0x7F005828	R/W	Baud rate divisior register 2	0x0000
UBRDIV3	0x7F005C28	R/W	Baud rate divisior register 3	0x0000

UBRDIV n	Bit	Description	Initial State
UBRDIV	[15:0]	Baud rate division value (When UART clock source is PCLK, UBRDIVn must be more than 0 (UBRDIVn >0))	-

Register	Address	R/W	Description	Reset Value
UDIVSLOT0	0x7F00502C	R/W	Baud rate divisior register 0	0x0000
UDIVSLOT1	0x7F00542C	R/W	Baud rate divisior register 1	0x0000
UDIVSLOT2	0x7F00582C	R/W	Baud rate divisior register 2	0x0000
UDIVSLOT3	0x7F005C2C	R/W	Baud rate divisior register 3	0x0000

UDIVSLOT n	Bit	Description	Initial State
UDIVSLOT	[15:0]	Select the slot where clock generator divide clock source	-

31.6.14 UART INTERRUPT PENDING REGISTER

Register	Address	R/W	Description	Reset Value
UINTP0	0x7F005030	R/W	Interrupt Pending Register for UART channel 0	0x0
UINTP1	0x7F005430	R/W	Interrupt Pending Register for UART channel 1	0x0
UINTP2	0x7F005830	R/W	Interrupt Pending Register for UART channel 2	0x0
UINTP3	0x7F005C30	R/W	Interrupt Pending Register for UART channel 3	0x0

Interrupt pending register contains the information of the interrupts, which are generated.

UINTPn	Bit	Description	Initial State
MODEM	[3]	Modem interrupt generated.	0
TXD	[2]	Transmit interrupt generated.	0
ERROR	[1]	Error interrupt generated.	0
RXD	[0]	Receive interrupt generated.	0

Whenever one of above 4 bits is logical high ('1'), each UART channel generates interrupt.
This register has to be cleared in the interrupt service routine.
You can clear specific bits of UINTP register by writing 1's to the bits that you want to clear.

31.6.15 UART INTERRUPT SOURCE PENDING REGISTER

Interrupt Source Pending Register contains the information which interrupt are generated regardless of the value of Interrupt Mask Register

You can clear specific bits of UINTSP register by writing 1's to the bits that you want to clear.

Register	Address	R/W	Description	Reset Value
UINTSP0	0x7F005034	R/W	Interrupt Source Pending Register 0	0x0
UINTSP1	0x7F005434	R/W	Interrupt Source Pending Register 1	0x0
UINTSP2	0x7F005834	R/W	Interrupt Source Pending Register 2	0x0
UINTSP3	0x7F005C34	R/W	Interrupt Source Pending Register 3	0x0

UINTSPn	Bit	Description	Initial State
MODEM	[3]	Modem interrupt generated.	0
TXD	[2]	Transmit interrupt generated.	0
ERROR	[1]	Error interrupt generated.	0
RXD	[0]	Receive interrupt generated.	0

31.6.16 UART 인터럽트 마스크 레지스터

인터럽트 마스트 레지스터는 mask된(인터럽트 떳음) 인터럽트 정보를 포함하고 있다. 만약 특별한 비트를 1로 설정하면 인터럽트 콘트롤러로의 인터럽트 요청 신호는 유사한 인터럽트가 발생한다 해도 생성되지 않는다. (INTSPn 레지스터에 부합하는 비트를 1로 설정하는 경우에도) 만약 mask 비트가 0이면, 인터럽트 요청은 유사한 인터럽트 소스로부터 제공받을 수 있다.

(Note that even in such a case, the corresponding bit of UINTSPn register is set to 1).

Register	Address	R/W	Description	Reset Value
UINTM0	0x7F005038	R/W	Interrupt Mask Register for UART channel 0	0x0
UINTM1	0x7F005438	R/W	Interrupt Mask Register for UART channel 1	0x0
UINTM2	0x7F005838	R/W	Interrupt Mask Register for UART channel 2	0x0
UINTM3	0x7F005C38	R/W	Interrupt Mask Register for UART channel 3	0x0

UINTMn	Bit	Description	Initial State
MODEM	[3]	Mask Modem interrupt.	0
TXD	[2]	Mask Transmit interrupt.	0
ERROR	[1]	Mask Error interrupt.	0
RXD	[0]	Mask Receive interrupt.	0

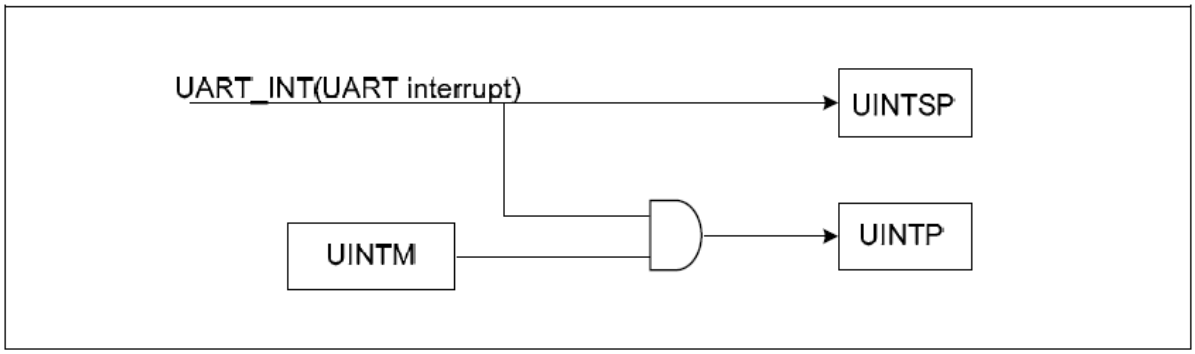

Figure 31-9. UINTSP,UINTP and UINTM block diagram

Revision History

Date	Editor	Version	Descriptions
2008-08-03	Sejong Lee	1.0	최초 작성