24 HOST INTERFACE

24.1 OVERVIEW

S3C6400X의 호스트 인터페이스 블록은 외부 호스트 장치(Ex:모뎀칩)의 간접적 접근을 지원한다. 선택된 호스트 인터페이스 프로토콜에 의해 다음의 동작이 지원된다.

- 16비트 프로토콜 레지스터
- 시스템 메모리 맵에서 SFR/memory 에 싱글 R/W
- 시스템 메모리 맵에서 SFR/memory 에 버스트 R/W
- 시스템 메모리 맵에서 SFR/memory 에 반복 버스트 쓰기
- S3C6400X에 연관된 낸드 플레쉬 없이 부팅 가능하도록 하는 모뎀 부팅을 지원

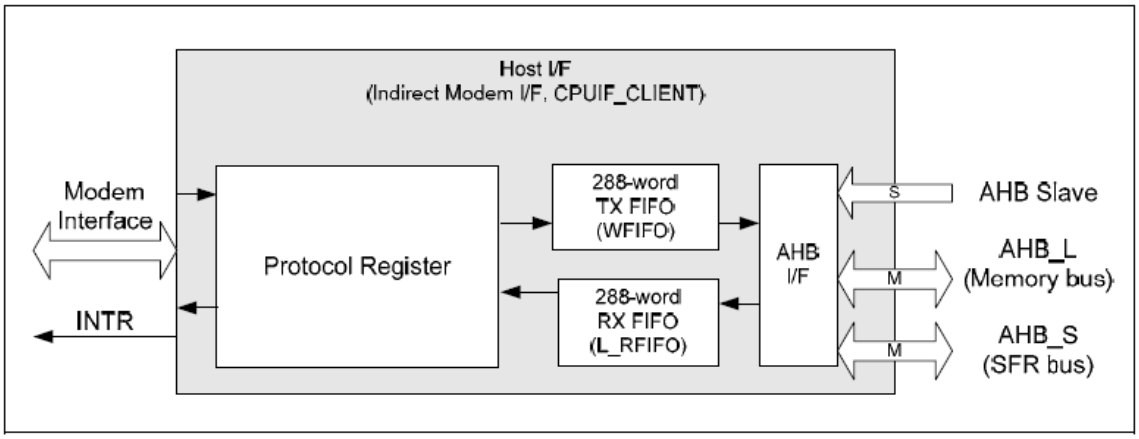

Figure 24-1. HOST I/F Block Diagram

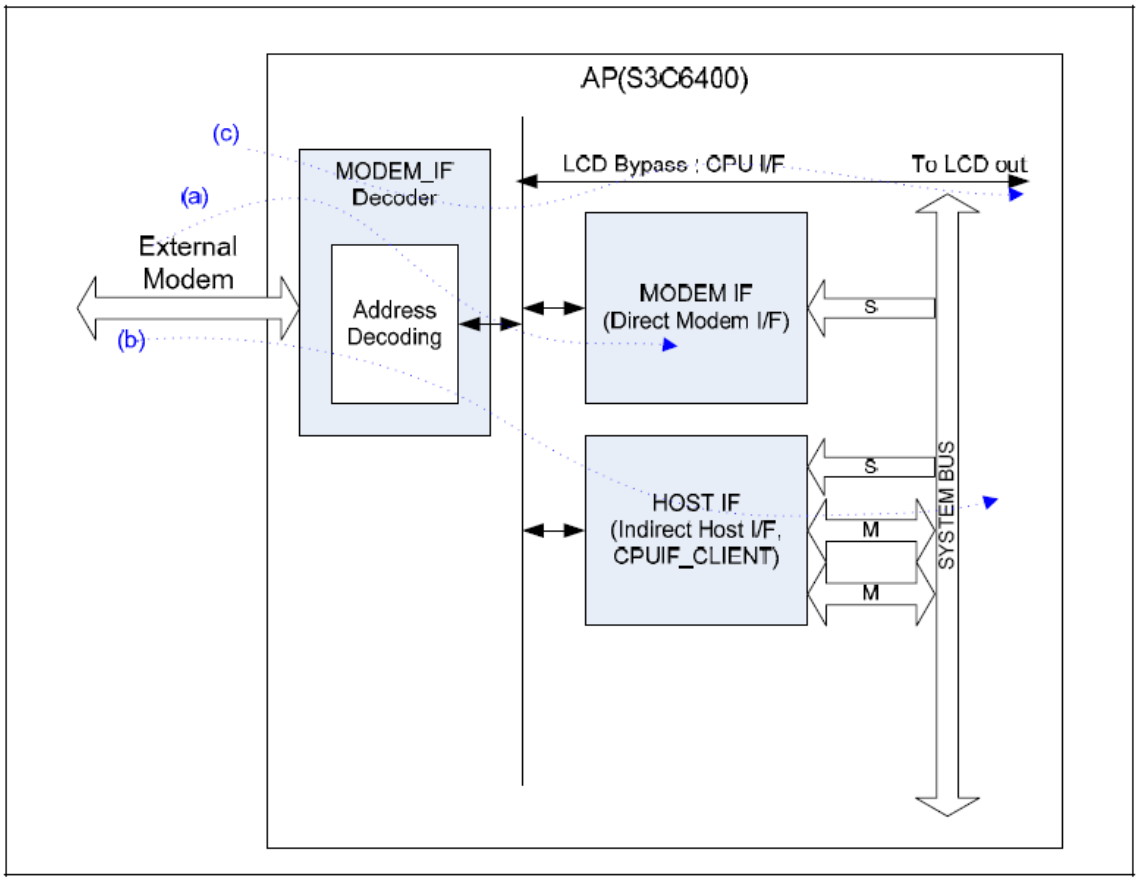

Figure 24-2. Data flow of the the External Host device (MODEM) and the AP

S3C6400X(AP)의 외부 호스트 인터페이스는 (a)다이렉트 인터페이스 패스(MODEM_IF),(b)간접적 인터페이스 패스(HOST_IF)와 (c)LCD 바이패스 패스(그림 24-2)를 지원한다.

XhiCSn='0'일때 모뎀쪽의 어드레스 매핑은 아래와 같다.

XhiADDR			Host/Modem Interface select	Description
[12]	[11:8]	[7]		
0	XXX	X	Modem Interface (Direct interface)	
1	0000	X	Host Interface (Indirect interface)	Xhi_ADDR[2] = '0' : Indirect Host I/F, Xhi_ADDR[2] = '1' : Reserved
1	0001	0	SLEEP/STOP mode Wakeup assert	Write Operation
1	0001	1	SLEEP/STOP mode Wakeup clear	Write Operation
1	100X	X	LCD Bypass main	
1	101X	X	LCD Bypass sub	

NOTE: Xhi_CSn_main, Xhi_CSn_sub : Another Chip Select signals for LCD Bypass main and sub

24.2 FEATURES

호스트 인터페이스(간접적 모뎀 인터페이스) 특징들

- 비동기식 간접적 16비트 SRAM 스타일 호스트 인터페이스(i80)
- 호스트 인터페이스를 위한 banked 16-bit protocol register
- 1KB까지 버스트 쓰기/읽기 전송을 지원하기위해 Write-FIFO, Read-FIFO
- 데이터 교환을 위한 32비트 in-mailbox 와 out-mailbox 레지스터

24.3 FUNCTIONAL DESCRIPTION

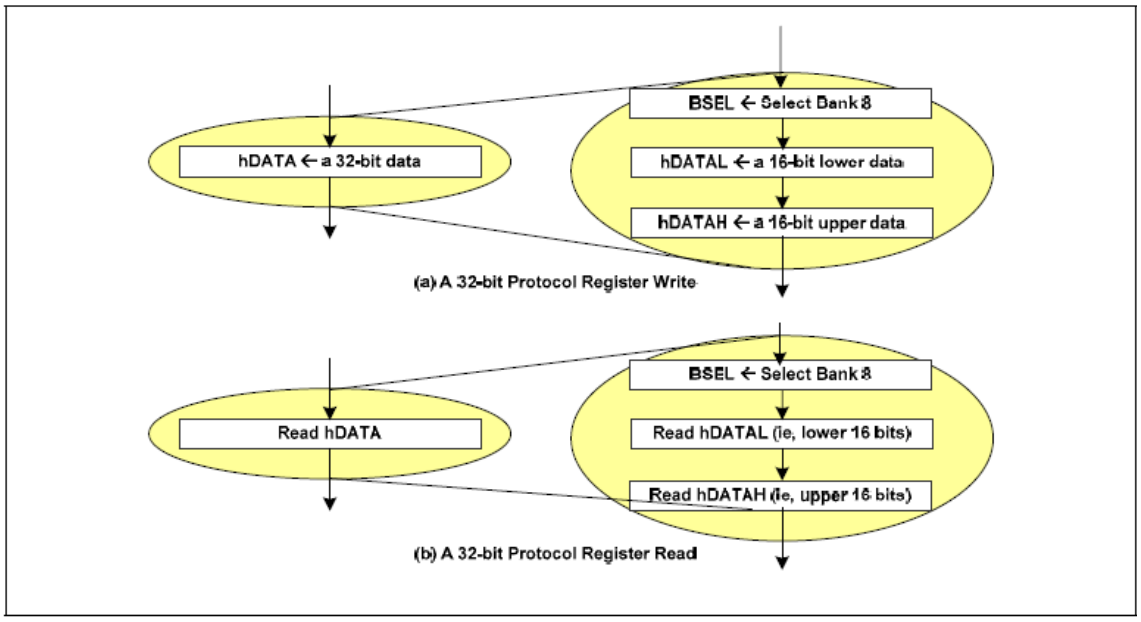

Figure24-3. A 32-bit Protocol Register Access by Using Two 16-bit Read/Write

NOTE:

hDATAL은 호스트 인터페이스 데이터 하위 레지스터이고 hDATAH는 호스트 인터페이스 데이터 상위 레지스터이다. 이 레지스터에 대한 더 많은 정보는 레지스터 설명 섹션을 참조하시오.

24.3.1 READ AND WRITE OF A 16-BIT PROTOCOL REGISTER

16비트 프로토콜 레지스터를 접근하기위해서 다음의 절차를 따라야한다.

1. 먼저 BSEL에 쓰기를 하므로써 상응하는 뱅크를 선택한 다음,
2. 프로토콜 레지스터에 읽기 혹은 쓰기를 한다.

24.3.2 READ AND WRITE OF TWO 16-BIT PROTOCOL REGISTER IN THE SAME BANK

같은 뱅크에서 두 개의 16비트 프로토콜 레지스터를 접근하기 위해 다음의 절차를 밟아야 한다.

1. 먼저 BSEL에 쓰기를 함으로써 상응하는 레지스터를 선택한다,
2. 하위 16비트 프로토콜 레지스터에 읽기 혹은 쓰기를 한 다음,
3. 상위 16비트 프로토콜 레지스터에 읽기 혹은 쓰기를 한다.

24.3.3 SIGNAL WRITE

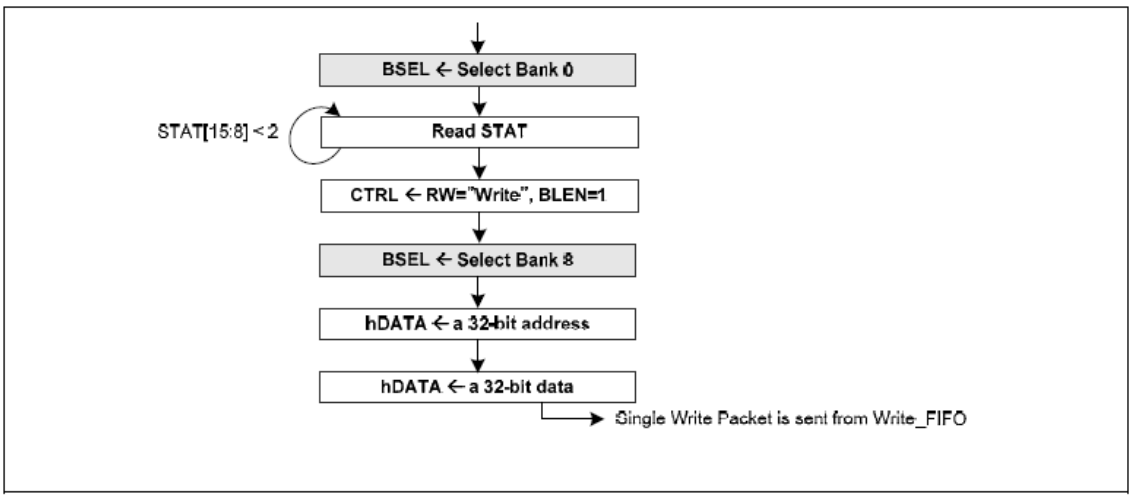

Figure 24-4. Single Write Procedure

24.3.4 SINGLE READ

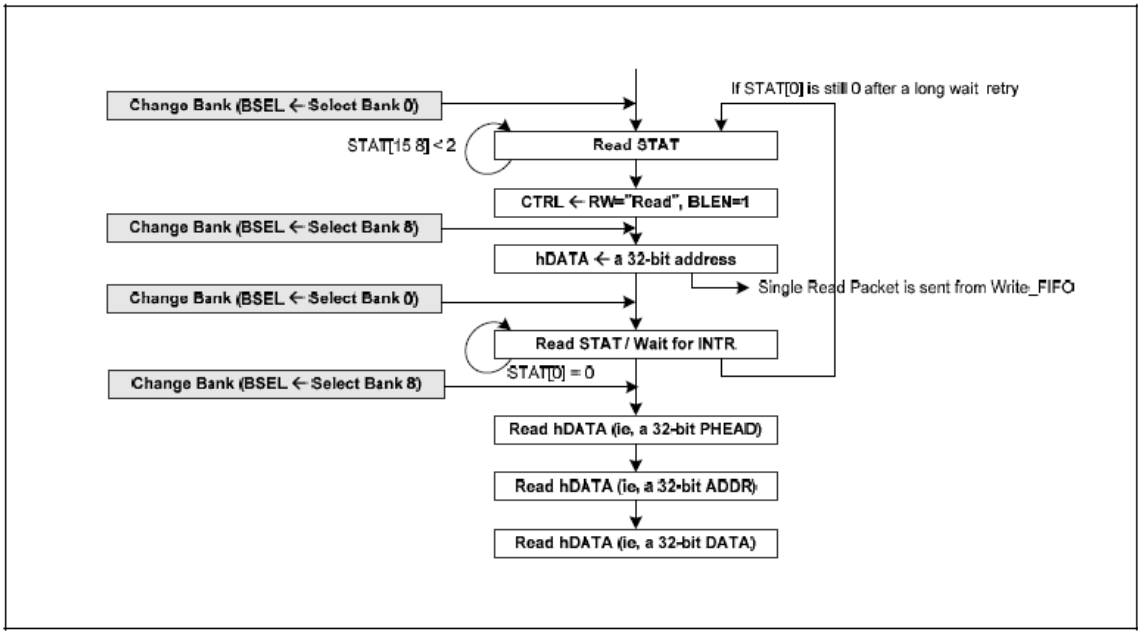

Figure 24-5. Single Read Procedure

이 섹션에서 "HOST I/F"의 이름은 호스트 인터페이스 블록을 의미하고 "HOST"의 이름은 외부 호스트 장치(ex.MODEM)을 의미한다.

HOST I/F AP(S3C6400X)로부터 결과를 읽고 그것은 이 전의 읽기 동작을 완료하기 전에 새로운 읽기 동작을 시작할 수 있다. 결과의 소스에 어떠한 정보도 없다. 그러므로 HOST는 다수의 읽기 동작의 결과가 뒤죽박죽 되었는지를 확인해야만 한다. 예를들어, "Source area A"로부터 버스트 읽기가 발생하였고 버스터 읽기에 대한 결과를 기다리지 않고 "Source area B"로부터 싱글 읽기가 발생하였다면 싱글 읽기에 결과가 읽기버퍼에 더 일찍 도달할 수 있다. 그 결과 받은 결과의 주소는 요청 주소와 비교를 해야만 한다.

그러나 같은 "Source area"에 다수의 읽기 동작을 위해 결과의 순서는 유지해야한다.

위의 상황(i.e., Out-order Execution Issue)을 피하기 위한 간단한 방법은 다른 읽기 명령(i.e., Single or Burst Read)이 발생하기 전에 이 전 결과가 완전히 읽었는지를 확인하는 것이다.

HOST는 16비트 상태레지스터(i.e.,STAT[0])를 폴링하거나 혹은 인터럽트를 사용하여(i.e.,INTR) 32비트 상태레지스터의 상태를 알 수 있다.

24.3.5 BURST WRITE

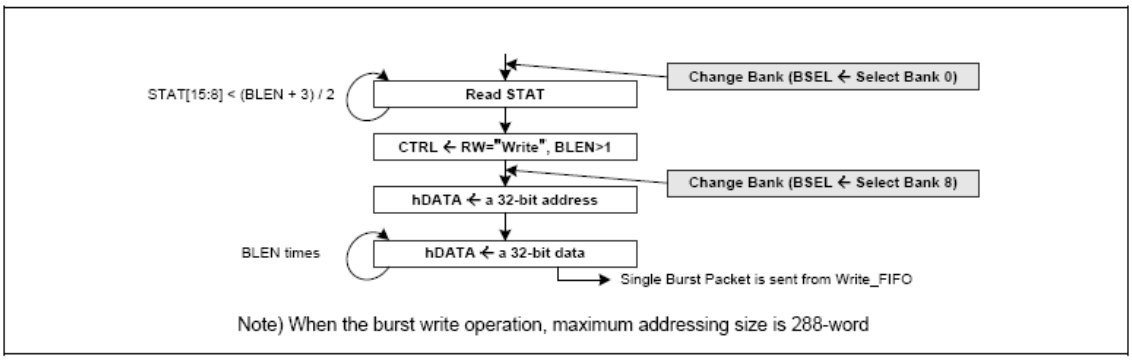

Figure 24-6. Burst Write Procedure

24.3.6 BURST READ

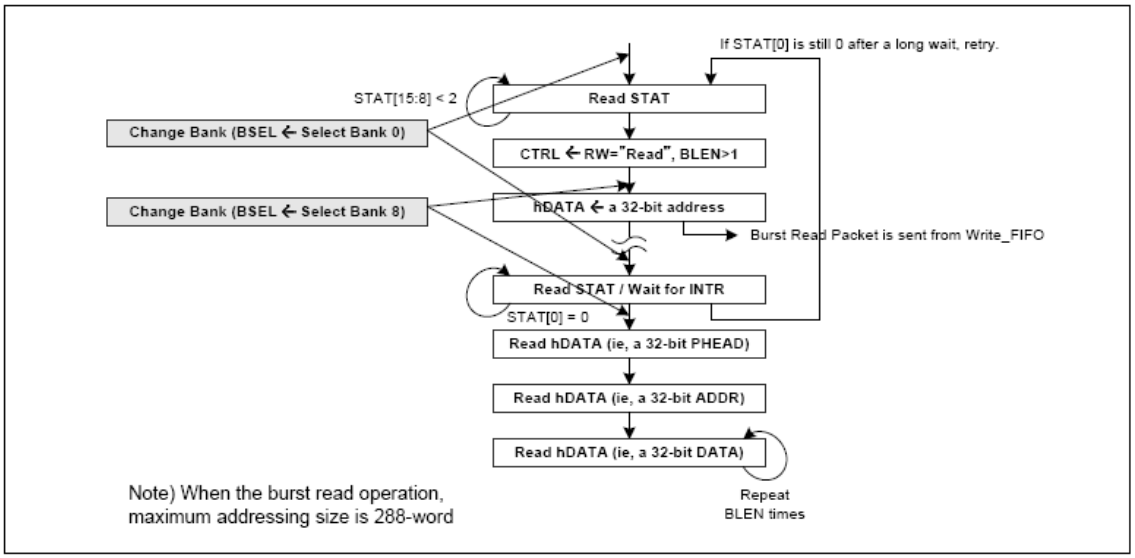

Figure 24-7. Burst Read Procedure

24.3.7 REPEATED BURST WRITE TO REDUCE THE HOST(EX.MODEM) OVERHEAD

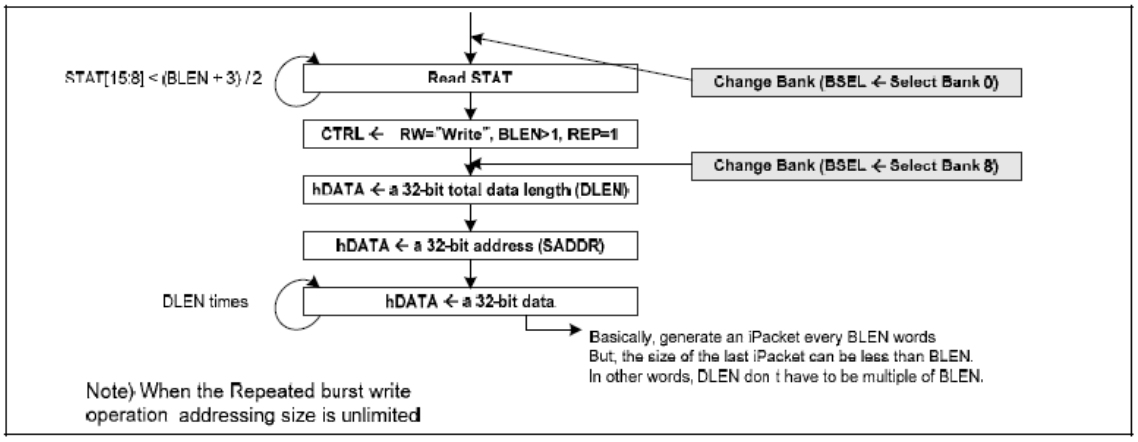

Figure24-8. Repeated Burst Write Procedure

24.3.8 MODEM BOOTING

모뎀 부팅은 HOST(Modem)가 리셋을 포함하여 AP(S3C6400) 부팅을 컨트롤하는 것을 의미한다. AP는 외부 부트메모리(낸드)를 요구하지 않는다. 모뎀은 AP 부트 코드를 모뎀의 부트 메모리로부터 스텝핑 스톤 메모리영역(4KB)에 HOST I/F(간접적 모뎀 인터페이스)블럭을 통해 다운로드를 한다. 그리고 나서 AP가 동작하도록 하기 위해 모뎀은 boot done 신호(SYS_CTRL레지스터의 it[0])를 활성화 시킨다.

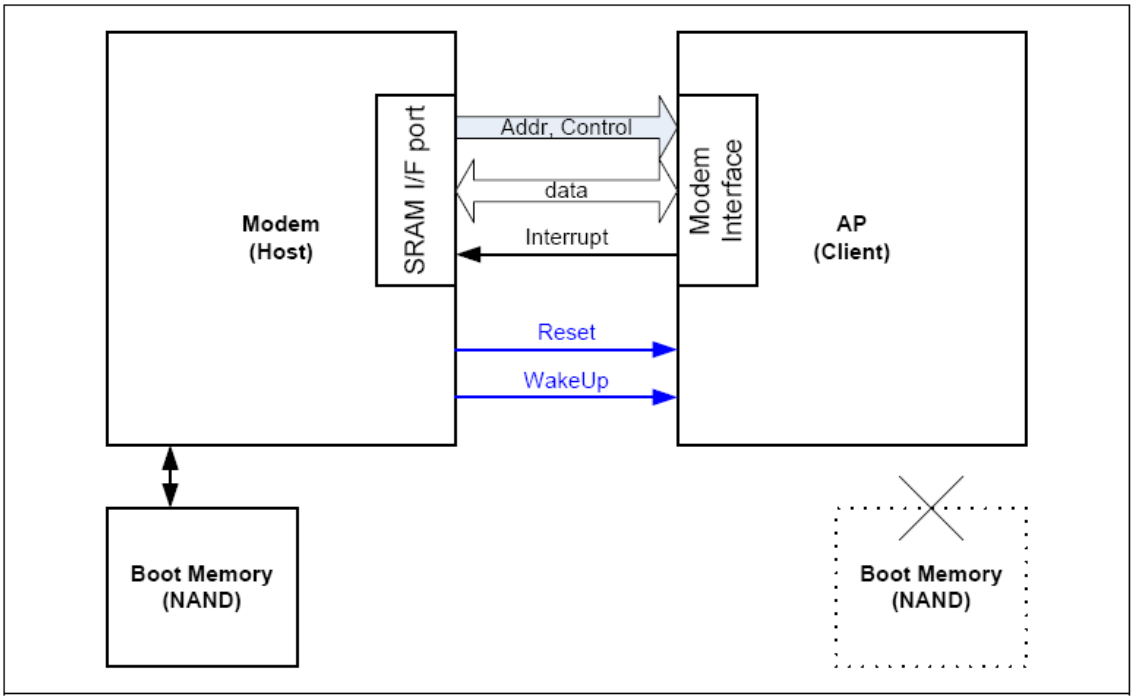

Figure24-9. Modem Boot connection diagram

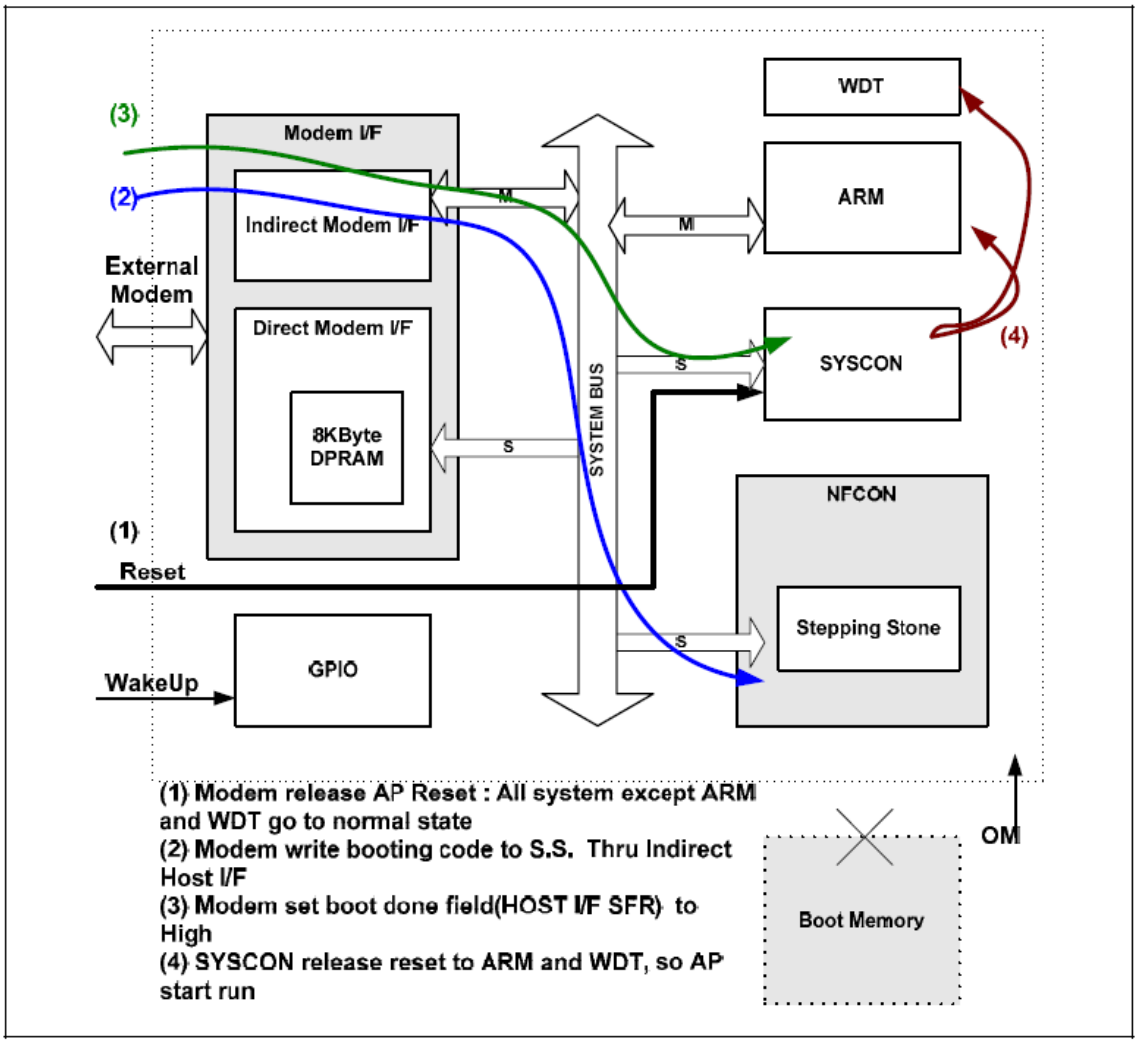

Figure 24-10. Modem Boot procedure

24.3.9 MAILBOX INTERFACE

모뎀은 32비트 in-mailbox, out-mailbox 레지스터를 모뎀과 AP(S3C6400)사이의 IPC(Inter Process Communication)을 위해 사용 할 수 있다.

24.3.10 MAILBOX BASIC OPERATION

모뎀이 32비트 데이터를 in-mailbox에 쓸 때, HOST I/F는 모뎀으로부터 요청을 알기위해 in-mailbox를 읽도록 AP에 인터럽트를 생성한다. in-mailbox의 포맷은 응용에 의해서 자유롭게 정의 될 수 있다. HOST I/F의 in-mailbox 플래그는 AP가 in-mailbox를 읽을 때 자동으로 클리어 된다.

AP가 32비트 데이터를 out-mailbox에 쓸 때, HOST I/F는 AP로부터 요청을 알기 위해 out-mailbox를 읽도록 모뎀에 인터럽트를 생성한다. out-mailbox의 포맷은 응용에 의해서 자유롭게 정의 될 수 있다. HOST I/F의 out-mailbox 플래그(i.e., STAT1[0])는 모뎀이 out-mailbox를 읽을 때 자동으로 클리어 된다.

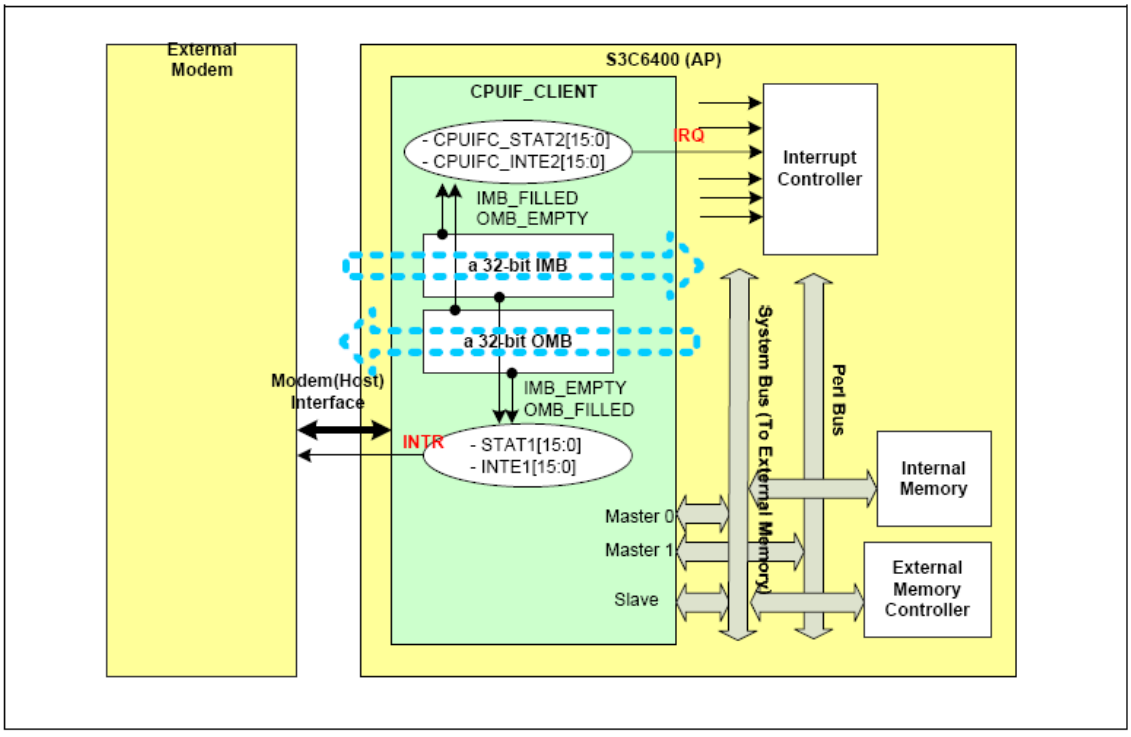

Figure 24-11. In/Out Mailbox between Modem and AP

24.3.11 MAILBOX OPERATION WITH A BULK DATA

32비트 mailbox가 정보를 전송하기에 충분하지 않을 때, AP의 어떠한 메모리를 버퍼로 사용할 수 있다.

예를들어, HOST에서 AP로 많은 양의 데이터를 전송하기 위해 호스트는 먼저 HOST I/F의 버스트 쓰기를 이용하여 데이터를 AP의 메모리에 쓴다. 상태 레지스터(ie,STAT[0]=0)를 확인하므로써 버스트 쓰기가 완료되었는지를 확인한 후에 호스트는 in-mailbox로 메시지를 쓴다.

AP에서 호스트로 많은 양의 데이터를 전송하기위해서 AP는 먼저 그것의 메모리에 데이터를 준비하고 out-mailbox로 SFR 접근을 이용하여 메시지를 쓴다. 쓰기는 호스트에 인터럽트를 생성할 것이다.

Table 24-1. Registers for Mailbox Interface

Group	Operation	Registers
Protocol register	Registers for mail-box	IMBL, IMBH, OMBL, OMBH
SFR	Mailbox	HOSTIFC_IMB, HOSTIFC_OMB

24.4 PROGRAMMER'S MODEL

24.4.1 THE REGISTERS OF HOST INTERFACE ARE CLASSIFIED INTO:

1. 모뎀에 의해 16비트 호스트 인터페이스를 통해 접근하는 프로토콜 레지스터, 그리고
2. 버스 마스터에 의해서 시스템 버스를 통해 접근할 수 있는 Special Function Register

프로토콜 레지스터를 이용해서, 모뎀은 다음의 동작을 실행할 수 있다.

1. Single transfer(Host Interface)
2. Burst transfer(Host Interface)
3. Reading of all address areas of the S3C6400X including Special Function Register
4. Writing of all address areas of the S3C6400X including Special Function Register
5. Write a 32-bit message into In-Mailbox
6. Read a 32-bit message into Out-Mailbox

SFR을 사용해서 다음의 동작을 지원한다.

1. Write a 32-bit message into Out-mailbox
2. Read a 32-bit message into In-mailbox

24.5 REGISTER DESCRIPTION(PROTOCOL REGISTERS)

Register	Bank	MP_A[1:0]	R/W	Description	Reset Value
CTRL	0x0	00	R/W	Control Register	0x0000
INTE		01	R/W	Interrupt Enable Register	0x2000
STAT		10	R	Status Register	0x90A2
CTRL1	0x1	00	R/W	Control1 Register	0x0000
INTE1		01	R/W	Interrupt Enable1 Register	0x0000
STAT1		10	R	Status1 Register	0x0002
IMBL	0x2	00	R/W	In-Mail Box Low Register	0x0000
IMBH		01	R/W	In-Mail Box High Register	0x0000
OMBL	0x3	00	R	Out-Mail Box Low Register	0x0000
OMBH		01	R	Out-Mail Box High Register	0x0000
hDATAL	0x8	00	R/W	Host Interface Data Low Register	-
hDATAH		01	R/W	Host Interface Data High Register	-
SYS_CTRL	0xB	00	R/W	System Control Register	0x0000
Reserved		01	R/W	Reserved	0x0005
Reserved		10	R	Reserved	-
BSEL	all banks	11	R/W	Bank Selection Register	0x0000

NOTE: MP_A[1:0] are input pin names "XhiADDR[1:0]", MP means Modem Processor and MP_A means MP Address.

24.5.1 PROTOCOL REGISTER MATRIX

테이블 24-2와 24-3에서, 프로토콜 레지스터는 BSEL[3:0]이 접근 전에 적당히 세팅되어야하는 16개 뱅크들로 분류되어 있다.

Table 24-2. Protocol Register Matrix (Bank0 ~ Bank7)

MP_A[1:0]	Protocol Register (Selected by BSEL[3:0])							
	Bank0 (0000)	Bank1 (0001)	Bank2 (0010)	Bank3 (0011)	Bank4 (0100)	Bank5 (0101)	Bank6 (0110)	Bank7 (0111)
00	CTRL	CTRL1	IMBL	OMBL	Reserved	Reserved	Reserved	Reserved
01	INTE	INTE1	IMBH	OMBH	Reserved	Reserved	Reserved	Reserved
10	STAT	STAT1	reserved	reserved	Reserved	Reserved	Reserved	Reserved
11	BSEL[3:0]							

Table 24-3. Protocol Register Matrix (Bank8 ~ Bank15)

MP_A[1:0]	Protocol Register (Selected by BSEL[3:0])							
	Bank8 (1000)	Bank9 (1001)	Bank10 (1010)	Bank11 (1011)	Bank12 (1100)	Bank13 (1101)	Bank14 (1110)	Bank15 (1111)
00	hDATAL	Reserved	Reserved	SYS_CTRL	Reserved	Reserved	Reserved	Reserved
01	hDATAH	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
10	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
11	BSEL[3:0]							

SFR-mirrored registers: INTE, INTE1, STAT, STAT1, IMBH, IBML, OMBH, OMBL
Mirrored-register means the register can be accessed by both AP and MODEM side.

24.5.2 CONTROL REGISTER(CTRL)

BSEL[3:0] = 0000, MP_A[1:0] = 00, R/W, Reset value = 0x0000

Field	Bit	Description	Initial State
Reserved	[15:13]		00
BLEN[8:0]	[12:4]	Burst length for transfer The basic unit is a 32-bit word. Maximum burst length is 256 words. 0 = No transaction 1 = Single Write or Single Read N = N-word * Note) BLEN must be 0 not to issue a new HOST I/F command.	0_0000_0000
REP_WRITE	[3]	Repeated Burst Write Enable 0 = No 'Repeated Burst Write' 1 = If set, "Burst Write" is treated as "Repeated Burst Write"	0
HOSTIF_RESET	[2]	Reset of the HOST I/F 0 = This bit is used a soft reset signal of the HOST I/F. 1 = Therefore, this bit must be de-asserted by software.	0
Reserved	[1]	This field must be fixed to '0'	0
READ_WRITE	[0]	Read or Write 0 = Write operation, 1 = Read operation	0

24.5.3 INTERRUPT ENABLE REGISTER(INTE)

BSEL[3:0] = 0000, MP_A[1:0] = 01, R/W, Reset Value = 0x2000

Field	Bit	Description	Initial State
WFIFO_THRES	[15:8]	Threshold of the empty elements in WFIFO This value specifies the threshold of the partial emptiness. For example, if WFIFO_THRES is 8, STAT[7] becomes 1 when 16 and more elements in WFIFO are empty.	0x20
WFIFO_PEMPTY	[7]	WFIFO partial empty interrupt enable Interrupt occurs (i.e., INTR becomes 1) when INTE [7] = 1 and STAT [7] = 1.	0
Reserved	[6:2]	-	0
WFIFO	[1]	WFIFO interrupt enable Interrupt occurs when INTE [1] = 1 and STAT [1] = 1.	0
RFIFO	[0]	RFIFO interrupt enable Interrupt occurs when INTE [0] = 1 and STAT [0] = 1.	0

24.5.4 STATUS REGISTER(STAT)

BSEL[3:0] = 0000, MP_A[1:0] = 10, R/W, Reset Value = 0x90A2

Field	Bit	Description	Initial State
WRITABLE_CNT	[15:8]	Writable word counts in wfifo: Read only This field shows how many words can be written into WFIFO without checking of the WFIFO fullness. For example, if this field is 0x08, there are currently 16 (8 x 2) entries of wfifo so that the HOST can write 16 words immediately. Note that the reset value is 0x90 so that 288 words can be written without overflow. Practically, since the packet head and address must be written into WFIFO, the recommend maximum data payload size is 256-word.	0x90
WFIFO_PEMPTY	[7]	WFIFO partial empty flag (from HOST I/F itself) This flag becomes 1 when the number of empty elements in WFIFO is larger than or equal to a threshold (ie, 2 x INTE [15:8]).	1
Reserved	[6:2]	-	0
WFIFO	[1]	WFIFO empty flag. (from HOST I/F itself) This flag becomes 1 when Write Buffer is empty so that the maximum capacity of Write Buffer is available right now. At least a single write into wfifo resets this flag.	1
RFIFO	[0]	RFIFO ready flag (from HOST I/F itself) This flag becomes 1 when Read Buffer is ready to read. The HOST read of DATAH resets this flag.	0

24.5.5 INTERRUPT ENABLE1 REGISTER(INTE1)

BSEL[3:0] = 0001, MP_A[1:0] = 01, R/W, Reset Value = 0x0000

Field	Bit	Description	Initial State
Reserved	[15:2]		0
IMB_EMPTY	[1]	IMB empty interrupt enable Interrupt occurs when INTE1 [1] = 1 and STAT1 [1] = 1.	0
OMB_FILLED	[0]	OMB filled interrupt enable Interrupt occurs when INTE1 [0] = 1 and STAT1 [0] = 1.	0

24.5.6 STATUS1 REGISTER(STAT1)

BSEL[3:0] = 0001, MP_A[1:0] = 10, R/W, Reset Value = 0x0002

Field	Bit	Description	Initial State
Reserved	[15:2]		0
IMB_EMPTY	[1]	IMB (In-Mail Box) empty flag This flag is an inversion of the IMB_FILLED (ie, HOSTIFC_STAT2[17]).	1
OMB_FILLED	[0]	OMB (Out-Mail Box) filled flag This flag is set when the out-mailbox is written by SFR access. In order to clear this flag, HIGH value must be written in this bit.	0

24.5.7 IN-MAIL BOX LOW REGISTER(IMBL)

BSEL[3:0] = 0010, MP_A[1:0] = 00, R/W, Reset Value = 0x0000

Field	Bit	Description	Initial State
IMBL	[15:0]	Lower 16 bits of In-Mail Box register HOST writes a 16-bit data into IMBL.	0x0000

24.5.8 IN-MAIL BOX HIGH REGISTER(IMBH)

BSEL[3:0] = 0010, MP_A[1:0] = 01, R/W, Reset Value = 0x0000

Field	Bit	Description	Initial State
IMBH	[15:0]	Upper 16 bits of In-Mail Box register After HOST writes a 16-bit data into IMBH, HOST I/F asserts 'IMB_flag' (an internal signal) in order to notify that a 32-bit IMB contains a new value. IMB_flag is automatically cleared when IMB is read by software.	0x0000

24.5.9 OUT-MAIL BOX LOW REGISTER(OMBL)

BSEL[3:0] = 0011, MP_A[1:0] = 00, R/W, Reset Value = 0x0000

Field	Bit	Description	Initial State
OMBL	[15:0]	Lower 16-bit of Out-Mail Box register HOST reads a lower 16-bit data of a 32-bit OMB.	0x0000

24.5.10 OUT-MAIL BOX HIGH REGISTER(OMBH)

BSEL[3:0] = 0011, MP_A[1:0] = 01, R/W, Reset Value = 0x0000

Field	Bit	Description	Initial State
OMBH	[15:0]	Upper 16 bits of Out-Mail Box register When the host reads an upper 16-bit data of a 32-bit OMB, STAT1[0] (ie, OMB flag) is automatically cleared.	0x0000

24.5.11 HOST INTERFACE DATA LOW REGISTER(HDATAL)

BSEL[3:0] = 1000, MP_A[1:0] = 00, R/W, Reset Value = (undefined)

Field	Bit	Description	Initial State
DATAL	[15:0]	Data Register	-

24.5.12 HOST INTERFACE DATA HIGH REGISTER(HDATAH)

BSEL[3:0] = 1000, MP_A[1:0] = 01, R/W, Reset Value = (undefined)

Field	Bit	Description	Initial State
DATAH	[15:0]	Data Register	-

24.5.13 SYSTEM CONTROL REGISTER(SYS_CTRL)

BSEL[3:0] = 1011, MP_A[1:0] = 00, R/W, Reset Value = 0x0000

Field	Bit	Description	Initial State
Reserved	[15:1]	Data Register	0
BOOTDONE	[0]	Boot Done for Modem Booting. When this bit is set to High, boot done signal is asserted to System Controller. S3C6400X(AP) boot operation starts. Host (Modem) must clear this bit to Low after Modem boot.	0

24.5.14 BANK SELECTION REGISTER(BSEL)

MP_A[1:0] = 11, R/W, Reset Value = 0x0000

Field	Bit	Description	Initial State
Reserved	[15:4]		0x000
BSEL	[3:0]	Bank selection 0000 = One of the protocol registers in Bank0 will be selected. 0001 = One of the protocol registers in Bank1 will be selected. … 1111 = One of the protocol registers in Bank15 will be selected.	0000

24.6 REGISTER DESCRIPTIONS(SPECIAL FUNCTION REGISTERS)

Base address : 0x7400_0000				
Register	**Offset**	**R/W**	**Description**	**Reset Value**
HOSTIFC_CTRL	0x000	R/W	HOST I/F Control Register	0x20FF_0100
Reserved	0x004	R/W	Reserved	0x0000_0006
HOSTIFC_TMP	0x008	R/W	HOST I/F Temporary Register	0x0000_0000
Reserved	0x00C	--	Reserved	0x0000_0000
HOSTIFC_IMB	0x010	R	HOST I/F IMB Register	0x0000_0000
HOSTIFC_OMB	0x014	R/W	HOST I/F OMB Register	0x0000_0000
HOSTIFC_MR_STAT	0x020	R	HOST I/F Status Mirrored Register	0x0000_90A2
HOSTIFC_MR_STAT1	0x024	R	HOST I/F Status1 Mirrored Register	0x0000_0002
HOSTIFC_STAT2	0x028	R/W	HOST I/F Status2 Register	0x0001_0000
Reserved	0x02C	--	Reserved	0x0000_0000
HOSTIFC_MR_INTE	0x030	R/W	HOST I/F Interrupt Enable Mirrored Register	0x0000_2000
HOSTIFC_MR_INTE1	0x034	R	HOST I/F Interrupt Enable1 Mirrored Register	0x0000_0000
HOSTIFC_INTE2	0x038	RW	HOST I/F Interrupt Enable2 Register	0x0000_0000
Reserved	0x03C	--	Reserved	0x0000_0000

24.6.1 HOST I/F CONTROL REGISTER(HOSTIFC_CTRL)

Register	address	R/W	Description	Reset Value
HOSTIFC_CTRL	0x74000000	R/W	HOST I/F Control Register	0x20FF0100

HOSTIFC_CTRL	Bit	Description	Initial State
Reserved	[31:30]	-	0
INV_INTR	[29]	Polarity inversion of INTR 0: INTR is active high so that INTR becomes HIGH when an interrupt occurs. 1: INTR is active low so that INTR becomes LOW when an interrupt occurs. **Note:** "INV_INTR" field of the HOST I/F block and "INT2M_LEVEL" of the MODEM I/F block must have same polarity.	1
Reserved	[28:24]	-	0x0
Reserved	[23:16]	-	0xFF
Reserved	[15:9]	-	0x0
Reserved	[8:0]	-	0x100

24.6.2 HOST I/F TEMPORARY REGISTER(HOSTIFC_TMP)

Register	address	R/W	Description	Reset Value
HOSTIFC_ TMP	0x74000008	R/W	HOST I/F Temporary Register	0x00000000

HOSTIFC_ TMP	Bit	Description	Initial State
DATA	[31:0]	Temporary register This register can be used for the design revision or the verification.	0x0000_0000

24.6.3 HOST I/F IMB REGISTER(HOSTIFC_IMB)

Register	address	R/W	Description	Reset Value
HOSTIFC_IMB	0x74000010	R	HOST I/F IMB Register	0x00000000

HOSTIFC_IMB	Bit	Description	Initial State
IMB	[31:0]	A 32-bit In-MailBox Shadow register	0x0000_0000

24.6.4 HOST I/F OMB REGISTER(HOSTIFC_OMB)

Register	Address	R/W	Description	Reset Value
HOSTIFC_OMB	0x74000014	R/W	HOST I/F OMB Register	0x00000000

HOSTIFC_OMB	Bit	Description	Initial State
OMB	[31:0]	A 32-bit Out-MailBox register	0x0000_0000

24.6.5 HOST I/F STATUS MIRRORED REGISTER(HOSTIFC_MR_STAT)

Register	Address	R/W	Description	Reset Value
HOSTIFC_MR_STAT	0x74000020	R	HOST I/F Status Mirrored Register	0x000090A2

HOSTIFC_MR_STAT	Bit	Description	Initial State
Reserved	[31:16]	-	0x0000
STAT	[15:0]	Mirrored Protocol Register of STAT[15:0]	0x90A2

24.6.6 HOST I/F STATUS1 MIRRORED REGISTER(HOSTIFC_MR_STAT1)

Register	Address	R/W	Description	Reset Value
HOSTIFC_MR_STAT1	0x74000024	R	HOST I/F Status1 Mirrored Register	0x00000002

HOSTIFC_MR_STAT1	Bit	Description	Initial State
Reserved	[31:16]	-	0x0000
STAT1	[15:0]	Mirrored Protocol Register of STAT1[15:0]	0x0002

24.6.7 HOST I/F STATUS2 REGISTER(HOSTIFC_STAT2)

Register	Address	R/W	Description	Reset Value
HOSTIFC_STAT2	0x74000028	R/W	HOST I/F Status2 Register	0x00010000

HOSTIFC_STAT2	Bit	Description	Initial State
Reserved	[31:20]	-	0x000
Reserved	[19]	-	0
RBURST_DONE	[18]	Repeated burst write done flag This flag is set when the repeated burst write is done. In order to clear the flag, write HIGH value.	0
IMB_FILLED	[17]	IMB (In-Mail Box) filled flag This flag is set when the in-mailbox is written by the modem. In order to clear this flag, HIGH value should be written in this bit.	0
OMB_EMPTY	[16]	OMB (Out-Mail Box) empty flag This flag is an inversion of the OMB_FILLED (ie, STAT1[0]).	1
Reserved	[15:8]	Reserved	0x00
RX_FIFO_OVER_RUN	[7]	The over-run flag of Local RX FIFO(L_RFIFO) in the HOST I/F	0
RX_FIFO_UNDER_RUN	[6]	The under-run flag of Local RX FIFO(L_RFIFO) in the HOST I/F	0
TX_FIFO_OVER_RUN	[5]	The over-run flag of TX FIFO(WFIFO) in the HOST I/F	0
TX_FIFO_UNDER_RUN	[4]	The under-run flag of TX FIFO(WFIFO) in the HOST I/F	0
Reserved	[3]	-	0
Reserved	[2]	-	0
Reserved	[1]	-	0
Reserved	[0]	-	0

24.6.8 HOST I/F INTERRUPT ENABLE MIRRORED REGISTER(HOSTIFC_MR_INTE)

Register	Address	R/W	Description	Reset Value
HOSTIFC_MR_INTE	0x74000030	R	HOST I/F Interrupt Enable Mirrored Register	0x00002000

HOSTIFC_MR_INTE	Bit	Description	Initial State
Reserved	[31:16]		0x0000
INTE	[15:0]	Mirrored Protocol Register of INTE[15:0]	0x2000

24.6.9 HOST I/F INTERRUPT ENABLE1 MIRRORED REGISTER(HOSTIFC_MR_INTE1)

Register	Address	R/W	Description	Reset Value
HOSTIFC_MR_INTE1	0x74000034	R	HOST I/F Interrupt Enable1 Mirrored Register	0x00000000

HOSTIFC_MR_INTE1	Bit	Description	Initial State
Reserved	[31:16]		0x0000
INTE1	[15:0]	Mirrored Protocol Register of INTE1[15:0]	0x0000

24.6.10 HOST I/F INTERRUPT ENABLE2 REGISTER(HOSTIFC_INTE2)

Register	Address	R/W	Description	Reset Value
HOSTIFC_INTE2	0x74000038	R/W	HOST I/F Interrupt Enable2 Register	0x00000000

HOSTIFC_INTE2	Bit	Description	Initial State
Reserved	[31:16]		0x0000
INTE2	[15:0]	Each bit is an interrupt enable control bit of the corresponding bit of HOSTIF_STAT2	0x0000

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