제24장 전기적인 특성

개요

절대적인 최대 값

표 24-1. 절대적인 최대 값

Parameter	Symbol	Rating		Unit
DC Supply Voltage	V_{DDi}	1.8V V_{DD}	2.7	V
	V_{DDIO}	3.3V V_{DD}	3.8	
DC Input Voltage	V_{IN}	3.3V Input buffer	3.8	
		3.3V Interface / 5V Tolerant input buffer	6.5	
DC Output Voltage	V_{OUT}	3.3V Output buffer	3.8	
DC Input (Latch-up) Current	I_{IN}	± 200		mA
Storage Temperature	T_{STG}	– 65 to 150		°C

추천하는 동작 조건

표 24-2. 추천하는 동작 조건

Parameter	Symbol	Rating		Unit
DC Supply Voltage for Internal	V_{DDi}	1.8V V_{DD}	1.8 ± 0.15	V
DC Supply Voltage for I/O Block	V_{DDIO}	3.3V V_{DD}	3.3 ± 0.3	
DC Supply Voltage for Analog Core	V_{DD}	3.3V V_{DD}	3.3 ± 5%	
DC Input Voltage	V_{IN}	3.3V Input buffer	3.3 ± 0.3	
		3.3V Interface / 5V Tolerant input buffer	3.0 – 5.25	
DC Output Voltage	V_{OUT}	3.3V Output buffer	3.3 ± 0.3	
Operating Temperature	T_{OPR}	Commercial	0 to 70	°C

D.C. 전기 특성

표 24-3과 24-4는 표준의 LVCMOS I/O 버퍼 용 DC 전기 특성을 규정하고 있다.

표 24-3. Normal I/O 패드 DC 전기 특성

(V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70 °C)

Symbol	Parameters	Condition	Min	Type	Max	Unit
V_{IH}	High level input voltage					
	LVCMOS interface		2.0			V
V_{IL}	Low level input voltage					
	LVCMOS interface				0.8	V
VT	Switching threshold			1.4		V
VT+	Schmitt trigger, positive-going threshold	CMOS			2.0	V
VT-	Schmitt trigger, negative-going threshold	CMOS	0.8			V
I_{IH}	High level input current					
	Input buffer	$V_{IN} = V_{DD}$	-10		10	μA
I_{IL}	Low level input current					
	Input buffer	$V_{IN} = V_{SS}$	-10		10	μA
	Input buffer with pull-up		-60	-33	-10	
V_{OH}	High level output voltage					
	Type B6	I_{OH}= - 6 mA	2.4			V
	Type B8	I_{OH}= - 8 mA				
	Type B12	I_{OH} = -12 mA				
V_{OL}	Low level output voltage					
	Type B6	I_{OL} = 6 mA			0.4	V
	Type B8	I_{OL} = 8 mA				
	Type B12	I_{OL} = 12 mA				

주의할 점:

1. Type B6은 6mA의 출력 드라이버 셀을 의미한다.
2. Type B8은 8mA의 출력 드라이버 셀을 의미한다.
3. Type B12은 12mA의 출력 드라이버 셀을 의미한다.

표 24-4. USB DC 전기 특성

Symbol	Parameter	Condition	Min	Max	Unit
V_{IH}	High level input voltage		2.5		V
V_{IL}	Low level input voltage			0.8	V
I_{IH}	High level input current	Vin = 3.3V	-10	10	μA
I_{IL}	Low level input current	Vin = 0.0V	-10	10	μA
V_{OH}	Static Output High	15KΩ to GND	2.8	3.6	V
V_{OL}	Static Output Low	1.5KΩ to 3.6V		0.3	V

표 24-5. S3C2410X 파워 서플라이 전압과 전류

Parameter	Value	Unit	Condition
Typical V_{DDi} / V_{DDIO}	1.8 / 3.3	V	
Max. Operating frequency (FCLK)	203	MHz	
Max. Operating frequency (HCLK)	101.5	MHz	
Max. Operating frequency (PCLK)	50.7	MHz	
Typical normal mode power NOTE(3) (Total V_{DDi} + V_{DDIO})	297	mW	NOTE(1)
Typical normal mode power NOTE(3) (Total V_{DDi} + V_{DDIO})	224	mW	NOTE(2)
Typical idle mode power NOTE(3) (Total V_{DDi} + V_{DDIO})	122	mW	FCLK = 203MHz (F:H:P = 1:2:4)
Typical slow mode power NOTE(3) (Total V_{DDi} + V_{DDIO})	33	mW	FCLK = 12MHz (F:H:P = 1:1:1)
Maximum Power_OFF mode power Typical Power_OFF mode power NOTE(3)	80 8	uA uA	@1.95V/3.6V, Room temperature All other I/O static.
Maximum RTC power Typical RTC power NOTE(3)	63 3	uA uA	@1.95V/3.6V, Room temperature X-tal = 32.768KHz for RTC

주의할 점:

1. I/O 캐쉬:ON, MMU:ON, SRAM 코드, FCLK:HCLK:PCLK=203MHz:101.5MHz:50.7MHz :LCD ON(320X240X16bppX60Hz, 컬러 TFT):타이머 내부 모드(5채널 구동) :오디오(IIS&DMA, CDCLK=16.9MHz, LRCK=44.1KHz):내부 데이터 quick sort(65536 EA)
2. WinCE 3.0 MPEG 플래이
3. Room 온도 특성

표 24-6. CLKCON 레지스터에 의해서 감소되는 전류(FCLK@202.8MHz)

(Unit: mA)

Peripherals	NFC	LCD	USBH	USBD	Timer	SDI	UART	RTC	ADC	IIC	IIS	SPI	Total
Current	2.9	5.8	0.4	2.9	0.5	1.9	3.6	0.4	0.4	0.6	0.5	0.5	20.4

주의할 점: 이 표는 각 주변장치의 전력소비를 나타내고 있다. 예로, IIS를 사용하지 않고 CLKCON 레지스터에서 IIS 블록을 턴-오프 하면 0.5mA의 소비를 줄일 수 있다.

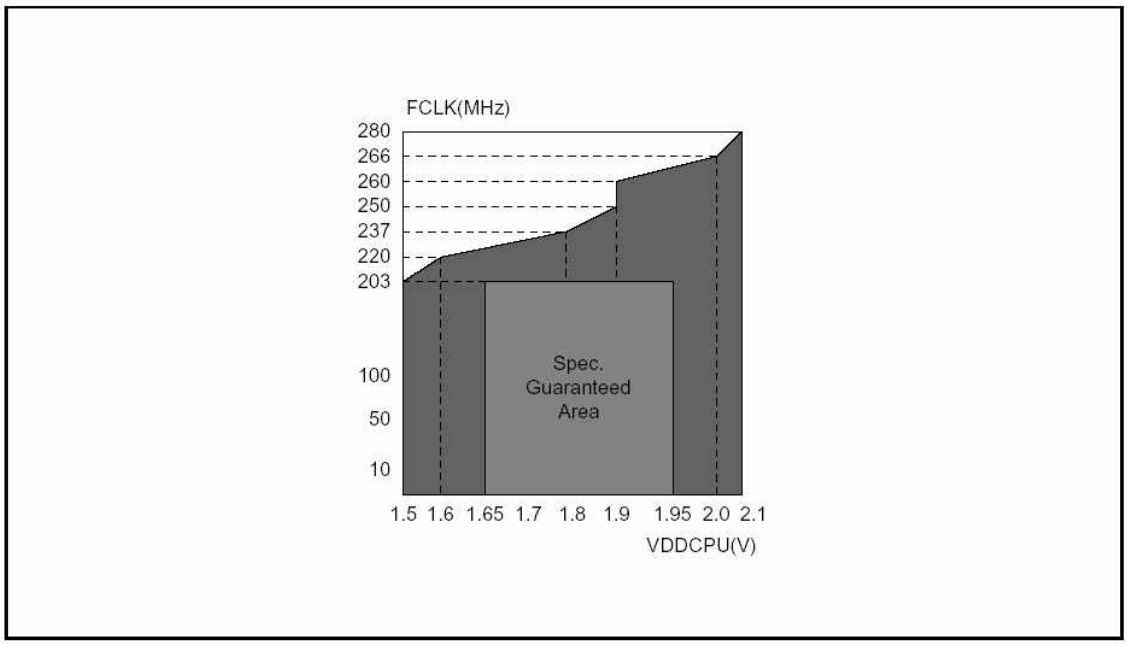

그림 24-1. 일반적인 전압/주파수 범위
(VDDIO=3.3V, @실내 온도 & SMDK2410 보드)

A.C. 전기적인 특성

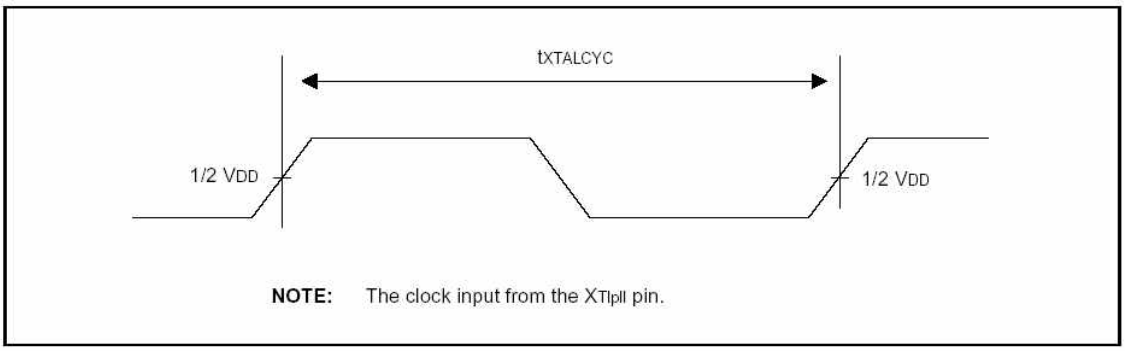

그림 24-2. XTIpll 클럭 타이밍

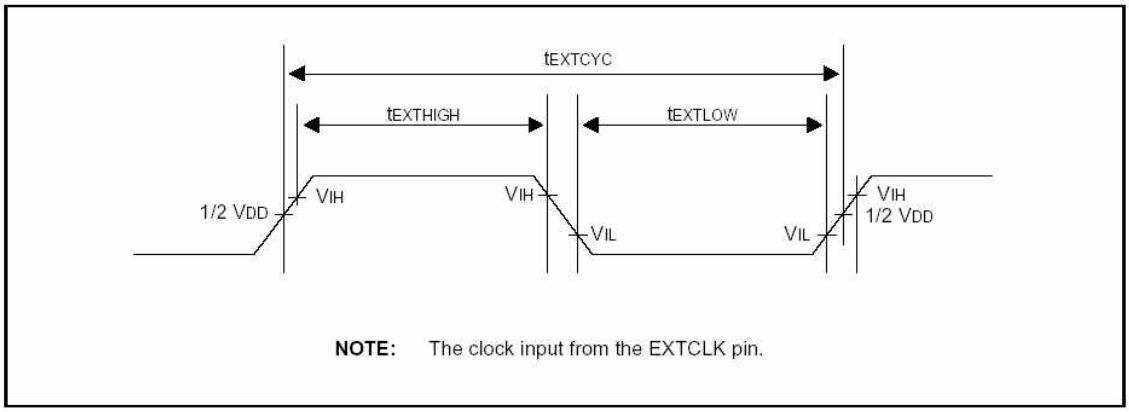

그림 24-3. EXTCLK 클럭 입력 타이밍

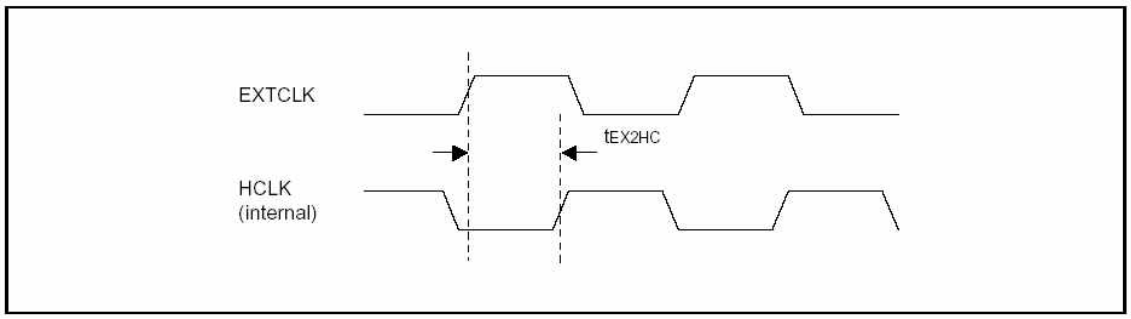

그림 24-4. EXTCLK가 PLL 없이 사용되는 경우의 EXTCLK/HCLK

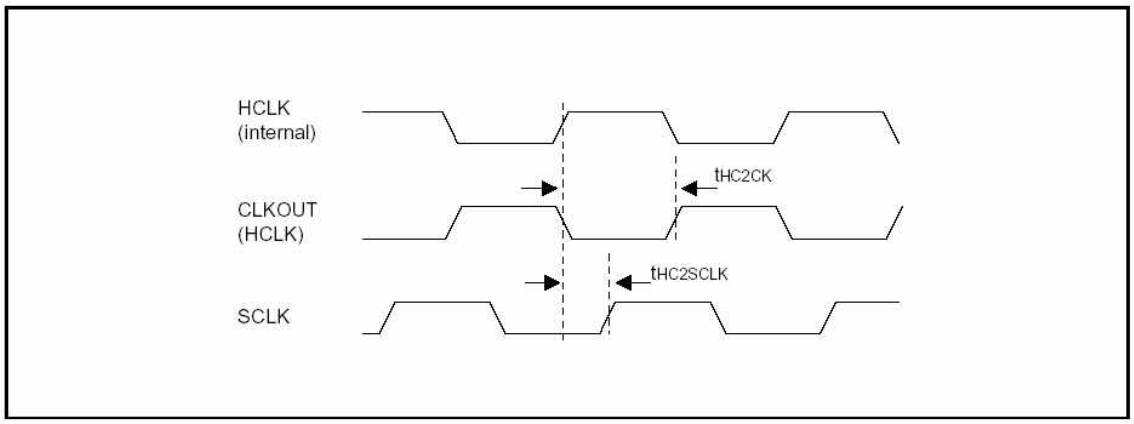

그림 24-5. EXTCLK가 사용되는 경우의 HCLK/CLKOUT/SCLK

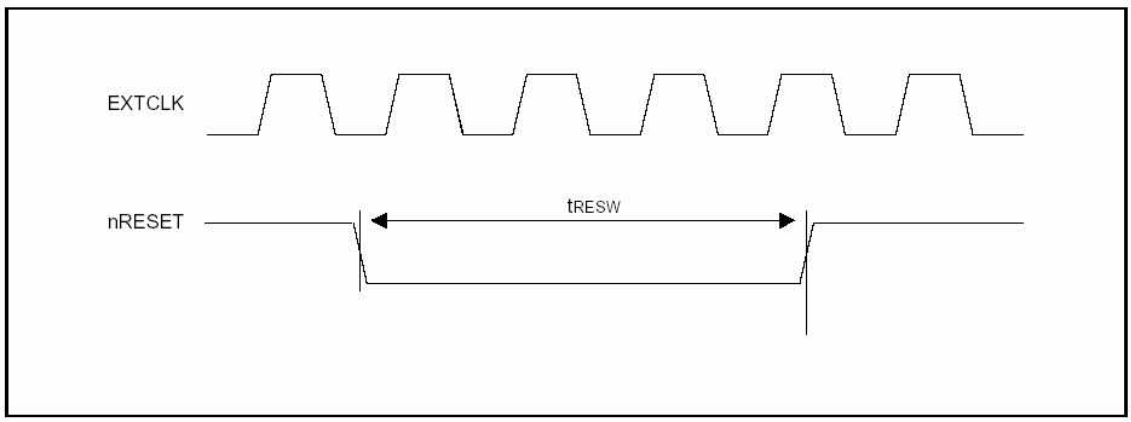

그림 24-6. 매뉴얼 리셋 입력 타이밍

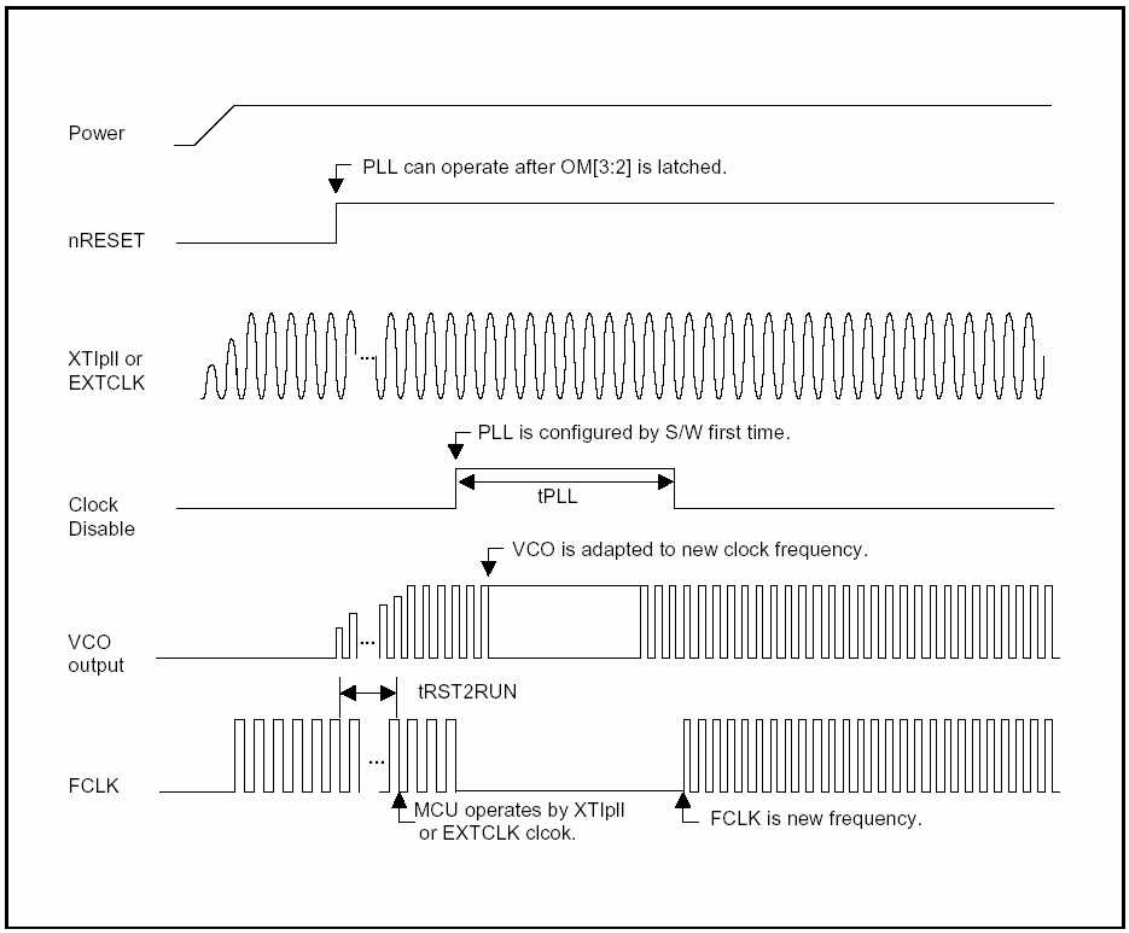

그림 24-7. 파워-온 오실레이션 셋팅 타이밍

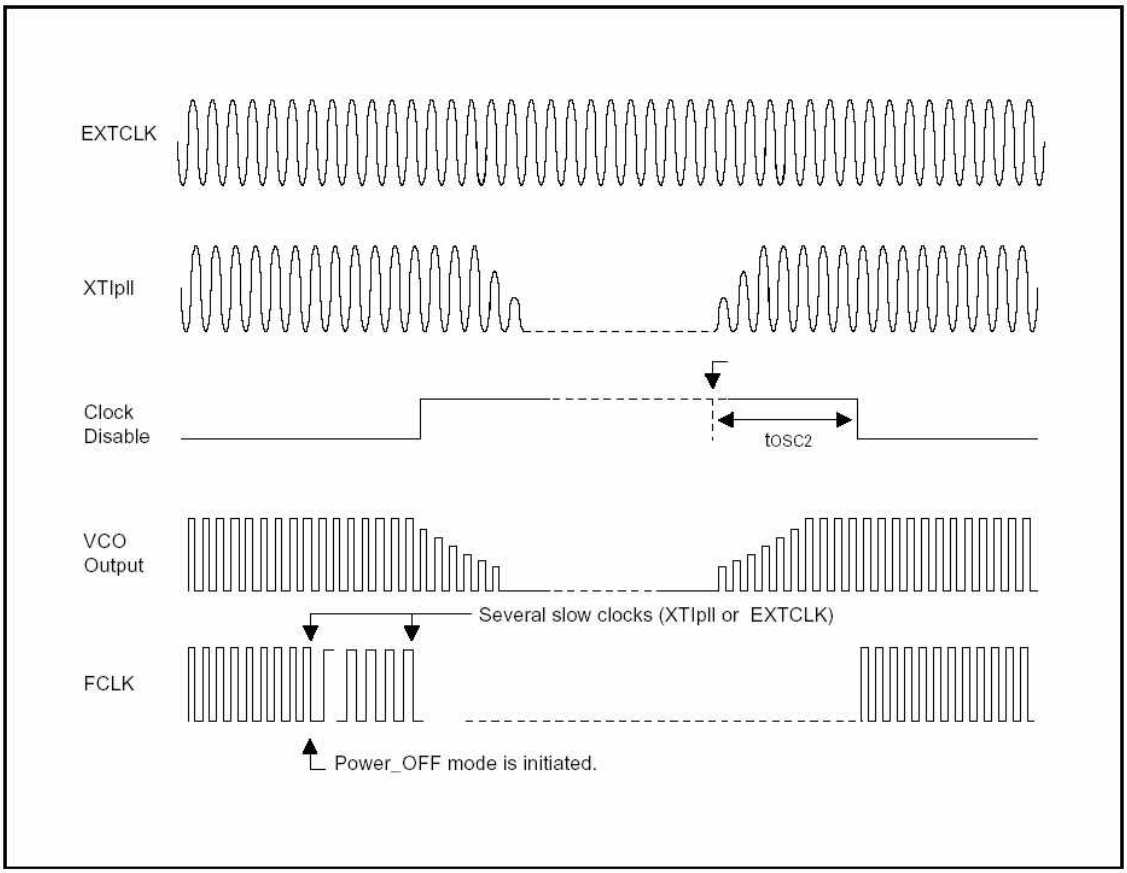

그림 24-8. 오실레이션 셋팅 타이밍을 반환하는 파워-오프 모드

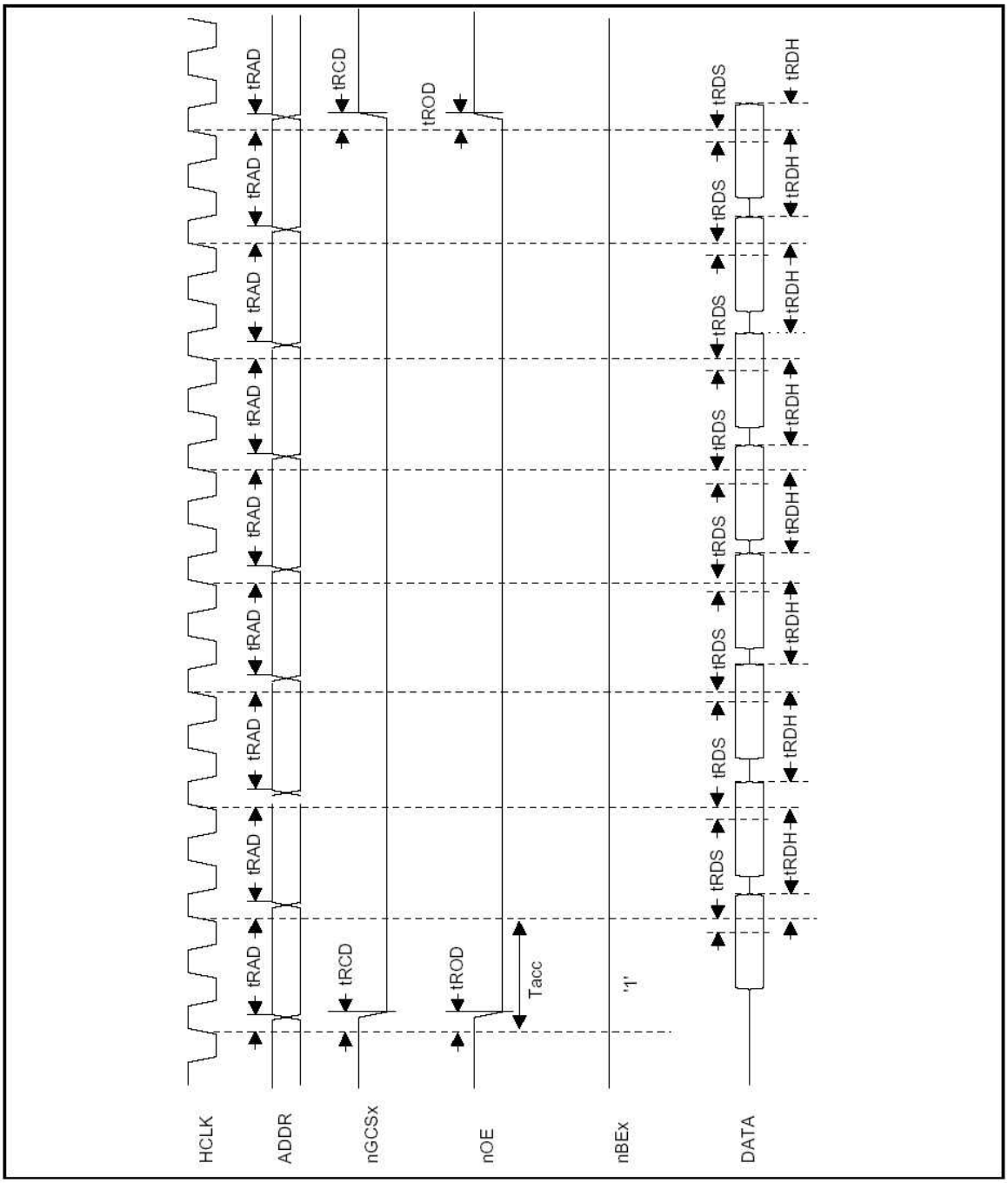

그림 24-9. ROM/SRAM Burst 읽기 타이밍(I)

(Tacs=0, Tcos=0, Tacc=2, Toch=0, Tcah=0, PMC=0, DW=16비트)

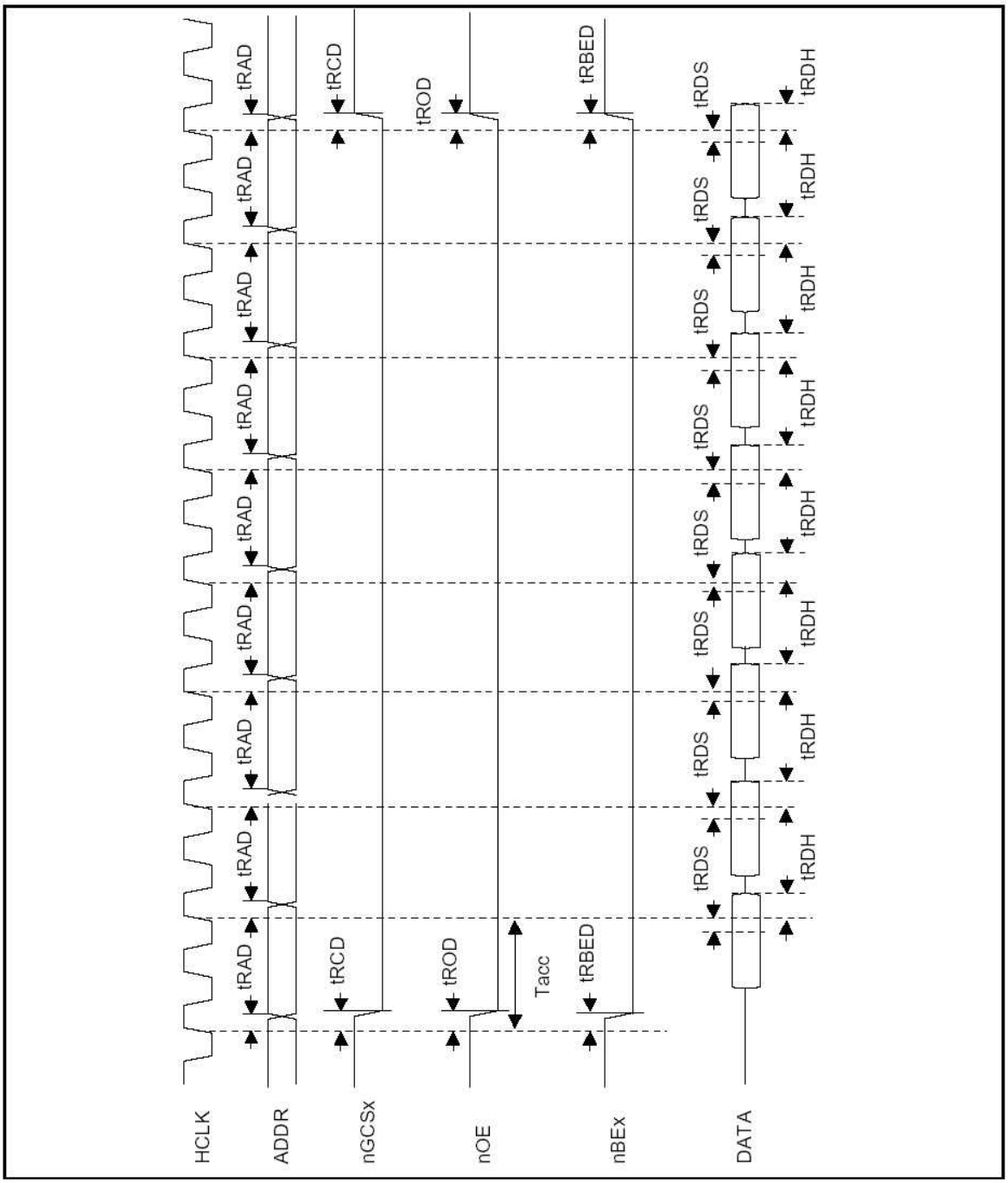

그림 24-10. ROM/SRAM Burst 읽기 타이밍(II)
(Tacs=0, Tcos=0, Tacc=2, Toch=0, Tcah=0, PMC=0, ST=1, DW=16비트)

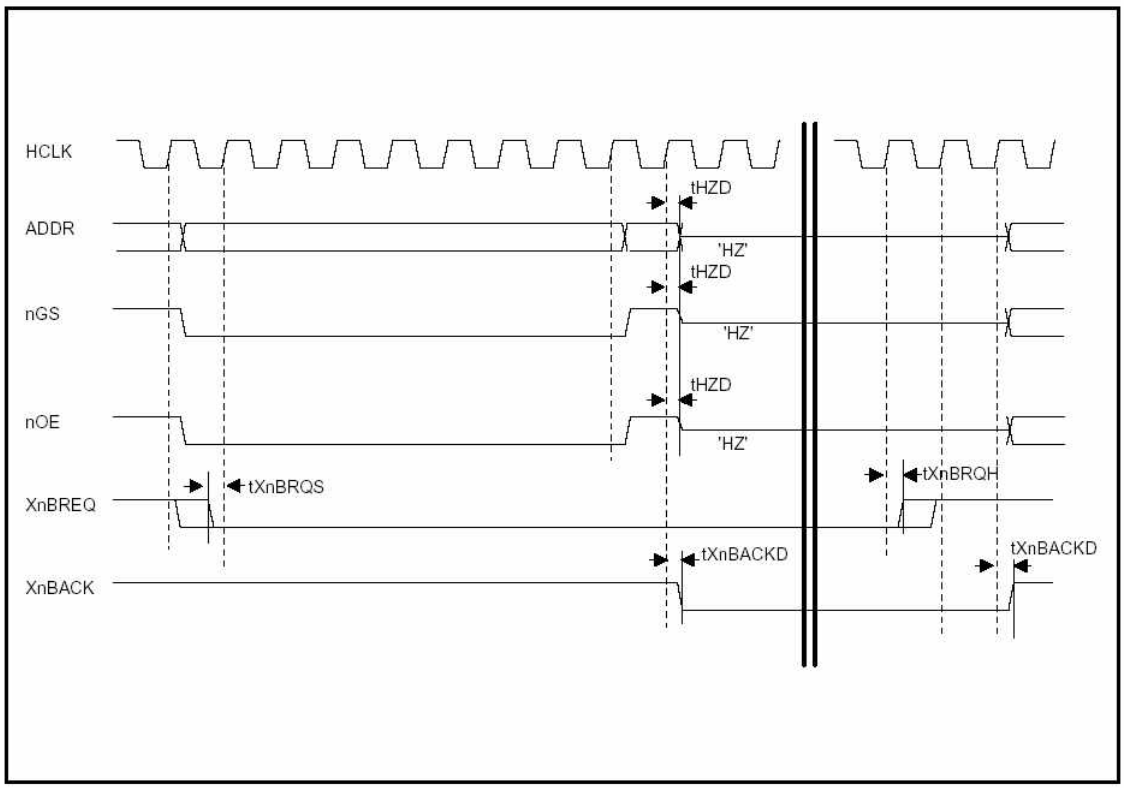

그림 24-11. ROM/SRAM 사이클의 외부 버스 요청
(Tacs=0, Tcos=0, Tacc=8, Toch=0, Tcah=0, PMC=0, ST=0)

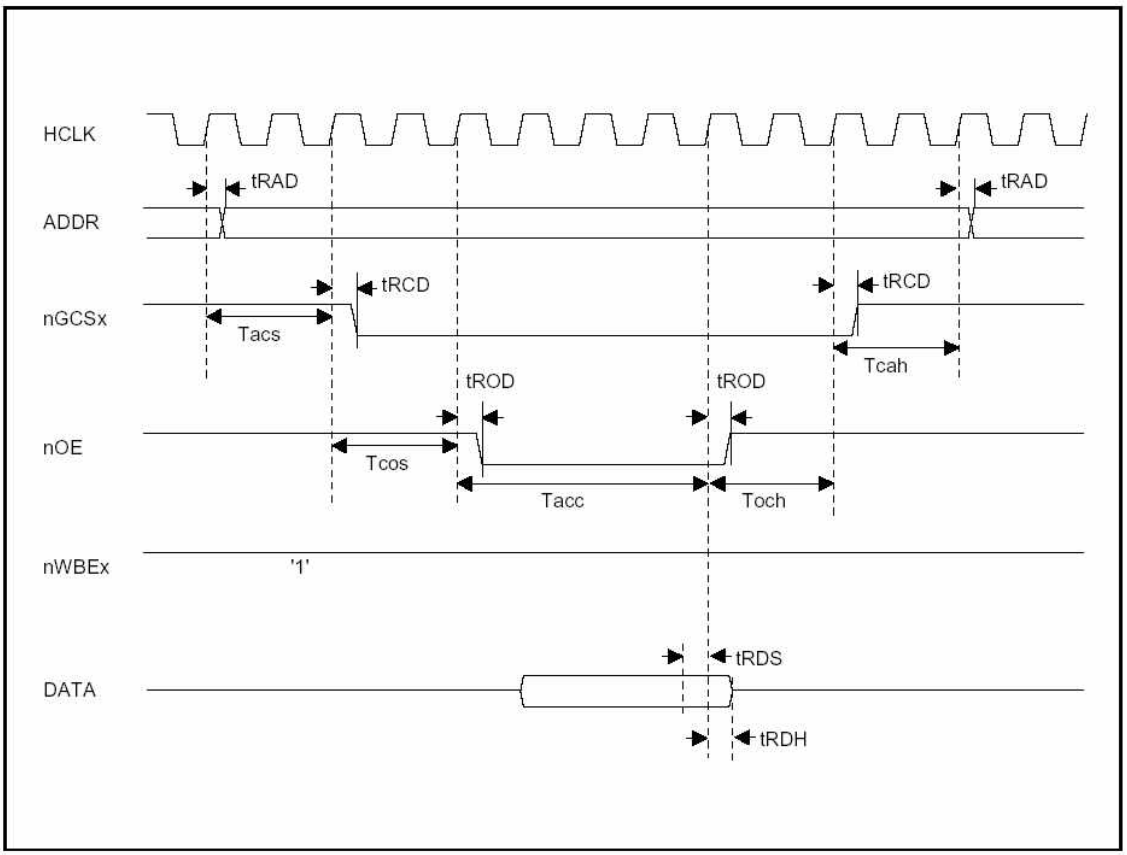

그림 24-12. ROM/SRAM 읽기 타이밍(I)
(Tacs=2, Tcos=2, Tacc=4, Toch=2, Tcah=2, PMC=0, ST=0)

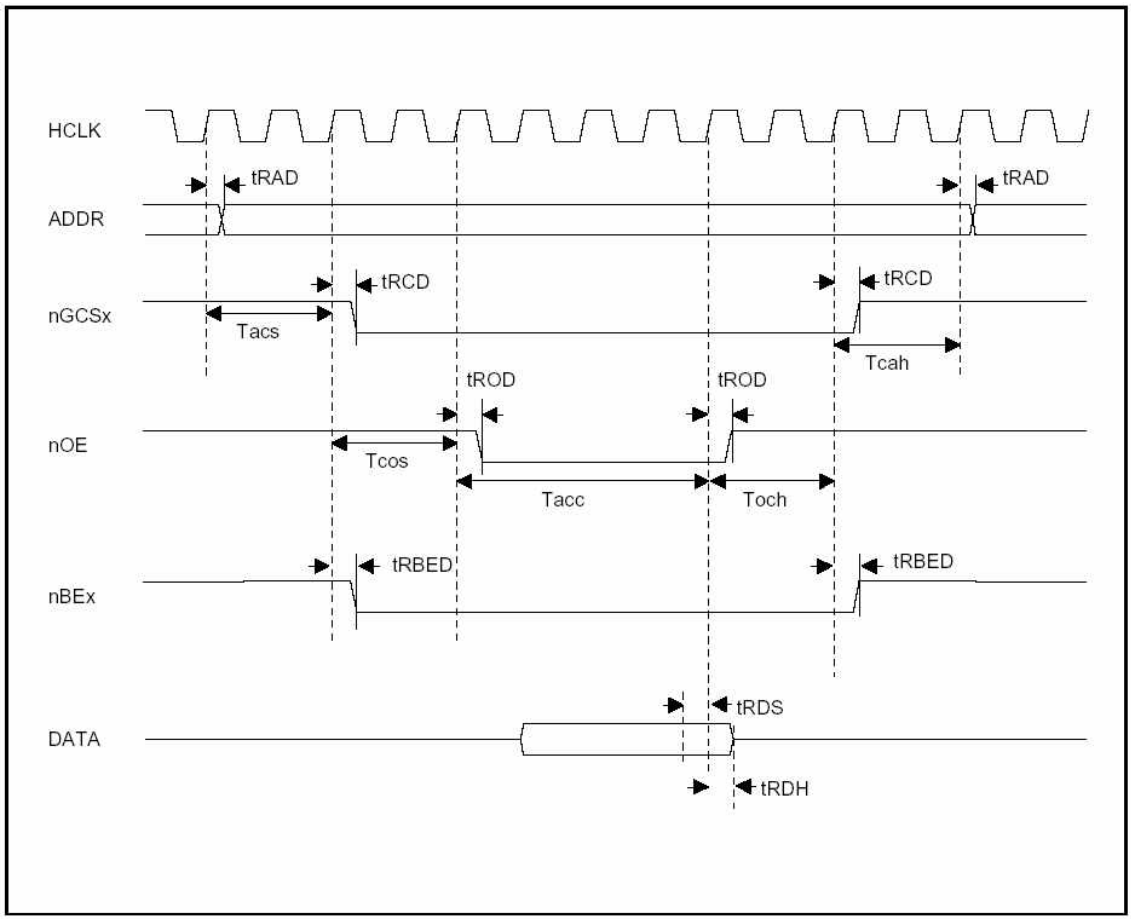

그림 24-13. ROM/SRAM 읽기 타이밍(II)

(Tacs=2, Tcos=2, Tacc=4, Toch=2, Tcah=2사이클, PMC=0, ST=1)

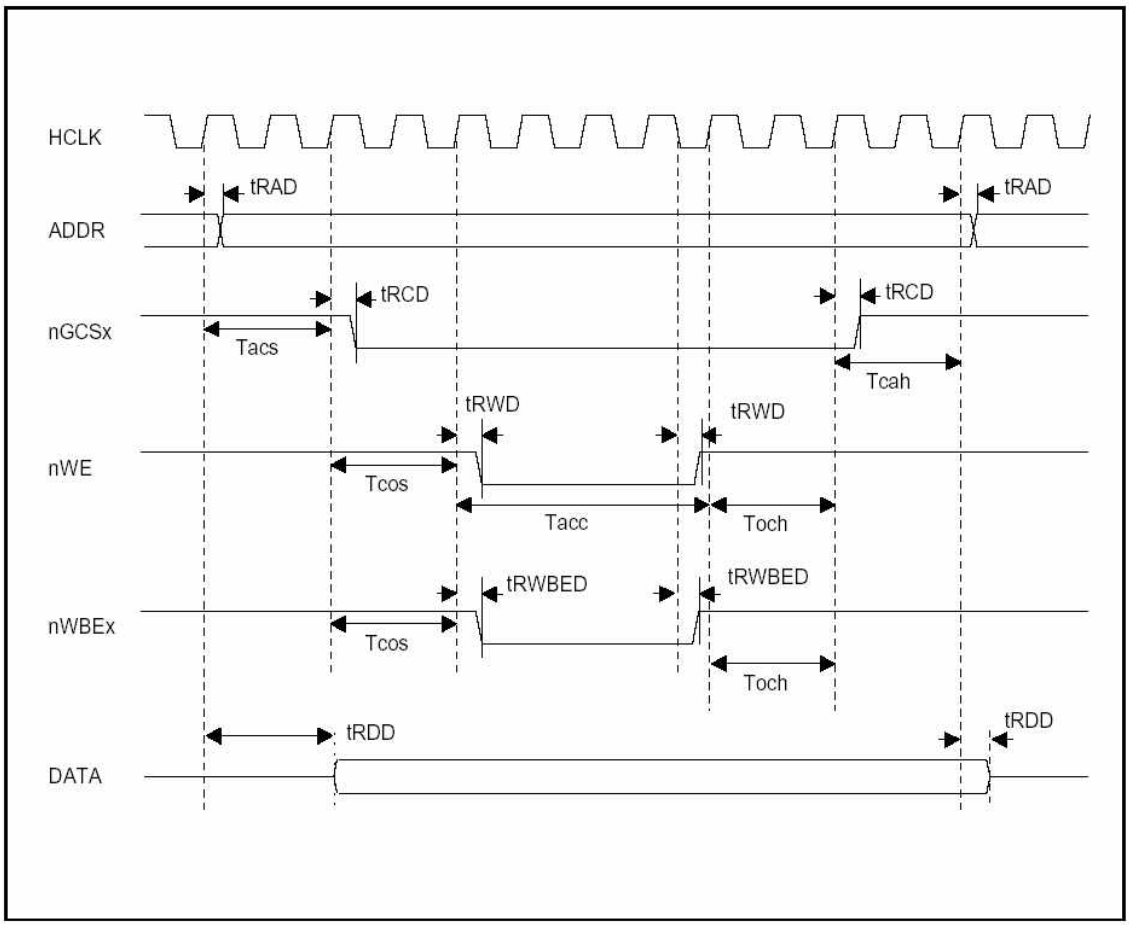

그림 24-14. ROM/SRAM 쓰기 타이밍(I)

(Tacs=2, Tcos=2, Tacc=4, Toch=2, Tcah=2, PMC=0, ST=0)

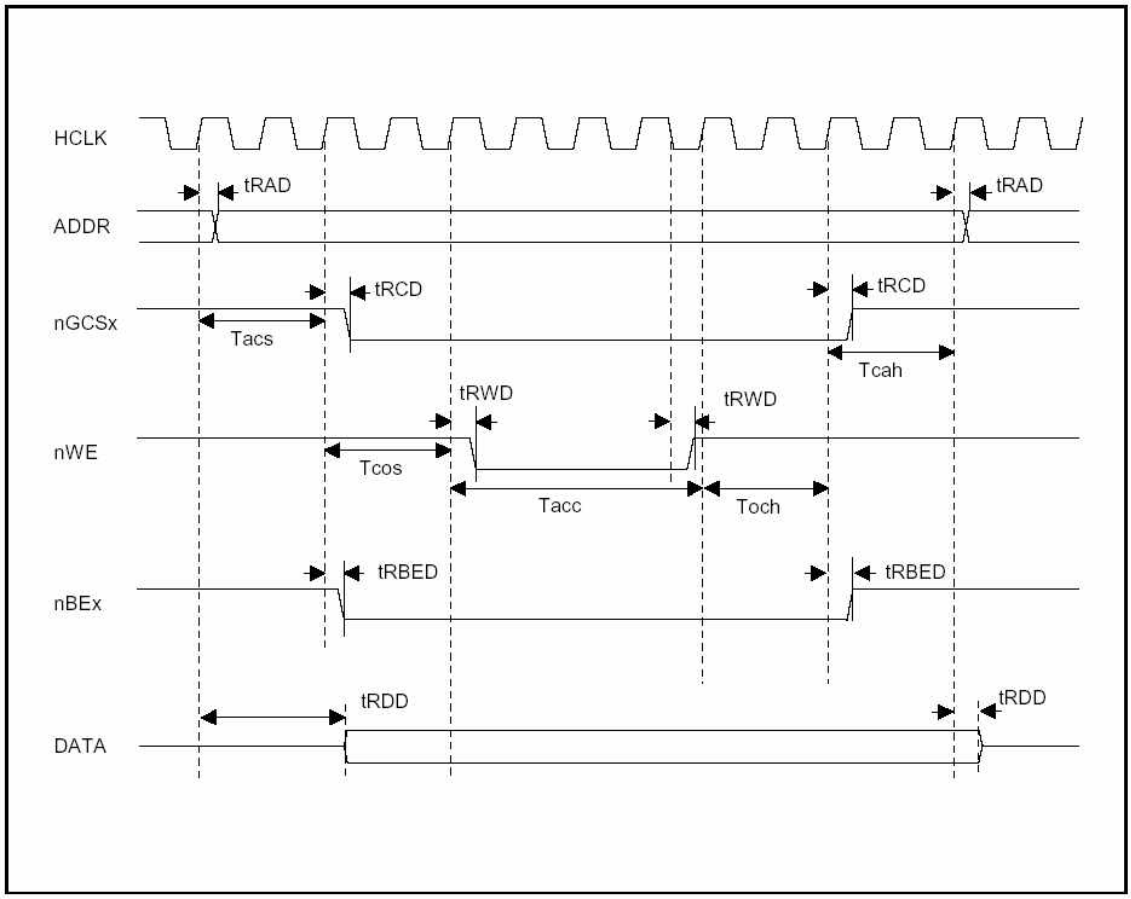

그림 24-15. ROM/SRAM 쓰기 타이밍(II)

(Tacs=2, Tcos=2, Tacc=4, Toch=2, Tcah=2, PMC=0, ST=1)

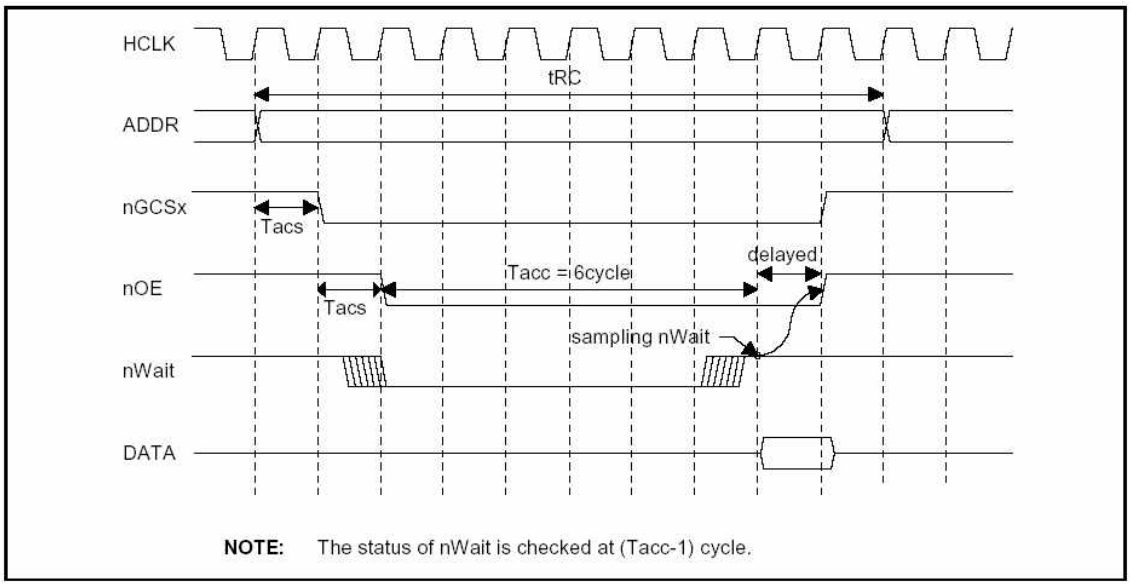

그림 24-16. 외부 nWAIT 읽기 타이밍

(Tacs=0, Tcos=0, Tacc=6, Toch=0, Tcah-0, PMC=0, ST=0)

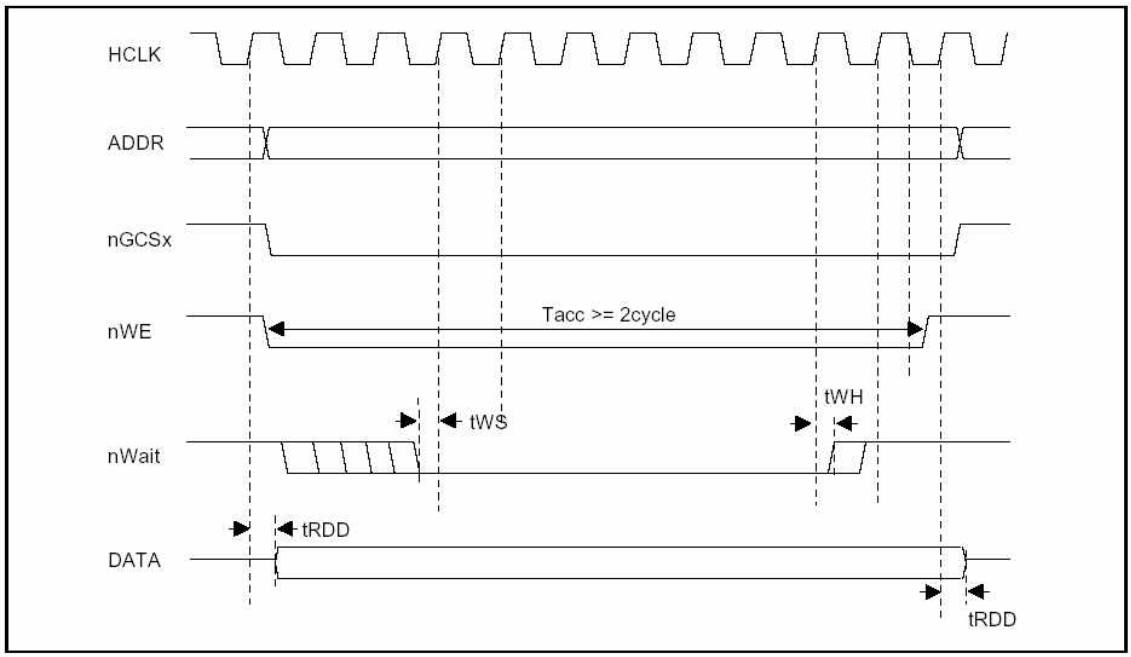

그림 24-17. 외부 nWAIT 쓰기 타이밍
(Tacs=0, Tcos-0, Tacc=4, Toch=0, Tcah=0, PMC=0, ST=0)

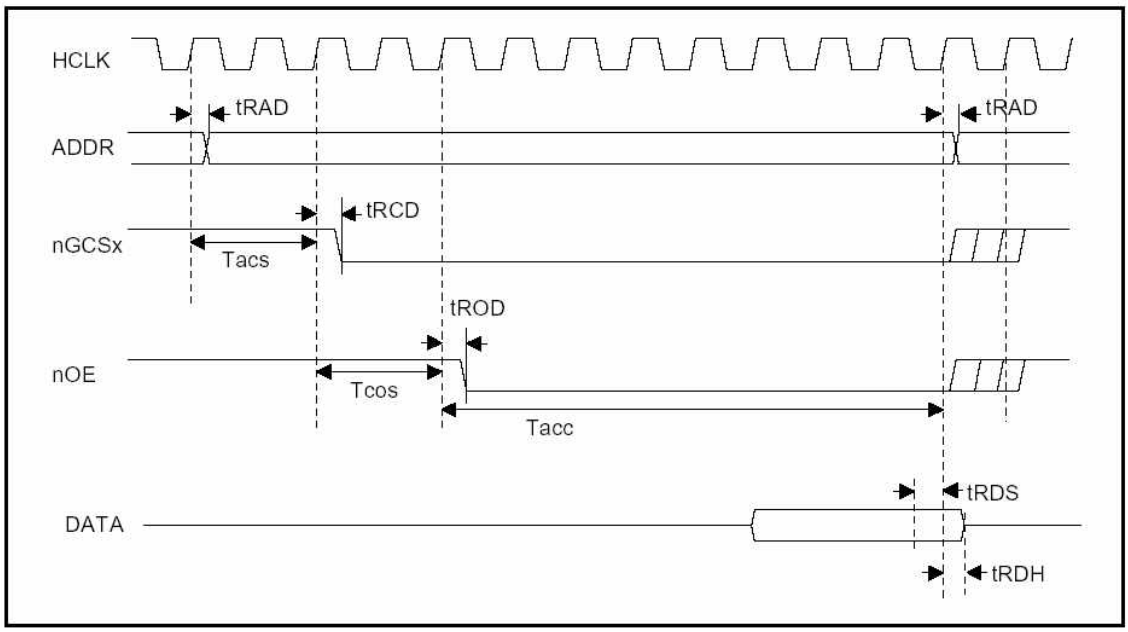

그림 24-18. 마스크 롬 single 읽기 타이밍
(Tacs=2, Tcos=2, Tacc=8, PMC=01/10/11)

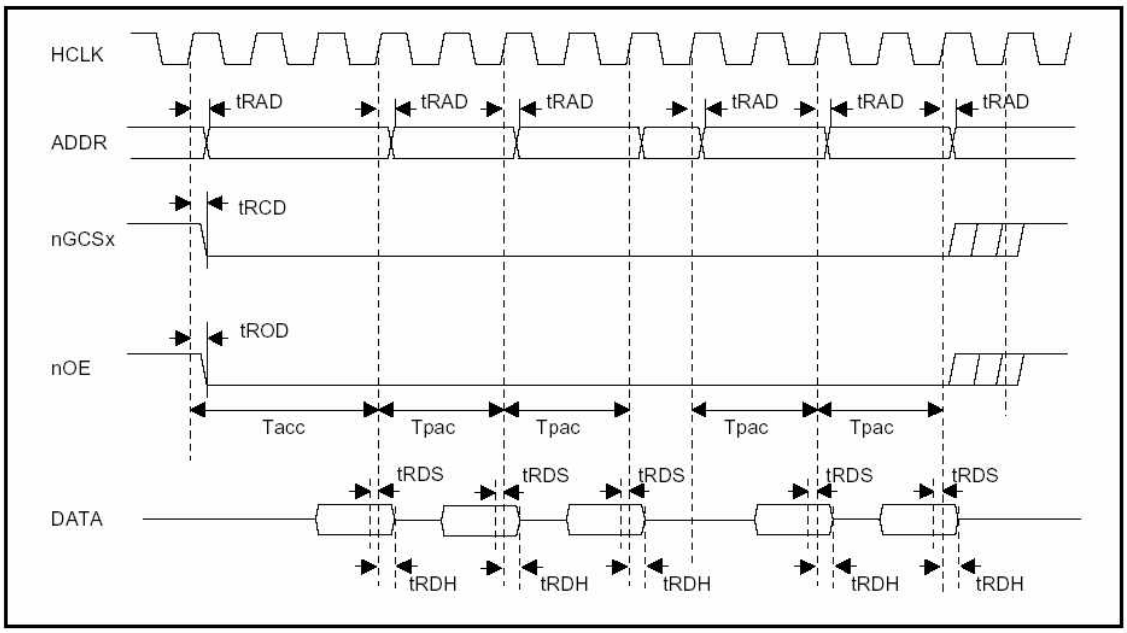

그림 24-19. 마스크 롬 consecutive 읽기 타이밍
(Tacs=0, Tcos=0, Tacc=3, Tpac=2, PMC=01/10/11)

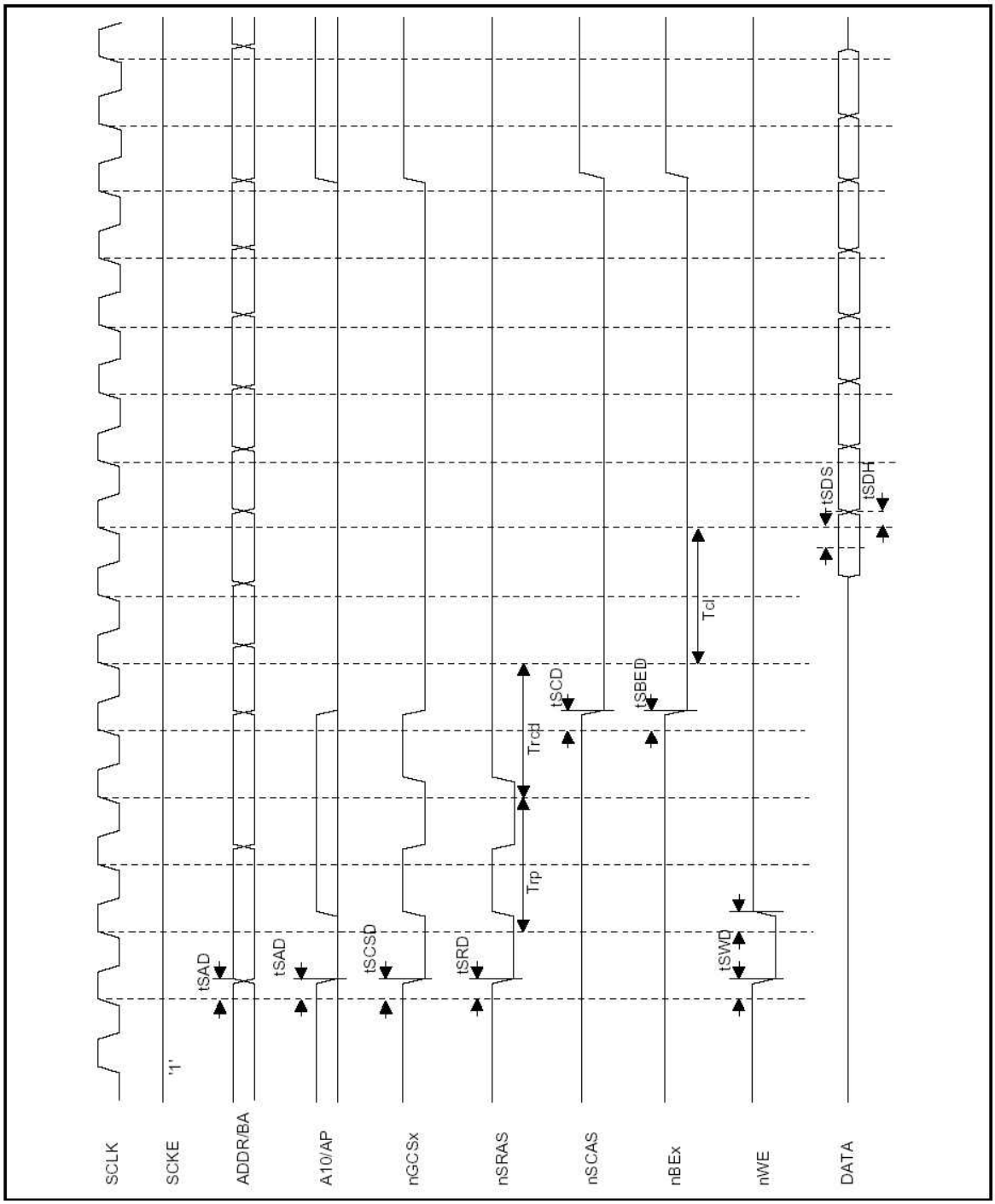

그림 24-20. SDRAM single burst 읽기 타이밍(Trp=2, Trcd=2, Tcl=2, DW=16비트)

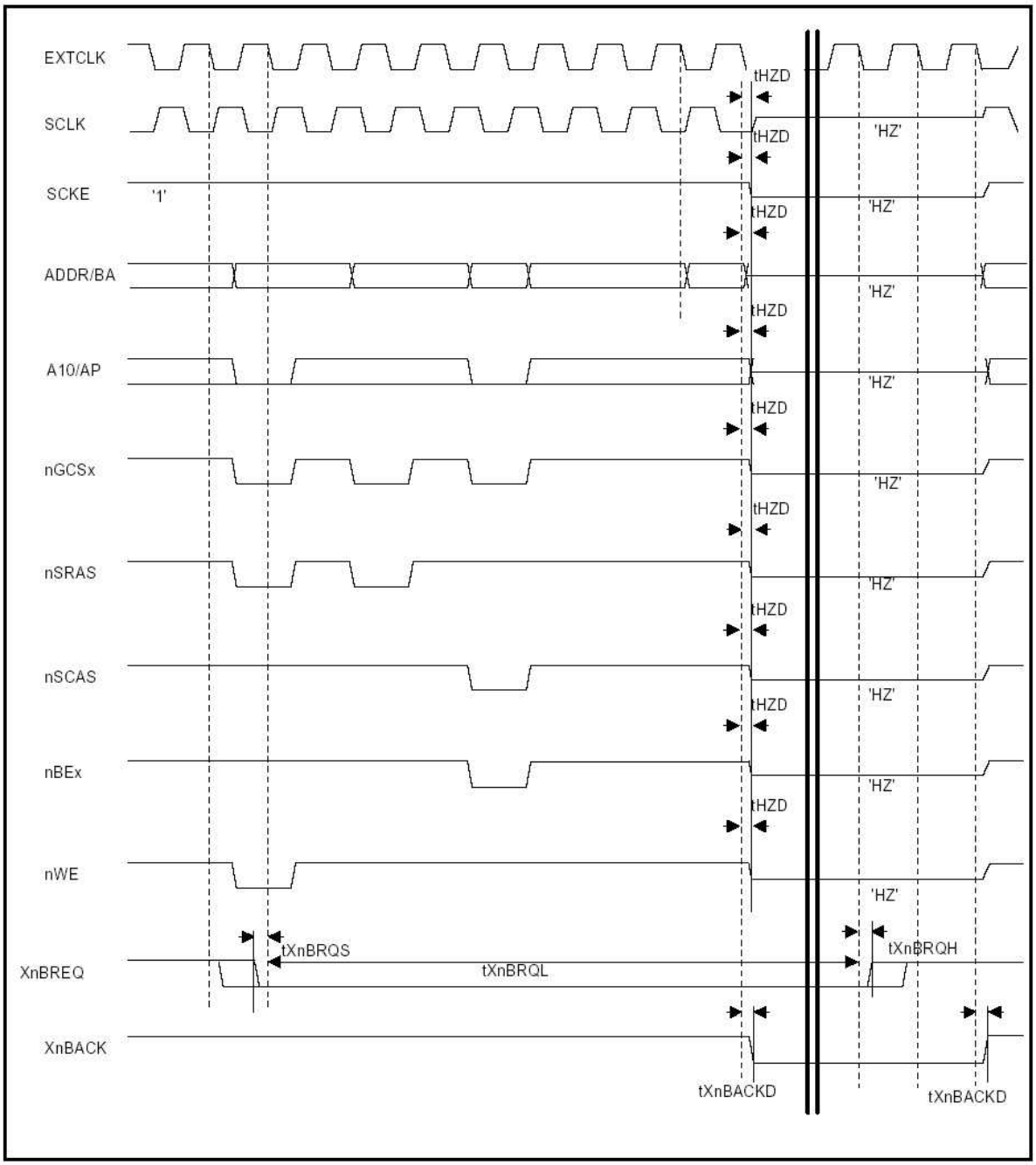

그림 24-21. SDRAM의 외부 버스 요청 타이밍(Trp=2, Trcd=2, Tcl=2)

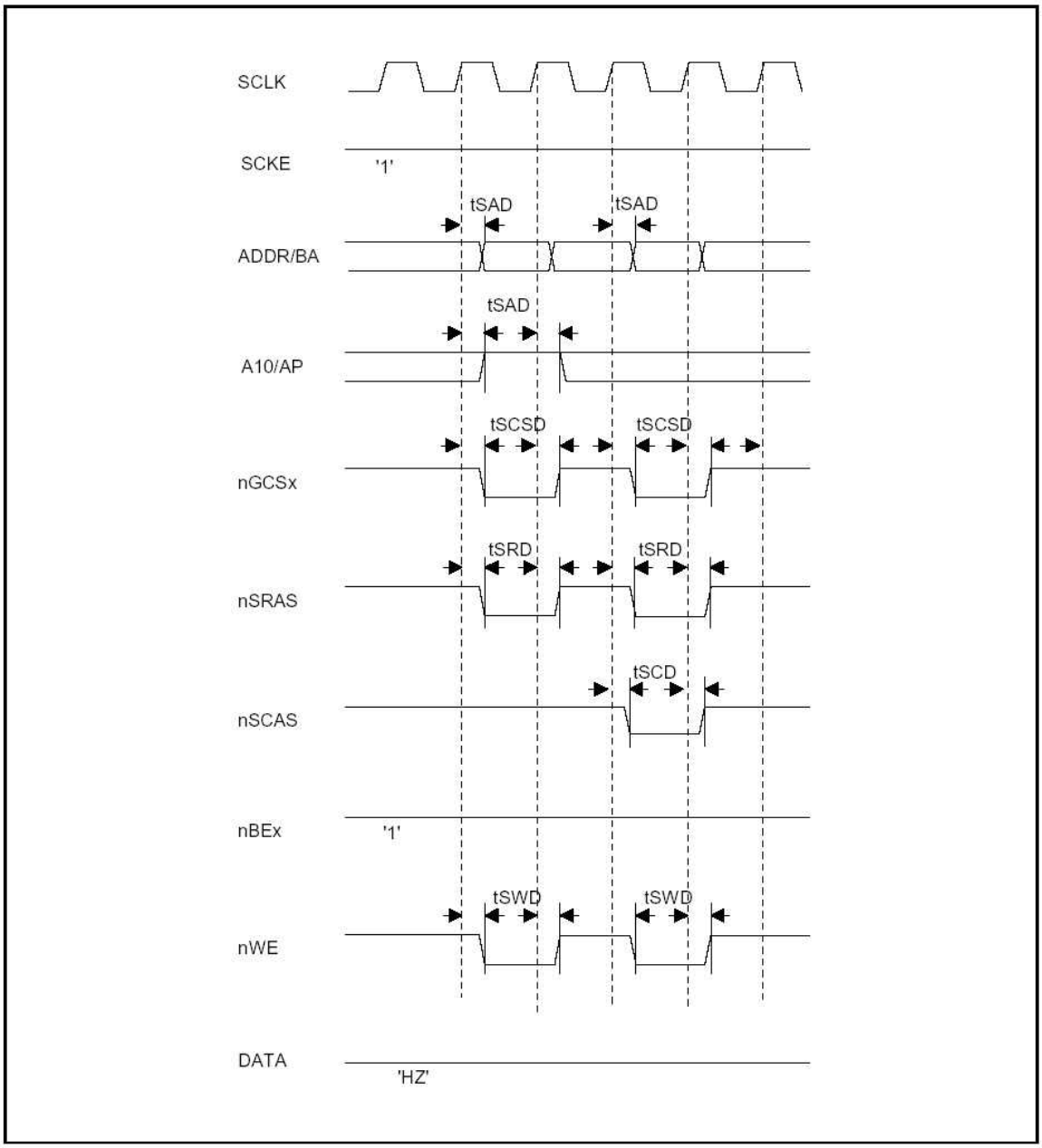

그림 24-22. SDRAM MRS 타이밍

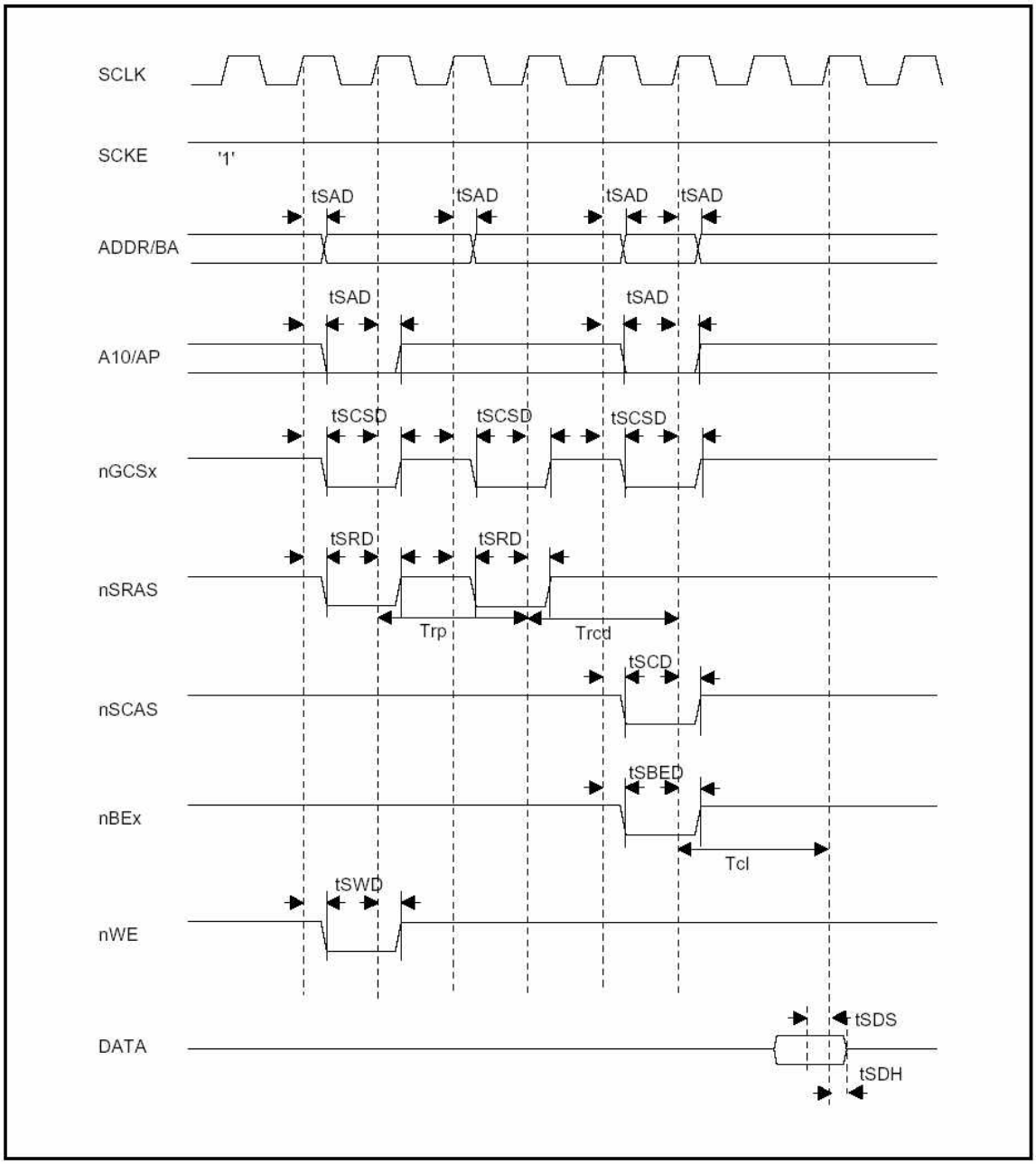

그림 24-23. SDRAM single 읽기 타이밍(I)
(Trp=2, Trcd=2, Tcl=2)

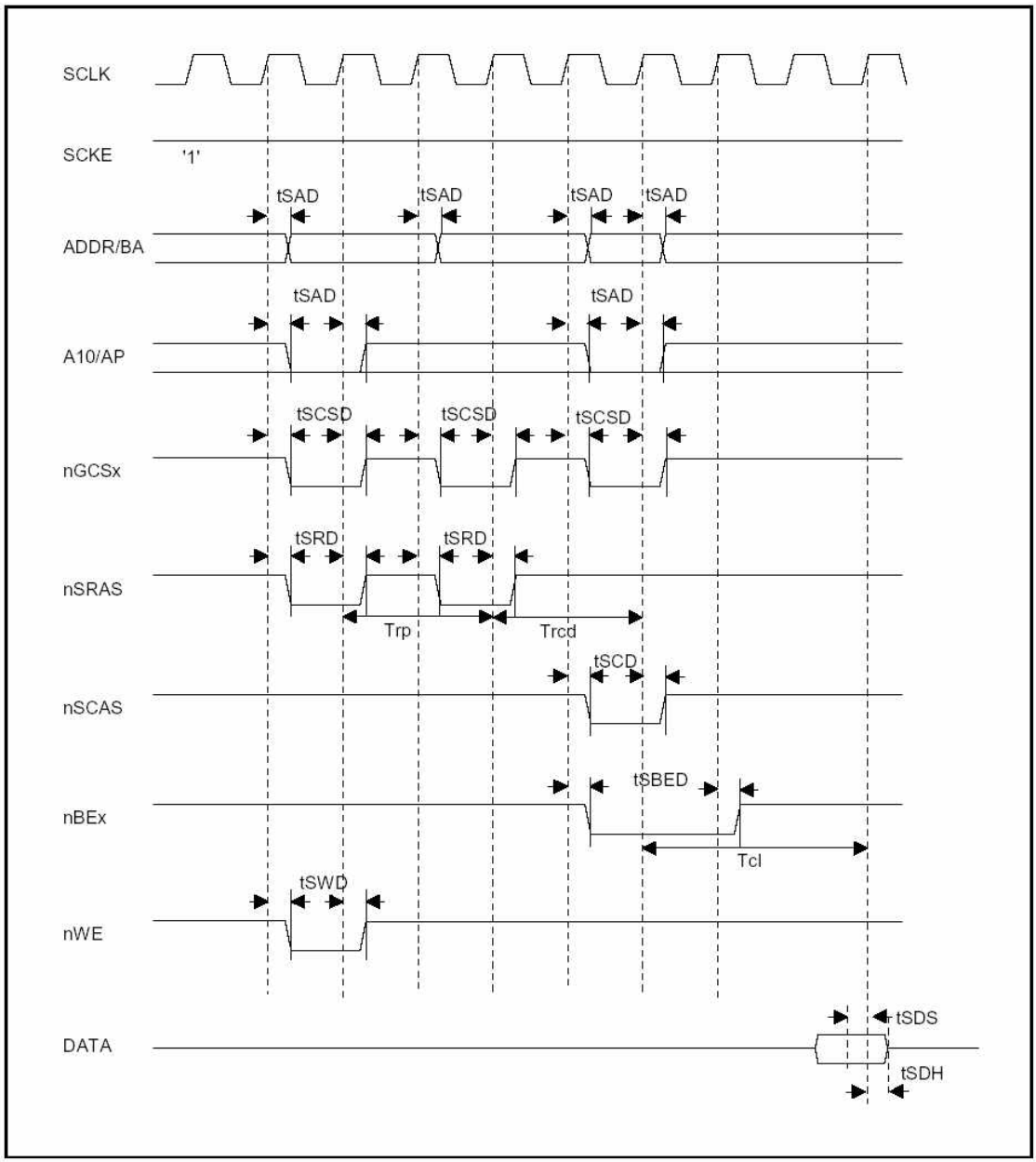

그림 24-24. SDRAM single 읽기 타이밍(II) (Trp=2, Trcd=2, Tcl=3)

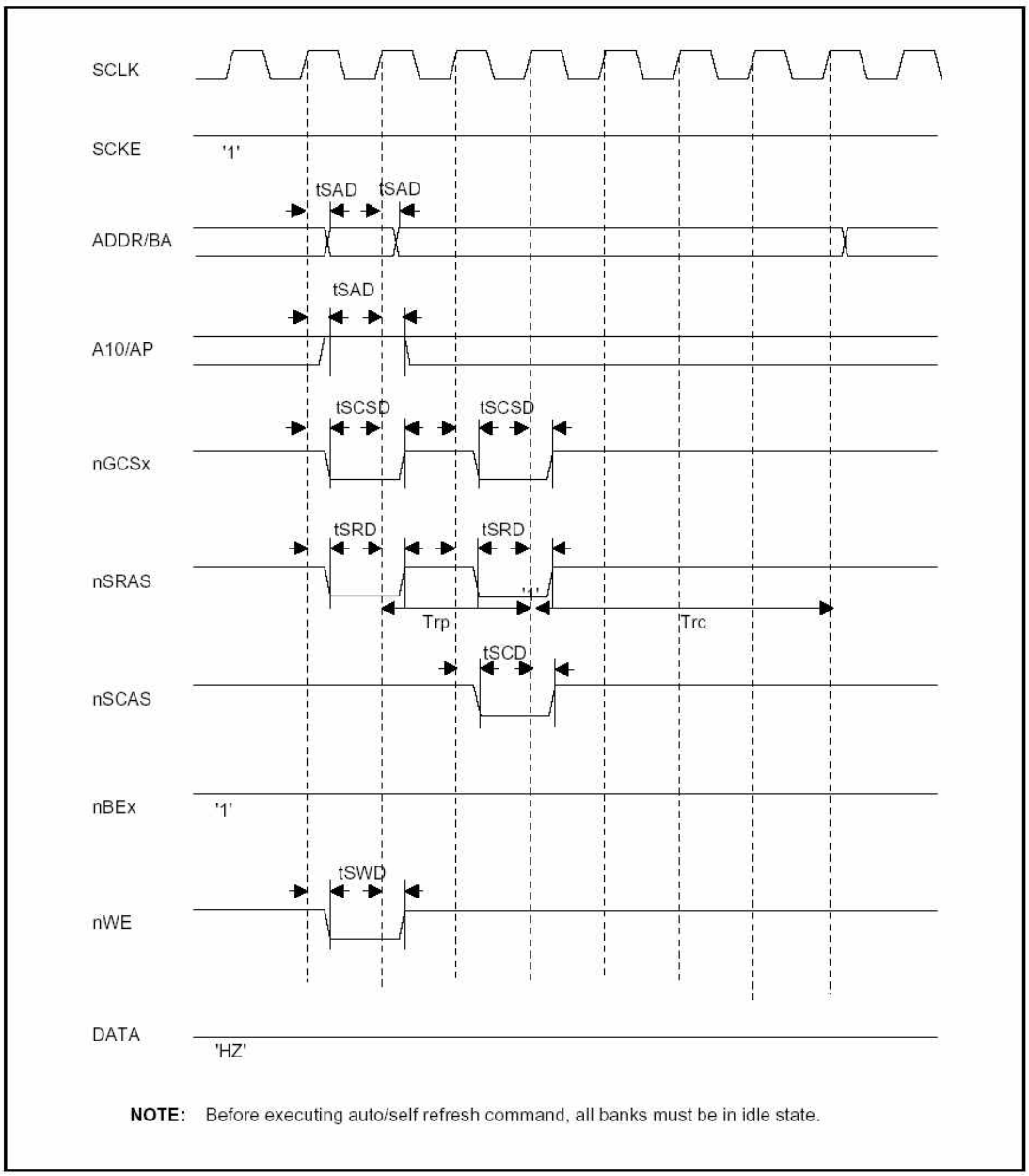

그림 24-25. SDRAM 오토 리프레쉬 타이밍(Trp=2, Trc=4)

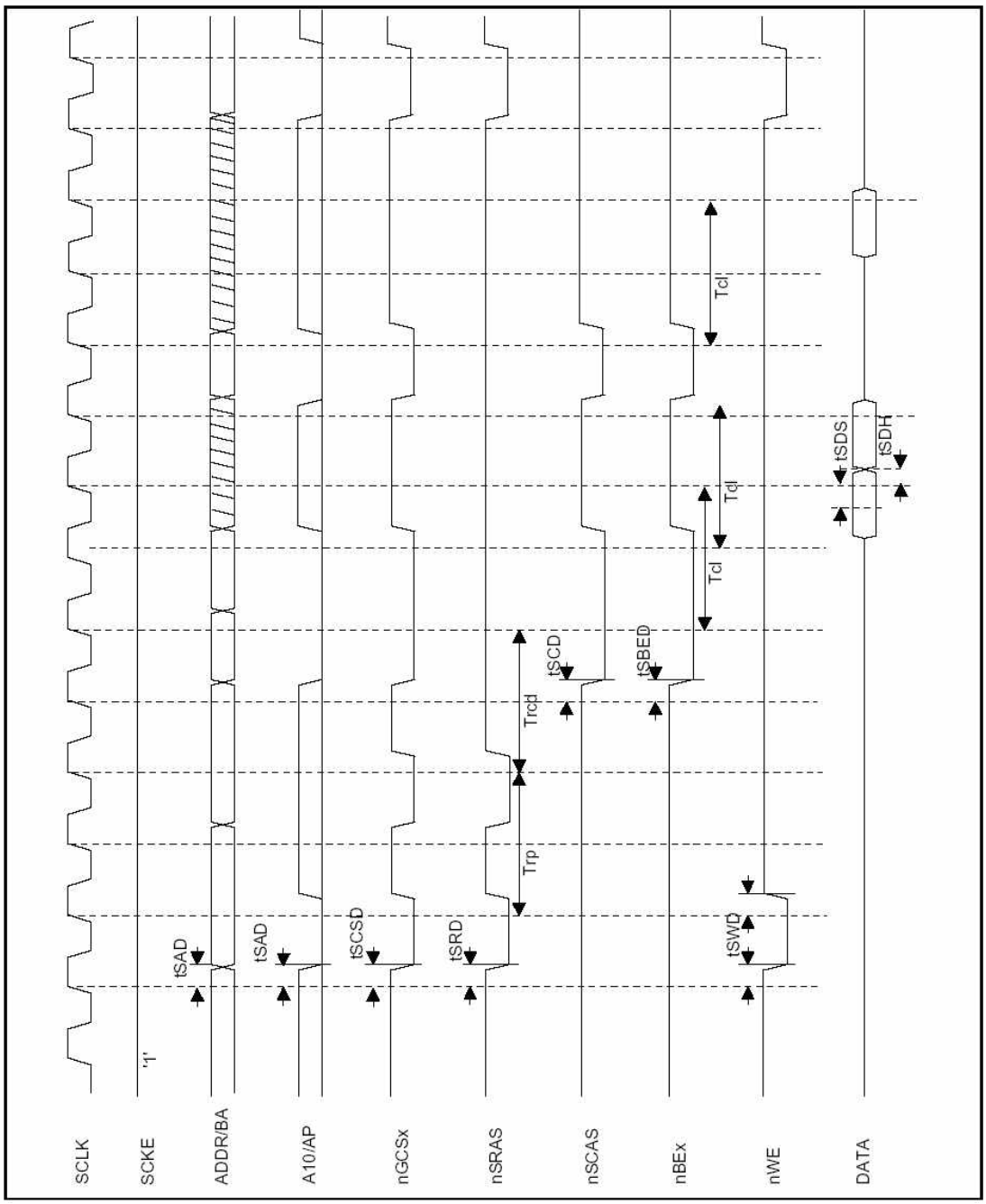

그림 24-26. SDRAM 페이지 Hit-Miss 읽기 타이밍(Trp=2, Trcd=2, Tcl=2)

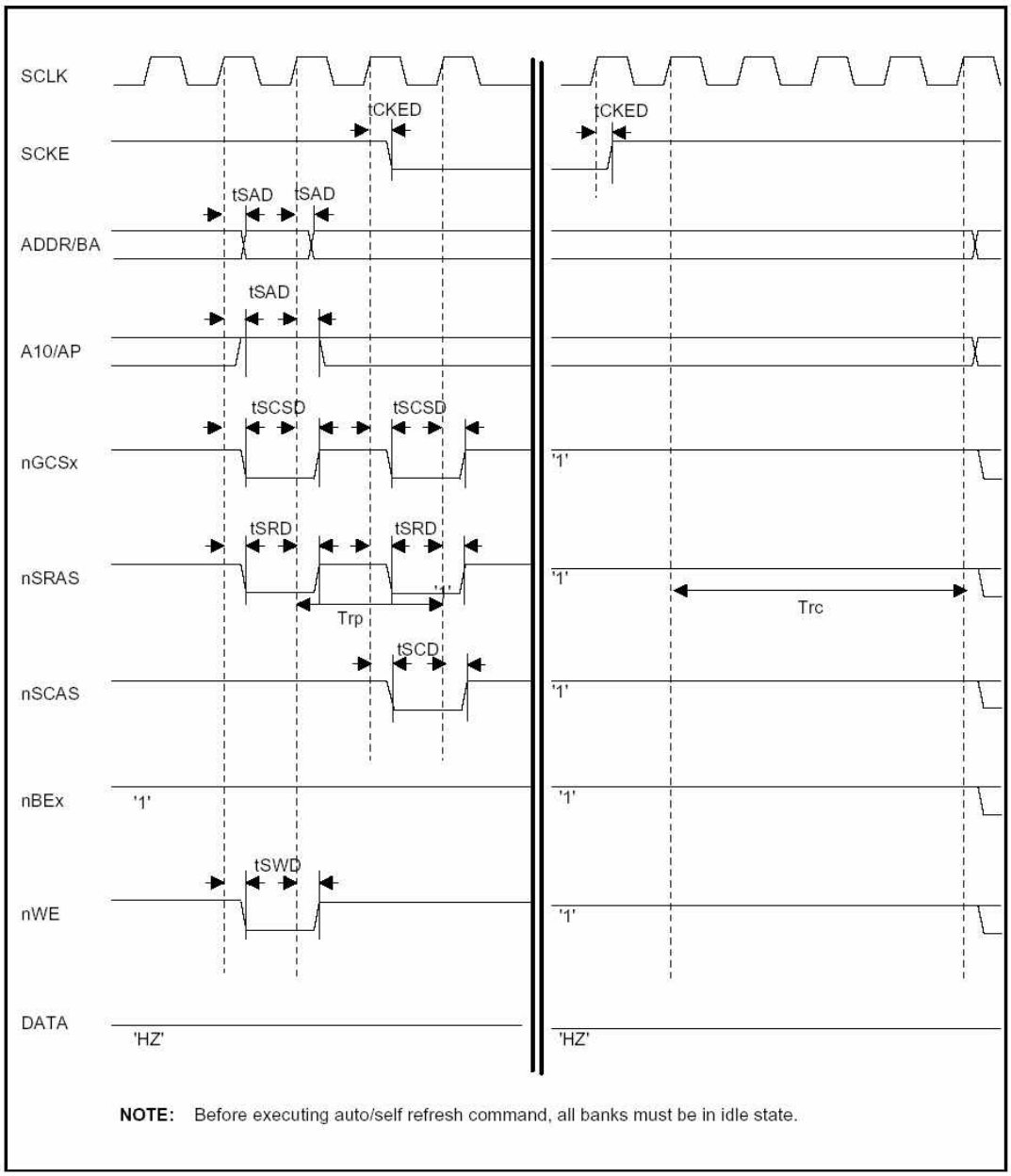

그림 24-27. SDRAM 셀프 리프레쉬 타이밍(Trp=2, Trc=4)

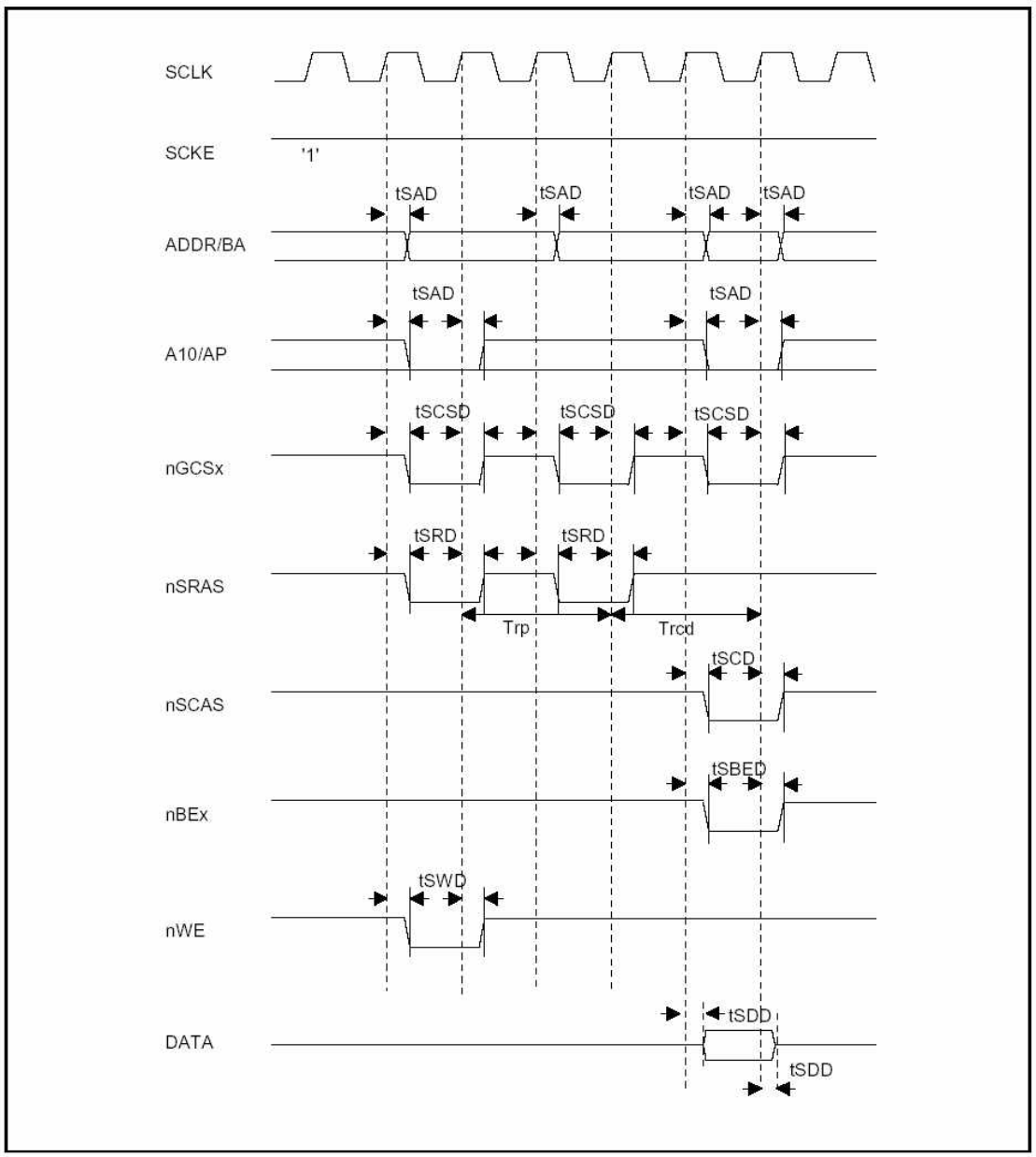

그림 24-28. SDRAM single 쓰기 타이밍(Trp=2, Trcd=2)

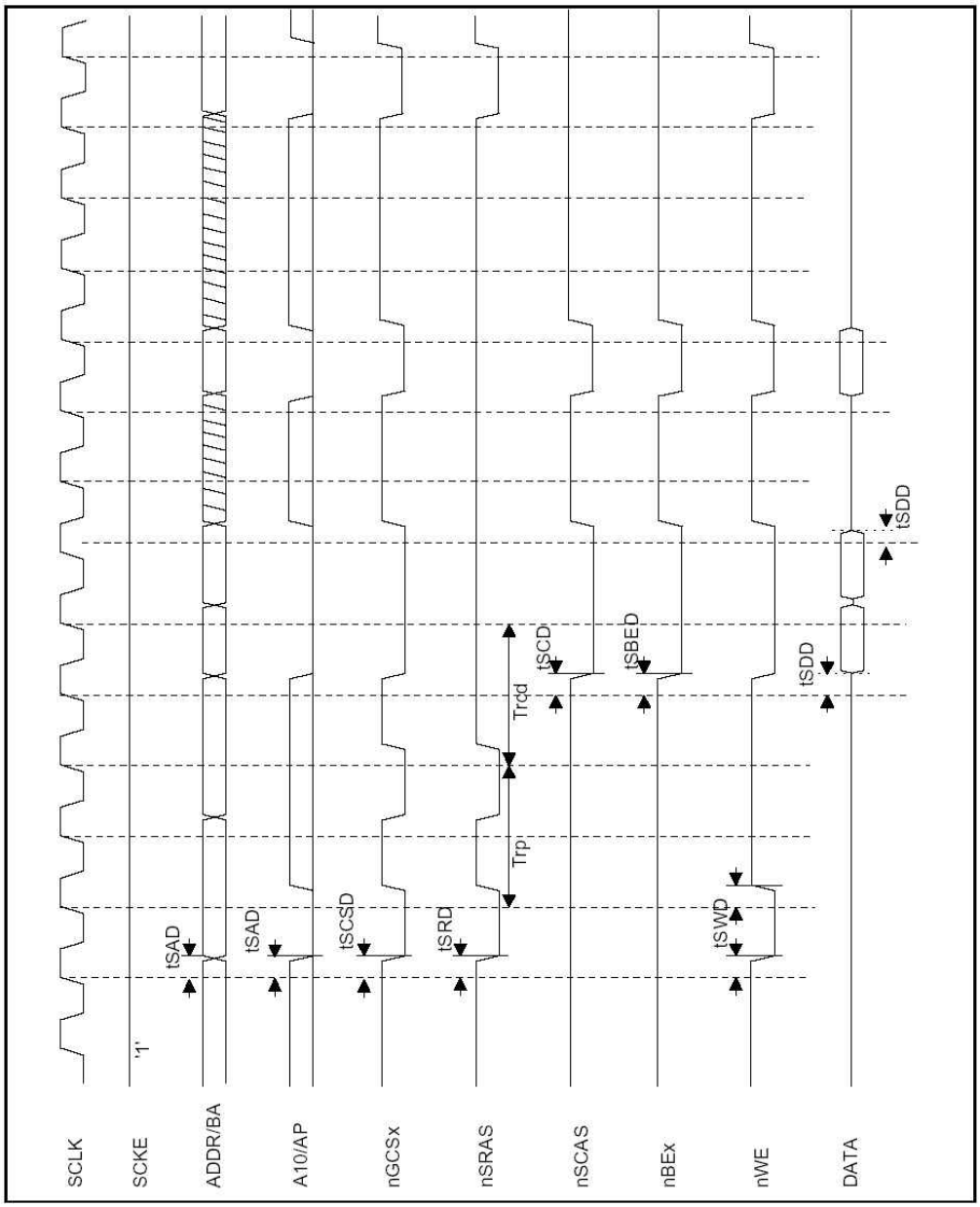

그림 24-29. SDRAM 페이지 Hit-Miss 쓰기 타이밍(Trp=2, Trcd=2, Tcl=2)

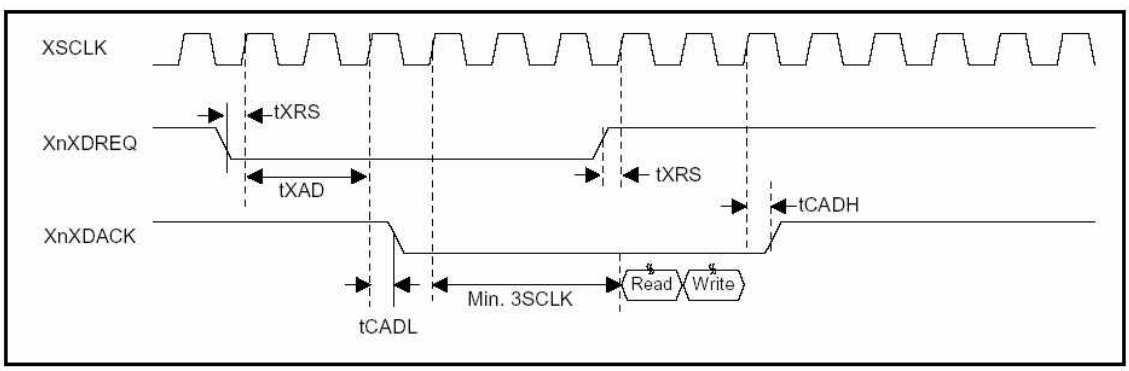

그림 24-30. 외부 DMA 타이밍(핸드쉐이크, single 전송)

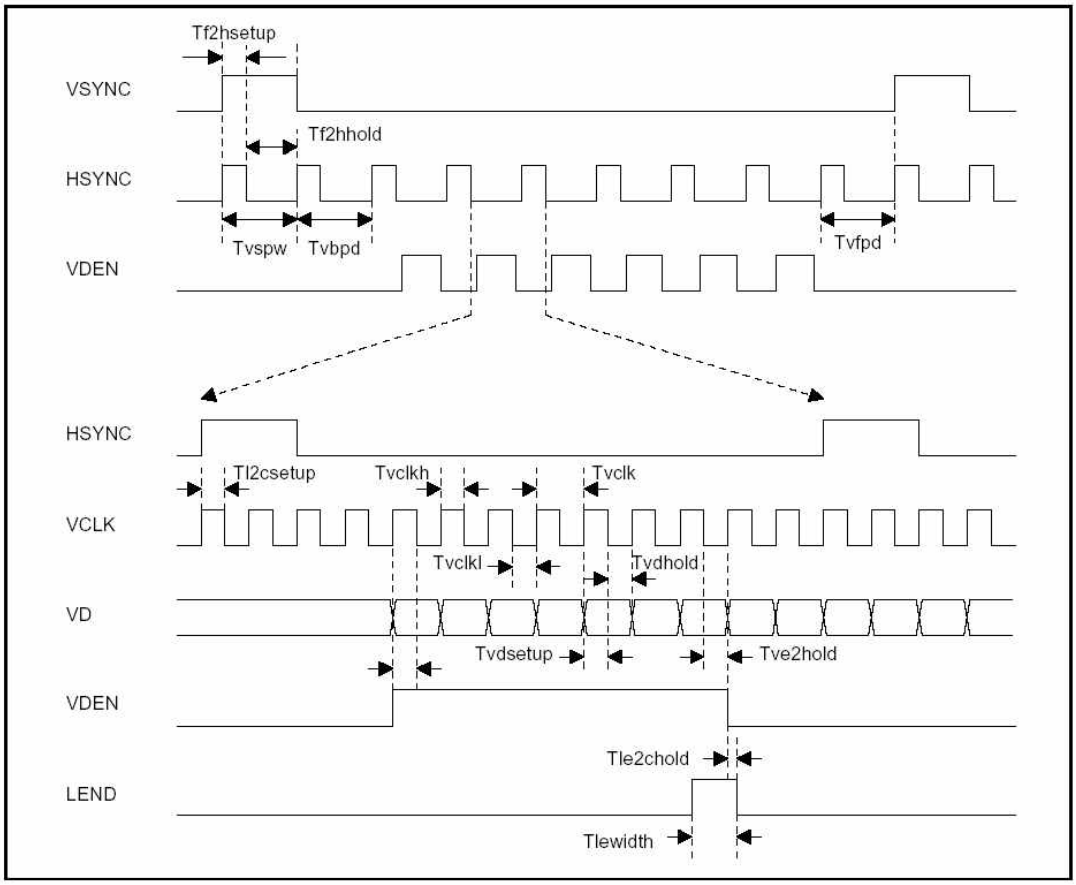

그림 24-31. TFT LCd 컨트롤러 타이밍

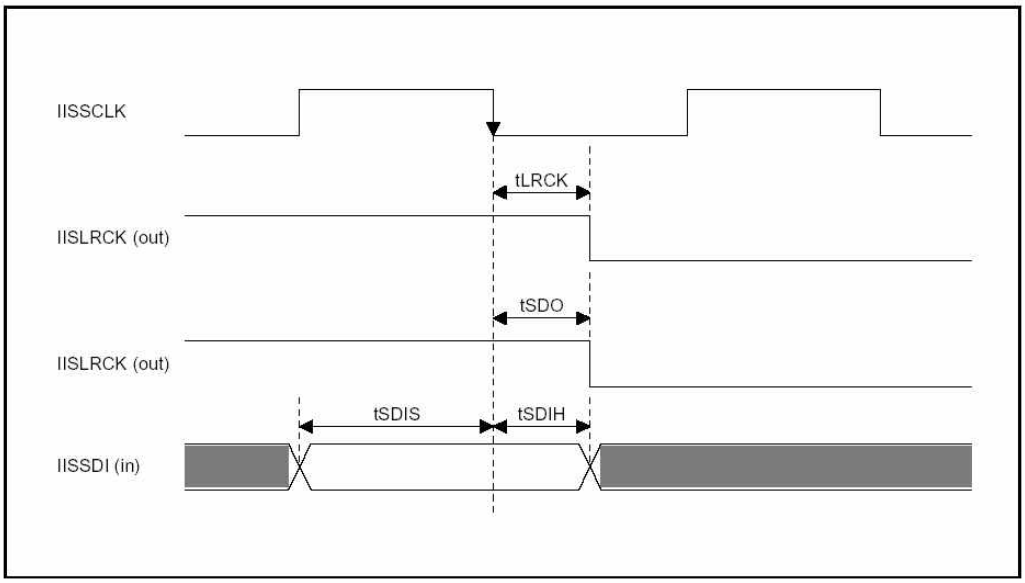

그림 24-32. IIS 인터페이스 타이밍

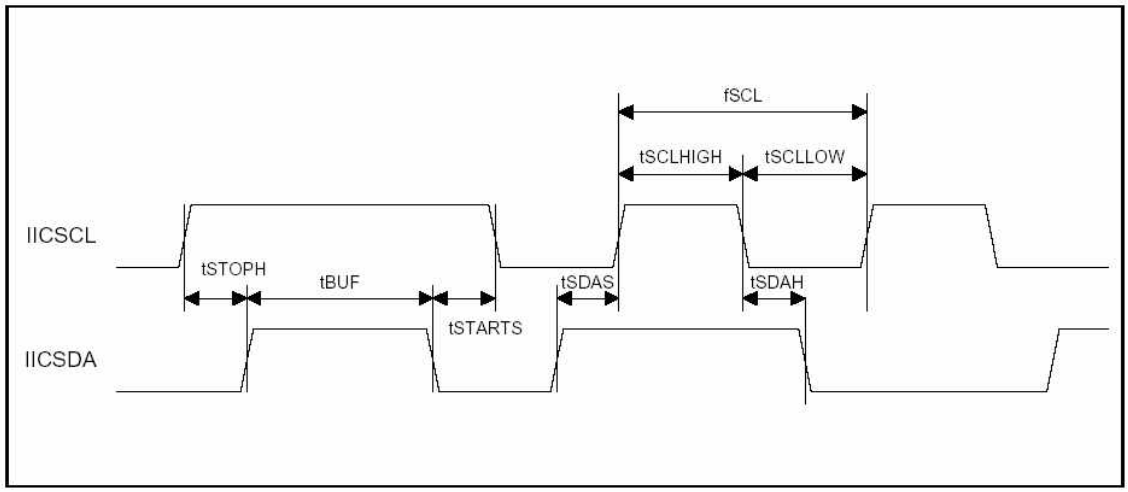

그림 24-33. IIC 인터페이스 타이밍

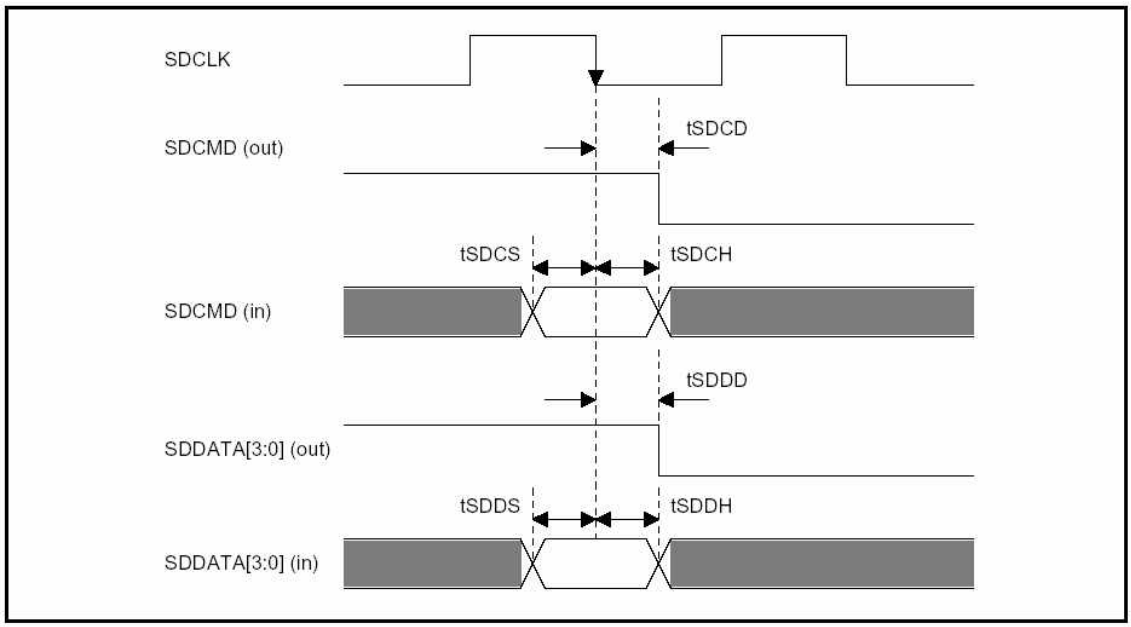

그림 24-34. SD/MMC 인터페이스 타이밍

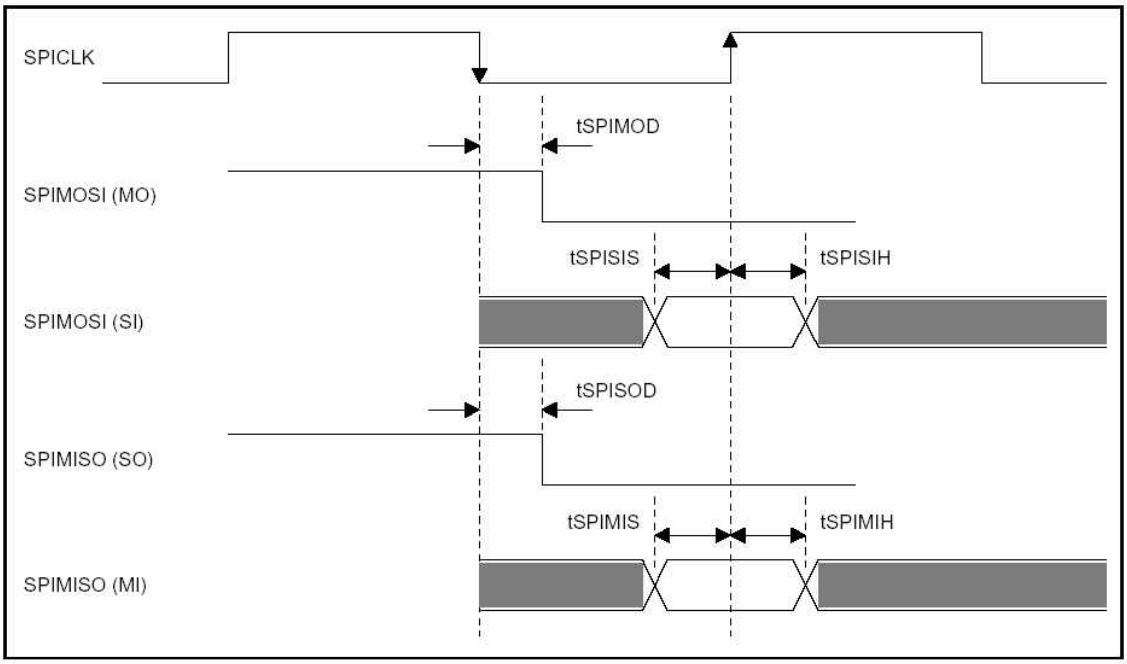

그림 24-35. SPI 인터페이스 타이밍(CPHA=1, CPOL=1)

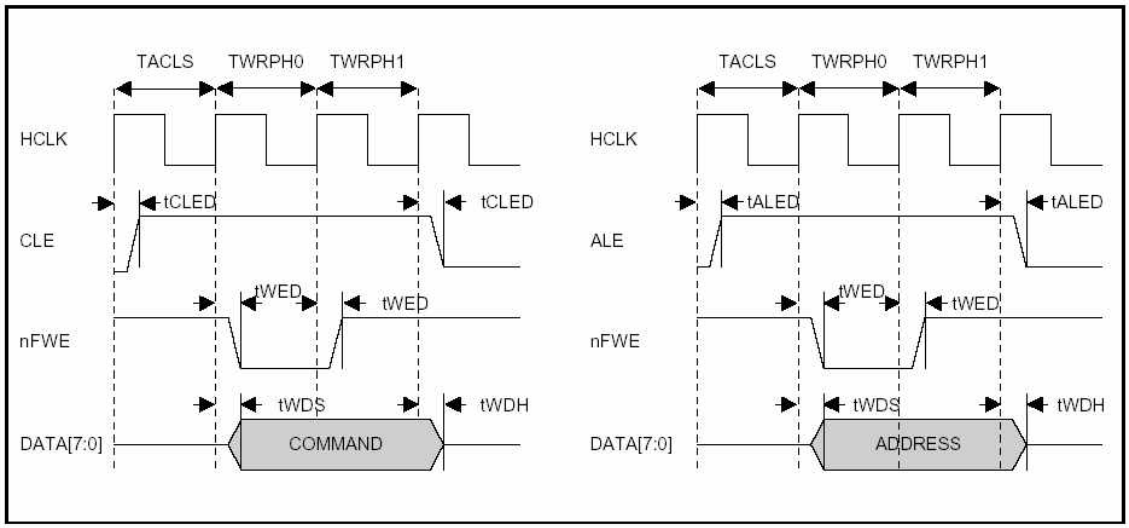

그림 24-36. 낸드 플래쉬 어드레스/커맨드 타이밍

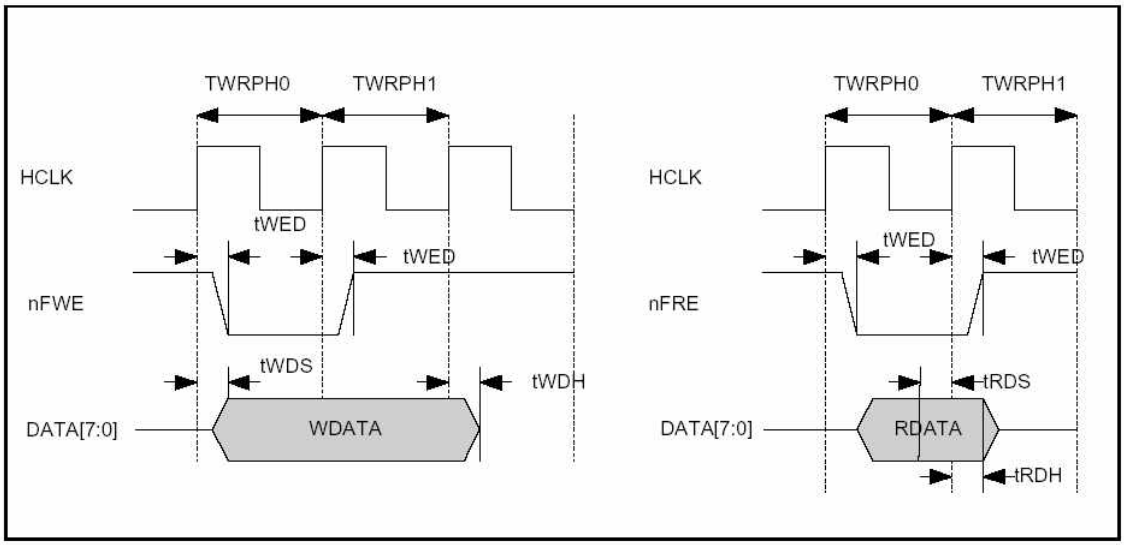

그림 24-37. 낸드 플래쉬 타이밍

표 24-7. 클럭 타이밍 상수

(V_{DDi}, $V_{DDalive}$, V_{DDiarm} = 1.8 V ± 0.15 V, T_A = 0 to 70 °C, V_{DDMOP} = 3.3V ± 0.3V)

Parameter	Symbol	Min	Typ	Max	Unit
Crystal clock input frequency	f_{XTAL}	10	–	20	MHz
Crystal clock input cycle time	$t_{XTALCYC}$	50	–	100	ns
External clock input frequency	f_{EXT}	–	–	66	MHz
External clock input cycle time	t_{EXTCYC}	15.0	–	–	ns
External clock input low level pulse width	t_{EXTLOW}	7	–	–	ns
External clock to HCLK (without PLL)	t_{EX2HC}	3	–	9	ns
HCLK (internal) to CLKOUT	t_{HC2CK}	3	–	11	ns
HCLK (internal) to SCLK	$t_{HC2SCLK}$	0	–	3	ns
External clock input high level pulse width	$t_{EXTHIGH}$	4	–	–	ns
Reset assert time after clock stabilization	t_{RESW}	4	–	–	XTIpll or EXTCLK
PLL Lock Time	t_{PLL}	200	–		uS
Power_OFF mode return oscillation setting time	t_{OSC2}	–	–	65536	XTIpll or EXTCLK
The interval before CPU runs after nRESET is released.	$t_{RST2RUN}$	–	7	–	XTIpll or EXTCLK

표 24-8. ROM/SRAM 버스 타이밍 상수

(V_{DDi}, $V_{DDalive}$, V_{DDiarm} = 1.8 V ± 0.15 V, T_A = 0 to 70 °C, V_{DDMOP} = 3.3V ± 0.3V)

Parameter	Symbol	Min	Typ	Max	Unit
ROM/SRAM Address Delay	t_{RAD}	3	–	11	ns
ROM/SRAM Chip select Delay	t_{RCD}	2	–	9	ns
ROM/SRAM Output enable Delay	t_{ROD}	2	–	8	ns
ROM/SRAM read Data Setup time.	t_{RDS}	4	–	–	ns
ROM/SRAM read Data Hold time.	t_{RDH}	0	–	–	ns
ROM/SRAM Byte Enable Delay	t_{RBED}	2	–	8	ns
ROM/SRAM Write Byte Enable Delay	t_{RWBED}	2	–	10	ns
ROM/SRAM output Data Delay	t_{RDD}	3	–	12	ns
ROM/SRAM external Wait Setup time	t_{WS}	5	–	–	ns
ROM/SRAM external Wait Hold time	t_{WH}	0	–	–	ns
ROM/SRAM Write enable Delay	t_{RWD}	2	–	9	ns

표 24-9. 메모리 인터페이스 타이밍 상수(3.3V)

(V_{DDi}, $V_{DDalive}$, V_{DDiarm} = 1.8 V ± 0.15 V, T_A = 0 to 70 °C, V_{DDMOP} = 3.3V ± 0.3V)

Parameter	Symbol	Min	Typ	Max	Unit
SDRAM Address Delay	t_{SAD}	2	–	7	ns
SDRAM Chip Select Delay	t_{SCSD}	2	–	6	ns
SDRAM Row active Delay	t_{SRD}	1	–	5	ns
SDRAM Column active Delay	t_{SCD}	1	–	5	ns
SDRAM Byte Enable Delay	t_{SBED}	2	–	6	ns
SDRAM Write enable Delay	t_{SWD}	2	–	6	ns
SDRAM read Data Setup time	t_{SDS}	4	–	–	ns
SDRAM read Data Hold time	t_{SDH}	0	–	–	ns
SDRAM output Data Delay	t_{SDD}	2	–	7	ns
SDRAM Clock Enable Delay	T_{cked}	2	–	5	ns

표 24-10. 외부 버스 요청 타이밍 상수

(V_{DD} = 1.8 V ± 0.15 V, T_A = 0 to 70 °C, V_{EXT} = 3.3V ± 0.3V)

Parameter	Symbol	Min	Typ.	Max	Unit
eXternal Bus Request Setup time	t_{XnBRQS}	2	–	5	ns
eXternal Bus Request Hold time	t_{XnBRQH}	–	–	1	ns
eXternal Bus Ack Delay	$t_{XnBACKD}$	9	–	11	ns
HZ Delay	t_{HZD}	4	–	12	ns

표 24-11. DMA 컨트롤 모듈 신호 타이밍 상수

(V_{DD} = 1.8 V ± 0.15 V, T_A = 0 to 70 °C, V_{EXT} = 3.3V ± 0.3V)

Parameter	Symbol	Min	Typ.	Max	Unit
eXternal Request Setup	t_{XRS}	2	–	6	ns
aCcess to Ack Delay when Low transition	t_{CADL}	9	–	11	ns
aCcess to Ack Delay when High transition	t_{CADH}	9	–	11	ns
eXternal Request Delay	t_{XAD}	2	–	–	SCLK

표 24-12. TFT LCD 컨트롤러 모듈 신호 타이밍 상수

(V_{DD} = 1.8 V ± 0.15 V, T_A = 0 to 70 °C, V_{EXT} = 3.3V ± 0.3V)

Parameter	Symbol	Min	Typ	Max	Units
Vertical sync pulse width	Tvspw	VSPW + 1	–	–	Phclk (note1)
Vertical back porch delay	Tvbpd	VBPD+1	–	–	Phclk
Vertical front porch dealy	Tvfpd	VFPD+1	–	–	Phclk
VCLK pulse width	Tvclk	1	–	–	Pvclk (note2)
VCLK pulse width high	Tvclkh	0.5	–	–	Pvclk
VCLK pulse width low	Tvclkl	0.5	–	–	Pvclk
Hsync setup to VCLK falling edge	Tl2csetup	0.5	–	–	Pvclk
VDEN set up to VCLK falling edge	Tde2csetup	0.5	–	–	Pvclk
VDEN hold from VCLK falling edge	Tde2chold	0.5	–	–	Pvclk
VD setup to VCLK falling edge	Tvd2csetup	0.5	–	–	Pvclk
VD hold from VCLK falling edge	Tvd2chold	0.5	–	–	Pvclk
LEND width	Tlewidth	–	1	–	Pvclk
LEND hold from VCLK rising edge	Tle2chold	3	–	–	ns
VSYNC setup to HSYNC falling edge	Tf2hsetup	HSPW + 1	–	–	Pvclk
VSYNC hold from HSYNC falling edge	Tf2hhold	HBPD + HFPD + HOZVAL + 3	–	–	Pvclk

주의할 점:

1. HSYNC 주기
2. VCLK 주기

표 24-13. IIS 컨트롤러 모듈 신호 타이밍 상수

(V_{DD} = 1.8 V ± 0.15 V, T_A = 0 to 70 °C, V_{EXT} = 3.3V ± 0.3V)

Parameter	Symbol	Min	Typ.	Max	Unit
IISLRCK delay time	t_{LRCK}	0.7	–	1.4	ns
IISDO delay time	t_{SDO}	0.8	–	1.7	ns
IISDI Input Setup time	t_{SDIS}	6.2	–	16.3	ns
IISDI Input Hold time	t_{SDIH}	0.1	–	0.1	ns
CODEC clock frequency	f_{CODEC}	1/16	–	1	f_{IIS_BLOCK}

표 24-14. IIC 버스 컨트롤러 모듈 신호 타이밍

(V_{DD} = 1.8 V ± 0.15 V, T_A = 0 to 70 °C, V_{EXT} = 3.3V ± 0.3V)

Parameter	Symbol	Min	Typ.	Max	Unit
SCL clock frequency	f_{SCL}	–	–	std. 100 fast 400	kHz
SCL high level pulse width	$t_{SCLHIGH}$	std. 4.0 fast 0.6	–	–	µs
SCL low level pulse width	t_{SCLLOW}	std. 4.7 fast 1.3	–	–	µs
Bus free time between STOP and START	t_{BUF}	std. 4.7 fast 1.3	–	–	µs
START hold time	t_{STARTS}	std. 4.0 fast 0.6	–	–	µs
SDA hold time	t_{SDAH}	std. 0 fast 0	–	std. - fast 0.9	µs
SDA setup time	t_{SDAS}	std. 250 fast 100	–	–	ns
STOP setup time	t_{STOPH}	std. 4.0 fast 0.6	–	–	µs

주의할 점: Std. 는 표준 모드를, fast는 빠른 모드를 말한다.

1. IIC 데이터 홀딩 시간(tSDAH)은 최소 0ns이다.
   (IIC 데이터 홀딩 시간은 IIC 스펙 v2.1에서 표준/빠른 버스 모드에 대해서 최소 0ns이다.)
   0ns인지 아닌지를 알아보려면 자신의 IIC 디바이스의 데이터 홀딩 시간을 체크한다.
2. IIC 컨트롤러는 IIC 버스 디바이스(표준/빠른 버스 모드)만 지원하며, C 버스 디바이스는 지원하지 않는다.

표 24-15. SD/MMC 인터페이스 송/수신 타이밍 상수

(V_{DD} = 1.8 V ± 0.15 V, T_A = 0 to 70 °C, V_{EXT} = 3.3V ± 0.3V)

Parameter	Symbol	Min	Typ.	Max	Unit
SD Command output Delay time	t_{SDCD}	0.5	–	1.3	ns
SD Command input Setup time	t_{SDCS}	5.8	–	15.2	ns
SD Command input Hold time	t_{SDCH}	0.1	–	0.1	ns
SD Data output Delay time	t_{SDDD}	0.3	–	0.6	ns
SD Data input Setup time	t_{SDDS}	6.3	–	15.3	ns
SD Data input Hold time	t_{SDDH}	0.1	–	0.1	ns

표 24-16. SPI 인터페이스 송/수신 타이밍 상수

(V_{DD} = 1.8 V ± 0.15 V, T_A = 0 to 70 °C, V_{EXT} = 3.3V ± 0.3V)

Parameter	Symbol	Min	Typ.	Max	Unit
SPI MOSI Master Output Delay time	t_{SPIMOD}	1.0	–	4.2	ns
SPI MOSI Slave Input Setup time	t_{SPISIS}	0.1	–	0.1	ns
SPI MOSI Slave Input Hold time	t_{SPISIH}	0.8	–	1.8	ns
SPI MISO Slave output Delay time	t_{SPISOD}	8.2	–	21.4	ns
SPI MISO Master Input Setup time	t_{SPIMIS}	5.6	–	14.7	ns
SPI MISO Master Input Hold time	t_{SPIMIH}	0.1	–	0.1	ns

표 24-17. USB의 전기적인 특성

(V_{DD} = 1.8 V ± 0.15 V, T_A = 0 to 70 °C, V_{EXT} = 3.3V ± 0.3V)

Parameter	Symbol	Condition	Min	Max	Unit
Supply Current					
Suspend Device	ICCS			10	μA
Leakage Current					
Hi-Z state Input Leakage	ILO	0V < VIN < 3.3V	-10	10	μA
Input Levels					
Differential Input Sensitivity	VDI	| (D+) – (D-) |	0.2		V
Differential Common Mode Range	VCM	Includes VDI range	0.8	2.5	
Single Ended Receiver Threshold	VSE		0.8	2.0	
Output Levels					
Static Output Low	VOL	RL of 1.5Kohm to 3.6V		0.3	V
Static Output High	VOH	RL of 15Kohm to GND	2.8	3.6	
Capacitance					
Transceiver Capacitance	CIN	Pin to GND		20	pF

표 24-18. USB Full Speed 출력 버퍼의 전기적인 특성

(V_{DD} = 1.8 V ± 0.15 V, T_A = 0 to 70 °C, V_{EXT} = 3.3V ± 0.3V)

Parameter	Symbol	Condition	Min	Max	Unit
Driver Characteristics					
Transition Time					
Rise Time	TR	CL = 50pF	4.0	2.0	ns
Fall Time	TF	CL = 50pF	4.0	2.0	
Rise/Fall Time Matching	TRFM	(TR / TF)	90	110	%
Output Signal Crossover Voltage	VCRS		1.3	2.0	V
Drive Output Resistance	ZDRV	Steady state drive	28	43	ohm

표 24-19. USB Low speed 출력 버퍼의 전기적인 특성

(V_{DD} = 1.8 V ± 0.15 V, T_A = 0 to 70 °C, V_{EXT} = 3.3V ± 0.3V)

Parameter	Symbol	Condition	Min	Max	Unit
Driver Characteristics					
Transition Time					
Rising Time	TR	CL = 50pF	75		ns
		CL = 350pF		300	
Falling Time	TF	CL = 50pF	75		
		CL = 350pF		300	
Rise/Fall Time Matching	TRFM	(TR / TF)	80	120	%
Output Signal Crossover Voltage	VCRS		1.3	2.0	V

표 24-20. 낸드 플래쉬 인터페이스 타이밍 상수

(V_{DDi}, $V_{DDalive}$, V_{DDiarm} = 1.8 V ± 0.15 V, T_A = 0 to 70 °C, V_{DDIO} = 3.3V ± 0.3V)

Parameter	Symbol	Min	Max	Unit
NFCON Chip Enable delay	t_{CED}	–	6.2	ns
NFCON CLE delay	t_{CLED}	–	7.1	ns
NFCON ALE delay	t_{ALED}	–	7.5	ns
NFCON Write Enable delay	t_{WED}	–	7.2	ns
NFCON Read Enable delay	t_{RED}	–	7.1	ns
NFCON Write Data Setup time	t_{WDS}	–	6.5	ns
NFCON Write Data Hold time	t_{WDH}	1.7	–	ns
NFCON Read Data Setup requirement time	t_{RDS}	0.3	–	ns
NFCON Read Data Hold requirement time	t_{RDH}	0.3	–	ns