# SDRAM의 모든것

BLACKDOT

# SDRAM의 기초 원리

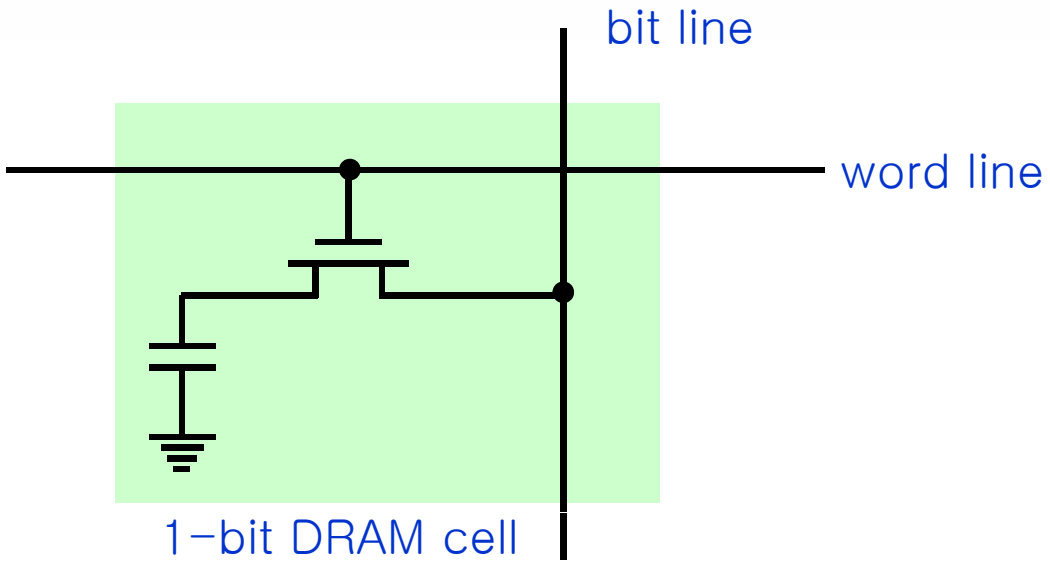


그림. Dynamic Memory Cell

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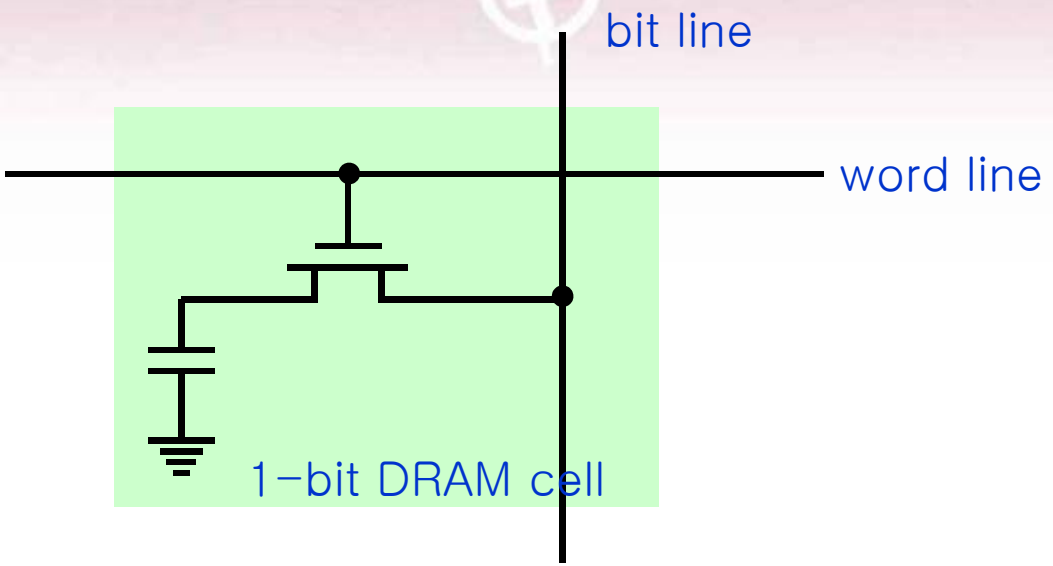
# SDRAM의 기초 원리




To store a 1 in this cell, a HIGH voltage is placed on the bit line, causing the capacitor to charge through the on transistor.

그림. Writing 1 in a Dynamic Memories

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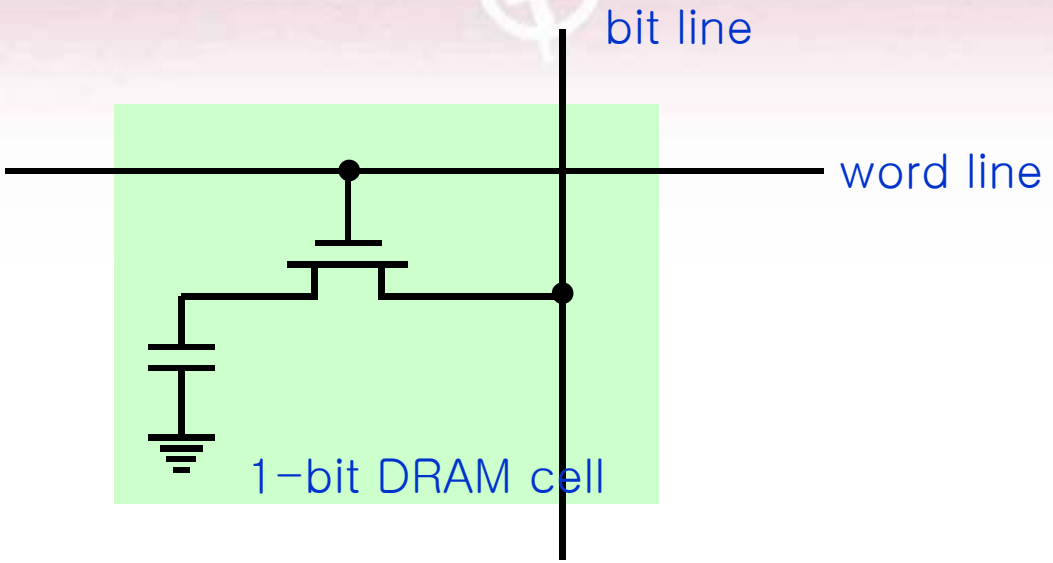
# SDRAM의 기초 원리

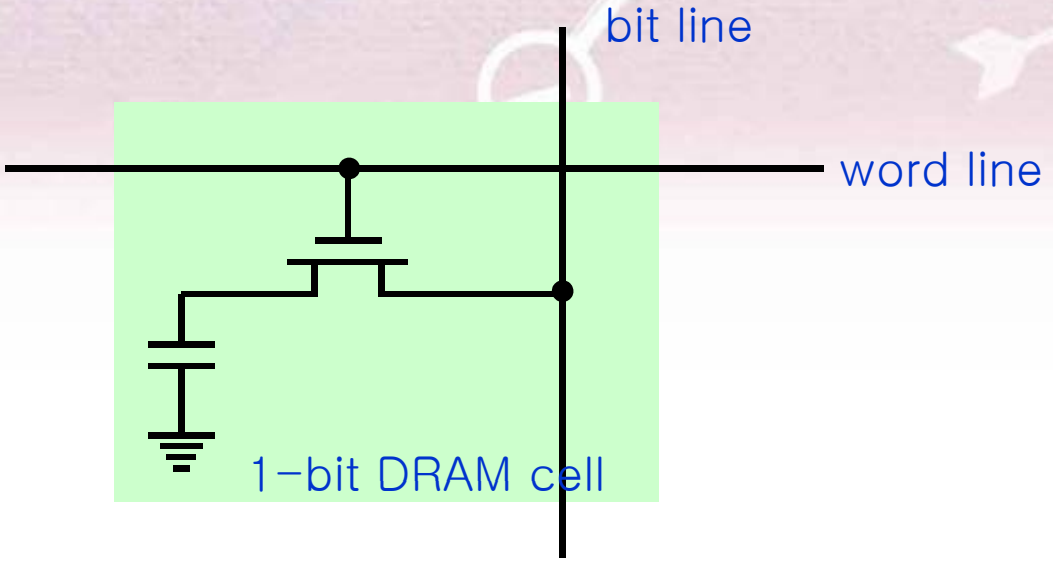



To store a 0 in this cell, a LOW voltage is placed on the bit line, causing the capacitor to discharge through the on transistor.

그림. Writing 0 in a Dynamic Memories

BLACKDOT

# SDRAM의 기초 원리




To read the DRAM cell, the bit line is precharged to a voltage halfway between HIGH and LOW, and then the word line is set HIGH.

Depending on the charge in the capacitor, the precharged bit line is pulled slightly higher or lower.

A sense amplifier detects this small change and recovers a 1 or a 0.

그림. Destructive Reads

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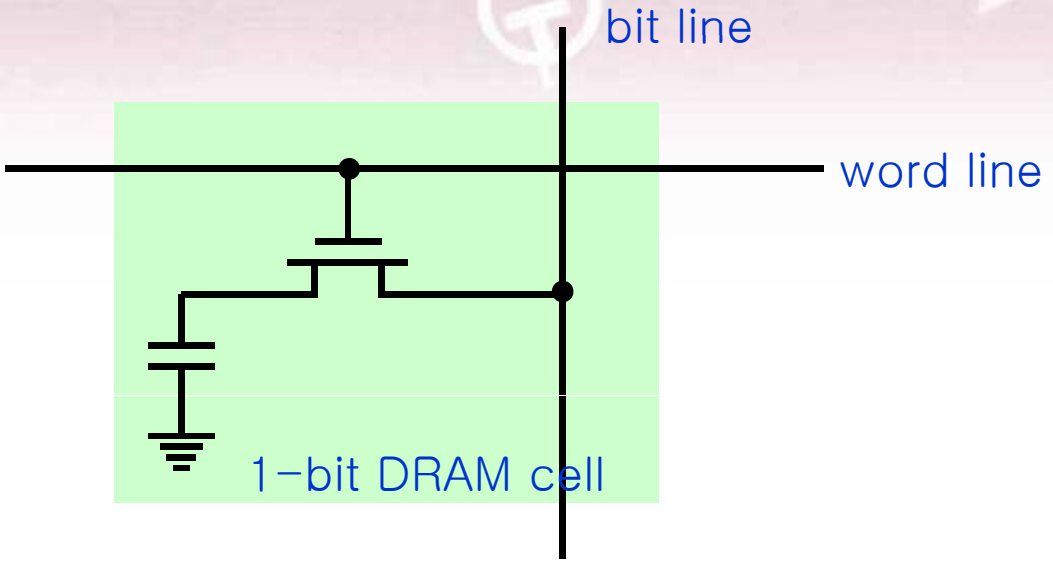
# SDRAM의 기초 원리




The read operation discharges the capacitor.
Therefore a read operation in a dynamic memory must be immediately followed by a write operation of the same value read to restore the capacitor charges.

그림. Recovering from Destructive Reads

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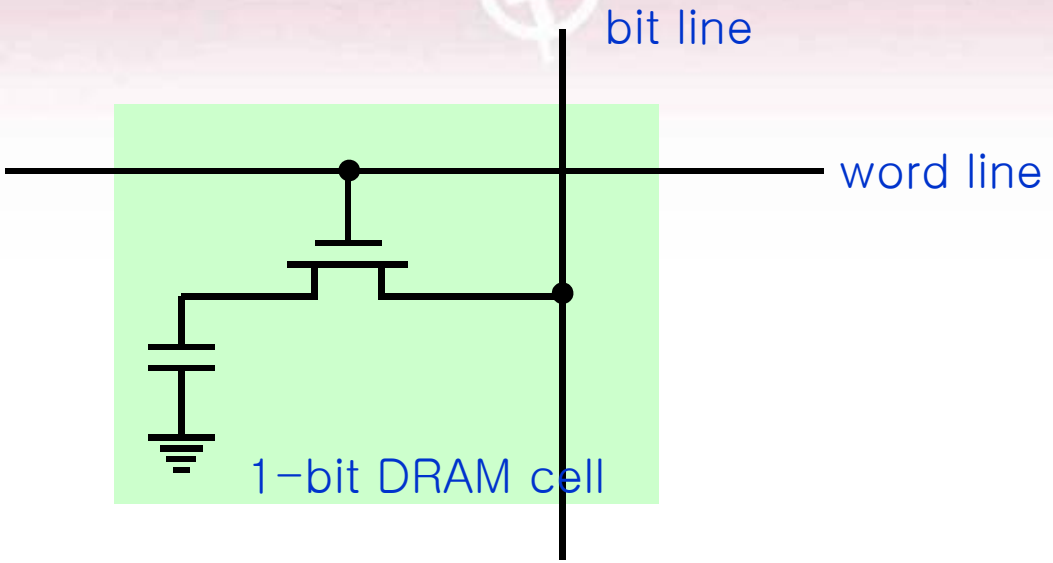
# SDRAM의 기초 원리




The problem with this cell is that it is not bi-stable: only the state 0 can be kept indefinitely, when the cell is in state 1, the charge stored in the capacitor slowly dissipates and the data is lost.

그림. Forgetful Memories

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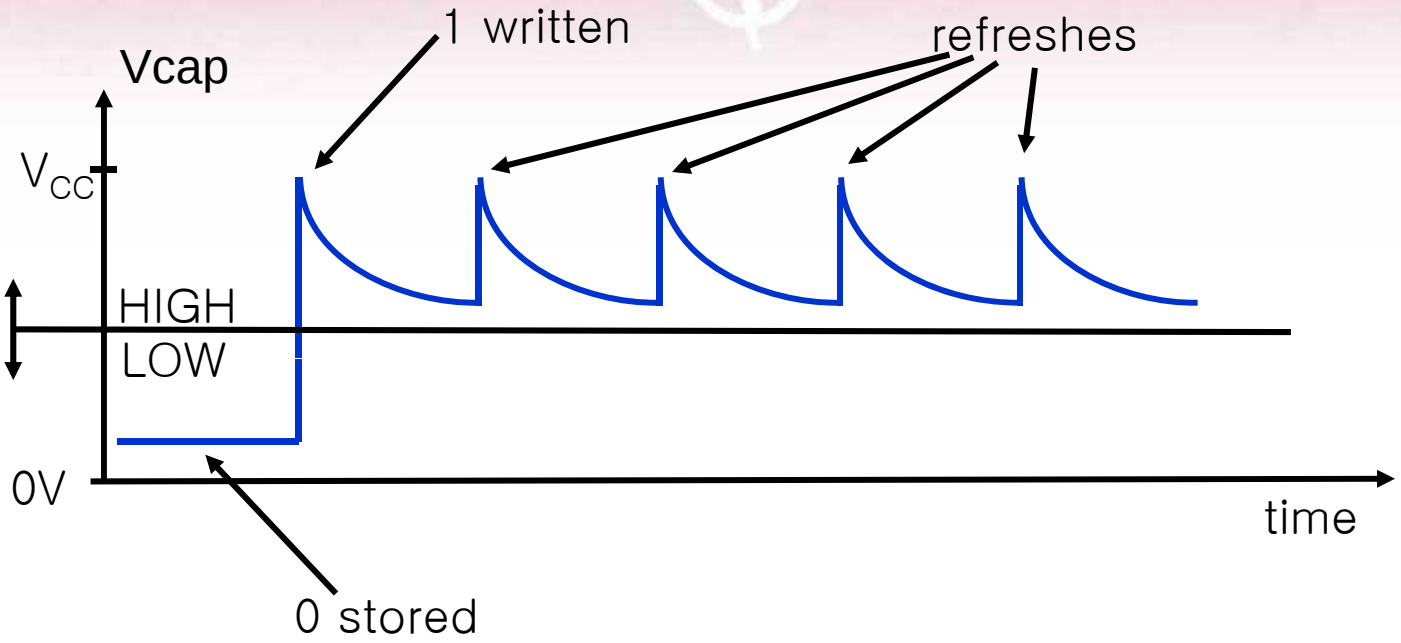
# SDRAM의 기초 원리




The solution is to periodically refresh the memory cells by reading and writing back each one of them.

그림. Refreshing the Memory

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# SDRAM CONTROLLER

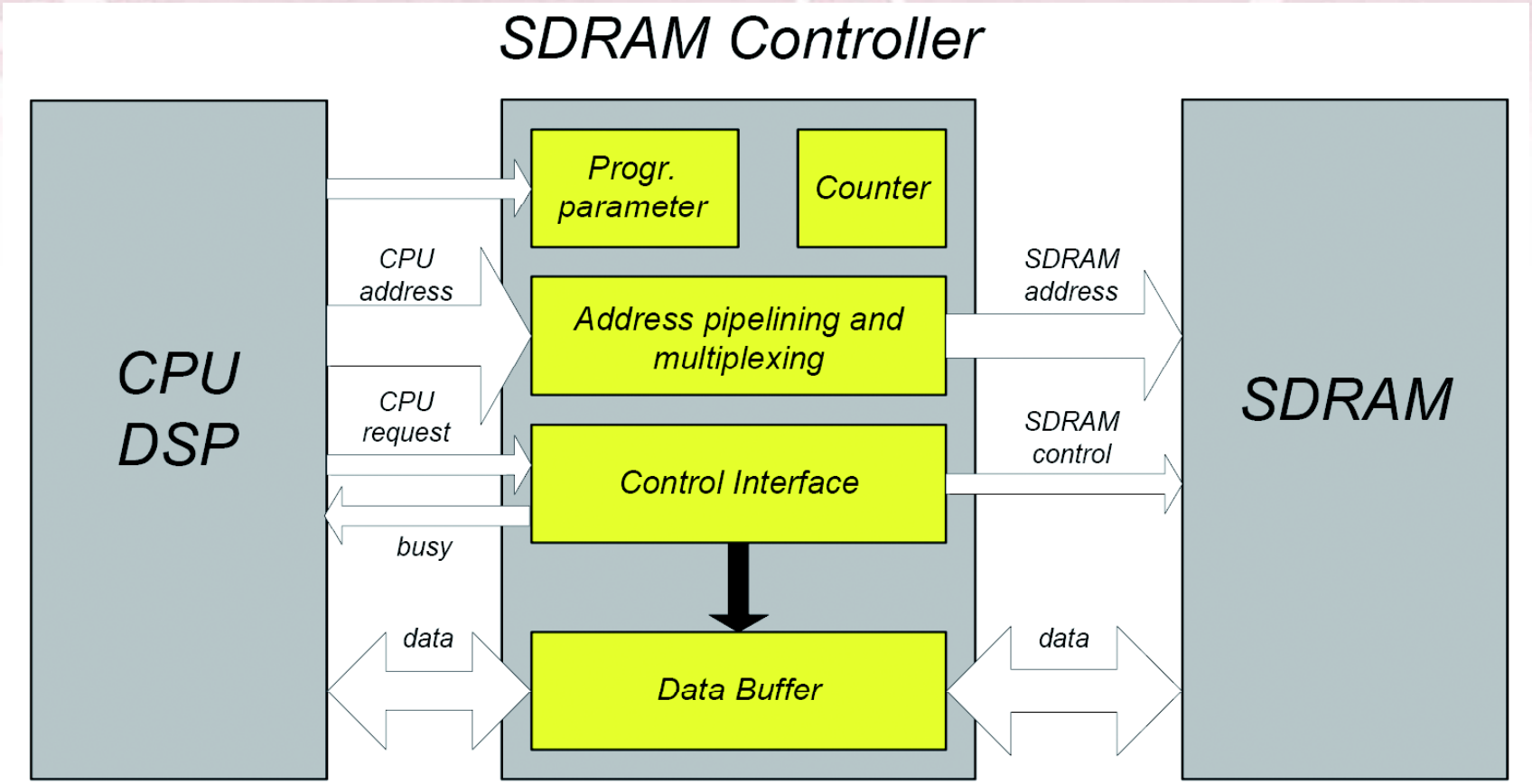


그림. Host Interface of SDRAM

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# x4, x8, x16

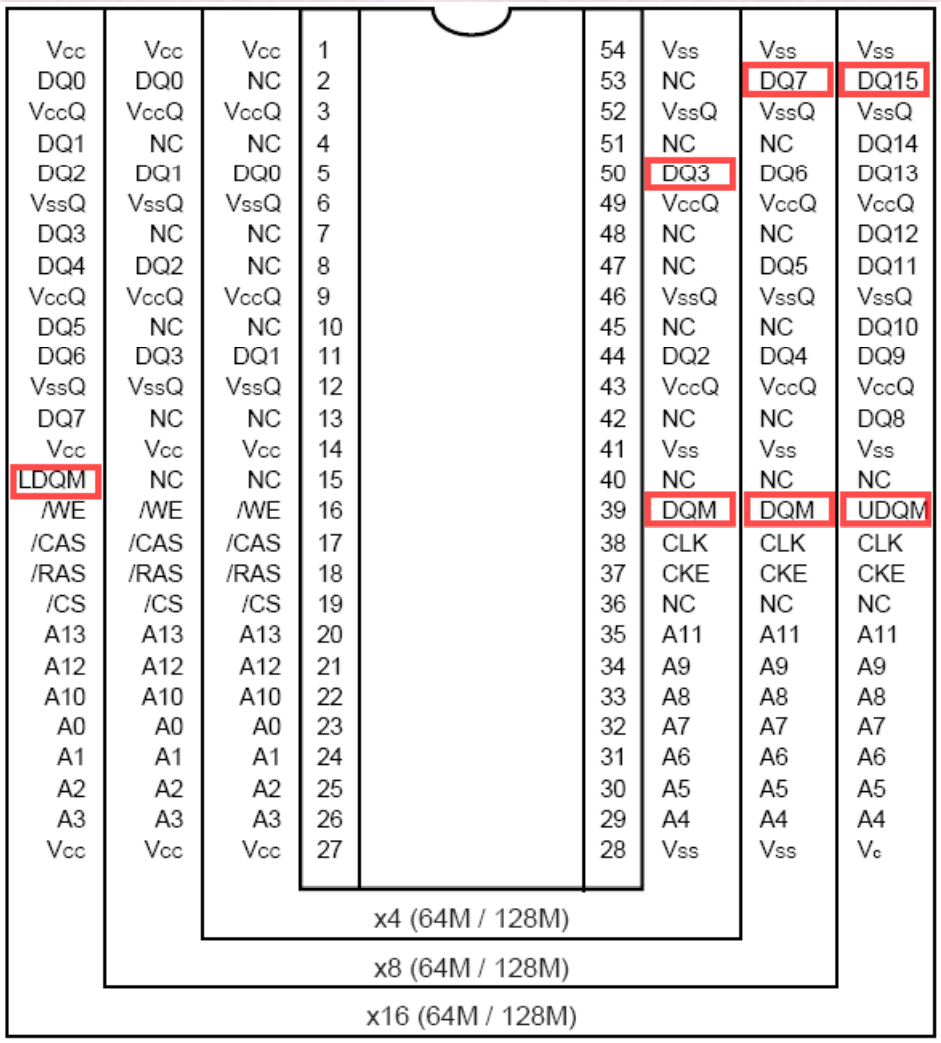


그림. Pin configuration of 64M/128M SDRAM

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# SDRAM의 내부 구조

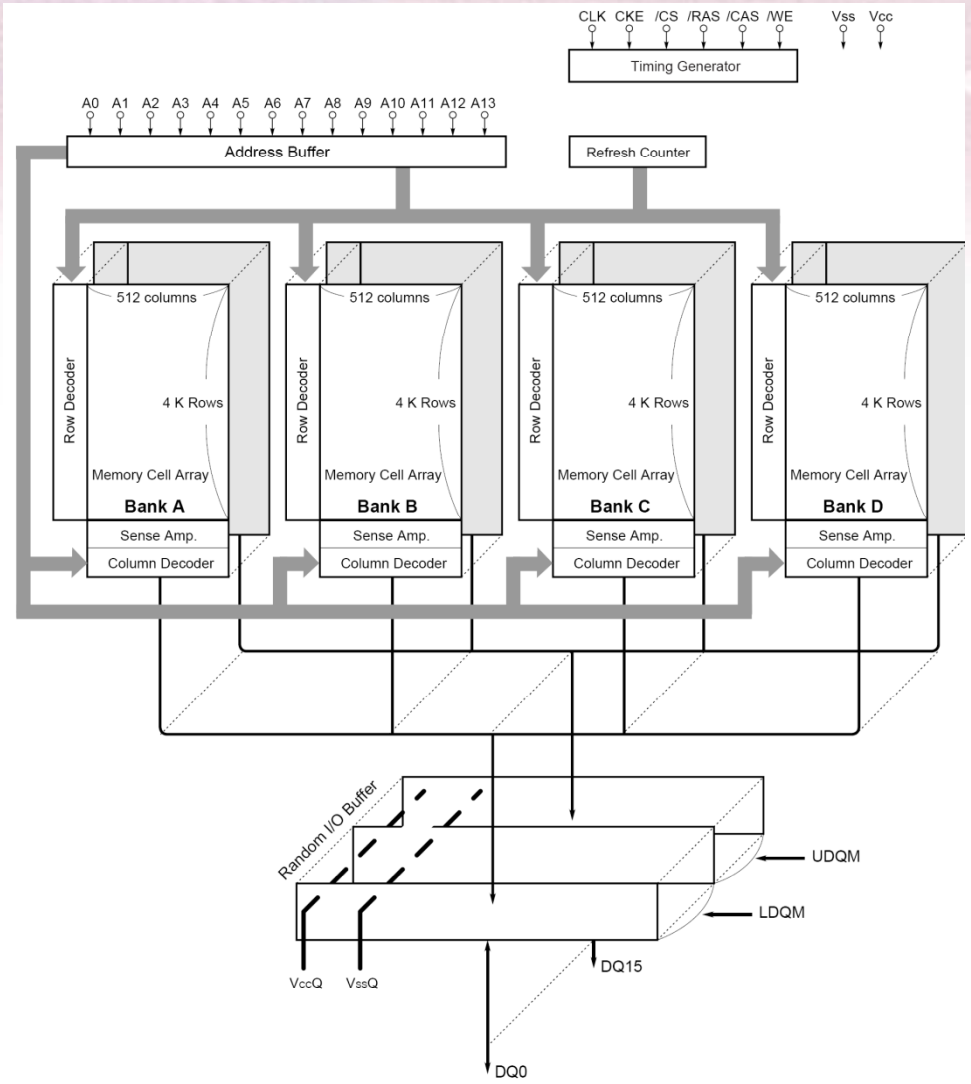


그림. Block diagram of 128M SDRAM

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# BANK

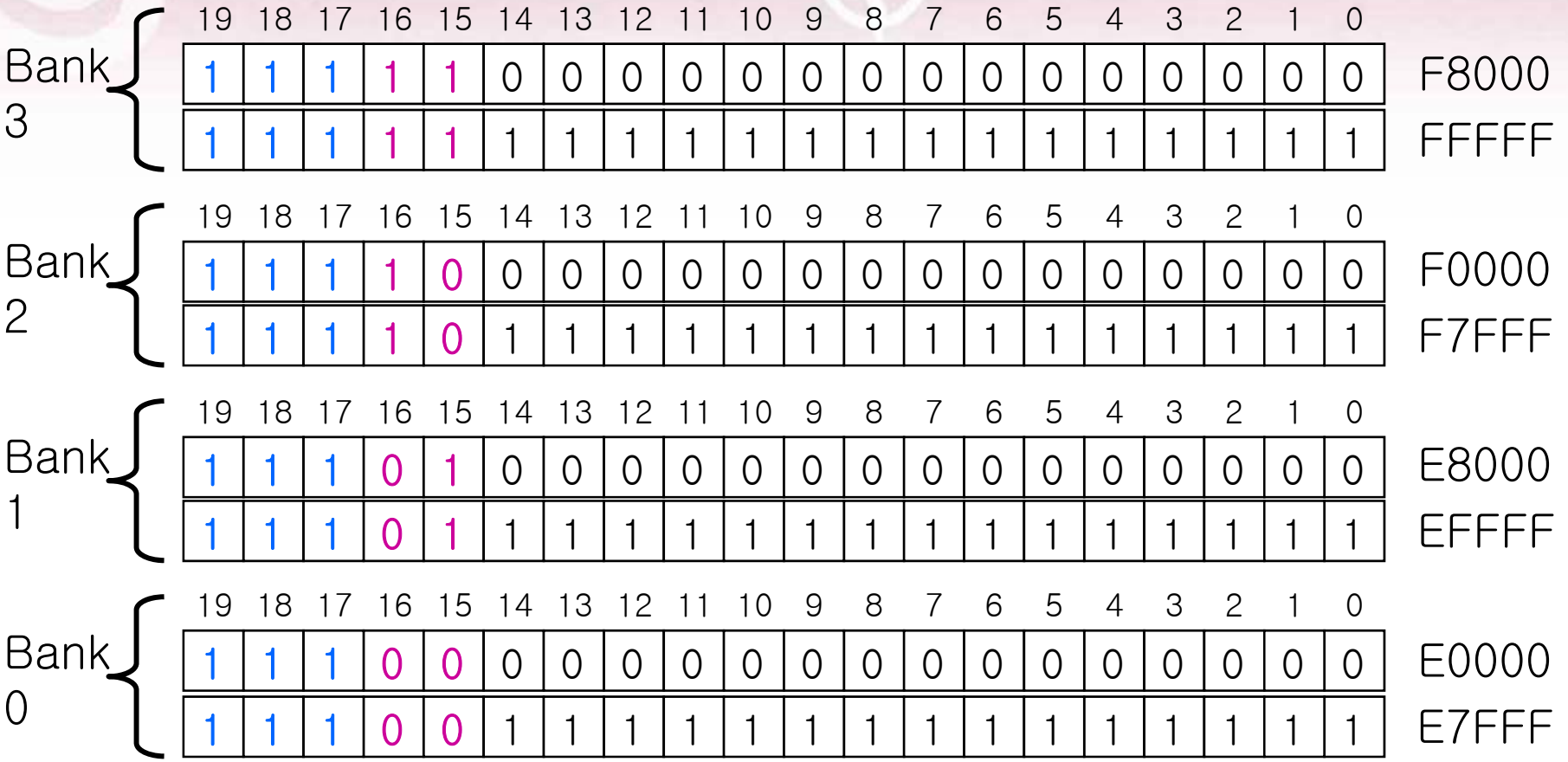


그림. BANK assignment rule

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# ADDRESS DECODING for SDRAM

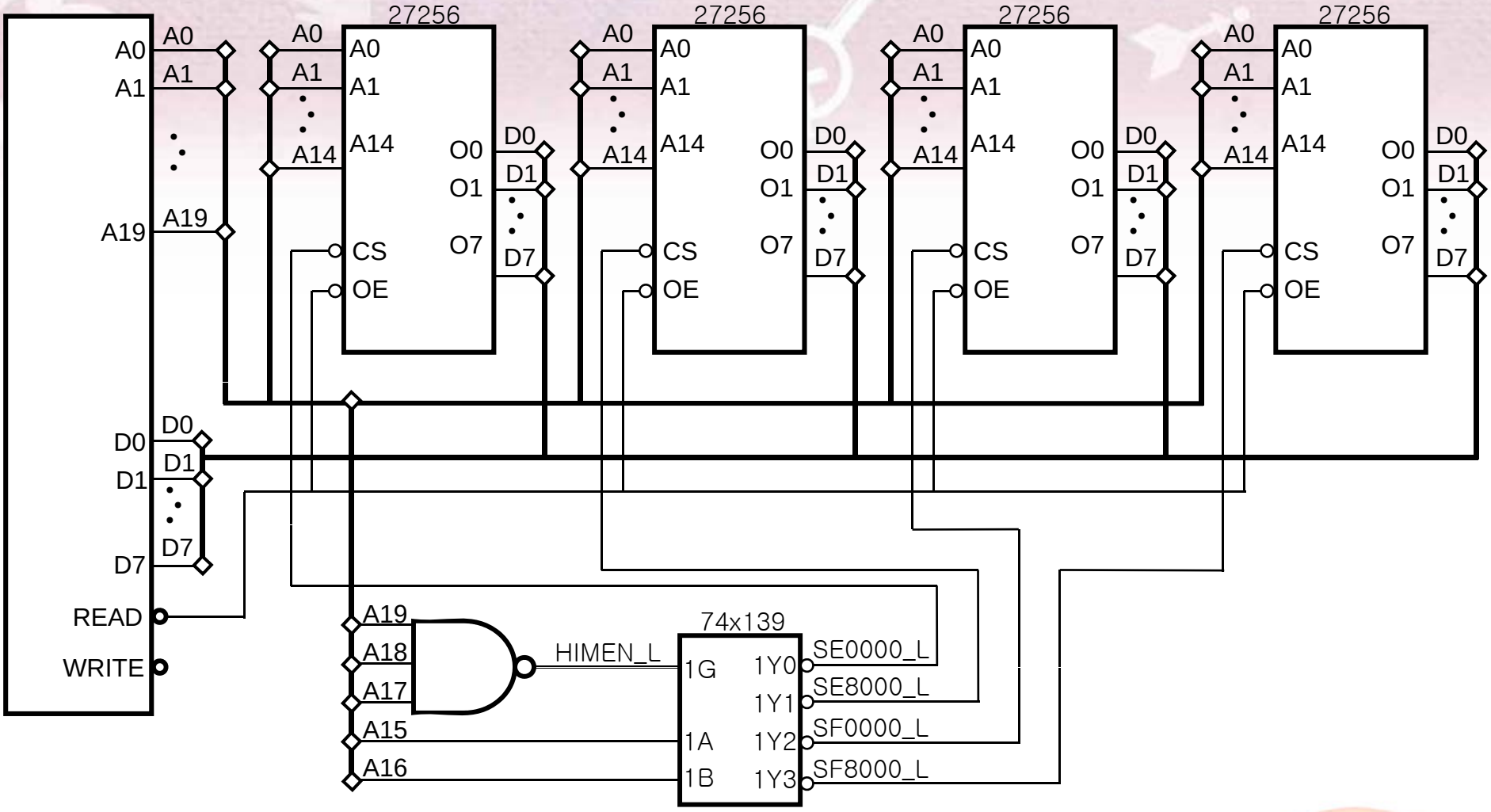


그림. Address Decoding

BLACKDOT

# SDRAM의 내부 구조

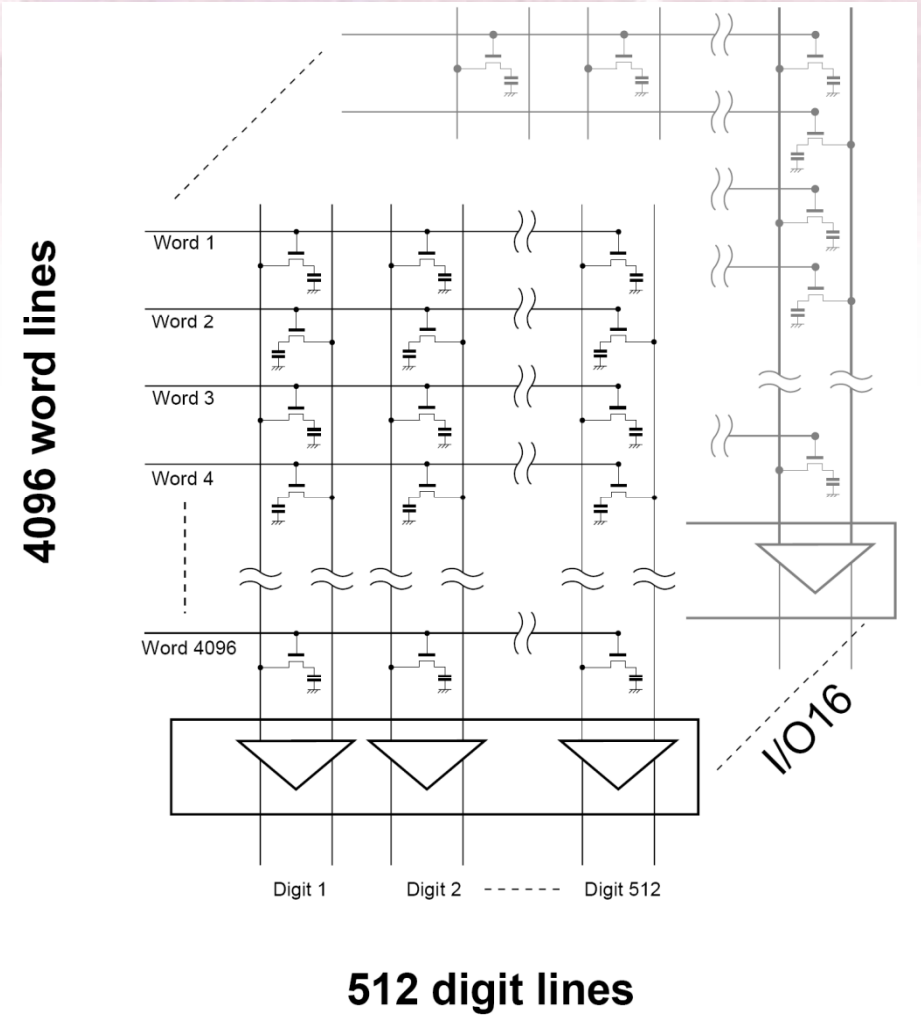


그림. Memory Cell Array

BLACKDOT

# SDRAM의 초기화

**Power-up sequence**

1. Apply VDD and VDDQ at the same time. Keep CKE low during power up.
2. Wait for stable power.
3. Start clock and drive CKE high.

**Caution** **Voltage on any input pin must not exceed VDD+0.3V during power up.**

**Initialization sequence**

4. After stable power and stable clock, wait 200$\mu$s.
5. Issue precharge all command (PALL).
6. After tRP delay, issue 8 or more auto refresh commands (REF).
7. Set the mode register set command (MRS) to initialize the mode register.

**Remark** **We recommend that you keep DQM and CKE high during initialization sequence to prevent data contention on the DQ bus.**

그림. Memory Cell Array

# SDRAM의 초기화

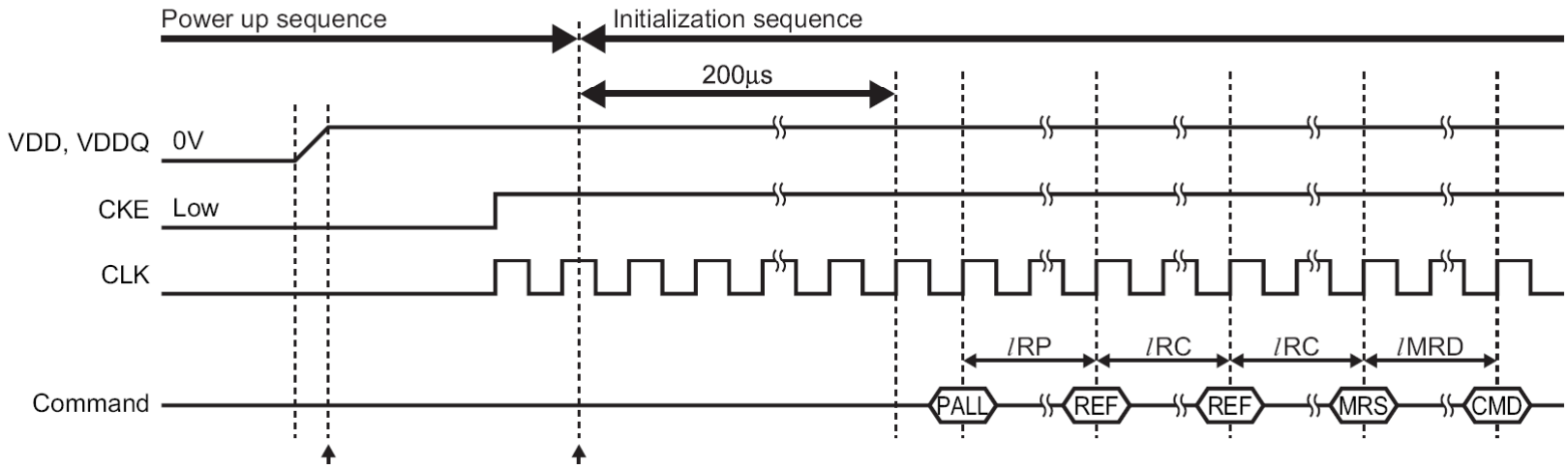


그림. Power up and Initialization Sequence

BLACKDOT

# SDRAM의 초기화

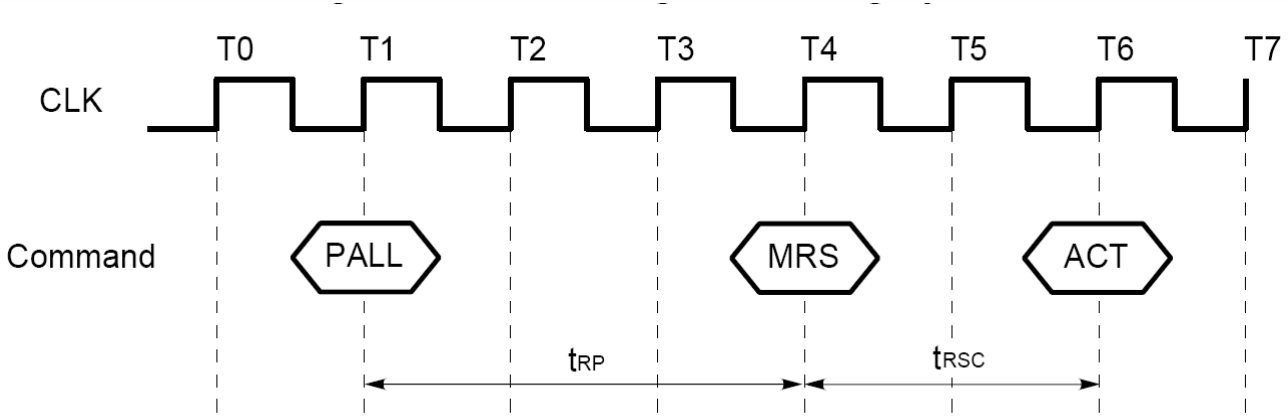


그림. Mode Register Setting Cycle

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# SDRAM의 초기화

| 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| x | x | x | x | 1 | 0 | 0 | LTMODE | | | WT | BL | | | Burst read & single write (for write through cache) |
| 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | LTMODE | | | WT | BL | | | Mode register setting |

Burst length

| A2 | A1 | A0 | WT = 0 | WT = 1 |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 2 | 2 |
| 0 | 1 | 0 | 4 | 4 |
| 0 | 1 | 1 | 8 | 8 |
| 1 | 0 | 0 | R (reserved) | R (reserved) |
| 1 | 0 | 1 | R (reserved) | R (reserved) |
| 1 | 1 | 0 | R (reserved) | R (reserved) |
| 1 | 1 | 1 | Full page | R (reserved) |

Wrap type

| A3 | Wrap type (WT) |
|---|---|
| 0 | Sequential |
| 1 | Interleave |

/CAS latency

| A6 | A5 | A4 | /CAS latency |
|---|---|---|---|
| 0 | 0 | 0 | R (reserved) |
| 0 | 0 | 1 | R (reserved) |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | R (reserved) |
| 1 | 0 | 1 | R (reserved) |
| 1 | 1 | 0 | R (reserved) |
| 1 | 1 | 1 | R (reserved) |

그림. Field of Mode Register (with 128M SDRAM)

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# 레이턴시

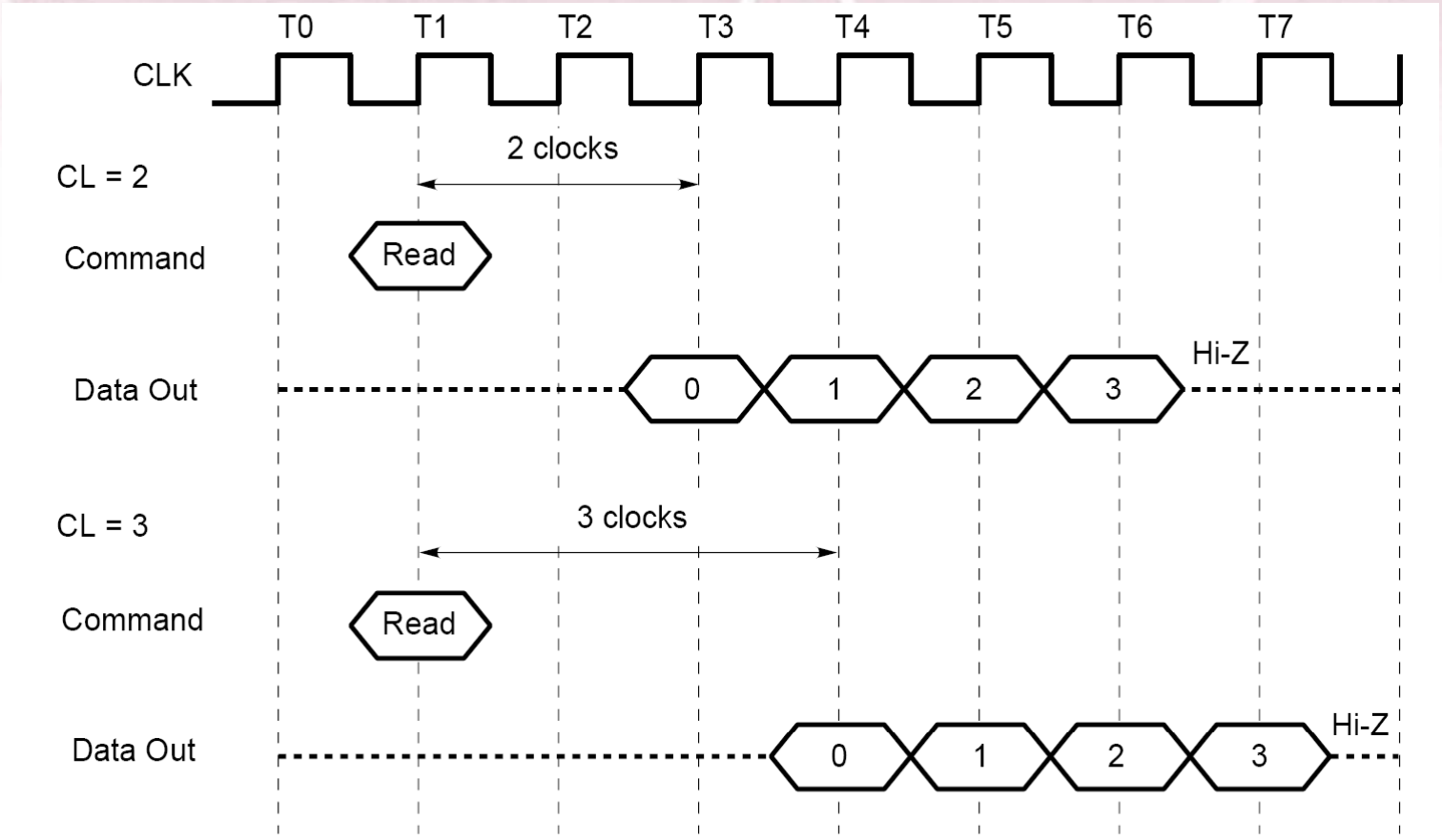


그림. Timing Differences between /CAS Latency = 2 and 3

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# BURST 오퍼레이션

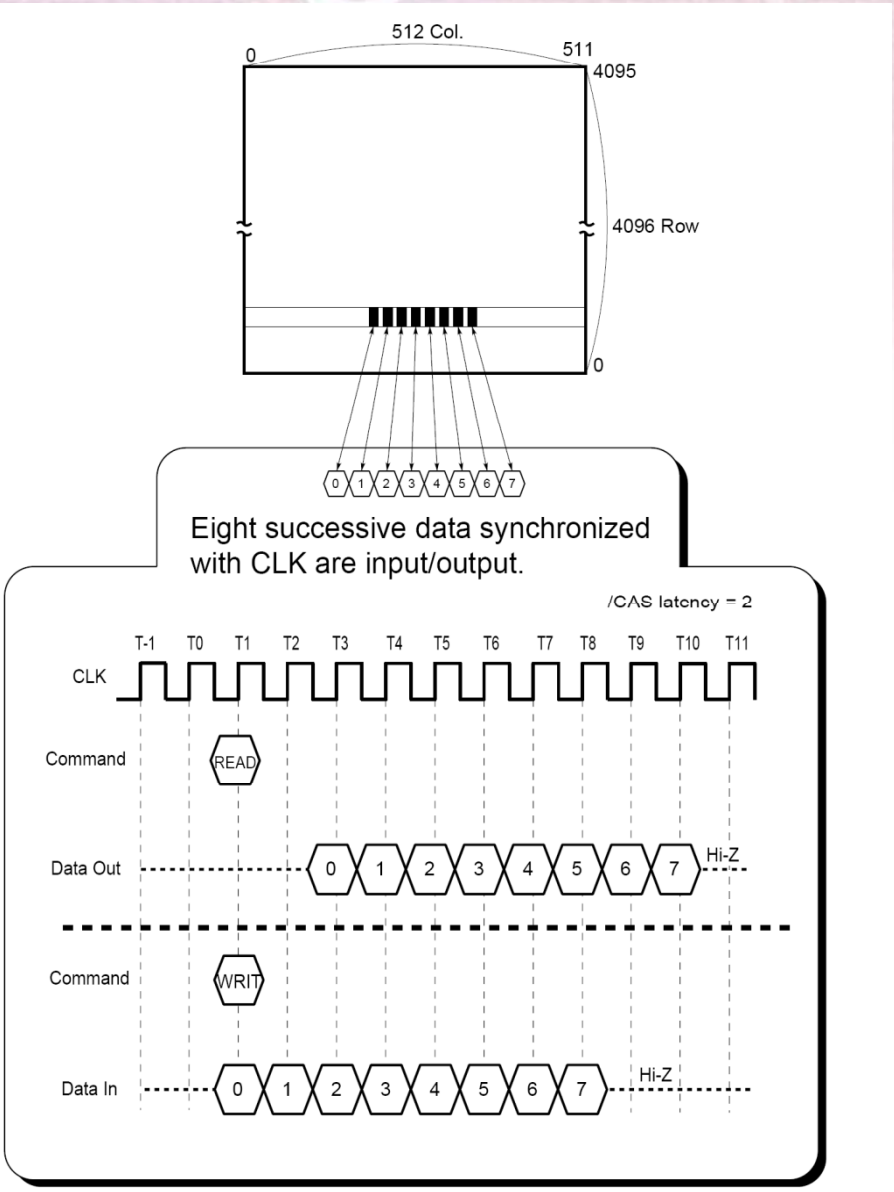


그림. Read/Write Cycle with Burst Length of 8

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# BURST 오퍼레이션

**[Burst length = 2]**

| Start Address<br>(column address A0, binary) | Sequential Addressing Sequence<br>(decimal) | Interleave Addressing Sequence<br>(decimal) |
|---|---|---|
| 0 | 0, 1 | 0, 1 |
| 1 | 1, 0 | 1, 0 |

**[Burst length = 4]**

| Start Address<br>(column address A1 through A0, binary) | Sequential Addressing Sequence<br>(decimal) | Interleave Addressing Sequence<br>(decimal) |
|---|---|---|
| 00 | 0, 1, 2, 3 | 0, 1, 2, 3 |
| 01 | 1, 2, 3, 0 | 1, 0, 3, 2 |
| 10 | 2, 3, 0, 1 | 2, 3, 0, 1 |
| 11 | 3, 0, 1, 2 | 3, 2, 1, 0 |

그림. Burst length and addressing sequence

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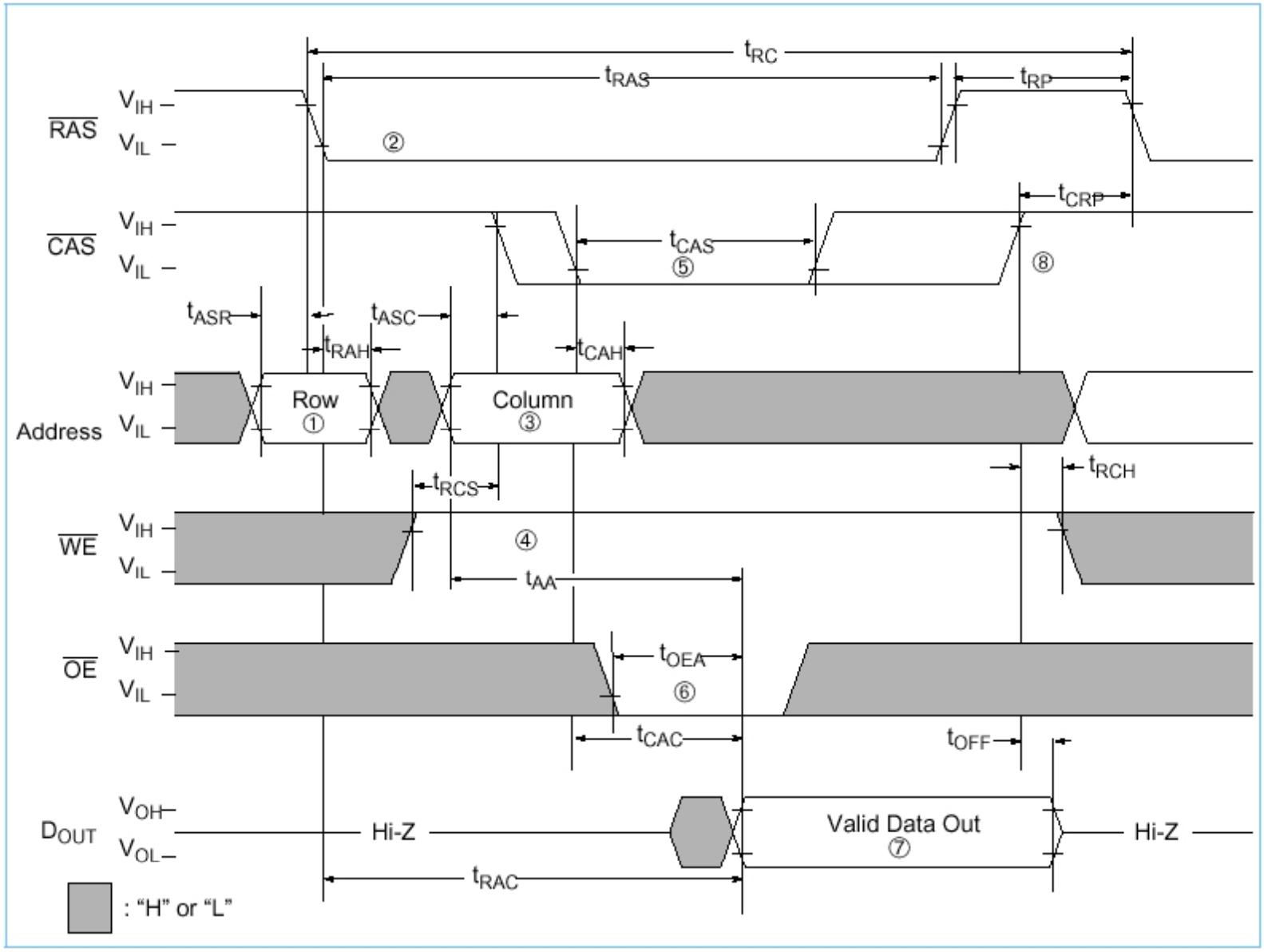
# SDRAM 커맨드 일람

| Command | Symbol | Command Executable (Input) Condition | Remark |
|---|---|---|---|
| Mode register set | MRS | All banks are in idle status. | |
| CBR (auto) refresh | REF | All banks are in idle status. | |
| Self refresh | SELF | All banks are in idle status. | |
| Precharge select bank | PRE | $t_{RAS}$ after active command input (selected bank) | |
| Precharge all banks | PALL | $t_{RAS}$ after active command input (all banks) | |
| Bank active | ACT | Selected bank is in idle status. | |
| Write | WRIT | $t_{RCD}$ after active command input (selected bank) | |
| Write with auto precharge | WRITA | $t_{RCD}$ after active command input (selected bank) | |
| Read | READ | $t_{RCD}$ after active command input (selected bank) | |
| Read with auto precharge | READA | $t_{RCD}$ after active command input (selected bank) | |
| Burst stop | BST | During read or write operation | |
| No operation | NOP | All status | |
| Device deselect | DESL | All status | |

그림. Command Executable Condition

BLACKDOT

# SDRAM 읽기 타이밍


tRC
tRAS
tRP
RAS
VIH
VIL
②
tCRP
CAS
tCAS
⑤
⑧
tASR
tASC
tRAH
tCAH
Address
Row
①
Column
③
tRCS
tRCH
WE
④
tAA
OE
tOEA
⑥
tCAC
tOFF
DOUT
VOH
VOL
Hi-Z
Valid Data Out
⑦
Hi-Z
tRAC
: "H" or "L"

# SDRAM 읽기 타이밍

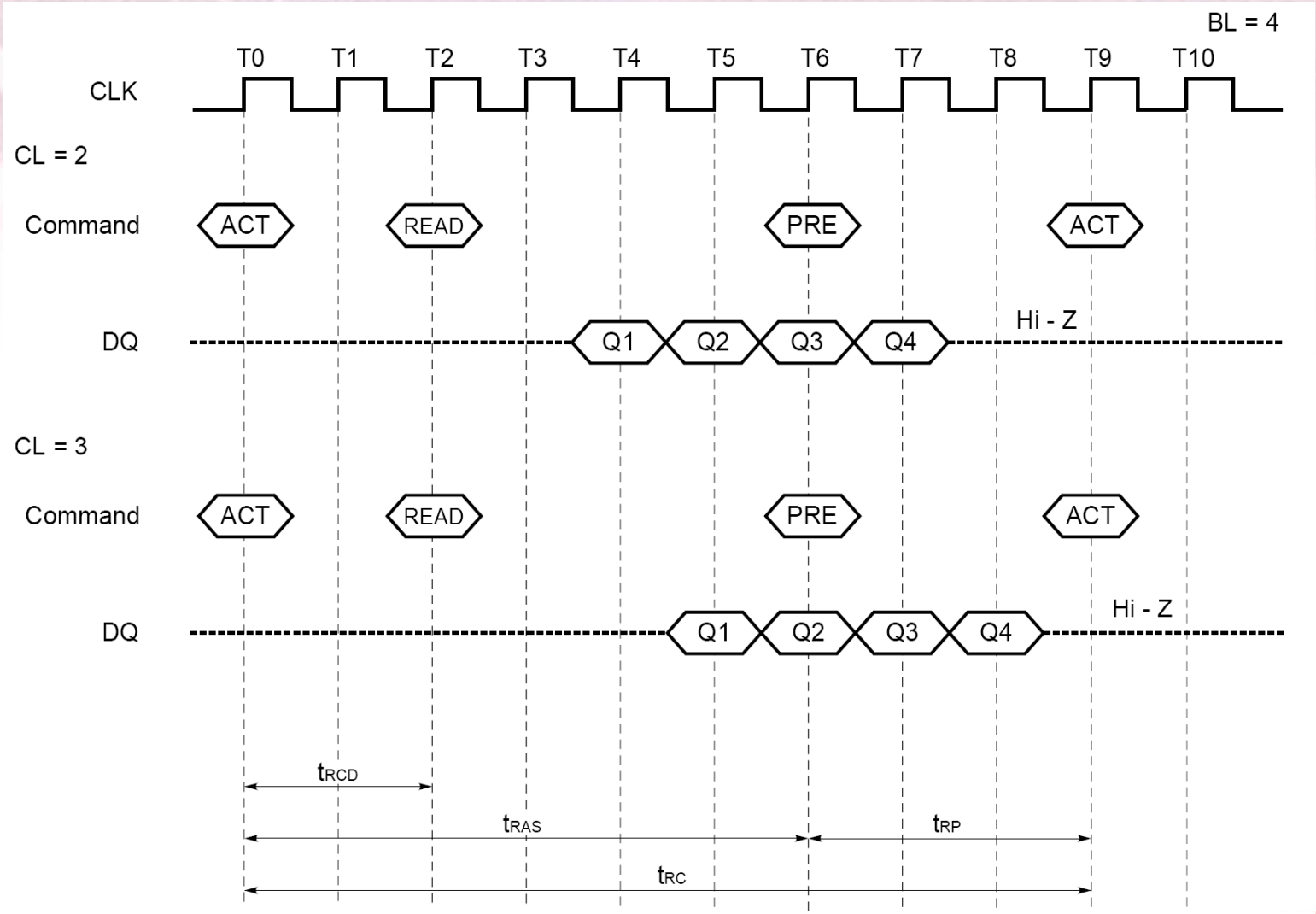



그림. Read Cycle

BLACKDOT

# SDRAM 읽기 타이밍

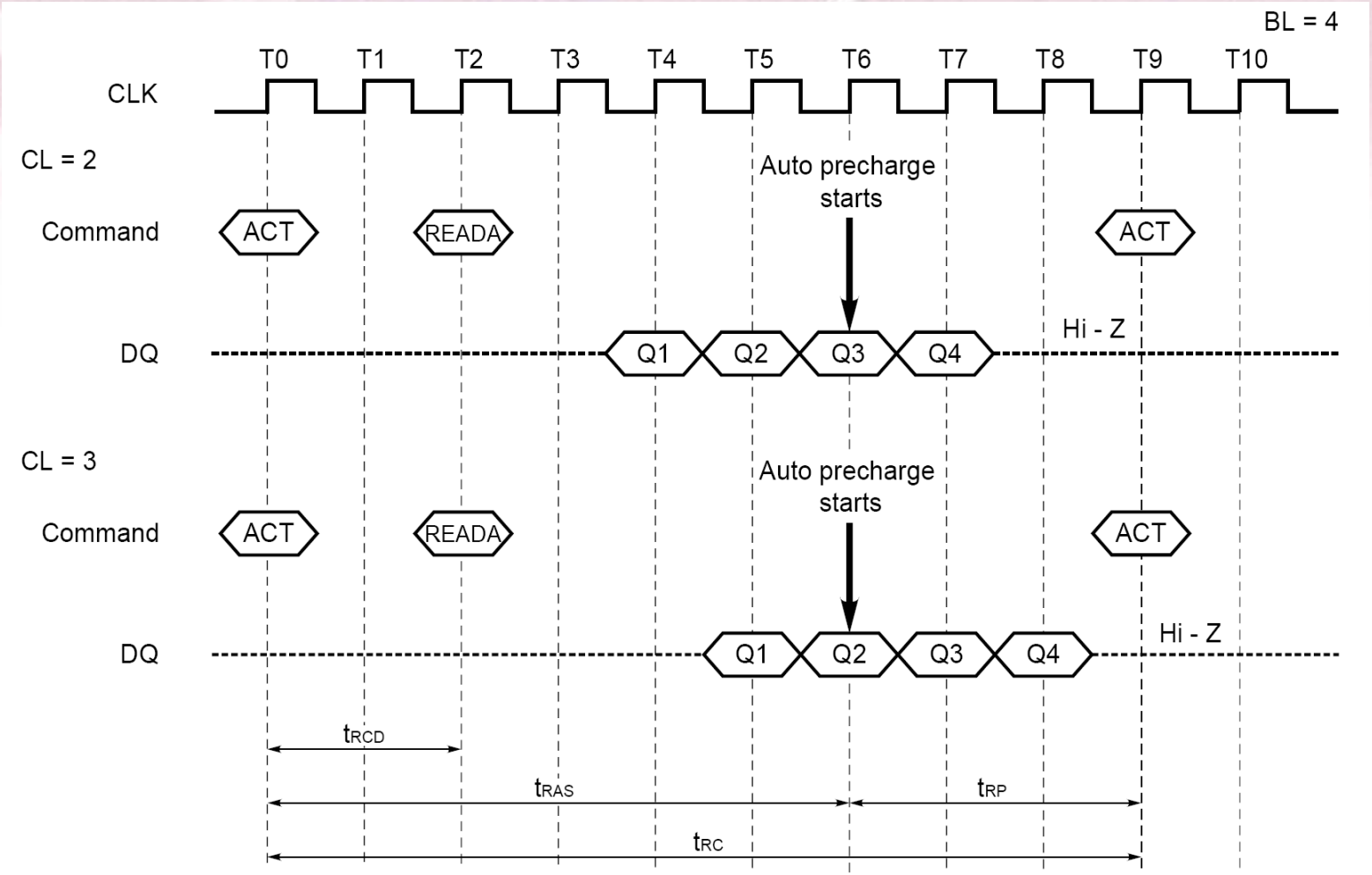
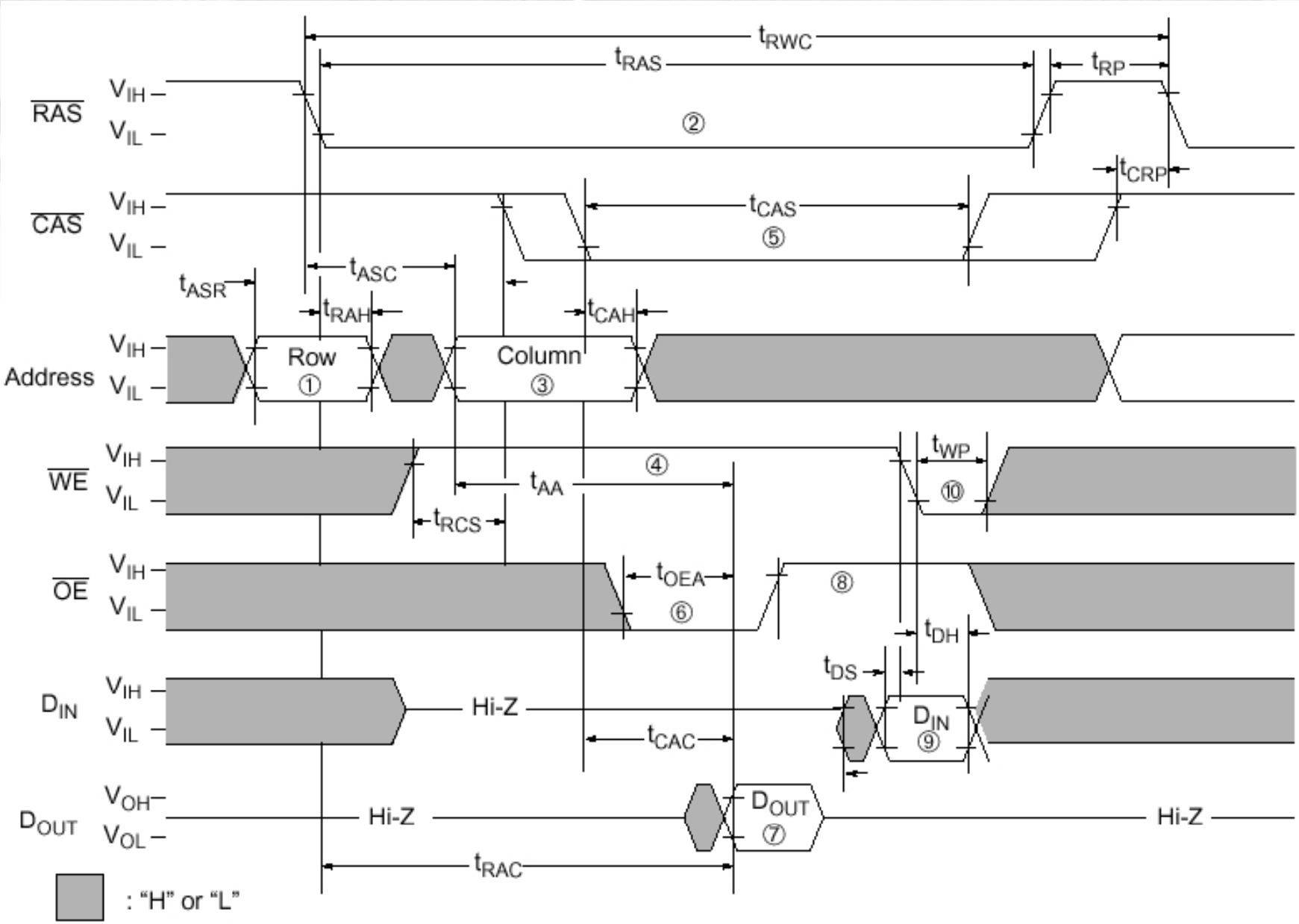



그림. Read Cycle with Auto Precharge

BLACKDOT

# SDRAM 쓰기 타이밍


tRWC
tRAS
tRP
RAS
VIH
VIL
②
tCRP
CAS
tCAS
⑤
tASR
tASC
tRAH
tCAH
Address
Row
①
Column
③
WE
④
tAA
tWP
⑩
tRCS
OE
tOEA
⑥
⑧
tDH
tDS
DIN
Hi-Z
tCAC
⑨
DOUT
VOH
VOL
⑦
tRAC
: "H" or "L"

# SDRAM 쓰기 타이밍

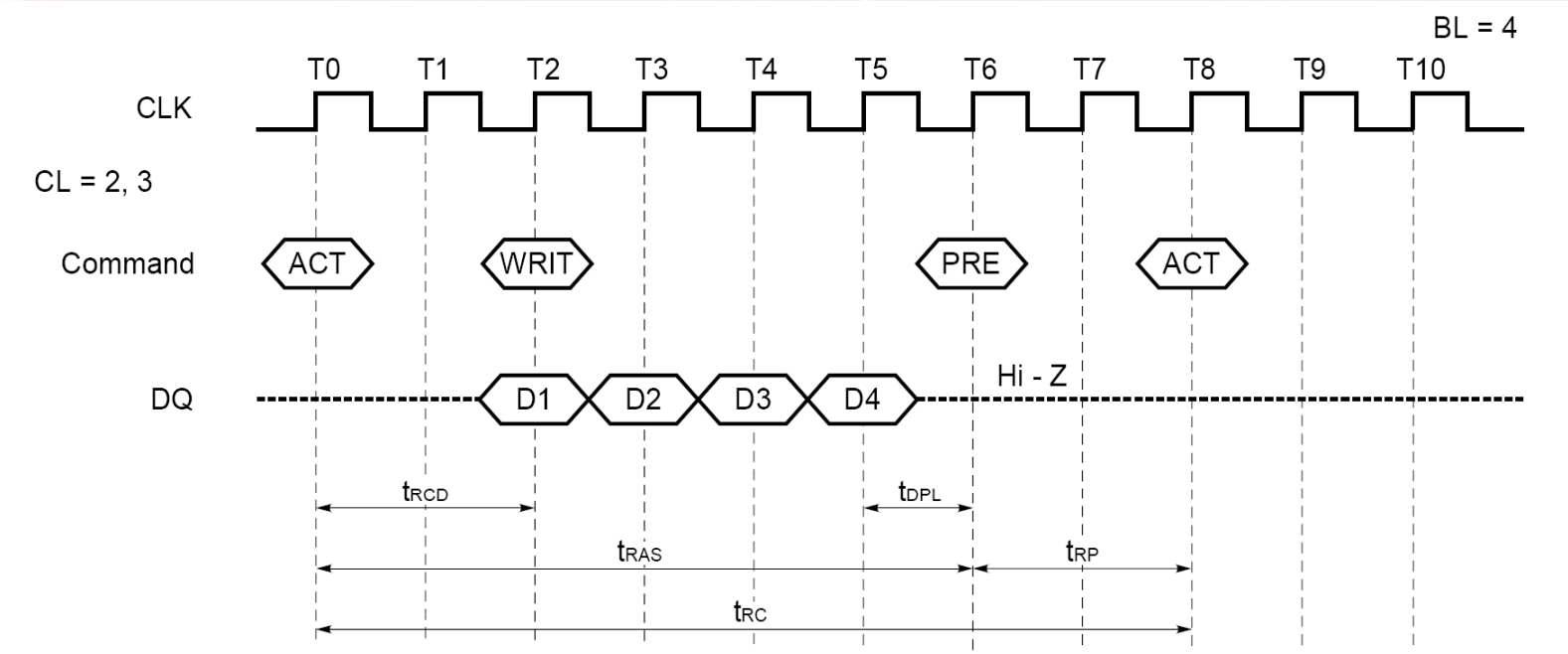



그림. Write Cycle

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# SDRAM 쓰기 타이밍

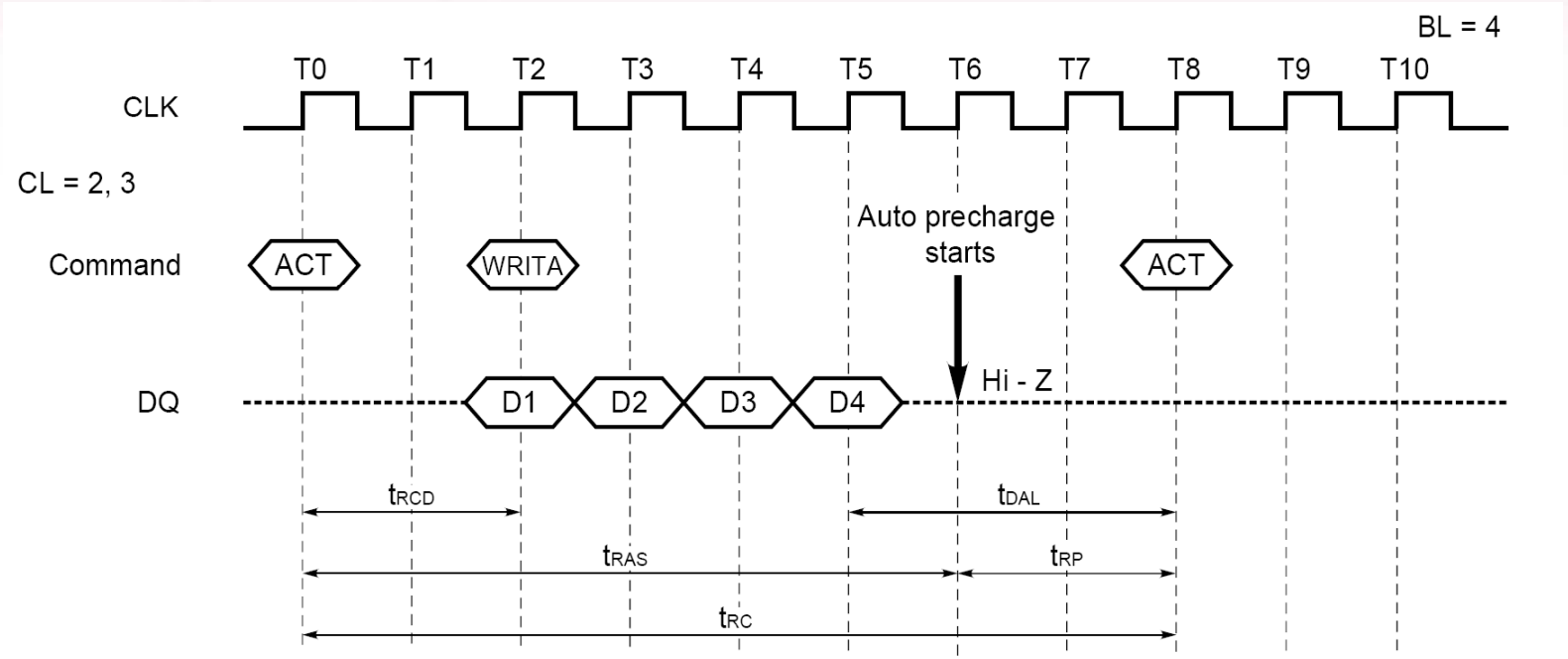


그림. Write Cycle with Auto Precharge

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# SDRAM 리플레쉬 타이밍

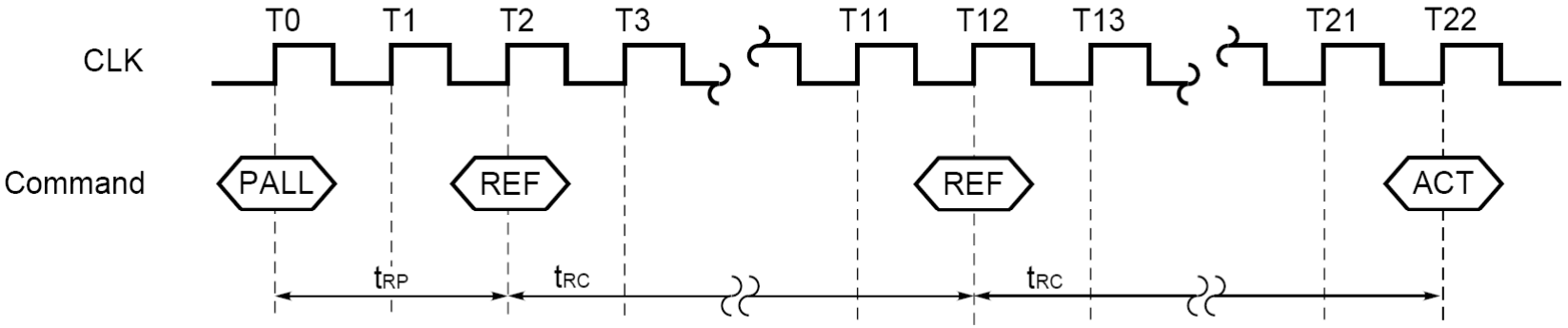


그림. CBR (Auto) Refresh Cycle

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# 주요 신호 분석(DQM)

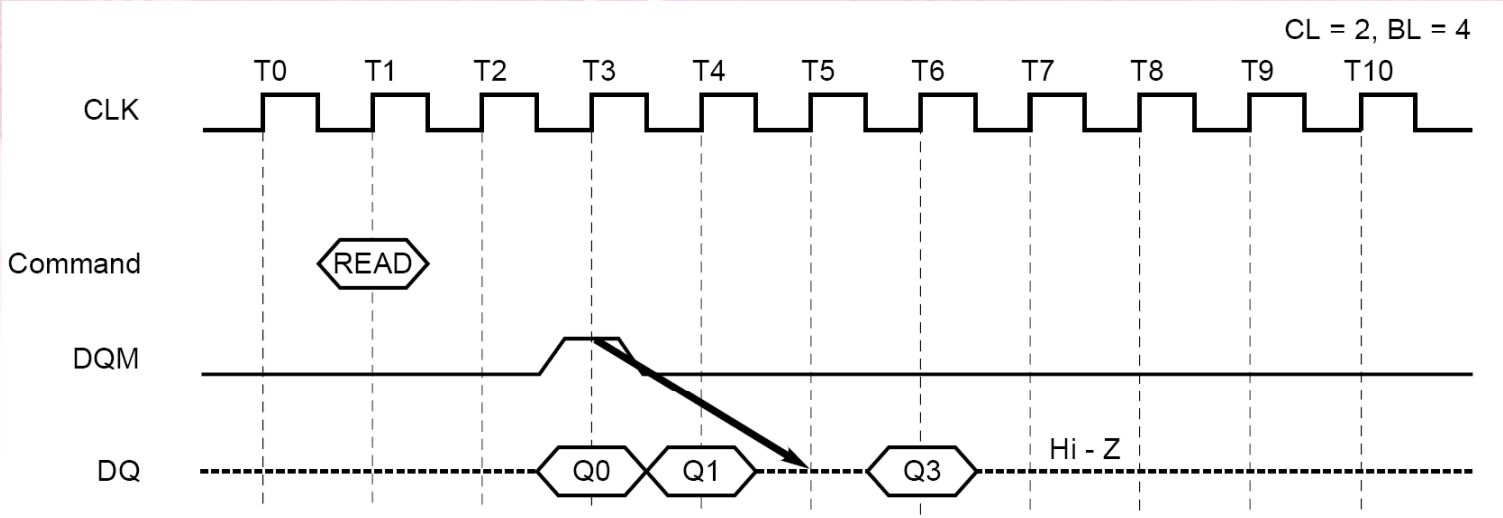


그림. DQM Control during Read Operation

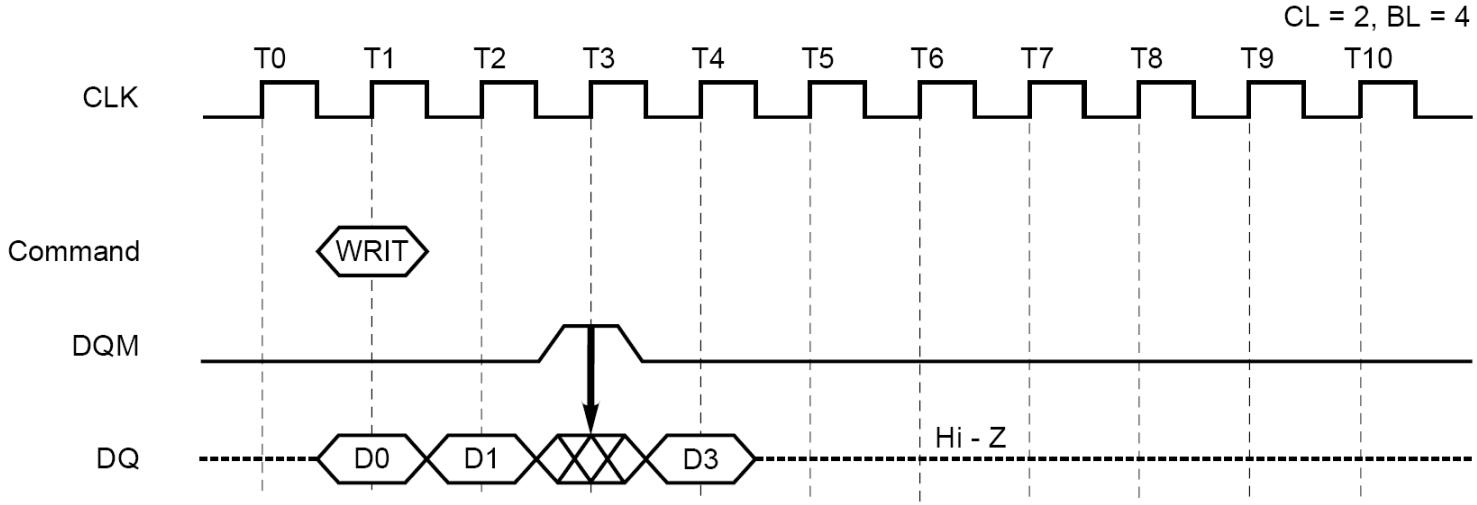


그림. DQM Control during Write Operation

BLACKDOT

# 주요 신호 분석(CKE)

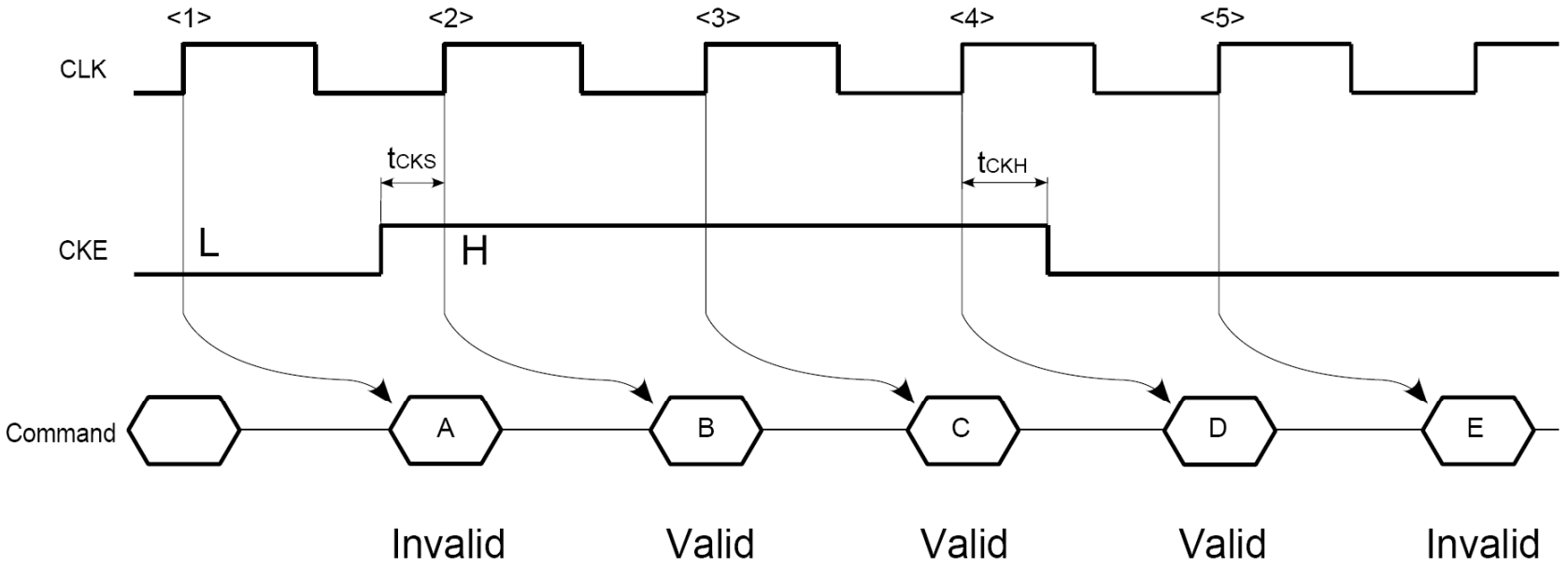


그림. Signal Input Timing Controlled by CKE

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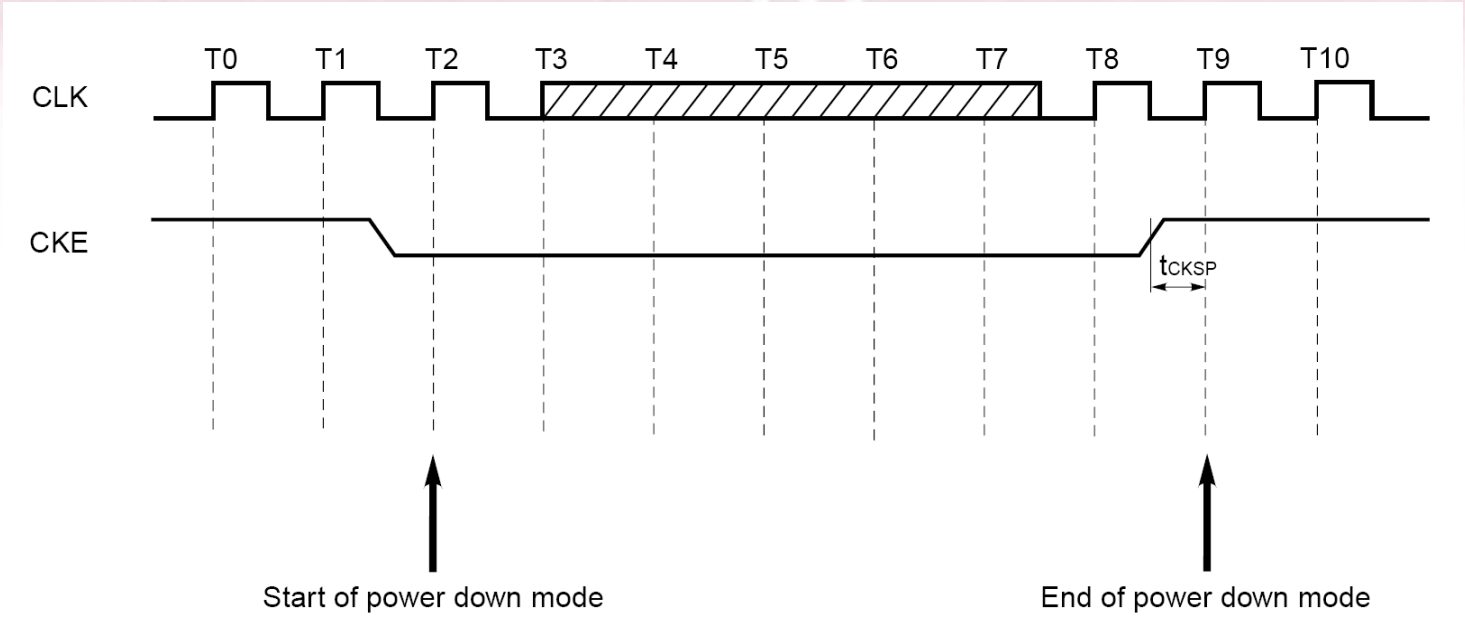
# SDRAM 과 파워다운




**Remarks 1.** Commands cannot be input in the power down mode.

**2.** Make sure that $t_{REF}$ is satisfied.

그림. Power Down Mode

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# SDRAM 과 파워다운

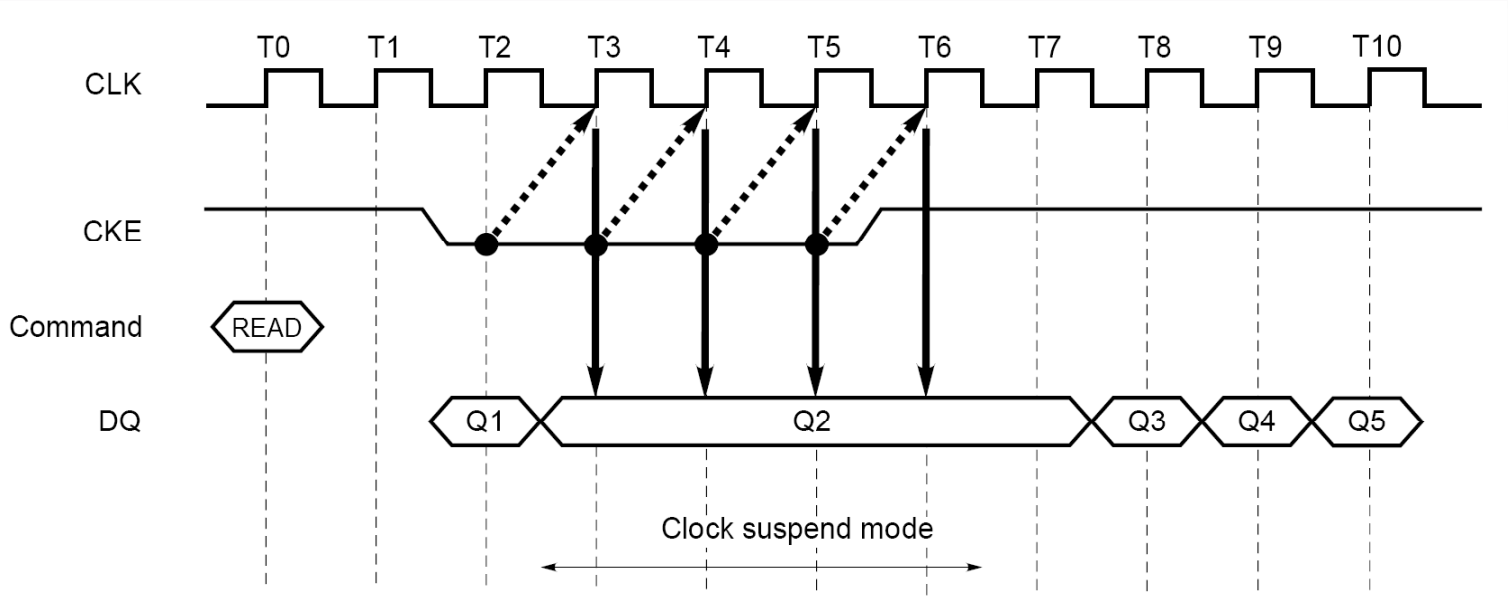


그림. Clock Suspend Mode (read cycle: CL = 2)

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# SDRAM 과 파워다운

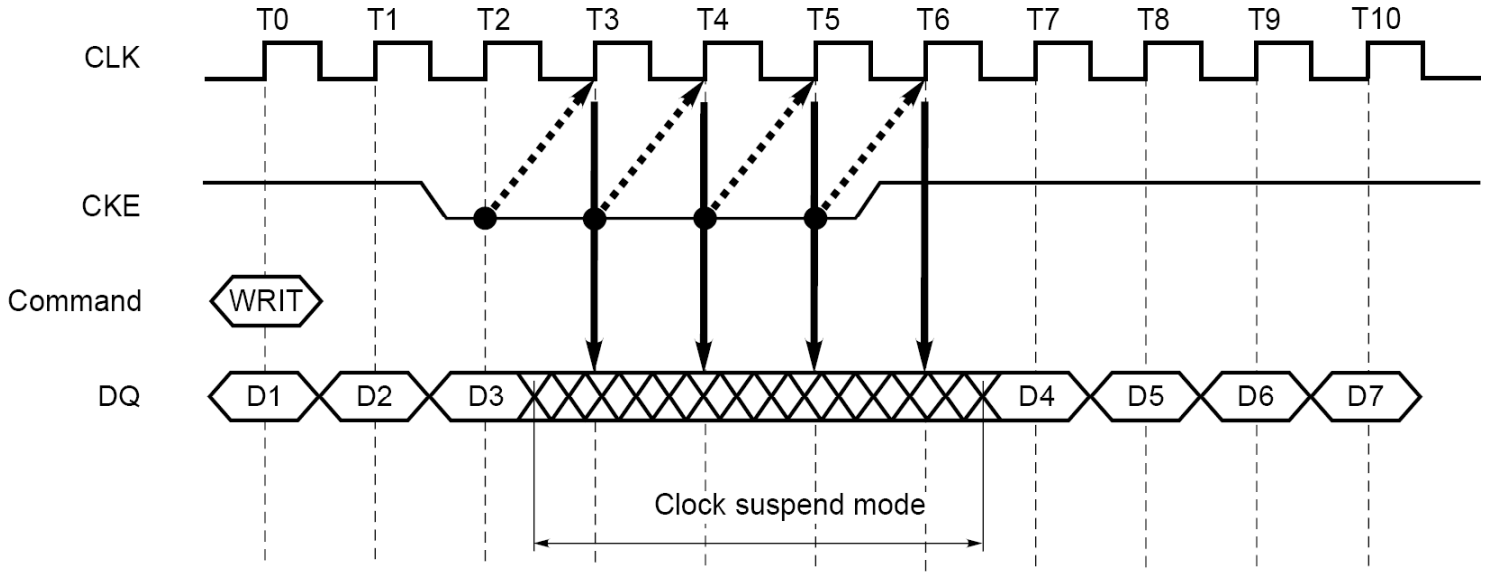
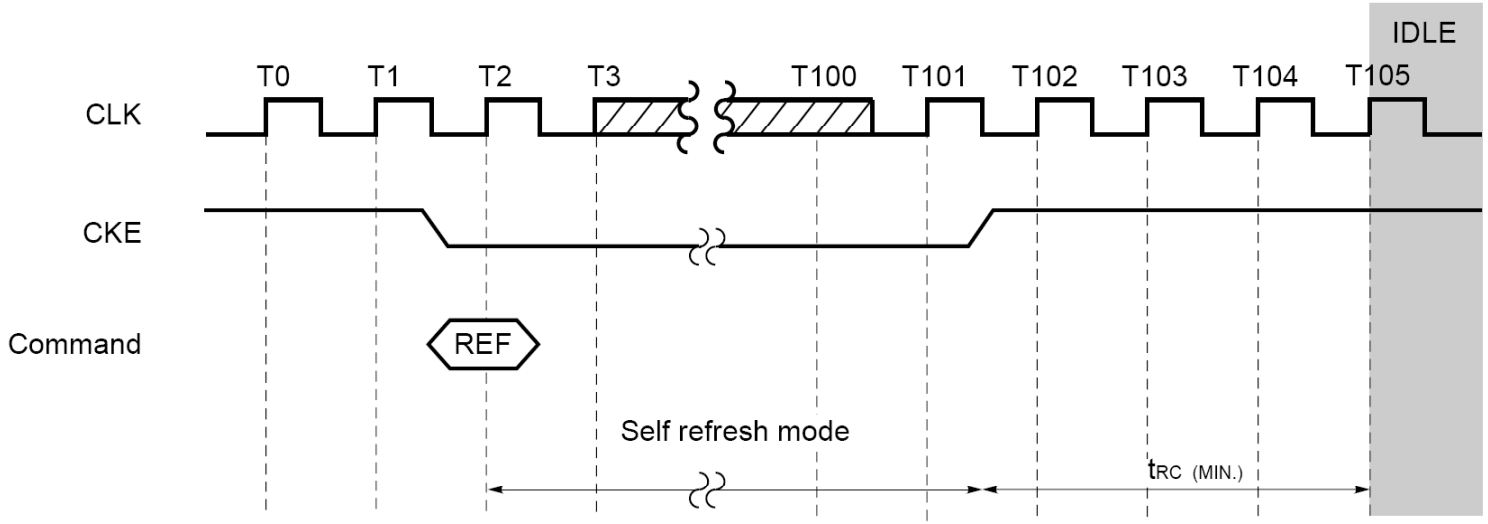



그림. Clock Suspend Mode (write cycle)

BLACKDOT

# SDRAM 과 파워다운




**Caution** **When using concentrated refresh during normal operation, CBR refresh (auto refresh) must be concentrated and executed for the duration of the total number of refresh cycles before and after the self refresh operation.**

그림. Self Refresh Mode

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# 총정리

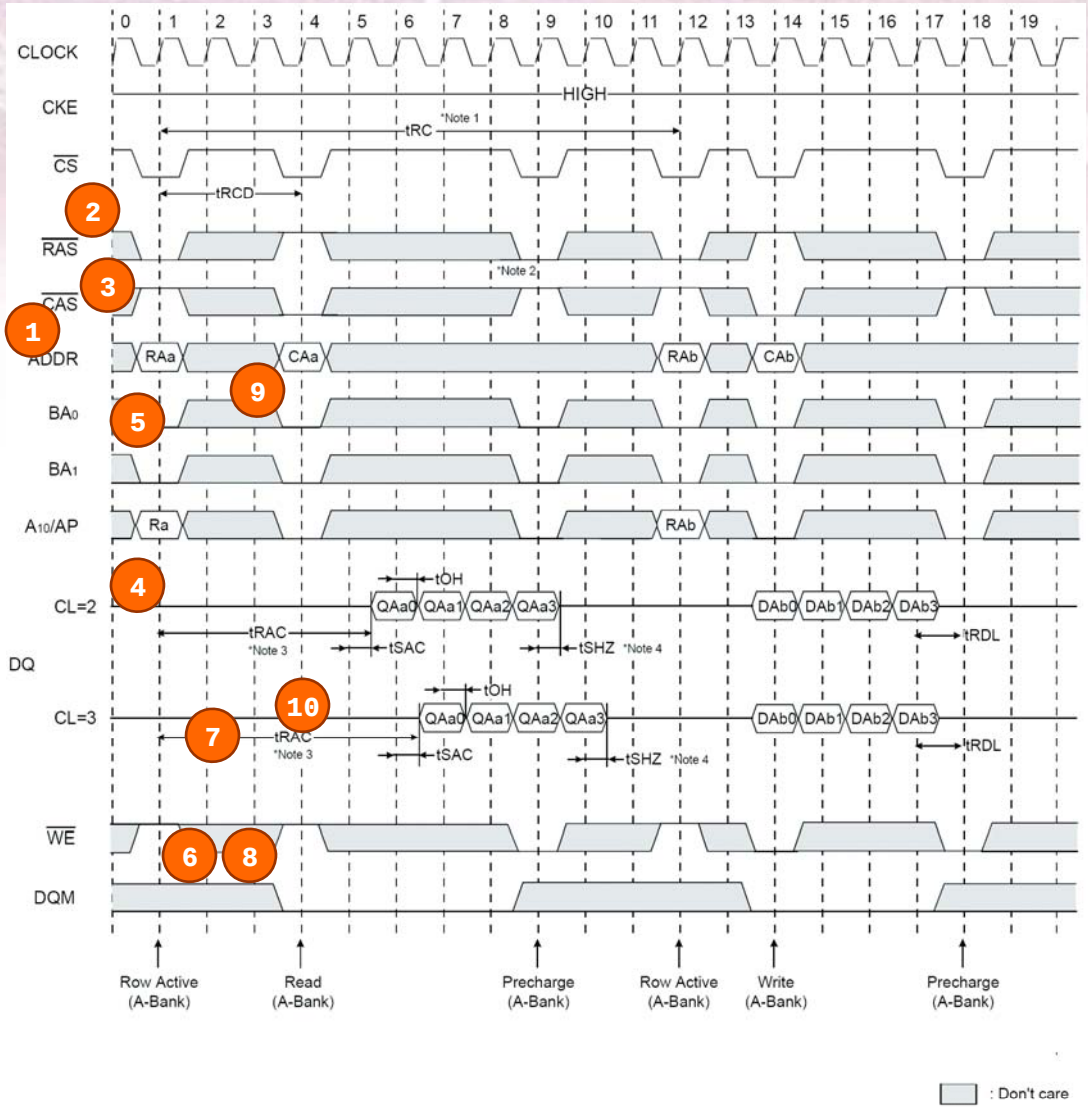


그림. SAMSUNG DATASHEET

BLACKDOT