NVIDIA

there were 10 questions..

4 X 3 marks
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1. room lighting.. room with 100 bulbs and switches..
100 people goes in one by one.
1st person toggles all switches
2nd person toggles all switeches which r multiles of 2 (2,4,6..)
and so on (till 100th person toggling only 100th switch)
once finished with all , which all bulbs r on..

2. ieee single precision format for 1/5.
form : 1 signbit, 8 bits for exponent, 23 bits for mantissa

3. elevator of 60 steps, one kid going up also climbs 15 steps during the upward motion. another kid runs up in the downward elevator and reaches top along with the first kid ?? how many steps are covered by second kid

(answer = 45 + 60 = 105)

4. find the minimal exp for a > b, where a=a0a1 and b=b0b1.

5 X 6 marks..
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5. find an fsm for any no which is divide by 3.

6. one c ++ class prog.. i don't remember it..

7. one digital logic ckt problem. in signal , clk and out signal are given.. give the ckt..

8. one cpu-cache hitting problem..

9. shift register.. (b0b1 selection bits..
00 - shift lft
01 - shift right
10 -
11 - toggles q1 q2 (hint : uinversal shift register)

10th question (8 marks, true or false)
total of 12 questions or so..
questions included on ASIC, HDL, TCP etc..

all the best...

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Hi guys this is nVIDIA paper
nVIDIA is a Graphics solutions (HARDWARE) provider and it also does Chipsets and chips for handheld devices for media processing.
It has started a new design centre in Bangalore this year.

This is the paper of written test conducted by "nVIDIA" at IIT Kharagpur on AUG 10th 2004.

Total 10 Qs (1st aptitude and remaining technical)

Questions carry variable marks. I could not remember the weightage .

Duration: 1 Hr.

1. Question on clocks ---see R.S.Aggarwal (3m)

Between 4:00 pm and 5:00 pm at what time will the hours and minutes hand be 10 degrees apart for the first time.....????

ans: 4:20 p.m.

2.a)Data compression is used for information storage and transmission .

you are to use encryption along with data compression. What will u do

i)Data compression first and then encrypt the compressed data

OR

ii)encrypt the data and then compress the encrypted data

Justify ur answer.

ans :
Compress the data and then encrypt the data.
Reason : 1) Encryption time is proportional to data size. Compressed data size will be less than normal data size.
2) It also hinders cryptanalysis because there's less chance of repeating patterns and moreover, cryptanalysis is always harder when there is less ciphertext to chew on.

b)Give Binary representation of -125.375 in fixed point 2C notation with 3 bits for fractional part and 8 bits for integer part. (4m)

3.Given a 4 bit binary number design a circuit that gives square of the number.

4.Given a 7 bit binary number design a circuit to find the number of 1s (Binary digit 1s) in the number using only Half Adders and Full Adders.

5.write a C functon IsLittleEndian() to return true if the machine stores LSB of a Multibyte number in Highest Address and false if it is the other way (Iam not sure whether it is LSB in Highet addr or MSB in highest Address ,check what is LittleEndian and BigEndian).

6.A question on FSM (lengthy Question 8 lines) I don't remember it .

7.A question on FF timing

Two FFs with combo logic blocks in B/w FF1 and FF2 with different delays and combo block b/w o/p of 2nd FF and i/p of 1st FF (feedback).

setup time ,hold time clock-to-Q delay were given

a)with a SKEW of "DELTA" what will be the

maximum clock frequency (numerical values were given).

b)for a hold time of "HOLD" ns what will be the maximum SKEW allowed????

8.A question on FSM design (it's a ARBITER problem Problem statement was given along with waveforms describing the function) You are required to draw the FSM showing expressions for state changes and output.

9.a) A binary number is enormously large, so it is divided by a fixed number and the remainder is used.What is this called and why it is called so????

b)Give two advantages and one disadvantege of Latch based designs over register based designs.

10.This is a Q from Low power design (circuits)

The technology used for a design is changed from 0.13 Um to 0.09 Um and VDD from 1.2v to 1.0 v.

If Area of a chip is 81mm2 and Power consumed is 1w and maximum frequency is 500 MHz,in the earlier 0.13 Um technology, what will be the Power consumed in the new Technology of 0.09Um and Vdd of 1.0v? what will be the area of the chip? What will be the maximum frequency if the Power consumed is kept same ???

Out of 50 members (attended written test) 8 were shortlisted for interview and 5 were selected for the job.

Interview was cool.

Basics of comp Architecture (those who said that they have learnt Compu arch were asked Qs on Compu arch) , CMOS circuits (transistor realization of Boolean functions), concepts of Pipelining, RC delay calculation, VERILOG (simple no need to panic , just want to know whether you know verilog or not.

to the bulbs question the answer is 10.

the analysis is as follows;

consider the factors of particular bulb excluding 1. first factor represents turning it OFF,second factor represents turning it ON,third factor represents turning it OFF ,fourth represents ON and so on.
1) bulb one is always ON.
2) bulb 2, factors are 2 only. so it is OFF forever.
3)bulb 3, factors are 3, so OFF forever
4) bulb 4,factors are 2,4. so it is ON forever.
like wise if we continue we notice that bulbs which are perfect squares are ON. so bulbs which are ON at the end are

1,4,9,16,...100. so total 10 bulbs. if i am wrong plzz correct me frnds.