CS6560 : Assignment 2

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1 IBM POWER9 :

IBM POWER9 is a collection of superscalar processor with symetric multiprocessing and is based on power architecture(a derivative power ISA) manufacutred by 14nmFinFet technology.

1.1 Processor variants:

- Based on design :
  1. IBM power9 SO : scale out variant with dual socket and Direct attached memmory(8 DDR4 Ports) with upto adaptive 64B/128B reads.
  2. IBM power9 SU : scale up variant based on NUMA architecture with 8 buffered channels and maximum bandwidth of 230GB/s.
- Based on Cores:
  here 4 and 8 are number of slices(a 64-bit processor with single ALU ,Load Store Unit , VSU(floating point and SMID)) and a super-slice is combination of two slices.
  1. SMT4 : 4 way multithreading suitable for Linux Ecosystem and has more virtualisation granularity.it has a 32kb L1 cache with 32kb L1 datacache and an instruction sequencing unit with an instruction fetch unit which gives instrcuions to 2 super-slices.
  2. SMT8 : 8 way multithreading for PowerVM Ecosystem. it has two sets of L1 caches and instruction fetch units and instruction sequencing units to give instructions to 4 super-slices

1.2 ISA and Pipelining:

12 stage pipelining 5 less than power8 processors with fetch to compute by reduced by 5 cycles (as removed the instruction grouping and reduced carcking in pipeline steps). Can complete upto 128 (64 for SMT4) instructions per cycle.

1.3 Cache Memory :

It has L3 cache of sixe 120MB based on shared memory NUCA architecture where each core has 10MB capicity and 512k L2 cache. the cache are 12*20 way cache associative caches are fed by 7 TB/s on-chip bandwidth.

1.4 Stucture of a Core(SMT4) :

- instruction Fecth : 32kb , 8-way instruction cache with 8 fetch and 5 decodes and 1 brach execution.
- Vector scalar units : it has 4x ALU and 4x FP ,2x Fixed divide and 1 Decimal FP and 1 Cryptography units.
- Load store : 32kb 8 way data cache with upto 4 DW load or store

2 AMD RYZEN :

Amd Ryzen branded cpus manufacture by 14nmFinFet technology and are based on Zen cpu microarchitecture created by AMD. Zen is based on SoC design and that allows it to scale from laptop and miniature desktops to large scale servers. It has 40% more IPC than its ancestor cpus and consumes lower power.

2.1 Zen Microarchitecture : Main Features

- fetches upto 4 x86 instructions : has 4-way instruction cache of size 64k
- 4 integer units with large namespace(168 registers)
- 2 load store units : 72 out of order loads supported
- 2 floating point units : has 4 builtin pipes
- 8-way L1-cache of size 32kb
- 8-way L2 cache of size 512kb
- supports SMT with upto 2 threads per core

2.2 Fetch And decpde :

- eatch fecth is 32 byte long and it uses Decoupled Branch Prediction
- The TLB heirachy has 8 entry L0 TLB with 64 entry L1 TLB and 512 entry L2 TLB
- The BTB has 2 branches and are divded into L1 and L2 BTBs
- Instruction cache is 4-way associative of size 64K
- Can decode 4 x86 instructions
- has Op cahe and Micro-op Queue

2.3 Execute :

- has 6x14 entry scheduling queues and 192 entry retire queue
- can execute 6 issue per cycle : 4 ALU , 2 AGU
- 168 entry Register File
- can execute 2 branches per cycle

2.4 Load and Store :

- Can handle 72 out of order loads
- 64 entry L1 TLB ,1.5K entry L2 TLB
- Data caches are 8 way of size 32kb

2.5 Cahe memory :

- L1 cache uses Write-Back policy
- Private 512k L2 cache
- large L3 cache where L3 is fillled with L2's victims
- Has L2 and L3 data prefetcher

3 INTEL SKYLAKE :

Skylake is the latest processor microarchitecture launched by intel based on 14nmFinFet manufacturing process technology. It has better CPU and GPU performance then its ancestor with lower power consuption. It supports upto 2 threads per core and come with various intel techonologies as intel advanced vectore extension, optane memory,intel hyper-threading technology and has Four-channel DDR4-2666 memory support.

3.1 Fetch and Decode:

- Complex CISC instructions are broken into RISC like micro-ops
- Predecoder handles variable length encoding and parallel decoder can handle upto 5 x86 per cycle.
- Sandy Bridge Predictor is used which is two level predictor and uses BTB for L1 as well as uop caches.
- Sandy Bridge returns a stack predictor with 16 entries.

3.2 Cache Memory :

- 8-way L0 cache with 32 sets
- Instruction Cache : 32K, 8-way L1-I cache , which are shared by two threads running on core
- Data cache : 32k , 8-way L1-D cache with write back policy
- 4-way ,256K unified L2 cache with non-inclusive with write back policy
- LLC : 2MB per core ,upto 16-way associative L3 cache with write back and inclusive.

3.3 Multithreading and SIMD :

- SMT enables two threads to share the pipeline
- its SIMD can process 512 bits of integer ot floating-point data with a single instruction

4 Sources :

- IBM power9 :
  1. Wikipedia
  2. IBM developerworks
- AMD :
  1. Wikipedia
- Skylake :
  1. wikichip.org
  2. Wikipedia