

Custom Stereo Bluetooth Speaker

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Project Overview

This project focuses on designing and building a custom stereo Bluetooth speaker system powered by a class-D amplifier. The amplifier was implemented using the TI TPA3122D2 chip, and the system was characterized through a series of measurements including modulation frequency, THD, frequency response, and efficiency. A demo of the speaker and amplifier circuit can be found here: [Speaker Demo.mov](#).

Materials and Equipment

- TI TPA3122D2 amplifier chip
- BOM components (capacitors, inductors, resistors)
- Agilent DSO6012A Oscilloscope
- Keysight 34461A Digital Voltmeter (DVM)
- Keysight 33500B Series Signal Generator
- 12 V Power Supply
- 3.5 mm Aux Bluetooth receiver module ([Amazon link](#))
- External speakers

BOM

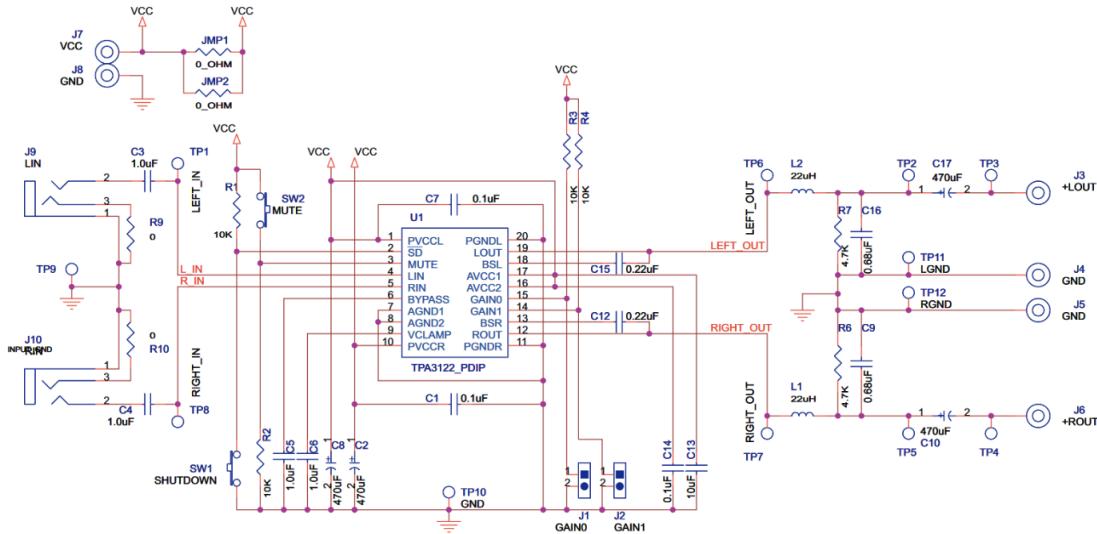
The BOM for the speaker circuit is listed below.

C1, C7	0.1 μ F ceramic capacitor
C2, C8, C10, C17	470 μ F electrolytic capacitor
C3, C4, C5, C6	1 μ F ceramic capacitor
C9, C16	0.68 μ F ceramic capacitor
C12, C15	0.22 μ F ceramic capacitor
C13	10 μ F ceramic capacitor
L1, L2	22 μ H inductor
R1	10 k Ω resistor to VCC, to keep the device on
R2	10 k Ω resistor to GND, to keep the device on

R3, R4	10 kΩ resistor to VCC, for the highest gain
R6, R7	4.7 kΩ resistor
C14	not required

Circuit Schematic

The schematic of the speaker circuit is shown below.



The amplifier is powered through dedicated supply pins for both the analog input stage (AVCC1 and AVCC2) and the power stage (PVCC1 and PVCC2). To ensure stable operation, the design requires decoupling: bulk bypass electrolytic capacitors ($470 \mu\text{F}$) are placed near the PVCC pins to act as a local energy reservoir, supplying transient current to the amplifier and preventing voltage fluctuations during large load changes, while smaller ceramic decoupling capacitors (0.1 and $1 \mu\text{F}$) are placed close to both PVCC and AVCC for high-frequency noise suppression. A bypass capacitor on the BYPASS pin stabilizes the chip's internal bias voltages. In addition, a VCLAMP pin with its decoupling capacitor stabilizes the chip's internal clamp regulator that helps protect the MOSFET gate drivers. Two ceramic bootstrap capacitors ($0.22 \mu\text{F}$) are also included, connected between each output pin and its corresponding bootstrap pin, enabling proper drive voltage for the high-side NMOS transistors on chip. Note that the decoupling capacitors were soldered as close to the pins as possible.

The input stage accepts left and right audio signals at the LIN and RIN pins. These signals are AC-coupled through input capacitors, which block any DC offset and set the lower cutoff frequency of the system. The gain of the amplifier is configured using two digital pins (GAIN0, GAIN1), which allow selection of fixed gains between 20 dB and 36 dB. The choice of input

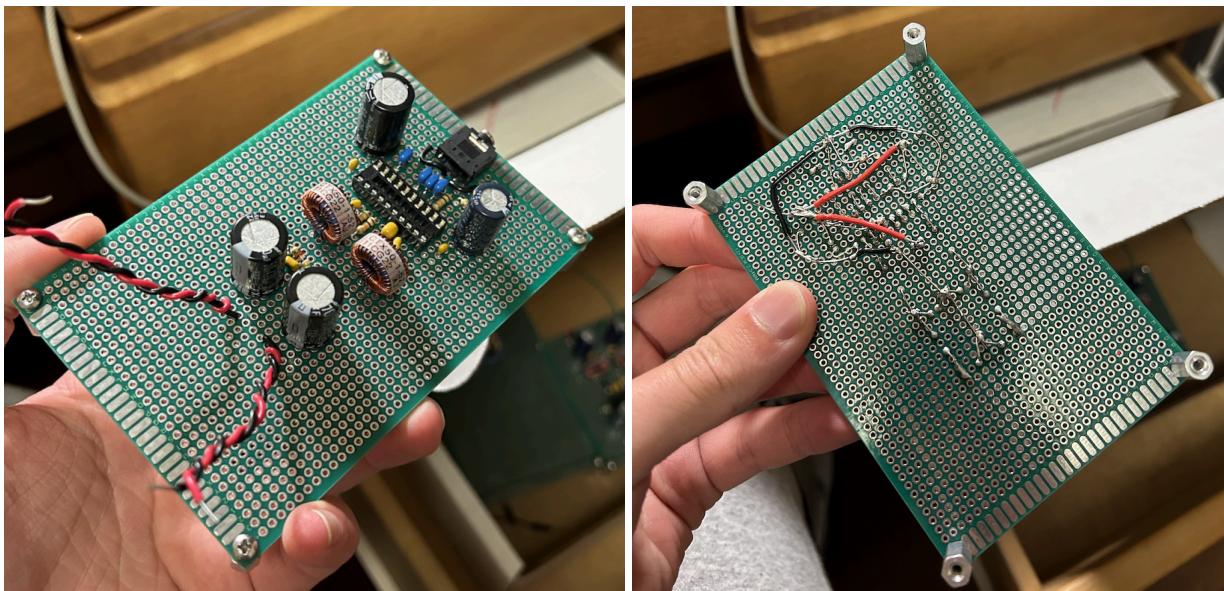
capacitor value, together with the input impedance of the amplifier, determines the high-pass cutoff, ensuring that bass frequencies are preserved.

On the output side, the amplifier drives the load through half-bridge switching outputs (L_{OUT} and R_{OUT}). Since the raw PWM signal must be filtered into a smooth analog waveform, each output is passed through an LC low-pass filter. The inductors and capacitors in this stage are chosen based on the load impedance of the connected speakers and are responsible for attenuating the high-frequency switching components while passing the audio band. In single-ended configurations, DC-blocking capacitors may also be used to prevent DC current from reaching the speakers.

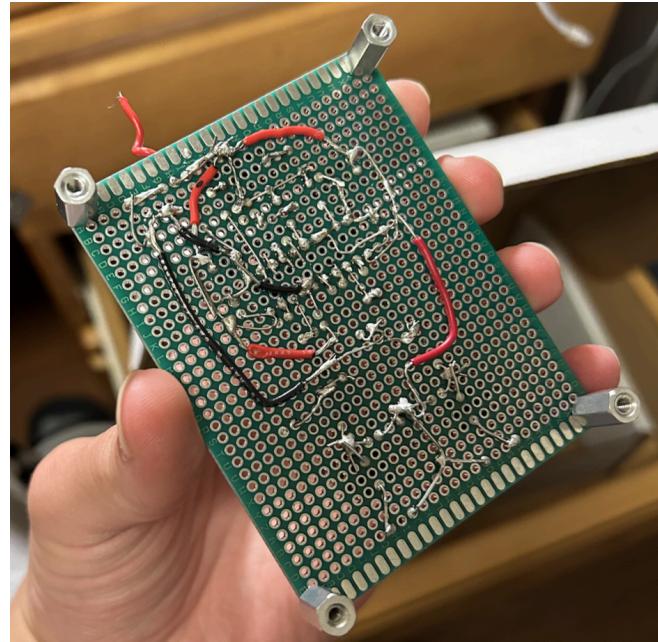
The schematic also includes basic control functionality. A SHUTDOWN pin allows the amplifier to be placed in a low-power state when not in use, while a MUTE pin forces the outputs to a 50% duty cycle to silence audio without powering down the device. Both signals are pulled up and down to defined logic levels to prevent erratic operation. Together with the decoupling, filtering, and protection features, these elements form a robust amplifier stage that can be integrated seamlessly with a Bluetooth audio receiver, enabling the final wireless speaker design.

Final Circuit Board

Pictures of the finished circuit board are shown below.



Shown below is a picture of a failed prototype board. The wiring on the backside is significantly messier, contributing to a harder debugging experience. The issue was eventually traced to a short and poor electrical connections due to the large amount of jumper wires.

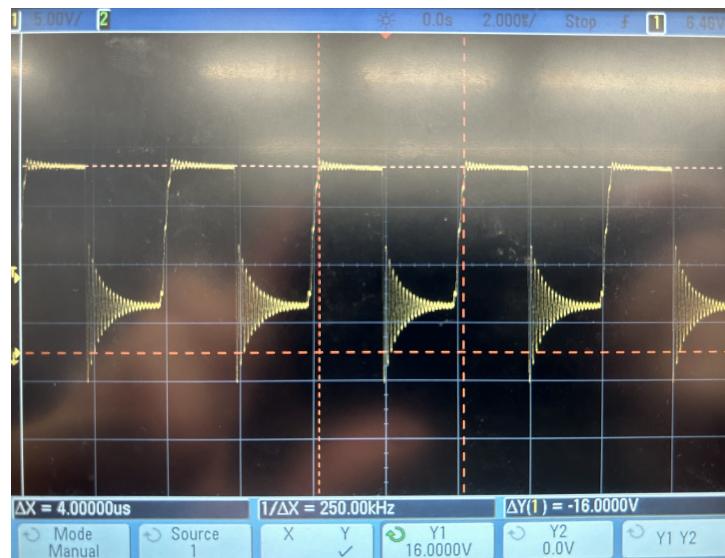


Speaker Measurements

This section outlines the measurements and calculations to verify the speaker circuit's functionality and to determine the THD and efficiency.

Chip Verification

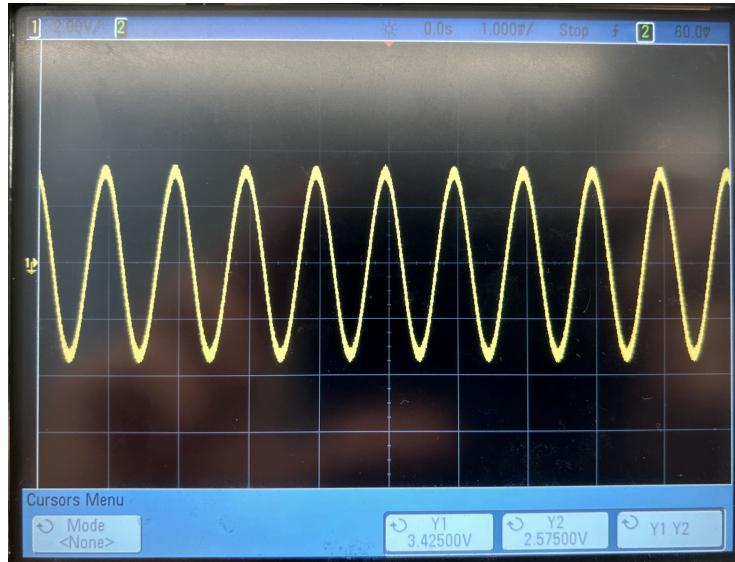
The measured current from the power supply is 17.6 mA.



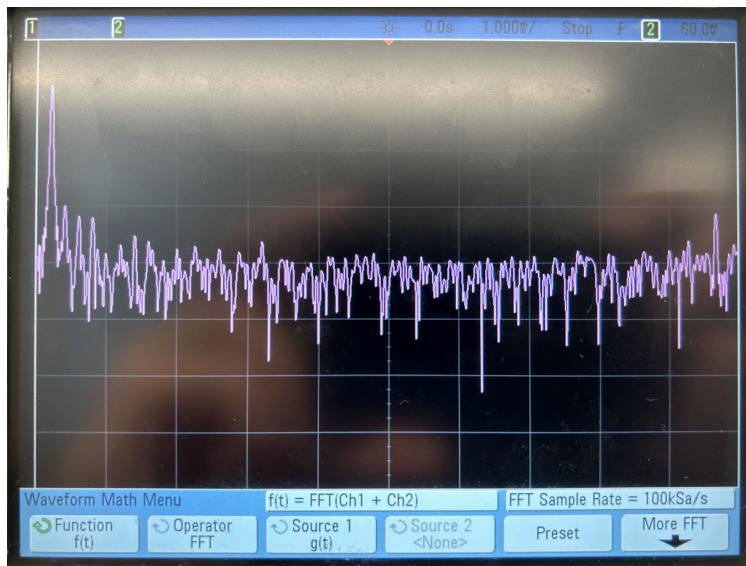
From the oscilloscope trace above, we see that the modulation frequency of the PWM signal is 250 kHz, which is expected for the TPA3122D2 chip.

Total Harmonic Distortion

To measure the THD, we input a 50 mV 1 kHz signal. The output signal of the amplifier is shown below, with a magnitude of about 3 V. So, we get that the amplifier has a gain of 35.6 dB, verifying that we set R3 and R4 optimally to set the gain close to the maximum of 36 dB.



Then, the FFT of the output signal is shown below. We see a spike at 1 kHz as expected, meaning that the output waveform is sufficiently sinusoidal with minimal visual distortion.

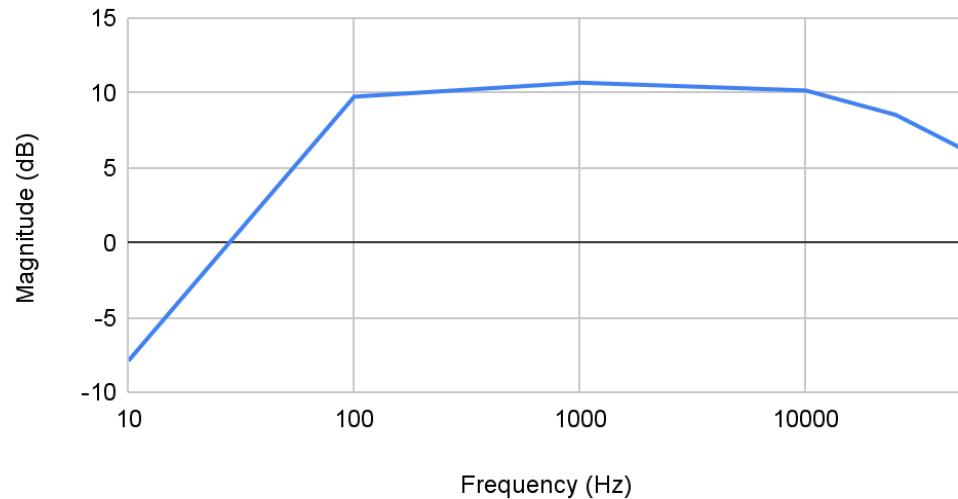


To verify this, we can extract the magnitudes of the first seven harmonics above the fundamental frequency of 1 kHz to approximate the THD. We calculate that the THD is $0.978\% < 1\%$, which is low enough for our purposes.

Frequency Response

To approximate the Bode plot, we can measure the magnitude of the output signal for frequencies swept between 10 Hz and 50 kHz. Then, the Bode plot is shown below.

Magnitude (dB) vs. Frequency (Hz)



We can see that the DC blocking capacitor is effective, since lower frequency signals below 100 Hz are attenuated. The LC filter is also effective, since higher frequency signals above 10 kHz are attenuated, as expected.

Speaker Efficiency

The table below shows supply current, average supply power, output voltage, and average load power. Note that average supply power is given by $P_S = V_{CC} I$ and the average load power is given by $P_L = V_{out}^2 / 2R_L$, where $V_{CC} = 12 \text{ V}$ and $R_L = 10 \Omega$. Then, we get that the efficiency is given by $\eta = P_L / P_S$.

Input Voltage (mV)	Efficiency
50	55.5%
60	64.2%
70	69.3%

We get that the efficiency of the amplifier is somewhere between 55% to 70% for various input signal magnitudes.