Luke Qiao

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EDUCATION

Stanford University **Stanford, CA**
BS/MS, Electrical Engineering (GPA: 4.07/4.0) *Sept 2023 – Jun 2027*

TECHNICAL SKILLS AND INTERESTS

Analog: Analog Circuit/IC Design, RF, PCB Design, KiCAD, Altium Designer, LTSPICE, HSPICE, Signal Processing, DSP
Digital: Digital System Design, Verilog, SystemVerilog, Xilinx Vivado, Synopsys EDA Tools, FPGA, Design Verification
CS: Python, Machine Learning, MATLAB, Linux, Computer Vision, C/C+, Java, ROS 2, Robotics, Robot Autonomy, Gazebo

EXPERIENCES

Sandia National Laboratories **Jun 2025 – Dec 2025**
R&D Intern / Co-op, III-V Microelectronics Group *Albuquerque, NM / Remote, CA*

- Led the design of a proof-of-concept rad-hard **RF amplifier** PCB using LTSpice, Keysight ADS, and Altium Designer
- Accounted for stability and **impedance matching**, designed **distributed components** to minimize effect of parasitics
- Achieved a gain of **~20 dB** in the **1-5 GHz range**, meeting required specs and **demonstrating for the first time** that the group's custom HBT technology was capable of RF applications.
- Substantially improved **heterojunction bipolar transistor (HBT)** noise modeling, reducing simulation error by **60%**

Apple **Jun – Sep 2024**
CAD Engineer Intern, Silicon Engineering Group *Santa Clara, CA*

- Built **machine learning (ML) models** in Python to reduce **physical design verification (PDV)** algorithm runtime (**50% decrease**) via optimal CPU allocation; deployed to production as a useful internal verification tool in Apple's design flow
- Developed **multithreaded** heuristic algorithms for efficient automated data collection; trained **neural networks & mathematical models** for PDV runtime prediction **(5% error)**; used predictions in custom CPU **scheduling algorithm**
- Gained technical experience in **VLSI, Verilog**, and **physical layout**; presented project to high-level Apple SEG executives

Stanford Radio Glaciology Research Group **Feb – June 2025**
Undergraduate Researcher *Stanford University*

- Leveraging multistatic **ApRES radar** for ice temperature & bed material estimation and high-res bed topography imaging
- Optimized onboard signal processing; mixed chirped Tx/Rx signals, applied **LPF and FFT** for object depth estimation
- Tested and characterized various **bowtie antenna** designs; deployed **RFoF links** to mitigate coaxial attenuation loss and impedance mismatch; performed **coherent phase-aligned averaging** to enhance SNR across trials

Stanford Student Space Initiative **Nov 2023 – Apr 2024**
Battery Board Co-Lead *Stanford University*

- Co-led the **Battery Board Thermal Circuit** project for SAMWISE, Stanford Student Space Initiative's 2U CubeSat
- Designed & analyzed circuit to regulate battery temp. using MOSFETs for **optimal power efficiency**, met required specs
- Created **PCB** schematic and layout in **KiCad**; simulated behavior in **LTSpice**; automated trace layout with **Python scripts**

SELECTED PROJECTS

SIMD Matrix Multiplication Accelerator | *SystemVerilog, Hardware Accelerators, Optimization, Synopsys Design Compiler*

- Built and optimized a **SIMD matrix multiplication accelerator** in **SystemVerilog** with **~4x** throughput via parallel MACs
- Optimized datapath using **pipelining** and **multiplier reuse**, resulting in a **85% decrease** in FoM from unoptimized baseline
- Synthesized using **Synopsys Design Compiler** and validated functionality with cycle-accurate **Python simulation model**

Custom CMOS Operational Amplifier | *Analog IC Design, LTSpice, Differential Amplifiers, PVT Robustness*

- Designed a **custom CMOS op-amp** in **LTSpice** with a **differential input stage** with differential-to-single-ended conversion, buffers, and amplification stages, achieving **~70 dB open-loop gain**, wide bandwidth, and **~120 dB CMRR**
- Implemented **sound analog circuit design practices** with **PVT-robust** biasing networks and multi-stage architecture, ensuring consistent operating points, stable open-loop gain, and preserved frequency response under variations

Custom Stereo Bluetooth Speaker | *Analog Circuits, ICs, FFT, Soldering, Oscilloscope*

- Engineered **stereo bluetooth speaker** from scratch; created a **class-D amplifier** to drive two speakers, with input signal via bluetooth receiver (achieved **< 1%** total harmonic distortion); designed custom **AC-DC converter** power brick
- Evaluated performance through **analog circuit analysis** and validated calculations from **oscilloscope** measurements
- Developed proficiency in soldering, oscilloscopes, multimeters, power supplies & function generators

HONORS AND AWARDS

- Professional Society Award Winner, Society of American Military Engineers
- 1st Place, California Science and Engineering Fair
- American Invitational Mathematics Examination Qualifier (Top 2.5%), Mathematical Association of America