**Progress report: cp2**

ROB size: 16

Instruction queue size: 16

Reservation sizes: 4x4

CDB:4 x struct.

Collapsed queue

ROB, RENAME, RS: leon ku

CDB, Register File, Function Unit: jimmy yu

Decoder, Control\_Rom, Hold\_register, Multiplier integration, Roadmap/progress report: Haoyu Yu

CPU module connect: Group

RVFI JSON: Group

Lint, Synth, Sim Debug: Group

Testing strategy: using testcode and debugging based on the verdi

**Progress report: cp3 (tentative)**

Multiple commits

Multiple fetching for “super scalar” (limited to 2 for simplicity) Circular queue used for ROB, load store queue, instruction queue

Load store queue size:16

Add support for control instructions: Haoyu Yu

Features or functionalities: Ensures that in the event that a branch prediction fails, the processor's state can be rolled back to the state before the branch instruction was executed, and then the instruction is reloaded and executed according to the branch's actual destination

Add support for memory instruction: leon ku

Features or functionalities: make sure the effect of wrong store is manageable.

Integrate cache with competition memory, address unit: jimmy yu

Features or functionalities: Disordered Execution and Data Consistency; Address Calculation and Conflict Detection; Delayed Determination of Memory Addresses; Maintenance of Sequential Memory Execution; Avoiding and Resolving Data Conflicts