National Tsing Hua University
Department of Electrical Engineering
EE4292 IC Design Laboratory
Fall 2018

Homework Assignment #3 **(5%)**

Logic Synthesis for Intensity-weighted Average Filter Engine

Assigned on Oct 18, 2018
Due by Nov 1, 2018

Assignment Description

Perform logic synthesis for the filter engine you designed in Homework #2. An RTL redesign to improve the performance is allowed and encouraged. Be sure that your RTL code can pass all the test pattern in Homework #2. The grading will be based on the following performance index:

A: Total area (shown in report/report_area_weighted_avg_filter_engine.out, e.g.Total area: 35151)
T: TEST_CYCLE (your timing constraint, e.g. 2.6 for a nice implementation)

Performance index (PI)= A*T (e.g. $9.13*10^4$ for the above examples)

The following attached files are provided for this assignment:

File Name	**Description**
HW3/hdl/weighted_avg_filter_engine.v	Empty Verilog file with I/O port definitions only (for reference)
HW3/syn/*.tcl	tcl file for DC scripts
HW3/syn/run_dc.bat	Batch file for running synthesis

For this problem, you need to complete the following missions:

1. Show the logic correctness and synthesizability by delivering a functional module *weighted_avg_filter_engine.v*, and its nLint report file (nLint rule set). You will get 0% for this homework if failing to achieve this requirement.
2. Perform logic synthesis with the provided scripts. Only two script files can be modified: 0_readfile.tcl for adding your self-defined RTL files, and synthesis.tcl for changing the clock

timing constraint TEST_CYCLE (e.g. 10 for 10 ns). Your timing slack should not be negative.

3. For this assignment, we have the following two grading ranks:
   - Rank A – Perform logic synthesis for the Part2 of HW2. (Pass all patterns in Part2)
   - Rank B – Perform logic synthesis for the Part1 of HW2. (Pass all patterns in Part1)

   The grading will be based on your performance index:

$$\text{For Rank A: } \begin{cases} 3\% & if\ \ \boldsymbol{PI} > 2.5 \times 10^5 \\ 4\% & if\ \ 2.5 \times 10^5 \geq \boldsymbol{PI} > 1.3 \times 10^5 \\ 5\% & if\ \ \boldsymbol{PI} \leq 1.3 \times 10^5 \end{cases}$$

$$\text{For Rank B: } \begin{cases} 1\% & if\ \ \boldsymbol{PI} > 8 \times 10^4 \\ 2\% & if\ \ 8 \times 10^4 \geq \boldsymbol{PI} > 3 \times 10^4 \\ 3\% & if\ \ \boldsymbol{PI} \leq 3 \times 10^4 \end{cases}$$

4. Bonus. For Rank A works, 2% will be given to the best work in terms of the performance index, and 1% given to the second best.

Deliverable

1. Synthesizable Verilog *weighted_avg_filter_engine.v* (or others if any), and nLint report file.
2. The two modified synthesis script files: ***0_readfile.tcl*** and ***synthesis.tcl***. The report files for area and timing: ***report_area_weighted_avg_filter_engine.out*** and ***report_time_weighted_avg_filter_engine.out***. The synthesis log file ***da.log***.
3. A text file misc.txt summarizing your Rank, performance index and your A, and T as well.

Delivery File Structure

HW3/

- hdl/
  - ***weighted_avg_filter_engine.v***
  - *Other RTL files(*.v) you use*
- syn/
  - ***0_readfile.tcl***
  - ***synthesis.tcl***
  - ***report_area_weighted_avg_filter_engine.out***
  - ***report_time_weighted_avg_filter_engine.out***
  - ***da.log***
- nLint/
  - ***nLint.rep***
- ***misc.txt***