RATAN LAL BUNKAR

System Integration and Test Solutions Engineer

+886-0975010438 ratanbunkar2@gmail.com

No. 36, Liufu Rd, Luzhu District, Taoyuan City, Taiwan-338.

Professional Summary

System Integration and Test Solutions Engineer with a strong background in New Product Development (NPD) for embedded electromechanical medical devices. Experienced in designing and implementing custom test systems to meet complex product requirements, including BLE-based functionality, timing-critical validations, and system-level compliance testing. Skilled in Python-based test automation, cross-functional collaboration, and regulatory-aligned equipment validation (IQ/OQ/PQ). Passionate about building scalable, low-cost test solutions and continuously improving test coverage, quality, and production readiness.

Work Experience

System Integration and Test Solutions Engineer

SHL Medical • May 2023 - Present

Drive end-to-end system integration and test solution development by defining requirements, collaborating cross-functionally, and ensuring regulatory alignment. Led test fixture design, automation implementation, and failure analysis to support NPD and design transfer activities.

KEY VALIDATION PROJECTS & TECHNICAL ACCOMPLISHMENTS

- Delivered fully automated test platforms to validate BLE-based embedded devices and timing-critical system behavior.
- Implemented ATE-style test solutions using Python, reducing test cost and increasing coverage.
- Developed algorithmic state machines for broadcast timing, margin testing, and protocol verification.
- Programmed test routines integrating BLE, UART, and serial protocols to support production validation.
- Conducted root cause analysis across hardware, firmware, and environmental factors.
- Authored test specs, validation protocols (IQ/OQ/PQ), EURS, SDS, and TMVs.
- Collaborated with NPI and manufacturing teams for DFM/DFA reviews and test optimization.
- Supported validation and debug of SmartHub (BLE data sync), Elexy (motor force timing), and Molly cCap (BLE latency).

Control Systems Engineering Intern

DCM Engineering Products • Mar – Aug 2019

- Learned to program Siemens PLCs using Ladder Logic and Simatic Step 7.
- Gained hands-on experience with HMI dashboards for test control and fault monitoring.
- Supported basic system commissioning tasks during automation upgrades.
- Assisted in creating signal maps and control flow diagrams to understand logic execution.

TECHNICAL SKILL SET

Systems & Engineering Competencies

1. **Requirements & Systems Engineering:** System lifecycle development, stakeholder collaboration, requirements gathering, system design documentation, DFMEA, design transfer
2. **Regulatory Compliance & Standards:** ISO 13485, ISO 14971, IEC 60601, ISO/IEC/IEEE 15288
3. **Modeling Languages & Tools** – SysML (Systems Modeling Language), UML (Unified Modeling Language); System Modeling Software including Enterprise Architect and Catia Cameo

Test Development & Automation

1. **Test Fixture Design & Automation**: Custom test jigs, ATE Test Fixtures, Python-based test automation, Computer-Aided Test Systems (CATS), Test Algorithm Development, State Machines
2. **Test Method Development & Equipment Validation**: Test Method Development & Validation (TMV), fixture qualification, **test protocol writing (IQ, OQ, PQ)**

Test Automation & Debug Tools

1. **Python for Test Automation & Verification:** pytest, unittest, logging
2. **Serial and BLE Communication:** pyserial, bleak, pyshark
3. **Data Logging & Analysis:** sqlite3, sqlalchemy, pandas, openpyxl, csv, json
4. **Signal Processing & Timing Validation:** scipy.signal, numpy
5. **Visualization & Reporting:** matplotlib, seaborn, tabulate
6. **Utility & Integration:** subprocess, threading

Embedded & Control Systems

1. **PLC Programming & Industrial Automation**: Familiar with PLC programming (Ladder Logic, HMI, SCADA), Simatic Step 7

Programming & Scripting Languages

1. **Core Languages & Web Technologies**: Python, C, C++

Memory & Validation Concepts

1. **DRAM Test Flow Understanding:** Validation routines for embedded memory triggers and timing
2. **State Machine–Based Test Logic:** Algorithmic test design for parametric validation
3. **Timing Margin Debug & Characterization:** Signal timing capture and tolerance validation

Data Processing & Analysis

1. **Analytical Techniques & Engineering Insights:**Signal processing, noise reduction, root cause analysis, data visualization, algorithm validation

EDUCATION BACKGROUND

Master's Degree (Electrical Engineering)• Feb 2021- Jan 2023

National Taiwan University of Technology Taipei, Taiwan

Bachelor's Degree (Electrical Engineering)• Apr 2016 - Aug 2020

Indian Institute of Technology, Ropar Ropar, Punjab, India