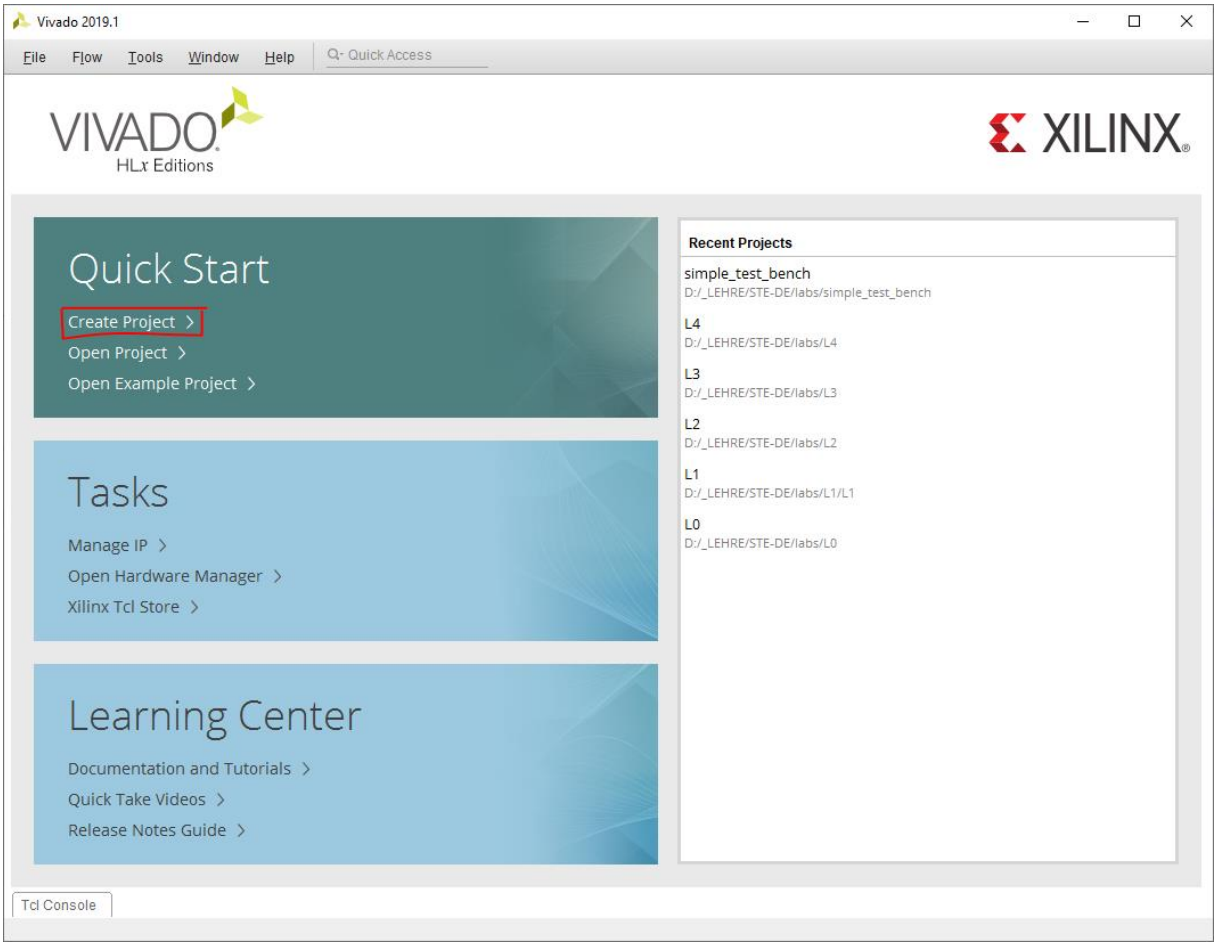
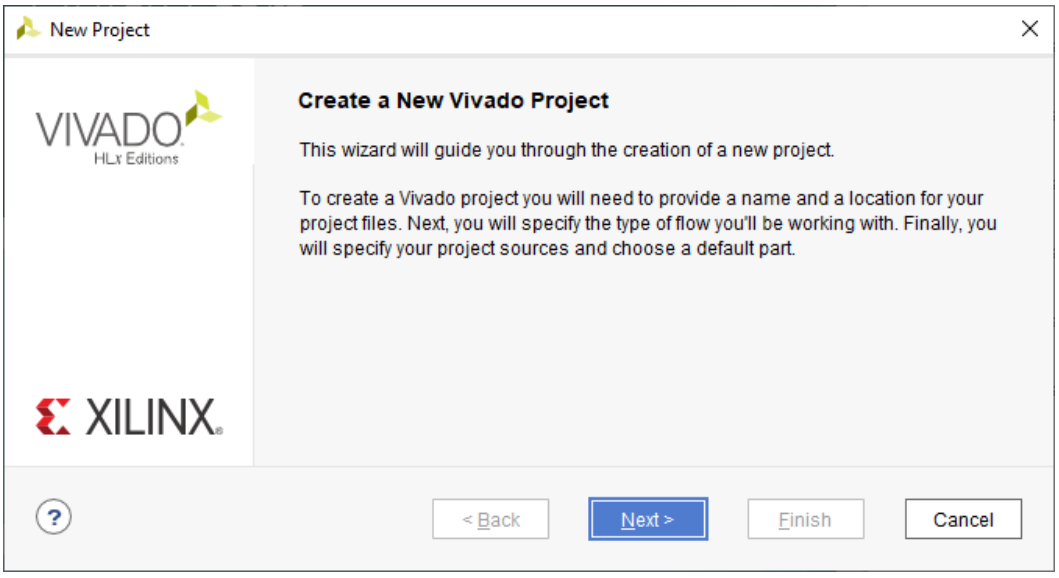
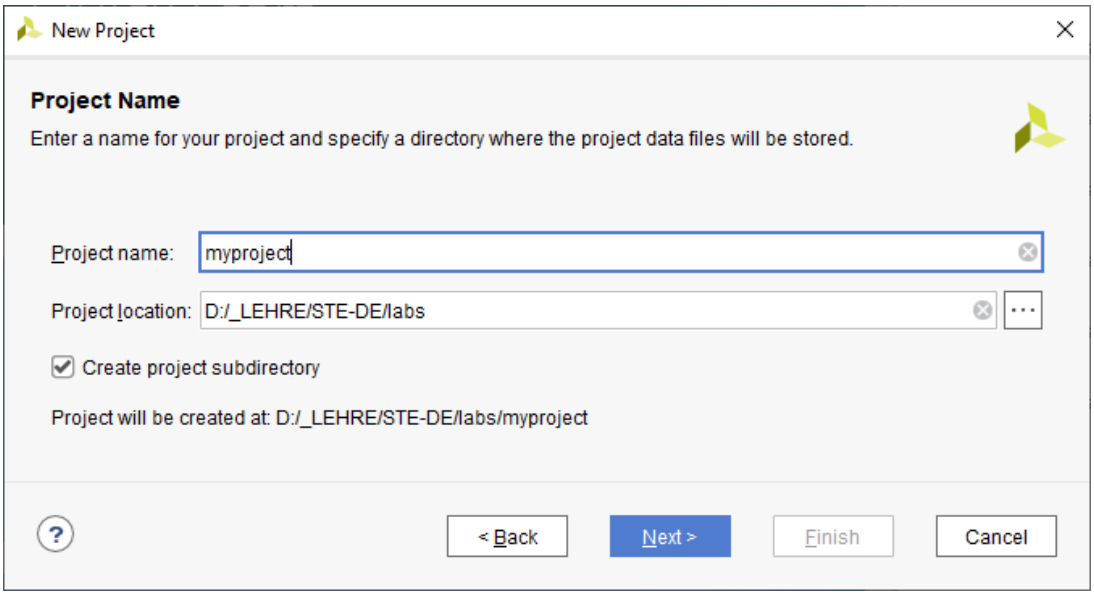
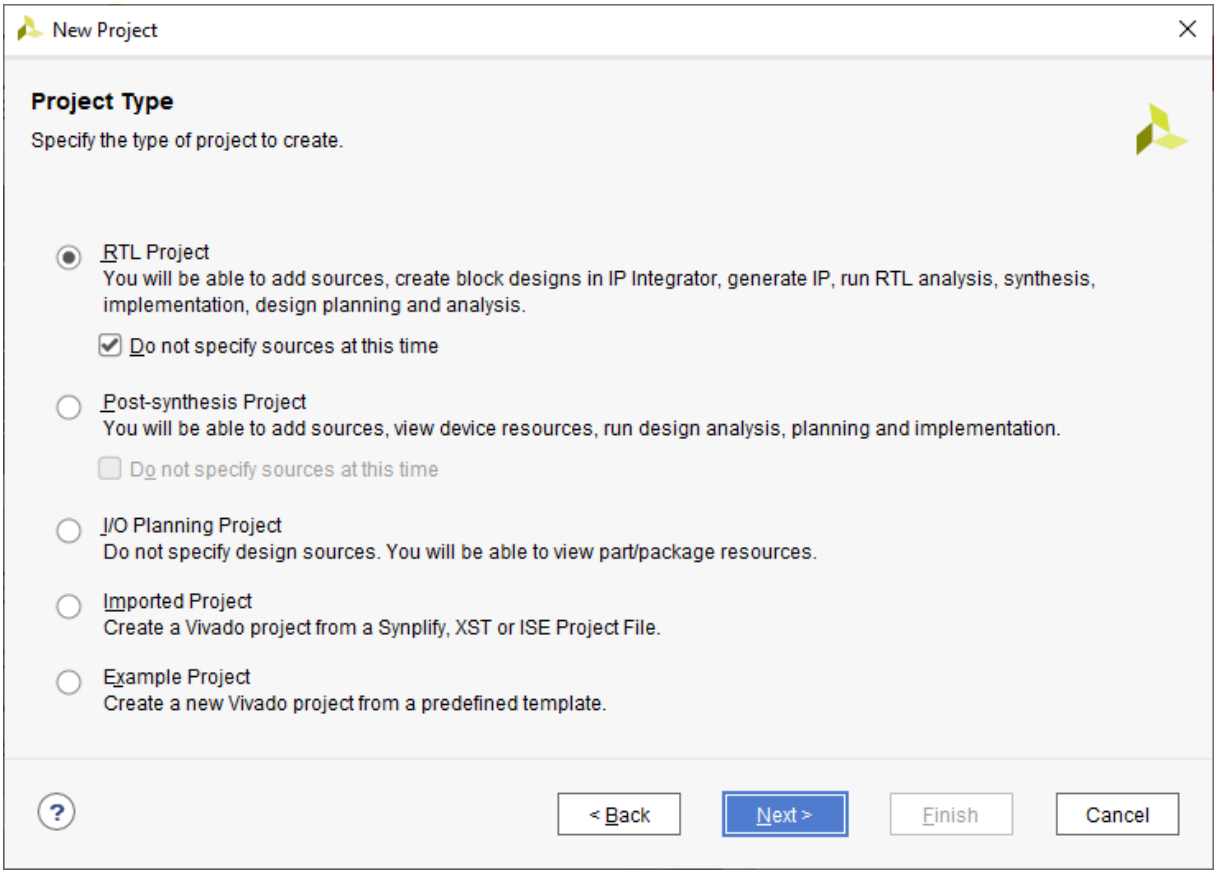
Vivado Tutorial 1 - Simulation

Create Project; name project; don't add source files; choose Basys3 board

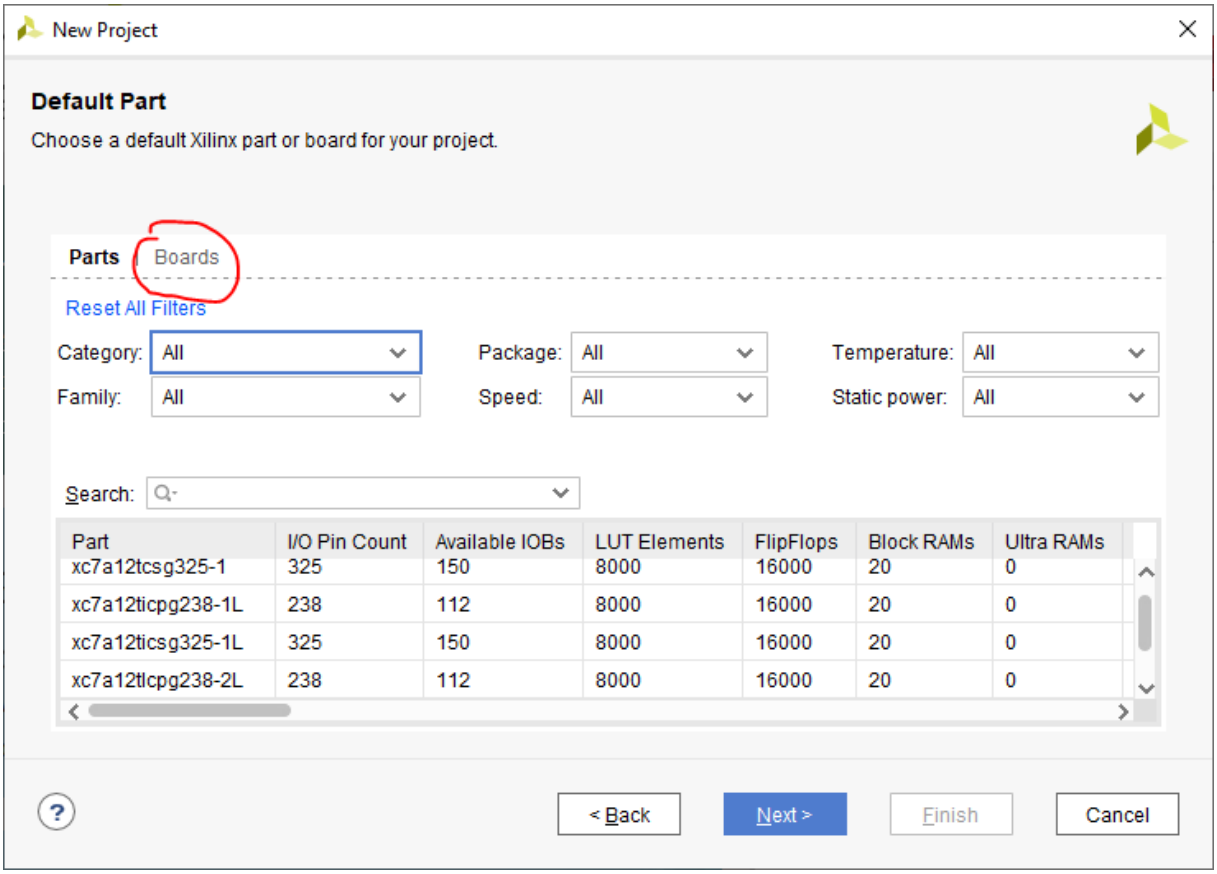


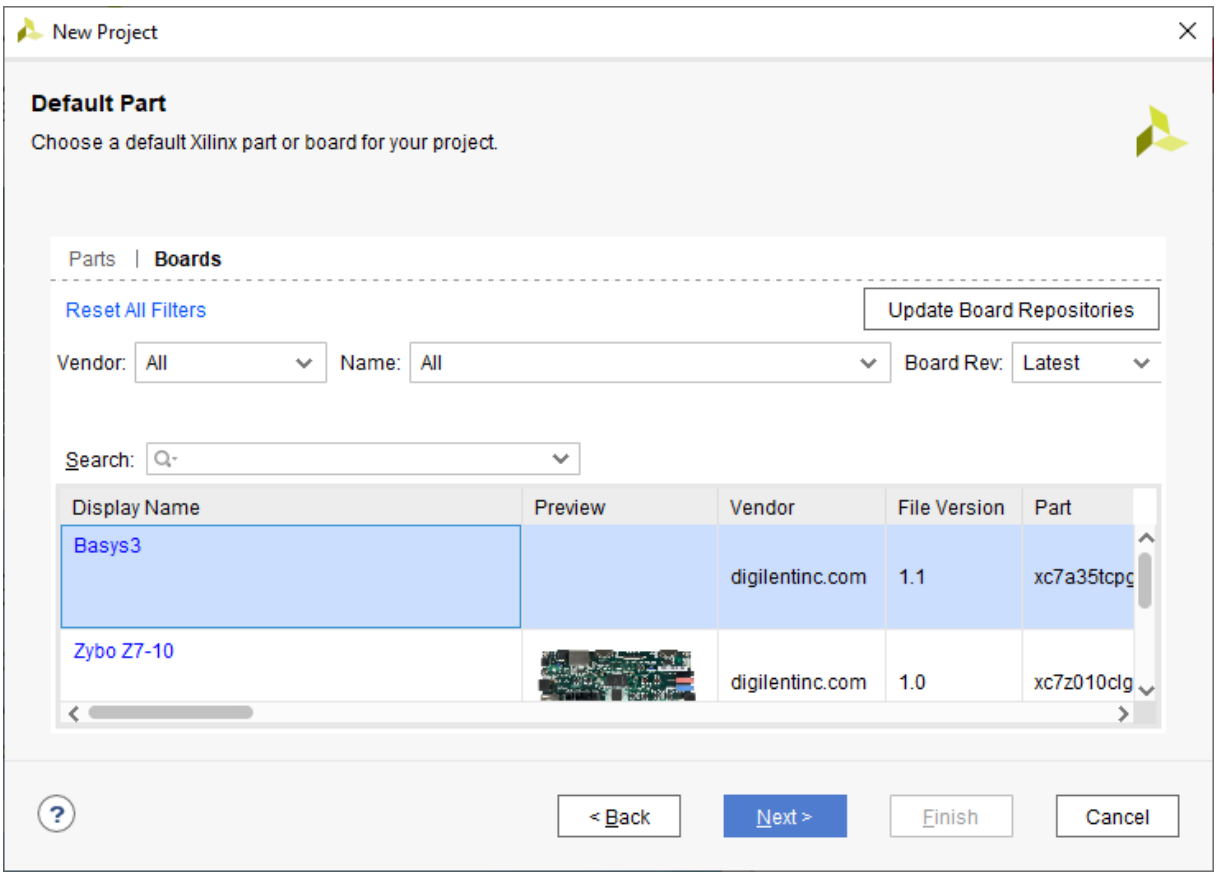


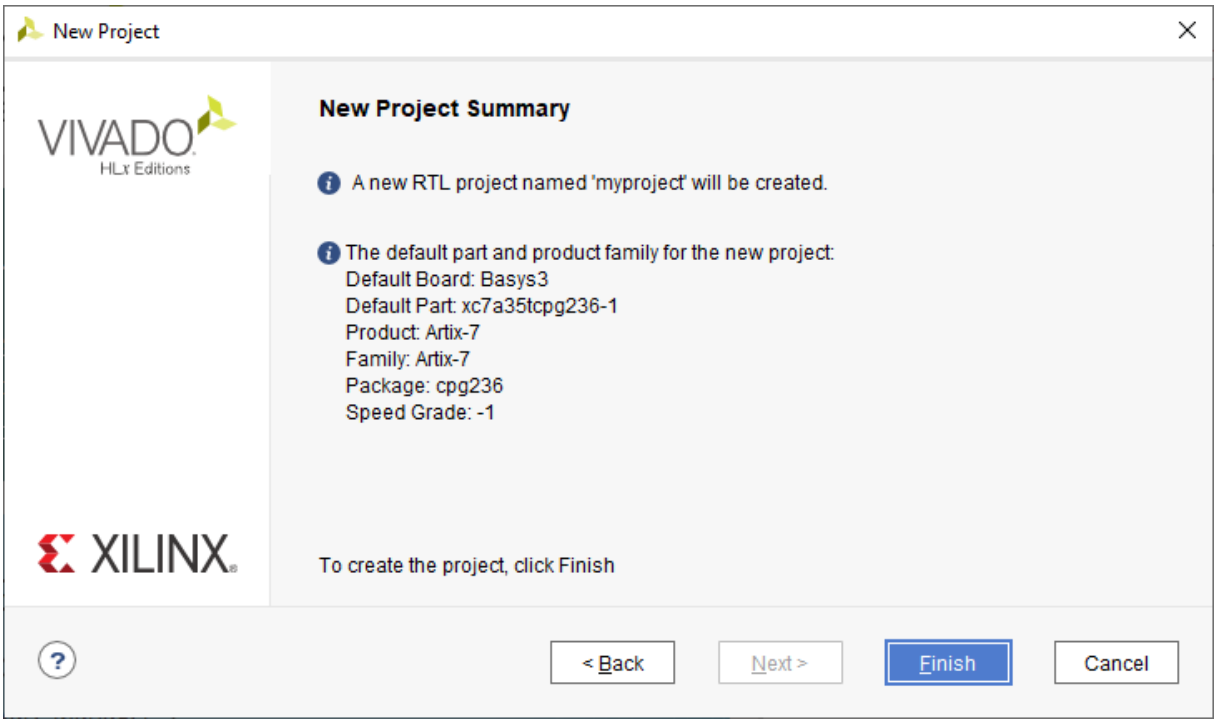

New Project
Project Name
Enter a name for your project and specify a directory where the project data files will be stored.
Project name:
myproject
Project location:
D:/_LEHRE/STE-DE/labs
Create project subdirectory
Project will be created at: D:/_LEHRE/STE-DE/labs/myproject
< Back
Next >
Finish
Cancel


New Project
Project Type
Specify the type of project to create.
RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
Do not specify sources at this time
Post-synthesis Project
You will be able to add sources, view device resources, run design analysis, planning and implementation.
Do not specify sources at this time
I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.
Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.
Example Project
Create a new Vivado project from a predefined template.
< Back
Next >
Finish
Cancel

If you have the board definition files installed, you can directly specify the basys3 board.
if not, you can also directly select the part xc7a35tcpg236-1.

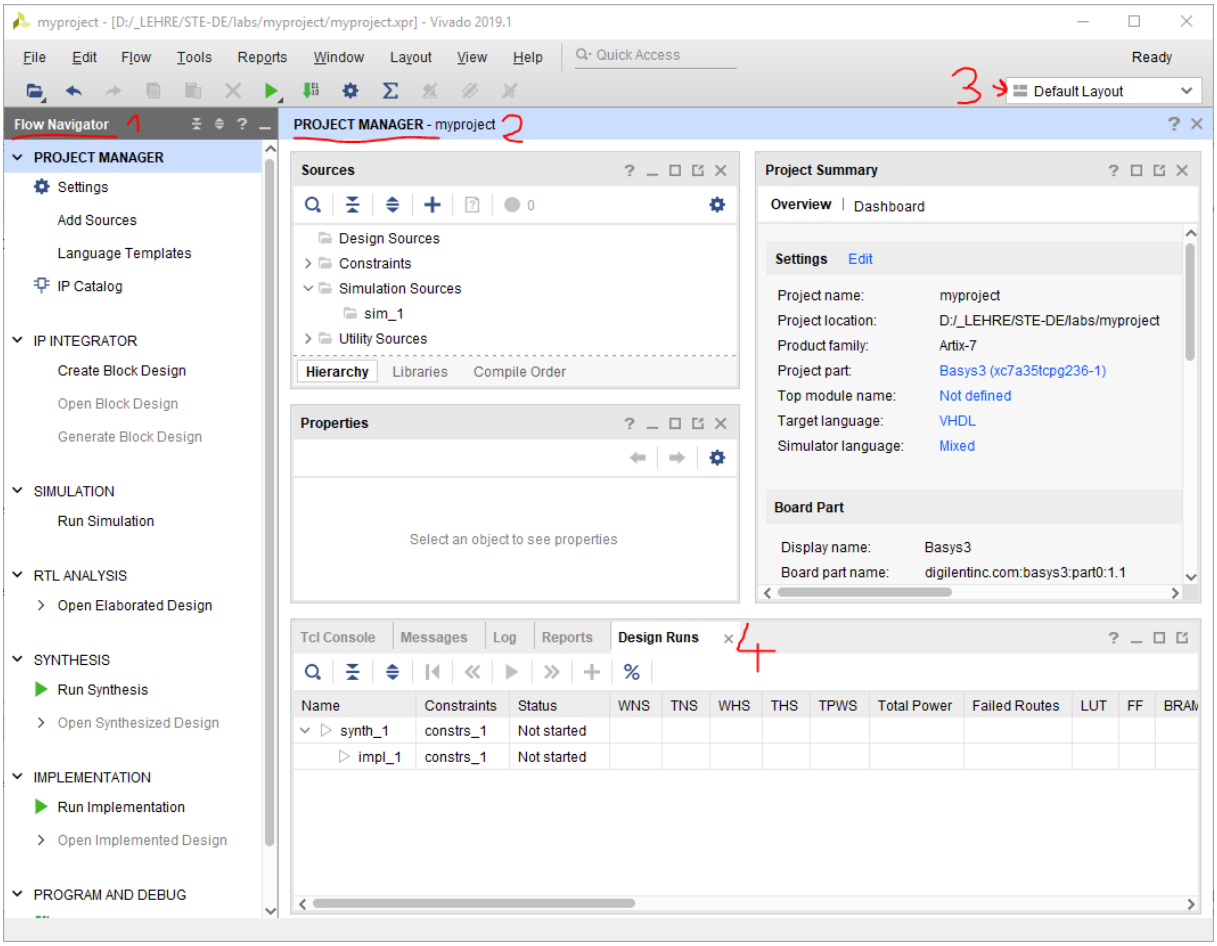






Click finish and wait for the project to be created.

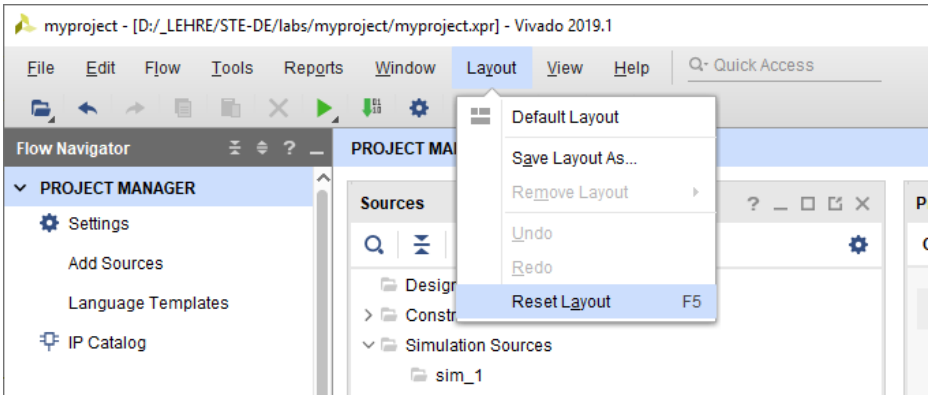
The following window will appear:



Below the Menu and Tool bar there are the following windows:

1. Flow Navigator where all the design steps, from adding source files until generating a bitstream, can be found.
2. Main Window, currently showing the Project Manager (the first element of the flow navigator) with the Sources, Properties and Project Summary windows.
3. With the Layout selector there are sometimes different view options possible. Especially when opening the Elaborate-, the Synthesized or the Implemented Design.
4. Bottom Window (for Messages, Log, Reports, Tcl Console, etc.)

Use the Reset Layout feature to restore your Vivado screen to the default, in case you accidentally closed or moved windows around:



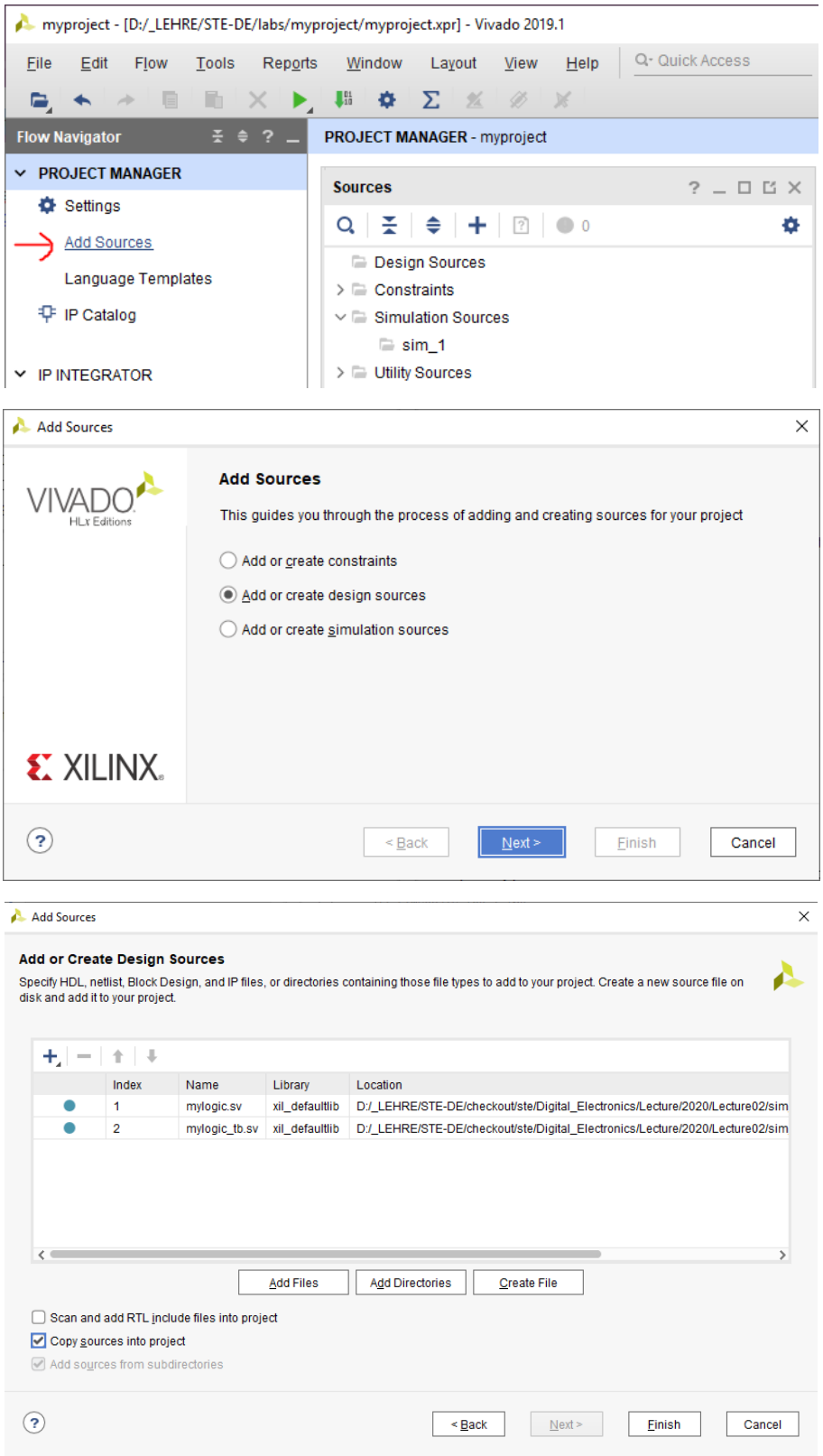
Create the following source files and import them into your Vivado project:

mylogic_tb.sv

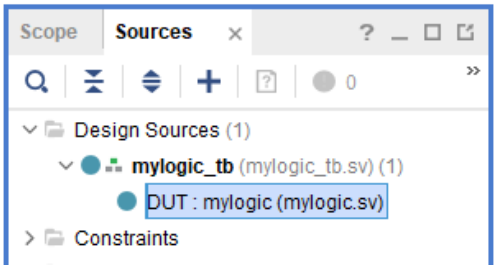
```
module mylogic_tb ( );

logic d;
logic [2:0] abe = 0; //vector of a,b & e

mylogic DUT(
     .a(abe[2]),
     .b(abe[1]),
     .e(abe[0]),
     .data(d));

initial
begin
  #1ns;
  #50ns;
  abe = 3'b101;
  #50ns;
  abe = 3'b111;
  #50ns;
  abe = 3'b100;
  #50ns;
  abe = 3'b000;
  #200ns;
  $finish;
end
endmodule
```

mylogic.sv

```
module mylogic (
     input a, b, e,
     output logic data
     );

always_comb
begin
 if (e)
  data = a & b;
 else
  data = a | b;
end
endmodule
```

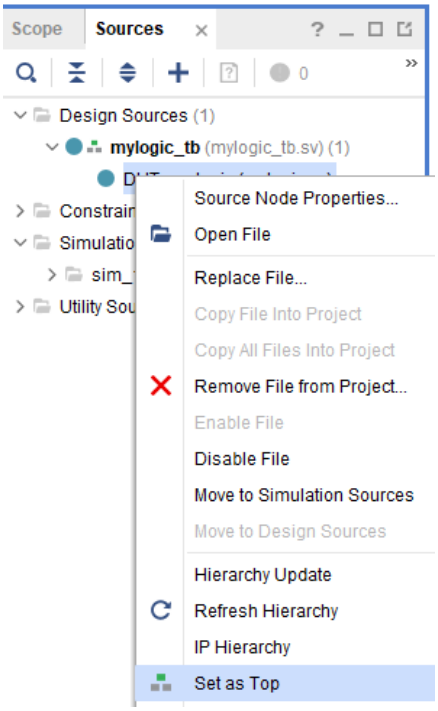


Make sure to select copy sources into project. A copy will be imported from the original file location. Otherwise the tool will just link to the original files and in case they are ever moved, the project will be unable to locate the source files.

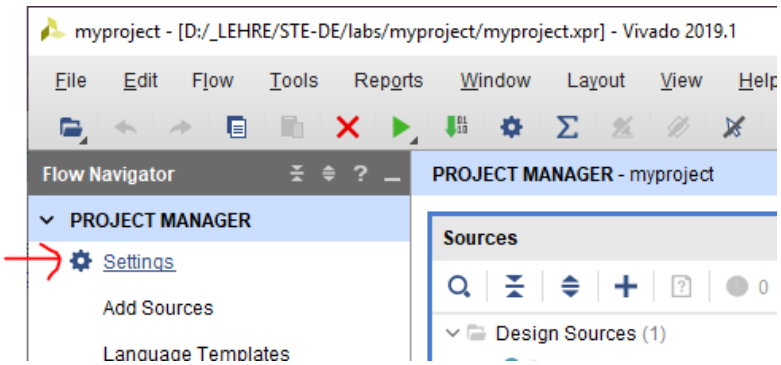


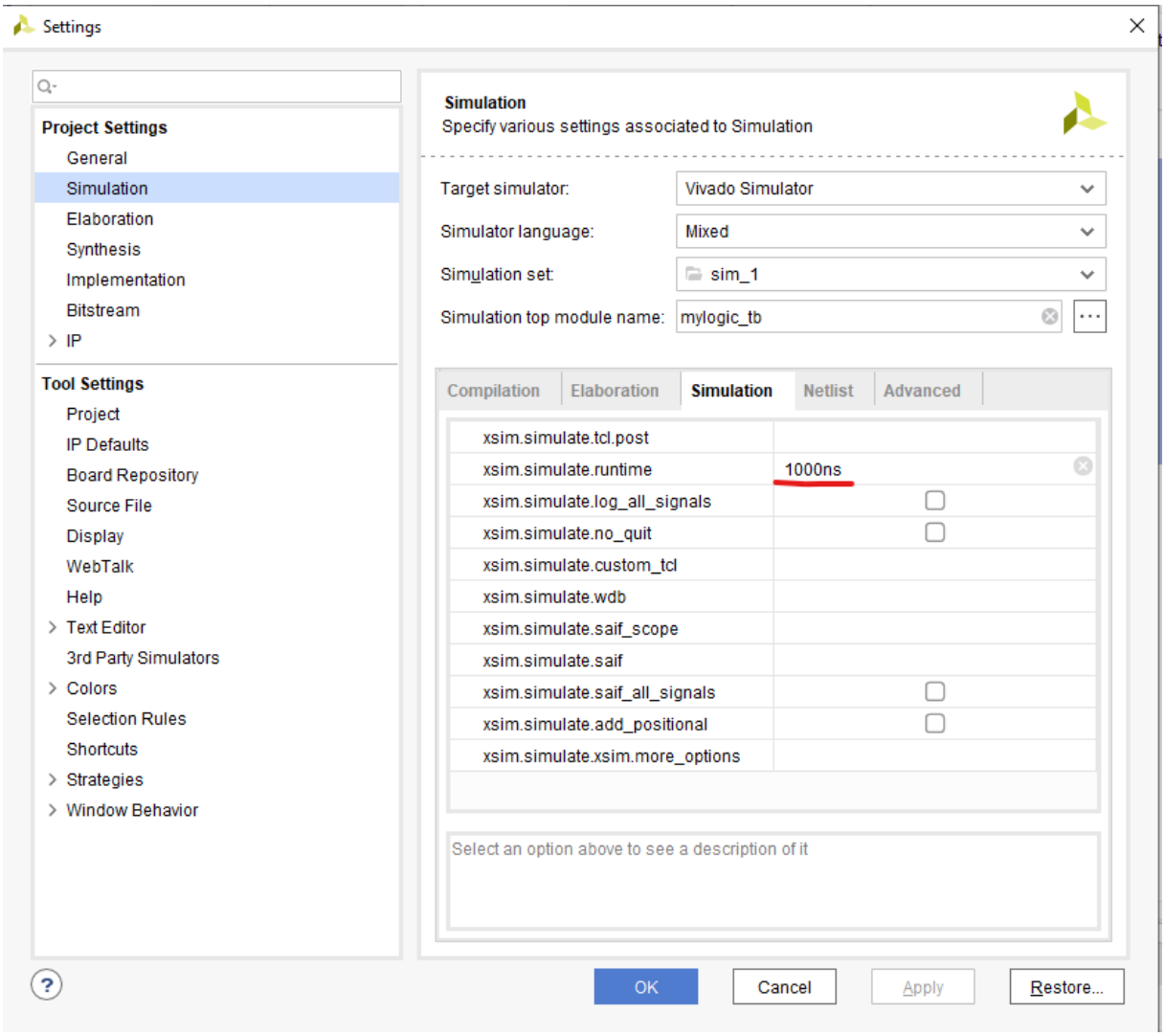
After the import the files will be visible within the source viewer, once under Design Sources and once under Simulation Sources. Notice that the hierarchical instantiation of mylogic within mylogic_tb is automatically detected and the outermost module is selected as the top level!

In case it is necessary to manually change the top level file, do so via the context menu (RMB):



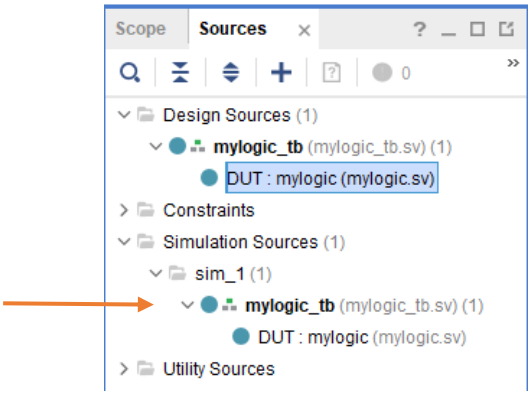
Click on settings to inspect the default simulations settings





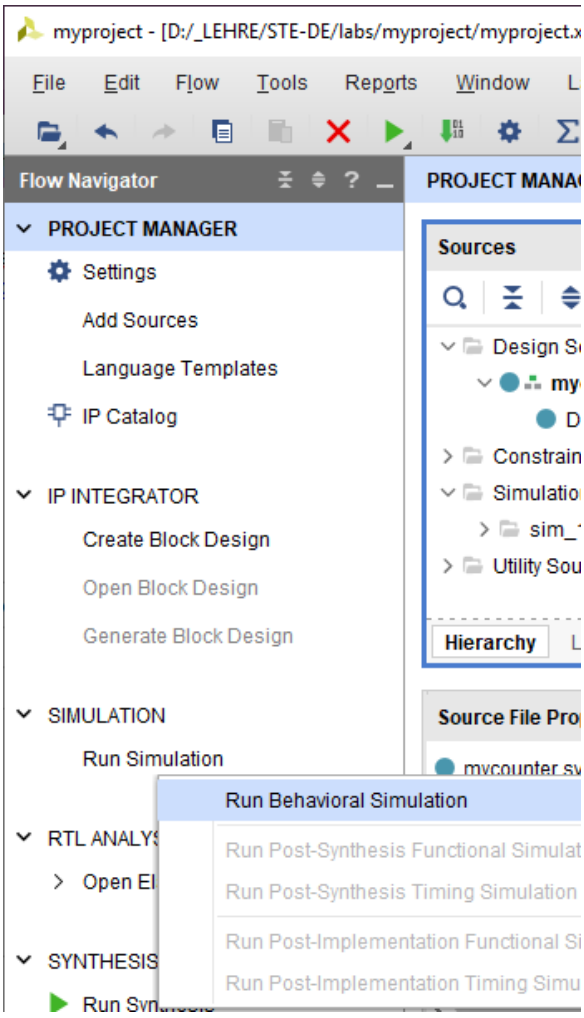
The default simulation time is 1000ns. In case this is not enough time to reach your $finish statement, consider increasing it or removing it at all! (make sure your $finish statement is reachable to avoid an infinitely running simulation)

When running a simulation, the top level file under the Simulation Sources is being chosen.

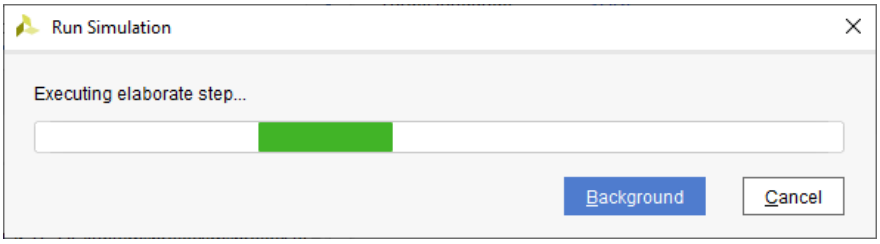


Verify that the test bench is selected as the top level under the simulation sources before continuing.

To start the simulation, click on Run Simulation within the Flow Navigator, and choose Run “Behavioral Simulation”.

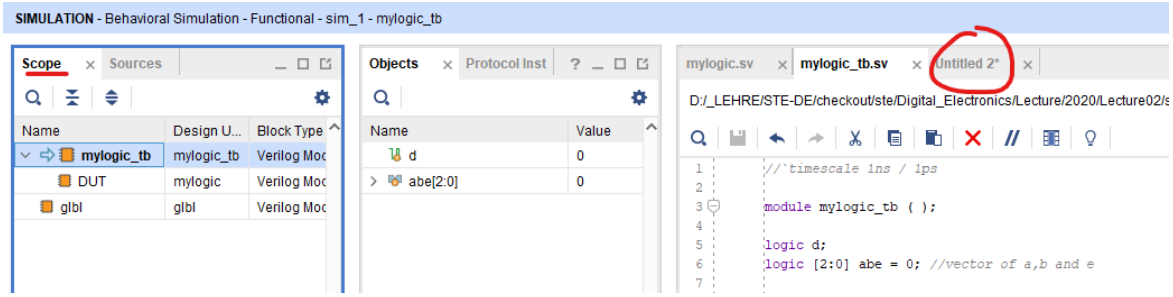


Wait for the simulation to complete:

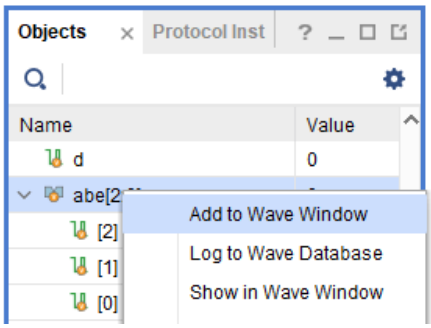


The simulation will be opened within the main window.

Under Scope the hierarchical components can be selected.

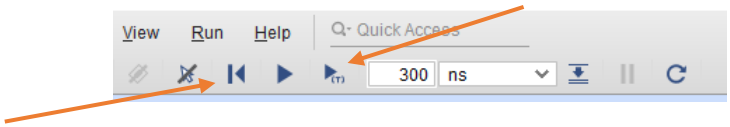


Under Objects you could also add additional signals to the wave window



Since I removed the default simulation time, my simulation did not run yet.

Use the Run All button to run the simulation or use the run for (T) x ns button.



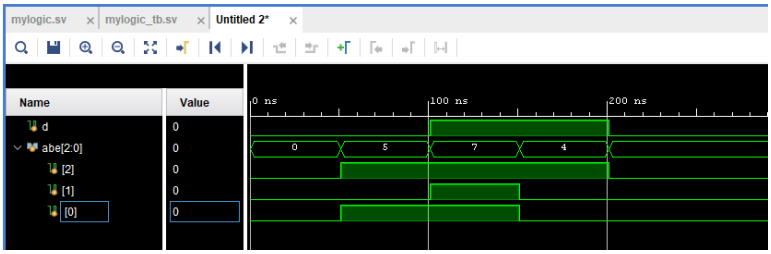
With the rewind button to the left the simulation time can be reset to zero.

The right most button with the circular arrow will restart the whole simulation (the same as running the simulation from the Flow Navigator)

After the simulation executed the test bench is opened and an arrow indicates the last instruction executed. It points to the line with $finish.

```
3   module mylogic_tb ( );
4
5   logic d;
6   logic [2:0] abe = 0; //vector of a,b and e
7
8   mylogic DUT(
9       .a(abe[2]),
.0      .b(abe[1]),
.1      .e(abe[0]),
.2      .data(d));
.3
.4  initial
.5  begin
.6    #1ns;
.7    #50ns;
.8    abe = 3'b101;
.9    #50ns;
:0    abe = 3'b111;
:1    #50ns;
:2    abe = 3'b100;
:3    #50ns;
:4    abe = 3'b000;
:5    #200ns;
:6    $finish;
:7  end
:8  endmodule
:9
```

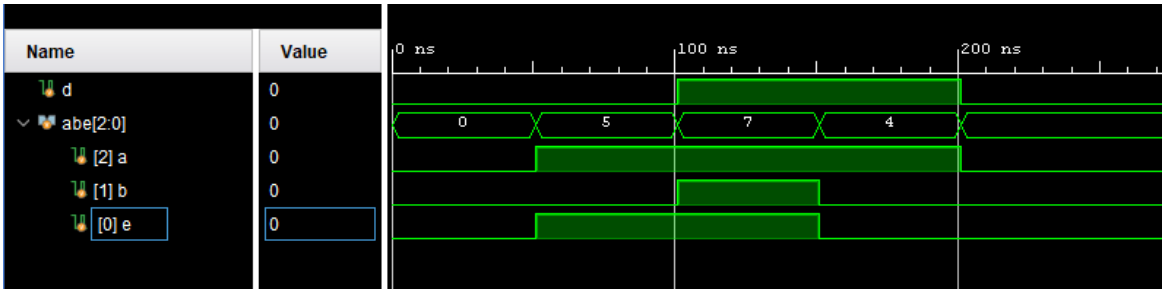
Switch back to the “Untitled 1” wave window and click onto “Zoom Fit”to see the waveforms:



Double clicking any tab, such as “untitled 1” will maximize the view for this tab.
Double clicking again will return the view to the default.

Remember that we assigned input a to abe[2], input b to abe[1] and input e to abe[0].

If you do not like the numbers, you can edit all signal names within the waveform window:



Notice that the input signals are zero during the first 51ns of the simulation, as specified by the test bench.

Then e will become active and the internal and gate's output will be mux'ed to the output d.
When both inputs a and b are high, d will go high.

Then e will become deactivated and the or gate's output is forwarded to d. Therefore, when a is high, the output is high already. Only when both inputs are low (after 201ns) the output will also be low.